Easergy MiCOM P64x
(P642, P643 & P645)

Transformer Protection Relay

P64x/EN M/E93

Software Version	B4
Hardware Suffix	L (P642) & M (P643/P645)
Date	07/2018

Technical Manual

Schneider Electric

Note The technical manual for this device gives instructions for its installation, commissioning, and operation. However, the manual cannot cover all conceivable circumstances or include detailed information on all topics. In the event of questions or specific problems, do not take any action without proper authorization. Contact the appropriate Schneider Electric technical sales office and request the necessary information.

Any agreements, commitments, and legal relationships and any obligations on the part of Schneider Electric including settlements of warranties, result solely from the applicable purchase contract, which is not affected by the contents of the technical manual.

This device MUST NOT be modified. If any modification is made without the express permission of Schneider Electric, it will invalidate the warranty, and may render the product unsafe.

CONTENTS

Date:	07/2018
Products covered by this chapter:	This chapter covers the specific versions of the MiCOM products listed below. This includes ***only*** the following combinations of Software Version and Hardware Suffix. MiCOM P64x (P642, P643 & P645)
Hardware Suffix:	L (P642) & M (P643/645)
Software Version:	B4 - P64x (P642, P643 & P645)
Connection Diagrams:	10P642xx (xx = 01 to 10) 10P643xx (xx = 01 to 06) 10P645xx (xx = 01 to 09)

INTRODUCTION

CHAPTER 1

Date:	07/2018
Products covered by this chapter:	This chapter covers the specific versions of the MiCOM products listed below. This includes ***only*** the following combinations of Software Version and Hardware Suffix.
Hardware Suffix:	L (P642) M (P643/P645)
Software Version:	B4 - P64x (P642, P643 & P645)
Connection Diagrams:	10P642xx (xx = 01 to 10) 10P643xx (xx = 01 to 06) 10P645xx (xx = 01 to 09)

CONTENTS

FIGURES

TABLES

Notes:

1 DOCUMENTATION STRUCTURE

This manual provides a functional and technical description of this MiCOM device, and gives a comprehensive set of instructions for it's use and application. A summary of the different chapters of this manual is given here:

	Description	Chapter Code
SI	**Safety Information**	**Px4x/EN SI**
	A guide to the safe handling, commissioning and testing of equipment. This provides typical information and advice which covers a range of MiCOM Px4x products. It explains how to work with equipment safely.	
1	**Introduction**	**P64x/EN IT**
	A guide to the MiCOM range of relays and the documentation structure. General safety aspects of handling Electronic Equipment are discussed with particular reference to relay safety symbols. Also a general functional overview of the relay and brief application summary is given.	
2	**Technical Data**	**P64x/EN TD**
	Technical data including setting ranges, accuracy limits, recommended operating conditions, ratings and performance data. Compliance with norms and international standards is quoted where appropriate.	
3	**Getting Started**	**P64x/EN GS**
	A guide to the different user interfaces of the IED describing how to start using it. This chapter provides detailed information regarding the communication interfaces of the IED, including a detailed description of how to access the settings database stored within the IED.	
4	**Settings**	**P64x/EN ST**
	List of all relay settings, including ranges, step sizes and defaults, together with a brief explanation of each setting.	
5	**Operation**	**P64x/EN OP**
	A comprehensive and detailed functional description of all protection and non-protection functions.	
6	**Application Notes**	**P64x/EN AP**
	This section includes a description of common power system applications of the relay, calculation of suitable settings, some typical worked examples, and how to apply the settings to the relay.	
7	**Using the PSL Editor**	**Px4x/EN SE**
	This provides a short introduction to using the PSL Editor application.	
8	**Programmable Logic**	**P64x/EN PL**
	Overview of the Programmable Scheme Logic (PSL) and a description of each logical node. This chapter includes the factory default and an explanation of typical applications.	
9	**Measurements and Recording**	**P64x/EN MR**
	Detailed description of the relays recording and measurements functions including the configuration of the event and disturbance recorder and measurement functions.	
10	**Product Design**	**P64x/EN PD**
	Overview of the operation of the relay's hardware and software. This chapter includes information on the self-checking features and diagnostics of the relay.	
11	**Commissioning**	**P64x/EN CM**
	Instructions on how to commission the relay, comprising checks on the calibration and functionality of the relay.	
12	**Test and Setting Records**	**P64x/EN RC**
	This is a list of the tests made and the settings stored on the MiCOM IED.	

	Description	Chapter Code
13	**Maintenance**	**Px4x/EN MT**
	A general maintenance policy for the relay is outlined.	
14	**Troubleshooting**	**Px4x/EN TS**
	Advice on how to recognize failure modes and the recommended course of action. Includes guidance on whom within Schneider Electric to contact for advice.	
15	**SCADA Communications**	**P64x/EN SC**
	This chapter provides an overview regarding the SCADA communication interfaces of the relay. Detailed protocol mappings, semantics, profiles and interoperability tables are not provided within this manual. Separate documents are available per protocol, available for download from our website.	
16	**Installation**	**Px4x/EN IN**
	Recommendations on unpacking, handling, inspection and storage of the relay. A guide to the mechanical and electrical installation of the relay is provided, incorporating earthing recommendations.	
17	**Connection Diagrams**	**P64x/EN CD**
	A list of connection diagrams, which show the relevant wiring details for this relay.	
18	**Cyber Security**	**Px4x/EN CS**
	An overview of cyber security protection (to secure communication and equipment within a substation environment). Relevant cyber security standards and implementation are described too.	
19	**Dual Redundant Ethernet Board (DREB)**	**Px4x/EN REB**
	Information about how MiCOM products can be equipped with Dual Redundant Ethernet Boards (DREBs) and the different protocols which are available. Also covers how to configure and commission these types of boards.	
20	**Parallel Redundancy Protocol (PRP) Notes**	**Px4x/EN PR**
	Includes an introduction to Parallel Redundancy Protocols (PRP) and the different networks PRP can be used with. Also includes details of PRP and MiCOM functions.	
21	**High-availability Seamless Redundancy (HSR)**	**Px4x/EN HS**
	Introduction to the High-availability Seamless Redundancy (HSR); and how it is implemented on MiCOM-based products manufactured by Schneider Electric.	
22	**Rapid Spanning Tree Protocol (RSTP) Notes**	**Px4x/EN TP**
	This section gives an introduction to the Rapid Spanning Tree Protocol (RSTP); and how it is implemented on MiCOM-based products manufactured by Schneider Electric.	
23	**Process Bus Notes (PB)**	**Px4x/EN PB**
	This section gives an introduction to the Process Bus Board (PB); and how it is implemented on MiCOM-based products manufactured by Schneider Electric.	
24	**Version History (of Firmware and Service Manual)**	**P64x/EN VH**
	This is a history of all hardware and software releases for this product.	
SG	**Symbols and Glossary**	**Px4x/EN SG**
	List of common technical terms, abbreviations and symbols found in this documentation.	

Some of these chapters are *Specific* to a particular MiCOM product. Others are *Generic* – meaning that they cover more than one MiCOM product. The generic chapters have a Chapter Code which starts with Px4x.

2 INTRODUCTION TO MICOM

About MiCOM Range

MiCOM is a comprehensive solution capable of meeting all electricity supply requirements. It comprises a range of components, systems and services from Schneider Electric.

Central to the MiCOM concept is flexibility. MiCOM provides the ability to define an application solution and, through extensive communication capabilities, integrate it with your power supply control system.

The components within MiCOM are:

- P range protection relays
- C range control products
- M range measurement products for accurate metering and monitoring
- S range versatile PC support and substation control packages

MiCOM products include extensive facilities for recording information on the state and behaviour of the power system using disturbance and fault records. They can also provide measurements of the system at regular intervals to a control centre enabling remote monitoring and control to take place.

For up-to-date information, please see:

www.schneider-electric.com

Note	*During 2011, the International Electrotechnical Commission classified the voltages into different levels (IEC 60038). The IEC defined LV, MV, HV and EHV as follows: LV is up to 1000V. MV is from 1000V up to 35 kV. HV is from 110 kV or 230 kV. EHV is above 230 KV.* *There is still ambiguity about where each band starts and ends. A voltage level defined as LV in one country or sector, may be described as MV in a different country or sector. Accordingly, LV, MV, HV and EHV suggests a possible range, rather than a fixed band. Please refer to your local Schneider Electric office for more guidance.*

3 PRODUCT SCOPE

The P64x (P642, P643 and P645) preserves transformer service life by offering fast protection for transformer faults. Hosted on an advanced IED platform, the P64x incorporates differential, REF, thermal, and overfluxing protection, plus backup protection for uncleared external faults. Model variants cover two and three winding transformers (including autotransformers), with up to five sets of 3-phase CT inputs. Large CT counts are common in ring bus or mesh corner applications, where the P64x summates currents to create each total winding current, easing application of backup protection. Backup overcurrent can be directionalized, where the user includes the optional 3-phase VT input in their chosen model.

3.1 Functional Overview

The P642/P643/P645 transformer protection relays have a wide variety of protection functions which are summarized in the following table.

ANSII No	Description	P64x
	Time synchronization port (modulated / unmodulated IRIG-B)	Option P642/P643/P645
	IEC 61850 Ed2 / Ed1	Option P642/P643/P645
87	Phase-segregated transformer biased differential protection is provided for high-speed discriminative protection for all fault types.	P642 / P643/ P645
64	Biased low-impedance restricted earth fault element can be used to provide high-speed earth fault protection. High impedance restricted earth fault element is also available. The 64 function is applicable to conventional transformers and autotransformers.	P642/ P643/ P645
50/51/67	Four overcurrent protection stages are provided which can be selected as non-directional, directional, forward or directional reverse. Stages 1 and 2 can be set as Inverse Definite Minimum Time (IDMT) or Definite Time (DT); stages 3 and 4 can be set as DT only.	P642/ P643/ P645
46OC	Four stages of negative phase sequence overcurrent protection are provided for remote back-up protection for both phase-to-earth and phase-to-phase faults. Each stage can be selected as non-directional, directional forward or directional reverse. Stages 1 and 2 can be set as Inverse Definite Minimum Time (IDMT) or Definite Time (DT); stages 3 and 4 can be set as DT only.	P642/ P643/ P645
49	Thermal overload protection based on IEEE Std C57.91-1995. Thermal trip can be based on either hot spot or top oil temperature, each with three time-delayed stages available. Four cooling modes are available to consider the transformer cooling classes.	P642/ P643/ P645
LoL	Two one-stage definite time delay alarms based on aging acceleration factor (F_{AA}) or Loss-of-Life (LoL) are available.	P642/ P643/ P645
Thru	Through faults are a major cause of transformer damage and failure. Both the insulation and the mechanical effects of fault currents are considered. A one-stage alarm is available for through-fault monitoring.	P642/ P643/ P645
50N/51N/67N	Up to three derived or measured standby earth fault elements are available. Four stages are provided which can be selected as non-directional, directional, forward or directional reverse. Stages 1 and 2 can be set as Inverse Definite Minimum Time (IDMT) or Definite Time (DT); stages 3 and 4 can be set as DT only	P642/ P643/ P645
59N	The 59N element is a two-stage design, each stage having separate voltage and time delay settings. Stage 1 can be set to operate on either an IDMT or DT characteristic, while stage 2 can be set to DT only.	P642/ P643/ P645
24	Two five-stage overfluxing (V/Hz) elements protect the transformer, against overexcitation. The first stage is a Definite Time alarm, the second stage can be used to provide an inverse or Definite Time trip characteristic and stages 3, 4 and 5 are Definite Time.	P642/ P643/ P645
27	A two-stage undervoltage protection element, configurable as either phase-to-phase or phase-to-neutral measuring is available, Stage 1 can be set as either IDMT or DT and stage 2 is DT only.	P643/ P645

ANSII No	Description	P64x
59	A two-stage overvoltage protection element, configurable as either phase-to-phase or phase-to-neutral measuring is available. Stage 1 can be set as either IDMT or DT and stage 2 is DT only.	P643/ P645
47	A one-stage negative phase sequence overvoltage protection element is available. It is DT only.	P642/ P643/ P645
81U/O	Four-stage Definite Time underfrequency and two-stage Definite Time overfrequency protection is provided for load shedding and back-up protection.	P642/ P643/ P645
RTD	Ten RTDs (PT100) are available to monitor the ambient and top oil temperature accurately. Each RTD has an instantaneous alarm and Definite Time trip stage.	Option P642/ P643/ P645
50BF	A two-stage circuit breaker failure function is provided with a 3-pole initiation input from external protection.	P642/ P643/ P645
37P	Phase undercurrent elements are available for use with, for example, the circuit breaker fail function.	P642/ P643/ P645
VTS	Voltage transformer supervision is provided (1, 2 & 3-phase fuse failure detection) to prevent mal-operation of voltage-dependent protection elements when a VT input signal is lost.	P642/ P643/ P645
CTS	Current transformer supervision prevents mal-operation of current-dependent protection elements when a CT input signal is lost.	P642/ P643/ P645
CLIO	Four analog or current loop inputs are provided for transducers such as vibration sensors and tachometers. Each input has a Definite Time trip and alarm stage, each input can be set to 'Over' or 'Under' operation, and each input can be independently selected as 0 to 1, 0 to 10, 0 to 20 or 4 to 20 mA. Four analogue (or current loop) outputs are provided for the analogue measurements in the relay. Each output can be independently selected as 0 to 1, 0 to 10, 0 to 20 or 4 to 20 mA.	Option P642/ P643/ P645
	CT saturation and no gap detection algorithms have been included to enhance to low set differential element operating time	P642/ P643/ P645
	External fault detection algorithm has bee included to maintain stability during external faults.	P642/ P643/ P645
	Zero crossing detection algorithm has been included to prevent circuit breaker failure mal-operations due to subsidence current.	P642/ P643/ P645
	Phase rotation. The rotation of the phases ABC or ACB for all 3-phase current and voltage channels can be selected. Also, for pumped storage applications, the swapping of two phases can be emulated independently for the 3-phase voltage and 3-phase current channels.	P642/ P643/ P645
	32 programmable user alarms	P642/ P643/ P645
	10 programmable function keys	P643/ P645
	18 programmable LEDs (tri-color P643/P645, red P642)	P642/ P643/ P645
	8 to 24 digital inputs (order option) depending on the model	P642/ P643/ P645
	Front communication port (EIA(RS)232)	P642/ P643/ P645
	Rear communication port (K-Bus/EIA(RS)485). The following communications protocols are supported: Courier, MODBUS, IEC870-5-103 (VDEW), DNP3.0.	P642/ P643/ P645
	Rear communication port (Fiber Optic). The following communications protocols are supported: Courier, MODBUS, IEC870-5-103 (VDEW) and DNP3.0.	Option P642/ P643/ P645
	Second rear communication port, EIA(RS)232/EIA(RS)485. Courier and K-Bus protocols.	Option P642/ P643/ P645
	Rear IEC 61850-8-1 Ethernet communication port.	Option P642/ P643/ P645
	Time synchronization port (IRIG-B)	Option P642/ P643/ P645

Table 1 - Protection functions overview

The relay supports these relay management functions as well as the ones shown above.

- Measurement of all instantaneous & integrated values
- Circuit breaker, status & condition monitoring
- Programmable Scheme Logic (PSL)
- Trip circuit and coil supervision (using PSL)
- Alternative setting groups
- Programmable function keys
- Control inputs
- Programmable allocation of digital inputs and outputs
- Sequence of event recording
- Comprehensive disturbance recording (waveform capture)
- Fault recording
- Fully customizable menu texts
- Power-up diagnostics and continuous self-monitoring of relay
- Commissioning test facilities
- Real time clock/time synchronization - time synchronization possible from IRIG-B input, opto input or communications
- Simple password management:
  CSL0 - No Security Administration Tool (SAT) required
- Advanced Cyber Security:
  CSL1 - Security Administration Tool (SAT) required
- Read only mode

3.2 Process Bus

The Process Bus board interfaces to IEC 61850-9-2LE (80 samples/cycle) and IEC61869-9 (F4800S2I4U4) compliant Merging Units (MU). The Process Bus board replaces the conventional analogue inputs (analogue module) and is available in these Easergy protection relays:

- P141, P142, P143, P145 (feeder protection)
- P442, P443, P445 and P446 (distance protection)
- P543, P546 (line differential protection)
- P642, P643 and P645 (transformer protection)
- P746 (busbar protection)
- P841(multifunction line terminal IED)

Process bus is mainly used to communicate the primary values of current and voltage to a protection relay via an Ethernet network. Merging Units form the data acquisition layer in the network. They connect to the primary sensor, determining the instantaneous primary measurements and publishing them on the process bus.

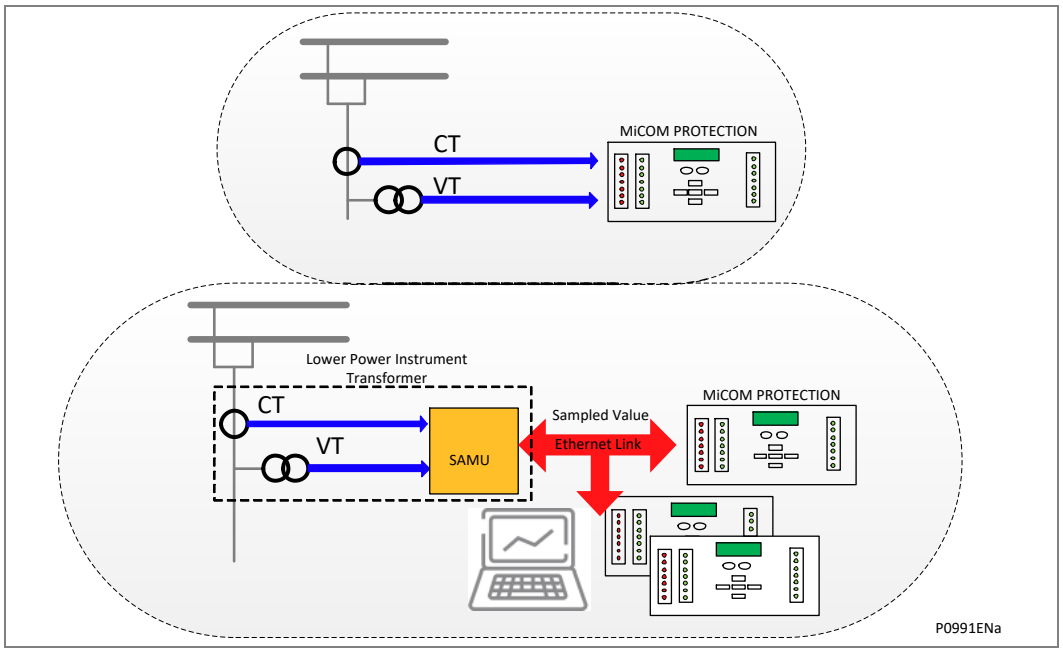


Figure 1 - Process Bus principle

The Process Bus philosophy is to be able to isolate from the secondary system such as protection or control IEDs the primary interfaces such as the breakers, isolators by interposing Breaker IED or Switch IED and/or CTs or VTs by interposing new primary equipment called LPIT (Low Power Instrument Transformers), previously known as NCIT (Non-Conventional Instrument Transformers) or Stand Alone Merging Units (SAMU). The Stand Alone Merging Unit (SAMU) converts 1/5A and 100/110V signals to process bus measurements (called Sampled Values). One feature that is mandatory for the Merging Unit is a very accurate clock source. Time is unique and common in the "analogue world" but is not in the digital world. Sampled values must be synchronized via IEC61850-9-3 (refer to IEC 61588/IEEE1588 Precision Time Protocol) or 1 Pulse Per Second (PPS) signal. The measurement values provided must be suitable for the protection application. This performance is ensured by the selection of primary sensors meeting the CT requirements of the protection application. These requirements must now be met by both the primary CT and the Merging Unit.

The IMU can embed other digital functionality, sending information such as position of breaker and isolators and receiving digital information such as close, open, trip or reclose commands over the process bus.

The process bus links allow multiple measurement streams as well as the digital information to be sent over common ethernet link which saves on the installation of secondary wiring. Also, the same stream can be utilized by multiple relays reducing the number of primary sensors required. This does, however, expose the system to a greater outage due to a link or switch failure. In most cases, redundancy such as IEC62439 PRP will be required to ensure system availability.

3.3 Application Overview

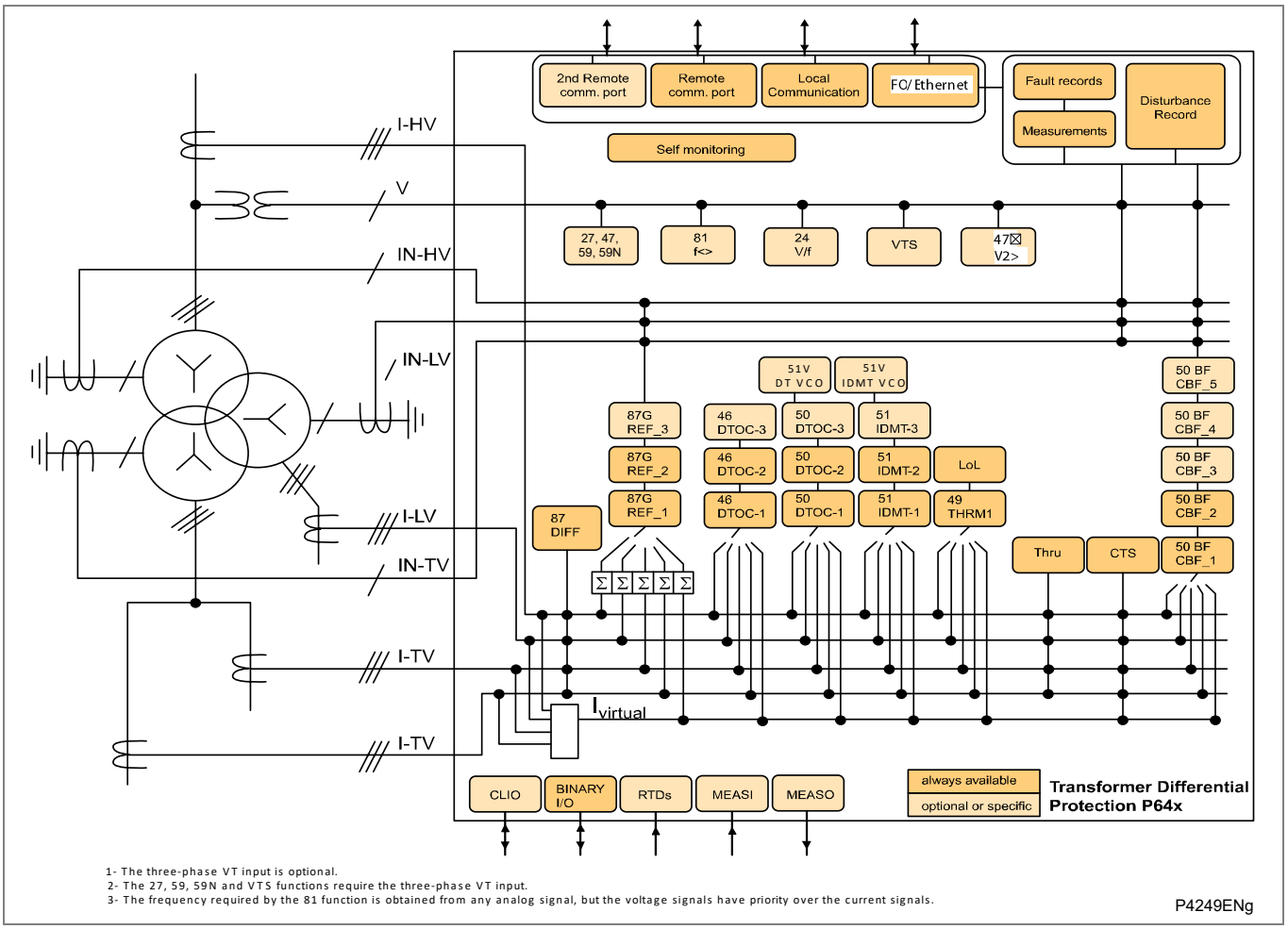


Figure 2 - Functional diagram

4 ORDERING OPTIONS

4.1 Information Required with Order - Software Version B4

The options vary from one product to another:

- P642 Transformer Protection
- P643 Transformer Protection
- P645 Transformer Protection

Note	*The following tables list the options available as of the date shown of this documentation. The most up-to-date versions of these tables can be found on our web site (www.schneider-electric.com). It may not be possible to select ALL of the options shown in this chart within a single item of equipment.*

4.2 P642 Transformer Protection

Order form		MiCOM P642										
		Ready-to-use configuration										
Transformer Relay With Sigma-Delta Input Module		**P642**		**1**				**M**				
Vx Aux Rating :												
24 - 32 Vdc			9									
48 - 110 Vdc			2									
110 - 250 Vdc (100 - 240 Vac)			3									
In/Vn Rating :												
HV-LV (In = 1A/5A), (Vn = 100/120V) (8CT/1VT)				1								
HV-LV (In = 1A/5A), (Vn = 100/120V) (8CT/2VT)				2								
Hardware Options :												
Standard - no options					1							
IRIG-B only (modulated)					2							
Fibre optic converter only					3							
IRIG-B (modulated) & fibre optic converter					4							
Second Rear Comms Port (Courier EIA232/EIA485/k-bus)					7							
Second Rear Comms Port + IRIG-B (modulated) (Courier EIA232/EIA485/k-bus)					8							
Redundant Ethernet (100Mbit/s) PRP or HSR and Dual IP, 2 LC ports + 1 RJ45 port + Modulated/Un-modulated IRIG-B					Q							
Redundant Ethernet (100Mbit/s) PRP or HSR and Dual IP, 3 RJ45 ports + Modulated/Un-modulated IRIG-B					R							
Ethernet (100Mbit/s), 1 RJ45 port + Modulated/Un-modulated IRIG-B					S							
Product Specific Options :												
Size 8 (40TE) Case, 8 Optos + 8 Relays						A						
Size 8 (40TE) Case, 8 Optos + 8 Relays + RTD						B						
Size 8 (40TE) Case, 8 Optos + 8 Relays + CLIO (mA I/O)						C						
Size 8 (40TE) Case, 12 Optos + 12 Relays						D						
Size 8 (40TE) Case, 8 Optos + 12 Relays (including 4 High Break)						E						
Protocol Options :												
K-Bus/Courier							1					
Modbus							2					
IEC60870-5-103							3					
DNP3.0							4					
IEC 61850 Edition 1 / 2 and Courier via rear K-Bus/RS485 with simple password management - CSL0							6					
IEC 61850 Edition 1 / 2 and DNP3 over Ethernet and DNP3.0 via rear RS485 with simple password management - CSL0							B					
IEC 61850 Edition 1 / 2 and Courier via rear K-Bus/RS485 with advanced Cyber Security - CSL1 - Security Administration Tool (SAT) required							G					
IEC 61850 Edition 1 / 2 and DNP3 over Ethernet and DNP3.0 via rear RS485 with advanced Cyber Security - CSL1 - Security Administration Tool (SAT) required							L					
Mounting Options :												
Panel Mounting								M				
Language Options :												
English, French, German, Spanish									0			
English, French, German, Russian									5			

Order form		**MiCOM P642**										
		Ready-to-use configuration										
Transformer Relay With Sigma-Delta Input Module		**P642**		**1**				**M**				
Chinese, English or French via HMI, with English or French only via Communications port									C			
Software Version Options :												
Unless specified the latest version will be delivered										B3		
Customisation:												
Default											8	
Customer Settings											9	
Design Suffix :												
Phase 3 CPU												L

4.3 P643 Transformer Protection

Order form		MiCOM P643										
		Ready-to-use configuration										
Transfromer Relay With Sigma-Delta Input Module		P643						M				
Vx Aux Rating :												
24 - 32 Vdc			9									
48 - 110 Vdc			2									
110 - 250 Vdc (100 - 240 Vac)			3									
In/Vn Rating :												
HV-LV In = 1A/5A, Vn = (100/120V) (12CT/1VT)				1								
HV-LV In = 1A/5A, Vn = (100/120V) (12CT/4VT)				2								
Hardware Options :												
Standard - no options					1							
IRIG-B only (modulated)					2							
Fibre optic converter only					3							
IRIG-B (modulated) & fibre optic converter					4							
Second Rear Comms Port (Courier EIA232/EIA485/kbus)					7							
Second Rear Comms Port + IRIG-B (modulated) (Courier EIA232/EIA485/kbus)					8							
Redundant Ethernet (100Mbit/s) PRP or HSR and Dual IP, 2 LC ports + 1 RJ45 port + Modulated/Un-modulated IRIG-B					Q							
Redundant Ethernet (100Mbit/s) PRP or HSR and Dual IP, 3 RJ45 ports + Modulated/Un-modulated IRIG-B					R							
Ethernet (100Mbit/s), 1 RJ45 port + Modulated/Un-modulated IRIG-B					S							
Product Specific Options :												
Size 12 (60TE) case, 16 optos + 16 relays						A						
Size 12 (60TE) case, 16 optos + 16 relays + RTD						B						
Size 12 (60TE) case, 16 optos + 16relays + CLIO (mA I/O)						C						
Size 12 (60TE) case, 24 optos + 16 relays						D						
Size 12 (60TE) case, 16 optos + 24 relays						E						
Size 12 (60TE) case, 16 optos + 20 relays (including 4 High Break)						F						
Protocol Options :												
K-Bus/Courier							1					
Modbus							2					
IEC60870-5-103							3					
DNP3.0							4					
IEC 61850 Edition 1 / 2 and Courier via rear K-Bus/RS485 with simple password management - CSL0							6					
IEC 61850 Edition 1 / 2 and DNP3 over Ethernet and DNP3.0 via rear RS485 with simple password management - CSL0							B					
IEC 61850 Edition 1 / 2 and Courier via rear K-Bus/RS485 with advanced Cyber Security - CSL1 - Security Administration Tool (SAT) required							G					
IEC 61850 Edition 1 / 2 and DNP3 over Ethernet and DNP3.0 via rear RS485 with advanced Cyber Security - CSL1 - Security Administration Tool (SAT) required							L					
Mounting Options :												
Panel Mounting								M				
Language Options :												
English, French, German, Spanish									0			
English, French, German, Russian									5			

Order form		MiCOM P643										
		Ready-to-use configuration										
Transfromer Relay With Sigma-Delta Input Module		**P643**						**M**				
Chinese, English or French via HMI, with English or French only via Communications port									C			
Software Version Options :												
Unless specified the latest version will be delivered										B3		
Settings Files Options:												
Default											8	
Customer Specific											9	
Design Suffix :												
Extended Phase 3 CPU												M

4.4 P645 Transformer Protection

Order form	MiCOM P645										
	Ready-to-use configuration										
P645 Transformer Relay With Sigma-Delta Input Module											
Vx Aux Rating :											
24 - 32 Vdc	9										
48 - 110 Vdc	2										
110 - 250 Vdc (100 - 240 Vac)	3										
In/Vn Rating :											
HV-LV In = 1A/5A, Vn = (100/120V) (18CT/1VT)		1									
HV-LV In = 1A/5A, Vn = (100/120V) (18CT/4VT)		2									
Hardware Options :											
Standard - no options			1								
IRIG-B only (modulated)			2								
Fibre optic converter only			3								
IRIG-B (modulated) & fibre optic converter			4								
Second Rear Comms Port (Courier EIA232/EIA485/k-bus)			7								
Second Rear Comms Port + IRIG-B (modulated) (Courier EIA232/EIA485/k-bus)			8								
Redundant Ethernet (100Mbit/s) PRP or HSR and Dual IP, 2 LC ports + 1 RJ45 port + Modulated/Un-modulated IRIG-B			Q								
Redundant Ethernet (100Mbit/s) PRP or HSR and Dual IP, 3 RJ45 ports + Modulated/Un-modulated IRIG-B			R								
Ethernet (100Mbit/s), 1 RJ45 port + Modulated/Un-modulated IRIG-B			S								
Product Specific Options :											
Size 12 (60TE) case, 16 optos + 16 relays				A							
Size 12 (60TE) case, 16 optos + 16 relays + RTD				B							
Size 12 (60TE) case, 16 optos + 16 relays + CLIO (mA I/O)				C							
Size 12 (60TE) case, 24 optos + 16 relays				D							
Size 12 (60TE) case, 16 optos + 24 relays				E							
Size 16 (80TE) case, 24 optos + 24 relays				F							
Size 16 (80TE) case, 24 optos + 24 relays + RTD				G							
Size 16 (80TE) case, 24 optos + 24 relays + CLIO (mA I/O)				H							
Size 16 (80TE) case, 24 optos + 24 relays + RTD + CLIO (mA I/O)				J							
Size 12 (60TE) case, 16 optos + 20 relays (including 4 high break)				K							
Size 16 (80TE) case, 24 optos + 20 relays (including 4 high break)				L							
Size 16 (80TE) case, 24 optos + 20 relays (including 4 high break) + RTD				M							
Size 16 (80TE) case, 24 optos + 20 relays (including 4 high break) + CLIO (mA I/O)				N							
Size 16 (80TE) case, 24 optos + 20 relays (including 4 high break) + RTD + CLIO (mA I/O)				P							
Size 16 (80TE) case, 16 optos + 24 relays (including 8 high break)				Q							
Size 16 (80TE) case, 16 optos + 24 relays (including 8 high break) + RTD				R							
Size 16 (80TE) case, 16 optos + 24 relays (including 8 high break) + CLIO (mA I/O)				S							

Order form		MiCOM P645										
		Ready-to-use configuration										
P645 Transformer Relay With Sigma-Delta Input Module												
Size 16 (80TE) case, 16 optos + 24 relays (including 8 high break) + RTD + CLIO (mA I/O)						T						
Protocol Options :												
K-Bus/Courier							1					
Modbus							2					
IEC60870-5-103							3					
DNP3.0							4					
IEC 61850 Edition 1 / 2 and Courier via rear K-Bus/RS485 with simple password management - CSL0							6					
IEC 61850 Edition 1 / 2 and DNP3 over Ethernet and DNP3.0 via rear RS485 with simple password management - CSL0							B					
IEC 61850 Edition 1 / 2 and Courier via rear K-Bus/RS485 with advanced Cyber Security - CSL1 - Security Administration Tool (SAT) required							G					
IEC 61850 Edition 1 / 2 and DNP3 over Ethernet and DNP3.0 via rear RS485 with advanced Cyber Security - CSL1 - Security Administration Tool (SAT) required							L					
Mounting Options :												
Panel Mounting								M				
Rack Mounting (only available on 80TE cases)								N				
Language Options :												
English, French, German, Spanish									0			
English, French, German, Russian									5			
Chinese, English or French via HMI, with English or French only via Communications port									C			
Software Version Options :												
Unless specified the latest version will be delivered										B3		
Settings Files Options :												
Default											8	
Customer Settings											9	
Design Suffix :												
Extended Phase 3 CPU												M

Notes:

TECHNICAL DATA

CHAPTER 2

Date:	07/2018
Products covered by this chapter:	This chapter covers the specific versions of the MiCOM products listed below. This includes ***only*** the following combinations of Software Version and Hardware Suffix.
Hardware Suffix:	L (P642) M (P643/P645)
Software Version:	B4 - P64x (P642, P643 & P645)
Connection Diagrams:	10P642xx (xx = 01 to 10) 10P643xx (xx = 01 to 06) 10P645xx (xx = 01 to 09)

CONTENTS

FIGURES

TABLES

Notes:

1 MECHANICAL SPECIFICATIONS

1.1 Design

Modular MiCOM Px40 platform relay:

- P642 in 40TE case
- P643 in 60TE case
- P645 in 60TE or 80TE case.

Mounting is front of panel flush mounting, or 19” rack mounted (ordering options).

1.2 Enclosure Protection

Per IEC 60529:

- IP 52 Protection (front panel) against dust and dripping water.
- IP 50 Protection for the rear and sides of the case against dust.
- IP 10 Product safety protection for the rear due to live connections on the terminal block.

1.3 Weight

Product:	Case:	Weight:
P642	(40TE)	7.9kg
P643	(60TE)	11.5kg
P645	(60TE)	11.5kg
P645	(80TE)	15.5kg

2 TERMINALS

2.1 AC Current and Voltage Measuring Inputs

Located on heavy duty (black) terminal block:
Threaded M4 terminals, for ring terminal connection.
CT inputs have integral safety shorting, upon removal of the terminal block.

2.2 General Input/Output Terminals

For power supply, opto inputs, output contacts and RP1, COM1 and optional COM2 rear communications.
Located on general purpose (grey) blocks:
Threaded M4 terminals, for ring lug/terminal connection.

2.3 Case Protective Earth Connection

Two rear stud connections, threaded M4.
Must be earthed (grounded) using the protective (earth) conductor for safety, minimum earth wire size 2.5mm^2.

2.4 Front Port Serial PC Interface

EIA(RS)-232 DCE, 9 pin D-type female connector Socket SK1.
Courier protocol for interface to MiCOM S1 Studio software.
Isolation to SELV/ELV (Safety/Extra Low Voltage) level / PEB (Protective Equipotential Bonded).
Maximum cable length 15m.

2.5 Front Download/Monitor Port

EIA(RS)-232, 25 pin D-type female connector Socket SK2.
For firmware and menu text downloads.
Isolation to SELV/PEB level.

2.6 Rear Communications Port (RP1)

EIA(RS)-485 signal levels, two wire connections located on general purpose block, M4 screw.
For screened twisted pair cable, multidrop, 1000 m max.
For Courier (K-Bus), IEC-60870-5-103 (not for P746/P849), MODBUS (not for P14x/P445/P44x/P54x/P547/P746/P841/P849) or DNP3.0 protocol (not for P24x/P746/P849) (ordering options).
Isolation to SELV (Safety Extra Low Voltage) level. Ethernet (copper and fibre).

2.7 Optional Rear Fiber Connection for SCADA/DCS

BFOC 2.5 -(ST)-interface for multi-mode glass fiber type 62.5, as for IEC 874-10.
850nm short-haul fibers, one Tx and one Rx. For Courier, IEC-60870-5-103, MODBUS or DNP3.0 (but, see different ordering options for each model).

2.8 Optional Second Rear Communications Port (RP2)

EIA(RS)-232, 9 pin D-type female connector, socket SK4.
Courier protocol: K-Bus, EIA(RS)-232, or EIA(RS)485 connection.
Isolation to SELV level.
Maximum cable length 15m.

2.9 Optional Rear IRIG-B Interface (Modulated or Unmodulated)

BNC plug
Isolation to SELV level.
50 ohm coaxial cable.

2.10 Optional Rear Ethernet Connection for IEC 61850 or DNP 3.0

2.10.1 Optional Redundant Rear Ethernet Connection (optical)

2.10.1.1 100BaseTX Communications

Interface in accordance with IEEE802.3 and IEC 61850

Isolation:	1.5 kV
Connector type:	RJ45
Cable type:	Screened Twisted Pair (STP)
Max. cable length:	100 m

2.10.1.2 100Base FX Interface

Interface in accordance with IEEE802.3 and IEC 61850

Wavelength:	1310 nm
Fiber:	multi-mode 50/125 µm or 62.5/125 µm
Connector type:	LC Connector Optical Interface

3 RATINGS

3.1 AC Measuring Inputs

Nominal frequency:	50 and 60 Hz (settable)
Operating range:	45 to 66 Hz
Phase rotation:	ABC or ACB

3.2 AC Current

Nominal current (In):	1 and 5 A dual rated.	
Nominal burden:	Phase <0.2 VA at In Earth <0.2 VA at In	
Thermal withstand:	continuous 4 In	for 10 s: 30 In for 1 s; 100 In
Standard:	linear to 64 In (non-offset AC current).	

3.3 AC Voltage

Nominal voltage (Vn):	100 to 120 V
Nominal burden per phase:	< 0.06 VA at 110 V
Thermal withstand:	continuous 2 Vn for 10s: 2.6 Vn Linear to 200V (100V/120V).

4 POWER SUPPLY

4.1 Auxiliary Voltage (Vx)

Three ordering options:

(i) Vx: 24 to 32 Vdc

(ii) Vx: 48 to 125 Vdc

(iii) Vx: 110 to 250 Vdc, and 100 to 240Vac (rms)

4.2 Operating Range

(i) 19 to 38V (dc only for this variant)

(ii) 37 to 150V (dc only for this variant)

(iii) 87 to 300V (dc), 80 to 265 V (ac).

With a tolerable ac ripple of up to 15% for a dc supply, per EN / IEC 60255-11, EN / IEC 60255-26.

4.3 Nominal Burden

Quiescent burden: 11W or 24 VA. (Extra 1.25 W when fitted with second rear communications board).

Additions for energized binary inputs/outputs:

For each opto input:

0.09 W (24 to 54 V)

0.12 W (110/125 V)

0.19 W (220/250 V)

For each energized output relay: 0.13W

4.4 Power-Up Time

Time to power up	<25 s
Ethernet Communications	<70 s

4.5 Power Supply Interruption

Per IEC60255-26: 2013

The relay will withstand a 20 ms interruption in the DC auxiliary supply, without deenergizing except process bus relays operating between 37 and 43V which have a 10 ms withstand.

The relay will withstand a 20 ms interruption in an AC auxiliary supply, without deenergizing.

4.6 Battery Backup

Regulated 48 Vdc
Current limited at 112 mA maximum output
Operating range 40 to 60 V

4.7 Field Voltage Output

Regulated 48 Vdc
Current limited at 112 mA maximum output
Operating range 40 to 60 V

4.8 Digital ("Opto") Inputs

Universal opto inputs with programmable voltage thresholds (24/27, 30/34, 48/54, 110/125, 220/250 V). May be energized from the 48 V field voltage, or the external battery supply.

Rated nominal voltage: 24 to 250 Vdc

Operating range: 19 to 265 Vdc

Withstand: 300 Vdc, 300 Vrms.

Peak current of opto input when energized is 3.5 mA (0-300 V)

Nominal pick-up and reset thresholds:

Pick-up approx 70% of battery nominal set

Reset approx 66% of battery nominal set

Nominal battery 24/27: 60 - 80% DO/PU
(logic 0) <16.2 (logic 1) >19.2
Nominal battery 24/27: 50 - 70% DO/PU
(logic 0) <12.0 (logic 1) >16.8
Nominal battery 30/34: 60 - 80% DO/PU
(logic 0) <20.4 (logic 1) >24.0
Nominal battery 30/34: 50 - 70% DO/PU
(logic 0) <15.0 (logic 1) >21.0
Nominal battery 48/54: 60 - 80% DO/PU
(logic 0) <32.4 (logic 1) >38.4
Nominal battery 48/54: 50 - 70% DO/PU
(logic 0) <24.0 (logic 1) >33.6
Nominal battery 110/125: 60 - 80% DO/PU
(logic 0) <75.0 (logic 1) >88.0
Nominal battery 110/125: 50 - 70% DO/PU
(logic 0) <55.0 (logic 1) >77.0
Nominal battery 220/250: 60 - 80% DO/PU
(logic 0) <150.0 (logic 1) >176.0
Nominal battery 220/250: 50 - 70% DO/PU
(logic 0) <110 (logic 1) >154

Recognition time:

<2 ms with long filter removed.

<12 ms with half cycle ac immunity filter on.

5 OUTPUT CONTACTS

5.1 Standard Contacts

General purpose relay outputs for signaling, tripping and alarming:

Rated voltage:	300 V	
Continuous current:	10 A	
Short-duration current:	30 A for 3 s	
Making capacity:	250 A for 30 ms	
Breaking capacity:	DC: 50 W resistive	
	DC: 62.5 W inductive	(L/R = 50 ms)
	AC: 2500 VA resistive	(cos ϕ = unity)
	AC: 2500 VA inductive	(cos ϕ = 0.7)
	AC: 1250 VA inductive	(cos ϕ = 0.5)
Subject to maxima of 10 A and 300 V		
Response to command:	< 5 ms	
Durability:	Loaded contact:	10 000 operations minimum,
	Unloaded contact:	100 000 operations minimum.

5.2 High Break Contacts

Relay outputs for tripping:

Rated voltage:	300 V	
Continuous current:	10 A dc	
Short-duration current:	30 A dc for 3 s	
Making capacity:	250 A dc for 30 ms	
Breaking capacity:	DC: 7500 W resistive	
	DC: 2500 W inductive	(L/R = 50 ms)
	Subject to maxima of 10 A and 300 V	
	Response to command: < 0.2 ms	
Durability:	Loaded contact:	10 000 operations minimum,
	Unloaded contact:	100 000 operations minimum.

5.3 Watchdog Contacts

Non-programmable contacts for relay healthy or relay fail indication:

Breaking capacity:	DC: 30 W resistive
	DC: 15 W inductive (L/R = 40 ms)
	AC: 375 VA inductive (cos ϕ = 0.7)

5.4 IRIG-B 12X Interface (Modulated)

External clock synchronization to IRIG standard 200-98, format B12x
Input impedance 6 kΩ at 1000 Hz
Modulation ratio: 3:1 to 6:1
Input signal, peak-peak: 200 mV to 20 V

5.5 IRIG-B B00X Interface (Un-Modulated)

External clock synchronization to IRIG standard 200-98, format B00X.
Input signal TTL level
Input impedance at dc 10 kΩ

6 ENVIRONMENTAL CONDITIONS

6.1 Ambient Temperature Range

Per EN 60068-2-1 & EN / IEC 60068-2-2

Operating temperature range:	-25°C to +55°C (or -13°F to +131°F)
Storage and transit:	-25°C to +70°C (or -13°F to +158°F)

6.2 Ambient Humidity Range

Per EN /IEC 60068-2-78:

56 days at 93% relative humidity and +40 °C

Per EN / IEC 60068-2-14

5 cycles, -25°C to +55 °C
1°C / min rate of change

Per EN / IEC 60068-2-30

Damp heat cyclic, six (12 + 12) hour cycles, +25 to +55°C

6.3 Corrosive Environments

Per EN / IEC 60068-2-60, Part 2, Test Ke, Method (class) 3
Industrial corrosive environment/poor environmental control, mixed gas flow test.
21 days at 75% relative humidity and +30°C
Exposure to elevated concentrations of H_2S, (100 ppb), NO_2, (200 ppb) & Cl_2 (20 ppb).
Per EN / IEC 60068-2-52 Salt mist (7 days)
Per EN / IEC 60068-2-43 for H_2S (21 days), 15 ppm
Per EN / IEC 60068-2-42 for SO_2 (21 days), 25 ppm

7 TYPE TESTS

7.1 Insulation

Per EN / IEC 60255-27:
Insulation resistance > 100 MΩ at 500 Vdc
(Using only electronic/brushless insulation tester).

7.2 Creepage Distances and Clearances

Per EN / IEC 60255-27:
Pollution degree 3, Overvoltage category III,

7.3 High Voltage (Dielectric) Withstand

(EIA RS-232 ports excepted and normally-open contacts of output relays excepted).

(i) As for EN / IEC 60255-27:

2 kV rms AC, 1 minute:
Between all independent circuits.
Between independent circuits and case earth (ground).
1 kV rms AC for 1 minute, across open watchdog contacts.
1 kV rms AC for 1 minute, across open contacts of changeover output relays.
1 kV rms AC for 1 minute for all D-type EIA(RS)-232 or EIA(RS)-485 ports between the communications port terminals and protective (earth) conductor terminal.
1 kV rms AC for 1 minute between RJ45 ports and the case earth (ground).

(ii) As for ANSI/IEEE C37.90:

1.5 kV rms AC for 1 minute, across open contacts of normally open output relays.
1 kV rms AC for 1 minute, across open watchdog contacts.
1 kV rms AC for 1 minute, across open contacts of changeover output relays.

7.4 Impulse Voltage Withstand Test

As for EN / IEC 60255-27:

(i) Front time: 1.2 µs, Time to half-value: 50 µs,
Peak value: 5 kV, 0.5 J
Between all independent circuits.
Between independent circuits and case earth ground.

(ii) Front time: 1.2 µs, Time to half-value: 50 µs,
Peak value: 1.5kV, 0.5 J
Between RJ45 ports and the case earth (ground).
EIA(RS)-232 & EIA(RS)-485 ports and normally open contacts of output relays excepted.

8 ELECTROMAGNETIC COMPATIBILITY (EMC)

8.1 1 MHz Burst High Frequency Disturbance Test

As for EN / IEC 60255-22-1, Class III,

Common-mode test voltage:	2.5 kV,
Differential test voltage:	1.0 kV,
Test duration:	2 s,
Source impedance:	200 Ω

(EIA(RS)-232 ports excepted).

8.2 100 kHz and 1 Mhz Damped Oscillatory Test

EN / IEC 61000-4-18:	Level 3
Common mode test voltage:	2.5 kV
Differential mode test voltage:	1 kV

8.3 Immunity to Electrostatic Discharge

As for EN / IEC 60255-22-2, EN / IEC 61000-4-2:

15kV discharge in air to user interface, display, communication ports and exposed metalwork.

6kV contact discharge to the screws on the front of the front communication ports.

8kV point contact discharge to any part of the front of the product.

8.4 Electrical Fast Transient or Burst Requirements

As for EN / IEC 60255-22-4, Class B:

±4.0 kV, 5kHz and 100kHz applied to all inputs / outputs excluding communication ports

±2.0 kV, 5kHz and 100kHz applied to all communication ports

As for EN / IEC 61000-4-4, severity level 4:

±2.0 kV, 5kHz and 100kHz applied to all inputs / outputs and communication ports excluding power supply and earth.

±4.0 kV, 5kHz and 100kHz applied to all power supply and earth port

Rise time of one pulse:	5 ns
Impulse duration (50% value):	50 ns
Burst duration:	15 ms or 0.75ms
Burst cycle:	300 ms
Source impedance:	50 Ω

8.5 Surge Withstand Capability

As for IEEE/ANSI C37.90.1:
4 kV fast transient and 2.5 kV oscillatory
applied directly across each output contact, optically isolated input, and power supply circuit.

8.6 Surge Immunity Test

As for EN / IEC 61000-4-5, EN / IEC 60255-26:

Time to half-value:	1.2 to 50 µs,
Amplitude:	4 kV between all groups and case earth (ground),
Amplitude:	2 kV between terminals of each group.
Amplitude:	1kV for LAN ports

8.7 Conducted/Radiated Immunity

For RTDs used for tripping applications the conducted and radiated immunity performance is guaranteed only when using totally shielded RTD cables (twisted leads).

8.8 Immunity to Radiated Electromagnetic Energy

Per EN / IEC 61000-4-3 and EN / IEC 60255-22-3, Class 3

Test field strength, frequency band 80 to 1000 MHz and
1.4 GHz to 2.7GHz: 10 V/m,
Test using AM: 1 kHz / 80%
Spot tests at: 80, 160, 450, 900, 1850, 2150 MHz

Per IEEE/ANSI C37.90.2:

80MHz to 1000MHz, zero and 100% square wave modulated.
Field strength of 35V/m.

8.9 Radiated Immunity from Digital Communications

As for EN / IEC61000-4-3, Level 4:
Test field strength, frequency band 800 to 960 MHz,
and 1.4 to 2.0 GHz: 30 V/m, Test using AM: 1 kHz/80%.

8.10 Radiated Immunity from Digital Radio Telephones

As for EN / IEC 61000-4-3: 10 V/m, 900 MHz and 1.89 GHz.

8.11 Immunity to Conducted Disturbances Induced by Radio Frequency Fields

As for EN / IEC 61000-4-6, Level 3, Disturbing test voltage: 10 V.

8.12 Power Frequency Magnetic Field Immunity

As for EN / IEC 61000-4-8, Level 5,

100 A/m applied continuously, 1000 A/m applied for 3 s.

As for EN / IEC 61000-4-9, Level 5,

1000 A/m applied in all planes.

As for EN / IEC 61000-4-10, Level 5,

100 A/m applied in all planes at 100 kHz and 1 MHz with a burst duration of 2 s.

8.13 Conducted Emissions

As for CISPR 22 Class A:

Power supply:

0.15 - 0.5 MHz, 79 dBµV (quasi peak) 66 dBµV (average)
0.5 - 30 MHz, 73 dBµV (quasi peak) 60 dBµV (average)

Permanently connected communications ports:

0.15 - 0.5MHz, 97dBµV (quasi peak) 84dBµV (average)
0.5 - 30MHz, 87dBµV (quasi peak) 74dBµV (average)

8.14 Radiated Emissions

As for CISPR 22 Class A:

30 to 230 MHz, 40 dBµV/m at 10m measurement distance

230 to 1 GHz, 47 dBµV/m at 10 m measurement distance.

1 – 3GHz, 76dBµV/m (peak), 56dBµV/m (average) at 3m measurement distance.

3 – 5GHz, 80dBµV/m (peak), 60dBµV/m (average) at 3m measurement distance.

9 EU DIRECTIVES

9.1 EMC Compliance

Electromagnetic Compatibility Directive (EMC) 2014/30/EU	Compliance demonstrated via a Technical File, with reference to EMC standards.

The following Product Specific Standard was used to establish compliance:

EN 60255-26: 2013

9.2 Product Safety

The following European directives may be applicable to the equipment, if so it will carry the relevant marking(s) shown below:

CE Compliance with all relevant European Community directives:

Product safety: Low Voltage Directive (LVD) 2014/35/EU EN 60255-27: 2014 EN 60255-1: 2010	Compliance demonstrated via a Technical File, with reference to product safety standards.

9.3 R&TTE Compliance

Radio and Telecommunications Terminal Equipment (R&TTE) directive 99/5/EC.

Compliance demonstrated by compliance to both the EMC directive and the Low voltage directive, down to zero volts.

Applicable to rear communications ports.

10 MECHANICAL ROBUSTNESS

10.1 Vibration Test

Per EN / IEC 60255-21-1	Response Class 2 Endurance Class 2

10.2 Shock and Bump

Per EN / IEC 60255-21-2	Shock response Class 2 Shock withstand Class 1 Bump Class 1

10.3 Seismic Test

Per EN / IEC 60255-21-3:	Class 2

11 PROTECTION FUNCTIONS

11.1 Transformer Differential Protection

Accuracy

Pick-up: formula ±5%
Drop-off: 95% of formula ±5%
Pick-up and drop-off repeatability: <1%
Low set differential element operating time:
<33 ms using normal contact, and
<28 ms using high-break contact, for currents applied at 3x pickup level or greater
High set 1 differential element operating time:
<15 ms for currents applied at 2x pickup level or greater
High set 2 differential element operating time:
<25 ms for currents applied at 2x pickup level or greater
DT operating time: ±5% or <33 ms using normal contact, and
<28 ms using high-break contact, for currents applied at 3x pickup level or greater
Operating time repeatability: < 2 ms
Disengagement time: <15 ms

11.2 Circuitry Fault Alarm

Accuracy

Pick-up:	formula ±5%
Drop-off:	0.95 of formula ±5%
Pick-up and drop-off repeatability:	<4%
Instantaneous operating time:	<26 ms at 2.5x pick-up value
Disengagement time:	<26 ms
Operating time repeatability:	<8 ms
Timer:	±2% or 50 ms, whichever is greater
ID>1 Alarm Timer:	±2% or 50 ms, whichever is greater

11.3 Low Impedance Restricted Earth Fault

Accuracy

Pick-up:	formula ±5%
Drop-off:	0.90 × formula ±5%
Pick-up and drop-off repeatability	<5%

Low impedance operating time: <45 ms for currents applied at 2x pickup level or greater

High impedance operating time:	<30 ms

Low impedance DT operation: < 45 ms for currents applied at 2x pickup level or greater

Operating time repeatability:	<5 ms
Disengagement time:	<30 ms

11.4 High Impedance Restricted Earth Fault

Accuracy

Pick-up:	formula ±5%
Drop-off:	0.90 × formula ±5%
Pick-up and drop-off repeatability:	<5%
High impedance operating time:	<30 ms
Operating time repeatability:	<5 ms
Disengagement time:	<30 ms

11.5 Through Fault Monitoring

Accuracy

TF I> pick-up:	setting ±5% or 50 mA whichever is greater
TF I> drop-off:	0.95 of setting ±5% or 50 mA whichever is greater
TF I^2t> pick-up:	setting ±2% or 5A^2s whichever is greater

12 SYSTEM BACK-UP

12.1 Transient Overreach and Overshoot

Accuracy

Additional tolerance due to increasing X/R ratios:	±5% over X/R 1 to 120
Overshoot of overcurrent elements:	<40 ms
Disengagement time:	<30 ms

12.2 Non-Directional/Directional Phase Sequence Overcurrent and Voltage Controlled Overcurrent

Accuracy

Pick-up:		Setting ±5% or 20 mA whichever is greater
Drop-off:		0.95 x Setting ±5% or 20 mA whichever is greater
$V_{VCO/VRO}$ pick-up:		Setting ±5% or 50 mV whichever is greater
$V_{VCO/VRO}$ drop-off:		0.95 × Setting ±5% or 50 mV whichever is greater
V_{POL} pick-up:		Setting ±5% or 50 mV whichever is greater
V_{POL} drop-off:		0.95 × Setting ±5% or 50 mV whichever is greater
Pick-up and drop-off repeatability:		<1%
Operating boundary pick-up:		±2% of RCA
Operating boundary hysteresis:		<2°
Operating boundary repeatability:		<2%
Instantaneous operating time:		< 60ms
Disengagement time:		<35ms
Operating time repeatability:		<6 ms
Characteristic:	UK curves:	IEC 60255-3 – 1998
	US curves:	IEEEC37.112 - 1996

12.3 Negative Phase Sequence Overcurrent

Accuracy

I2>Pick-up:		Setting ±5% or 20 mA, whichever is greater
I2> Drop-off:		0.95 x Setting ±5% or 20 mA, whichever is greater
Vpol Pick-up:		Setting ±5% or 50 mV whichever is greater
Vpol Drop-off:		0.95 x Setting ±5% or 50 mV, whichever is greater
Pick-up and drop-off repeatability:		<1%
Operating boundary pick-up:		±2° of RCA ±90°
Operating boundary hysteresis:		< 2°
Operating boundary repeatability:		<2%
DT operation:		±2% or 65 ms, whichever is greater
Instantaneous operating time:		<65 ms
Disengagement time:		<35 ms
Operating time repeatability:		<6 ms
Characteristic:	UK curves:	IEC 60255-3 - 1998
	US curves:	IEEEC37.112 - 1996

12.4 Thermal Overload

Accuracy

Hot Spot> Pick-up:	Expected pick-up time ±5% or 50ms whichever is greater (expected pick-up time is the time required to reach the temperature setting)
Hot Spot> DT:	±5%or 50 ms whichever is greater
Top Oil> Pick-up:	Expected Pick-up Time ±5% or 50ms whichever is greater (expected pick-up time is the time required to reach the temperature setting)
Top Oil> DT:	±5%or 50 ms whichever is greater
Repeatability:	<2.5%

12.5 Non-Directional/Directional Earth Fault

Accuracy

Measured pick-up:	Setting ±5% or 20mA whichever is greater
Measured drop-off:	95% × setting ±5% or 20mA whichever is greater
Derived pick-up:	Setting ±5% or 20mA whichever is greater
Derived drop-off:	90% × setting ±5% or 20mA whichever is greater
Pick-up and drop-off repeatability:	<1%
Vpol pick-up:	Vpol ± 5% or 50mV whichever is greater
Vpol drop-off:	0.95 × Vpol ± 5% or 50mV whichever is greater
Operating boundary pick-up:	±2% of RCA
Operating boundary hysteresis:	<1°
Operating boundary repeatability:	<1%
Instantaneous operating time:	< 60ms
Disengagement time:	<35 ms
Operating time repeatability:	<6 ms

12.6 2-Stage Neutral Displacement or Residual Overvoltage

Accuracy

Pick-up VN>	±5% or 50 mV whichever is greater
Drop-off:	0.95 x Setting ±5%
Pick-up and Drop-off Repeatability:	<1%
IDMT shape:	±2% or 55 ms whichever is greater
DT operation:	±2% or 70 ms whichever is greater
Reset:	<50 ms
Timer repeatability:	<10 ms
Disengagement time	<35 ms

12.7 Volts/Hz

Accuracy

Pick-up:	V/Hz> ±5%
Drop-off:	98% of V/Hz> ±5%
Repeatability (operating threshold):	<1%
IDMT operating time:	±5% or 50 ms whichever is greater
Definite time:	±2% or 50 ms whichever is greater
Instantaneous Operation:	<50 ms
Disengagement time:	<50 ms
Repeatability (operating times):	<10 ms
V/Hz measurement:	±1%
Reset time:	±2% or 50 ms whichever is greater

12.8 2-Stage Undervoltage

Accuracy

Pick-up for DT and IDMT:	Setting ±5%
Drop-off:	1.02 x Setting ±5%
IDMT shape:	±2% or 50 ms whichever is greater
DT operation:	±2% or 50 ms whichever is greater
Reset:	<50 ms
Repeatability:	<1%

12.9 2-Stage Overvoltage

Accuracy

DT Pick-up:	Setting ±5%
IDMT Pick-up:	Setting ±5%
Drop-off:	0.98 x Setting ±5%
IDMT characteristic shape:	±2% or 50 ms whichever is greater
DT operation:	±2% or 50 ms whichever is greater
Reset:	<50 ms
Repeatability:	<1%

12.10 1-Stage NPS Overvoltage

Accuracy

Pick-up:	Setting ±5%
Drop-off:	0.95 x Setting ±5%
Repeatability (operating threshold):	<1%
Instantaneous operating time (accelerated mode)	<50 ms
Instantaneous operating time (normal mode)	<60 ms
DT operation (accelerated mode):	±2% or 50 ms whichever is greater
DT operation (normal mode):	±2% or 100 ms whichever is greater
Disengagement time:	<35 ms
Operating time repeatability:	<52 ms

12.11 4-Stage Underfrequency

Accuracy

Pick-up:	Setting ±0.01 Hz
Drop-off:	(Setting +0.025 Hz) ±0.01 Hz
DT operation:	±2% or 70 ms whichever is greater.
Repeatability:	<1%

The operation also includes a time for the relay to frequency track (20 Hz/second)

12.12 2-Stage Overfrequency

Accuracy

Pick-up:	Setting ±0.01 Hz
Drop-off:	(Setting -0.025 Hz) ±0.01 Hz
Repeatability:	<1%
DT operation:	±2% or 70 ms whichever is greater.

The operation also includes a time for the relay to frequency track (20 Hz/second)

12.13 CB Fail

Accuracy

I < Pick-up:	110% of setting ±5% or 20 mA whichever is greater
I < Drop-off:	100% of setting ±5% or 20 mA whichever is greater
Pick-up and drop-off repeatability:	<1%
Timers:	±2% or 50 ms whichever is greater
Disengagement time:	<30ms
Reset time:	< 1 cycle fully offset current waveforms considered

12.14 Pole Dead

I > Pick-up:	Fixed Threshold (50 mA) ±20 mA
I > Drop-off:	Fixed Threshold (55 mA) ±20 mA
V< Pick-up:	Fixed Threshold (10 V) ±5%
V< Drop-off:	Fixed Threshold (30 V) ±5%
Instantaneous operation:	< 50 ms

13 SUPERVISION FUNCTIONS

13.1 Voltage Transformer Supervision (VTS)

Accuracy

VTS I> Pick-up: Setting ±5% or 50 mA whichever is greater
VTS I> Drop-off: 90% of setting ±5% or 50 mA whichever is greater
VTS I2> Pick-up: Setting ±5% or 50 mA whichever is greater
VTS I2> Drop-off: 95% of setting ±5% or 50 mA whichever is greater
P643/P645 models:
VTS V< Pick-up: Fixed Threshold (10 V) ±5%
VTS V< Drop-off: Fixed Threshold (30 V) ±5%
P642 model:
VTS V< Pick-up: Fixed Threshold (70 V) ±5%
VTS V< Drop-off: Fixed Threshold (95 V) ±5%
VTS V2> Pick-up: Fixed Threshold (10 V) ±5%
VTS V2> Drop-off: Fixed Threshold (9.5 V) ±5%
Pick-up and drop-off repeatability: <1%
Fast block operation: <25 ms
Fast block reset: <30 ms
Time delay: Setting ±2% or 50 ms whichever is greater

13.2 Differential Current Transformer Supervision (CTS)

Accuracy

CTS I1 Pick-up ratio:	Setting ±5% or 20 mA whichever is greater
CTS I2/I1>1 Pick-up ratio:	95% of setting ±5% or 20 mA whichever is greater
CTS I2/I1>2 Pick-up ratio:	105% of setting ±5% or 20 mA whichever is greater
CTS I1 Drop-off ratio:	95% of setting ±5% or 20 mA whichever is greater
CTS I2/I1>1 Drop-off ratio:	setting ±5% or 20 mA whichever is greater
CTS I2/I1>2 Drop-off ratio:	setting ±5% or 20 mA whichever is greater
Pick-up and drop-off repeatability:	<3%
Time delay operation:	±2% or 50 ms whichever is greater
CTS terminal block operation:	<25 ms
CTS differential block operation	< 30 ms
CTS reset	< 25 ms
CTS Disengagement time	<30 ms

14 PROGRAMMABLE SCHEME LOGIC

Output conditioner timer:	Setting ±2% or 50 ms whichever is greater
Dwell conditioner timer:	Setting ±2% or 50 ms whichever is greater
Pulse conditioner timer:	Setting ±2% or 50 ms whichever is greater

15 MEASUREMENTS AND RECORDING FACILITIES

15.1 Measurements

Accuracy

Current:	0.05 to 3 In:	±1% or 3 mA of reading
Voltage:	0.05 to 2 Vn:	±1% of reading
Power (W):	0.2 to 2 Vn, 0.05 to 3 In:	±5% of reading at unity power factor
Reactive Power (VArs):	0.2 to 2 Vn, 0.05 to 3 In:	±5% of reading at zero power factor
Apparent Power (VA):	0.2 to 2 Vn, 0.05 to 3 In:	±5% of reading
Energy (Wh):	0.2 to 2 Vn, 0.2 to 3 In:	±5% of reading at zero power factor
Energy (Varh):	0.2 to 2 Vn, 0.2 to 3 In:	±5% of reading at zero power factor
Phase accuracy:	0° to 360°:	±0.5°
Frequency:	5 to 70 Hz:	±0.025 Hz

15.2 IRIG-B and Real-Time Clock

Performance

Year 2000:	Compliant
Real time accuracy:	< ±1 second / day
External clock synchronisation:	Conforms to IRIG standard 200-98, format B

Features

Real time 24 hour clock settable in hours, minutes and seconds
Calendar settable from January 1994 to December 2092
Clock and calendar maintained via battery after loss of auxiliary supply
Internal clock synchronization using IRIG-B Interface for IRIG-B signal is BNC

15.3 Current Loop Inputs and Outputs

Accuracy

Current loop input accuracy:	±1% of full scale
CLI drop-off threshold Under:	setting ±1% of full scale
CLI drop-off threshold Over:	setting ±1% of full scale
CLI sampling interval:	50 ms
CLI instantaneous operating time:	< 200 ms for 20 Hz to 70 Hz; < 300 ms for 5 Hz to 20 Hz
CLI DT operating time:	±2% setting or 150 ms whichever is the greater for 20 Hz to 70 Hz; ±2% setting or 200 ms whichever is the greater for 5 Hz to 20 Hz
CLO conversion interval:	50 ms
CLO latency:	< 1.07 s or <70 ms depending on CLO output parameter's internal refresh rate - (1 s or 0.5 cycle)
Current loop output accuracy:	±0.5% of full scale
Repeatability:	<5%

CLI - Current Loop Input
CLO - Current Loop Output

Other Specifications

CLI load resistance 0-1 mA:	< 4 kΩ
CLI load resistance 0-1 mA/0-20 mA /4-20 mA:	<300 Ω
Isolation between common input channels:	zero
Isolation between input channels and case earth/other circuits:	2 kV rms for 1 minute
CLO compliance voltage 0-1 mA / 0 10 mA:	10 V
CLO compliance voltage 0-20 mA / 4-20 mA:	8.8 V
Current Loop output open circuit voltage:	< 15 V

15.4 Disturbance Records

Accuracy

Magnitude and relative phases:	±5% of applied quantities
Duration:	±2%
Trigger Position:	±2% (minimum 100 ms)
Record length:	50 records each 1.5 s duration 75 s total memory with 19, 26 or 30 analog channels and 32 digital channels.

15.5 Event, Fault and Maintenance Records

Maximum 512 events in a cyclic memory
Maximum 5 fault records
Maximum 10 maintenance records
Accuracy
Event time stamp resolution: 1 ms

15.6 IEC 61850 Ethernet Data

15.6.1 100 Base FX Interface

15.6.1.1 Transmitter Optical Characteristics (LC)

Parameter	Sym	Min.	Typ.	Max.	Unit
Output Optical Power 62.5/125 µm, NA = 0.275 Fiber	PO	-20	-17.0	-14	dBm avg.
Output Optical Power 50/125 µm, NA = 0.20 Fiber	PO	-23.5	-20.0	-14	dBm avg.
Optical Extinction Ratio				10	dB
Output Optical Power at Logic "0" State	PO ("0")			-45	dBm avg.

Table 1 - Transmitter optical characteristics (LC)

15.6.1.2 Receiver Optical Characteristics (LC)

Parameter	Sym	Min.	Typ.	Max.	Unit
Input Optical Power	PIN	-31		-14	dBm avg.
Note: The 10BaseFL connection will no longer be supported as IEC 61850 does not specify this interface.					

Table 2 - Receiver optical characteristics (LC)

16 SETTINGS LIST

16.1 Global Settings (System Data)

Language:	English/French/German/Spanish English/French/German/Russian Chinese/English/French
Frequency:	50/60 Hz
IEC61850 Edition	1 or 2
ETH COMM Mode	Dual IP, PRP or HSR

16.2 Date and Time

IRIG-B Sync:	Disabled/Enabled
Battery Alarm:	Disabled/Enabled
LocalTime Enable:	Disabled/Fixed/Flexible
LocalTime Offset:	-720 min…720 min
DST Enable:	Disabled/Enabled
DST Offset:	30 min…60 min
DST Start:	First/Second/Third/Fourth/Last
DST Start Day:	Sun/Mon/Tues/Wed/Thurs/Fri/Sat
DST Start Month:	Jan/Feb/Mar/Apr/May/Jun/Jul/Aug/Sept/Oct/Nov/Dec
DST Start Mins:	0 min…1425 min
DST End:	First/Second/Third/Fourth/Last
DST End Day:	Sun/Mon/Tues/Wed/Thurs/Fri/Sat
DST End Month:	Jan/Feb/Mar/Apr/May/Jun/Jul/Aug/Sept/Oct/Nov/Dec
DST End Mins:	0 min…1425 min
RP1 Time Zone:	UTC/Local
RP2 Time Zone:	UTC/Local
Tunnel Time Zone:	UTC/Local

16.3 Configuration

Restore Defaults:	No Operation/All settings, Setting Group 1, Setting Group 2, Setting Group 3, Setting Group 4
Setting Group:	Select from Menu / Select from Opto
Active Settings:	Group 1/2/3/4
Save Changes:	No Operation / Save / Abort
Copy From:	Group 1/2/3/4
Copy To:	Group 1/2/3/4
Setting Group 1:	Disabled/Enabled
Setting Group 2:	Disabled/Enabled
Setting Group 3:	Disabled/Enabled
Setting Group 4:	Disabled/Enabled

Diff Protection	Disabled/Enabled
REF Protection	Disabled/Enabled
Overcurrent	Disabled/Enabled
NPS Overcurrent	Disabled/Enabled
Thermal Overload	Disabled/Enabled
Earth Fault	Disabled/Enabled
Residual O/V NVD	Disabled/Enabled
V/Hz	Disabled/Enabled
Through Fault	Disabled/Enabled
Volt Protection	Disabled/Enabled
Freq Protection	Disabled/Enabled
RTD Inputs	Disabled/Enabled
CB Fail	Disabled/Enabled
Supervision:	Disabled/Enabled
Input Labels:	Invisible/Visible
Output Labels:	Invisible/Visible
RTD Labels:	Invisible/Visible
CT & VT Ratios:	Invisible/Visible
Record Control	Invisible/Visible
Disturb Recorder:	Invisible/Visible
Measure't Setup:	Invisible/Visible
Comms Settings:	Invisible/Visible
Commission Tests:	Invisible/Visible
Setting Values:	Primary/Secondary
Control Inputs:	Invisible/Visible
CLIO Inputs:	Disabled/Enabled
CLIO Outputs:	Disabled/Enabled
Ctrl I/P Config:	Invisible/Visible
Ctrl I/P Labels:	Invisible/Visible
Direct Access:	Disabled/Enabled/Hotkey
IEC GOOSE:	Invisible/Visible
Function Keys:	Invisible/Visible
LCD Contrast:	0…31

16.4 CT and VT Ratios

Main VT Location	HV/LV/TV		
Aux' VT Location	HV/LV		
Main VT Primary:	100...1 000 000 V		
Main VT Secondary:	80...140 V (100/120 V)		
Aux' VT Primary:	100...1 000 000 V		
Aux' VT Secondary:	80...140 V (100/120 V)		
T1 CT:	CT Polarity	/	Standard/Inverted
CT Primary:	1 A…60 kA		
CT Secondary:	1 A / 5 A		
T2 CT:	CT Polarity	/	Standard/Inverted
CT Primary:	1 A…60 KA		
CT Secondary:	1 A / 5 A		
T3 CT:	CT Polarity	/	Standard/Inverted
CT Primary:	1 A…60 KA		
CT Secondary:	1 A / 5 A		
T4 CT:	CT Polarity	/	Standard/Inverted
CT Primary:	1 A…60 KA		
CT Secondary:	1 A / 5 A		
T5 CT:	CT Polarity	/	Standard/Inverted
CT Primary:	1 A…60 KA		
CT Secondary:	1 A / 5 A		
TN1 CT:	CT Polarity	/	Standard/Inverted
CT Primary:	1 A…60 KA		
CT Secondary:	1 A / 5 A		
TN2 CT:	CT Polarity	/	Standard/Inverted
CT Primary:	1 A…60 KA		
CT Secondary:	1 A / 5 A		
TN3 CT:	CT Polarity	/	Standard/Inverted
CT Primary:	1 A…60 KA		
CT Secondary:	1 A / 5 A		

16.5 Sequence of Event Recorder (Record Control)

Clear Events:	No/Yes
Clear Faults:	No/Yes
Clear Maint:	No/Yes
Alarm Event:	Disabled/Enabled
Relay O/P Event:	Disabled/Enabled
Opto Input Event:	Disabled/Enabled
General Event:	Disabled/Enabled
Fault Rec Event:	Disabled/Enabled
Maint Rec Event:	Disabled/Enabled
Protection Event:	Disabled/Enabled
Clear Dist Recs:	No/Yes
DDB 31 - 0:	*(up to):*
DDB 2047 - 2016:	Binary function link strings selects which DDB signals are stored as events and which are filtered out.

16.6 Oscillography (Disturbance Recorder)

Duration:	0.10…10.50 s
Trigger Position:	0.0…100.0%
Trigger Mode:	Single/Extended
Analog Channel 1:	*(up to):*
Analog Channel 30	depending on model):
Disturbance channels	selected from:
	IA-1 / IB-1 / IC-1 / IN-1 / IA-2 / IB-2 / IC-2 / IN-2, etc (*depending on model)*
Digital Input 1:	*(up to):*
Digital Input 32:	Selected binary channel assignment from any DDB status point in the relay such as opto input, output contact, alarms, starts, trips, controls, logic.
Input 1 Trigger:	No Trigger /
(up to):	Trigger L/H/
Input 32 Trigger:	Trigger H/L
Notes	L/H (Low to High) H/L (High to Low)

16.7 Measured Operating Data (Measure't Setup)

Default Display:	3Ph + N Current / 3Ph Neutral Voltage / Power / Date and Time / Description / Plant Reference / Frequency
Access Permissions	
Local Values:	Primary/Secondary
Remote Values:	Primary/Secondary
Measurement Ref:	Vx, VA, VB, VC, IA1, IB1, IC1, IA2, IB2, IC2, IA3, IB3, IC3, IA4, IB4, IC4, IA5, IB5, IC5, VAB or VBC
Measurement Mode:	0 / 1 / 2 / 3

16.8 Communications

RP2 Protocol:	(data)	
RP1 Address:	(Courier or IEC870-5-103): 0…254	
RP1 Address:	*(DNP3.0):* 0…65519	
RP1 Address:	*(MODBUS):* 1…247	
RP1 InactivTimer:	1…30 mins	
RP1 Baud Rate:	(IEC870-5-103):	9600/19200/38400 bits/s
RP1 Baud Rate:	(MODBUS, Courier):	9600/19200/38400 bits/s
RP1 Baud Rate:	*(DNP3.0):*	9600/19200/38400 bits/s
RP1 Parity:	Odd/Even/None	(MODBUS, DNP3.0)
RP1 Meas Period:	1…60 s	(IEC870-5-103)
RP1 PhysicalLink:	Copper (EIA(RS)-485 or K bus) or Fiber Optic	
RP1 Time Sync:	Disabled/Enabled	

MODBUS IEC Timer:	Standard/Reverse
RP1 CS103Blocking:	Disabled Monitor Blocking Command Blocking
RP1 Card Status:	(data) K-Bus OK EIA485 OK Fiber Optic OK (Courier)
RP1 Port Config:	*(Courier):* K Bus EIA485 (RS485)
RP1 Comms Mode:	*(Courier):*
IEC60870 FT1.2	IEC60870 10-bit, no parity
RP1 Baud Rate:	9600/19200/38400 bits/s

Note	*If RP1 Port Config is K Bus the baudrate is fixed at 64 kbits/s*

DNP Need Time:	1…30 mins
DNP App Fragment:	100…2048 bytes
DNP App Timeout:	1…120 s
DNP SBO Timeout:	1…10 s
DNP Link Timeout:	0.1…60 s
MAC Addr 1	Factory Setting
MAC Addr 2	Factory Setting
MAC Addr 3	Factory Setting
IP Address	0.0.0.0. The default IP address is encoded from the MAC address. 169.254.2.zzz, zzz = mod (The last byte of MAC3, 128) + 1.
Subnet Mask	255.255.255.0
Gateway	169.254.2.250

16.9 Optional Ethernet or Redundant Ethernet Port

NIC Protocol:	data
NIC MAC Address:	data
NIC Tunl Timeout:	1...30 mins
NIC Link Timeout:	0.1...60 s

16.10 Optional Additional Second Rear Communication (Rear Port2 (RP2))

RP2 Protocol:	(data)
RP2 Card Status:	(data) Unsupported Card not fitted EIA232 OK EIA485 OK Kbus OK
RP2 Port Config:	EIA(RS)-232 / EIA(RS)-485 / K-Bus
RP2 Comms Mode:	IEC60870 FT1.2 IEC60870 10-bit no parity
RP2 Address:	0…255
RP2 InactivTimer:	1…30 mins
RP2 Baud Rate:	9600/19200/38400 bits/s

Note	*If RP2 Port Config is K Bus the baud rate is fixed at 64 kbits/s*

DNP Need Time:	1…30 mins
DNP App Fragment:	100…2048 bytes
DNP App Timeout:	1…120 s
DNP SBO Timeout:	1…10 s

16.11 Commission Tests

Opto I/P Status:	(data) indicates the status of the opto inputs.
Rly O/P Status:	(data) indicates the status of the output relays.
Test Port Status:	(data) indicates the status of monitor bits 1 to 8.
Monitor bit 1: (up to): Monitor bit 8:	Binary function link strings, selecting which DDB signals have their status visible in the Commissioning menu, for test purposes
Test Mode:	Disabled Test Mode Blocked Contacts
Test Pattern:	Configuration of which output contacts are to be energized when the contact test is applied

16.12 Opto Coupled Binary Inputs (Opto Config)

Global Nominal V: 24 – 27 V / 30 – 34 V / 48 – 54 V / 110 – 125 V / 220 – 250 V / Custom

Opto Input 1: (up to):

Opto Input #. (# = max. opto no. fitted):

Custom options allow independent thresholds to be set for each opto, from the same range as above.

Opto Filter Control: Binary function link string, selecting which optos have an extra 1/2 cycle noise filter, and which do not.

Characteristics: Standard 60% - 80% / 50% - 70%

16.13 Control Inputs into PSL (Ctrl. I/P Config.)

Hotkey Enabled:	Binary function link string, selecting which of the control inputs are driven from Hotkeys.
Control Input 1 (up to):	Latched/Pulsed
Control Input 32:	
Ctrl Command 1 (up to):	On/Off / Set/Reset / In/Out / Enabled/Disabled
Ctrl Command 32:	

16.14 Function Keys

Fn. Key Status 1 (up to) 10:	Disable / Lock / Unlock / Enable
Fn. Key 1 Mode (up to) 10:	Toggled/Normal
Fn. Key 1 Label (up to) 10:	User defined text string to describe the function of the particular function key.

16.15 IED Configurator

Switch Conf. Bank:	No Action/Switch Banks
Restore Conf.:	No Action or Restore MCL
IP Address 1	0.0.0.0. The default IP address is encoded from the MAC address. 169.254.0.xxx, xxx = mod (The last byte of MAC1, 128) + 1.
Subnet Mask 1	255.255.255.0
Gateway 1	169.254.0.250
IP Address 2	0.0.0.0. The default IP address is encoded from the MAC address. 169.254.1.yyy, yyy = mod (The last byte of MAC2, 128) + 1.
Subnet Mask 2	255.255.255.0
Gateway 2	169.254.1.250

16.16 IEC 61850 GOOSE

GoEna:	0000000000000000(bin)... 1111111111111111(bin)
Pub.Simul.Goose:	0000000000000000(bin)... 1111111111111111(bin)
Sub.Simul.Goose:	No/Yes

16.17 Control Input User Labels (Ctrl. I/P Labels)

Control Input 1:	User defined text string
(up to):	to describe the function
Control Input 32:	of the particular control input

16.18 Settings in Multiple Groups

Note	*All settings here onwards apply for setting groups # = 1 to 4.*

17 PROTECTION FUNCTIONS

17.1 System Config

Winding Config:	HV+LV+TV, HV+LV
Winding Type:	Conventional/Auto
HV CT Terminals:	00001
LV CT Terminals:	10000
TV CT Terminals:	00100
Ref power S:	100kVA to 5GVA
HV Connection:	D-Delta / Y-Wye / Z-Zigzag
HV Grounding:	Grounded/Ungrounded
HV Nominal:	100 V to 100 MV
HV Rating:	100 KVA to 5 GVA
Reactance:	1.00% to 100.00%
LV Vector Group:	0 to 11
LV Connection:	D-Delta / Y-Wye / Z-Zigzag
LV Grounding:	Grounded/Ungrounded
LV Nominal:	100 V to 100 MV
LV Rating:	100 kVA to 5 GVA
TV Vector Group:	0 to 11
TV Connection:	D-Delta / Y-Wye / Z-Zigzag
TV Grounding:	Grounded/Ungrounded
TV Nominal:	100 V to 100 MV
TV Rating:	100 kVA to 5 GVA
Match Factor CT1:	0.05 to 20
Match Factor CT2:	0.05 to 20
Match Factor CT3:	0.05 to 20
Match Factor CT4:	0.05 to 20
Match Factor CT5:	0.05 to 20
Phase Sequence:	Standard ABC / Reverse ACB
VT Reversal:	No Swap / A-B Swapped / B-C Swapped / C-A Swapped
CT1 Reversal:	No Swap / A-B Swapped / B-C Swapped / C-A Swapped
CT2 Reversal:	No Swap / A-B Swapped / B-C Swapped / C-A Swapped
CT3 Reversal:	No Swap / A-B Swapped / B-C Swapped / C-A Swapped
CT4 Reversal:	No Swap / A-B Swapped / B-C Swapped / C-A Swapped
CT5 Reversal:	No Swap / A-B Swapped / B-C Swapped / C-A Swapped

17.2 Differential Protection

Trans Diff:	Enabled/Disabled
Set Mode:	Simple/Advance
Is1:	100.0e-3 to 2.500 PU
K1:	0 to 150.0%
Is2:	100.0e-3 to 10 PU
K2:	15 to 150.00%
tDIFF LS:	0 to 10.00 s
Is-CTS:	100.0e-3 to 2.500 PU
Is-HS1:	2.500 to 32.00 PU
H2S status:	Enabled/Disabled
Is-HS2:	2.500 to 32.00 PU
Diff calc remove:	Enabled/Disabled
Transient bias:	Enabled/Disabled
Zero seq filt HV:	Enabled/Disabled
Zero seq filt LV:	Enabled/Disabled
Zero seq filt TV:	Enabled/Disabled
2nd harmonic blocked:	Enabled/Disabled
Ih(2)%>:	5.000 to 50.000%
Cross blocking:	Enabled/Disabled
CTSat and NoGap:	Enabled/Disabled
5th harm blocked:	Enabled/Disabled
Ih(5)%>:	0 to 100.00%
Circuitry Fail:	Enabled/Disabled
Is-cctfail>:	30.00e-3 to 1.000 PU
K-cctfail:	0 to 50.00%
tIs-cctfail>:	0 to 10.00 s

17.3 REF Protection

REF HV status:	LowZ REF/HighZ REF/Disabled
HV CT input:	TN1
HV IS1 Set:	0.02In to 1In
HV IS2 Set:	0.1In to 10In
HV IREF K1:	0 to 150.0%
HV IREF K2:	15.00 to 150.0%
HV tREF:	0 to 10.00 s
HV Trans. Bias	Enabled/Disabled
REF LV status:	LowZ REF/HighZ REF/Disabled
LV CT input:	TN2
LV IS1 Set:	0.02In to 1In
LV IS2 Set:	0.1In to 10In
LV IREF K1:	0 to 150.0%
LV IREF K2:	15.00 to 150.0%
LV tREF:	0 to 10.00 s
LV Trans. Bias	Enabled/Disabled
REF TV status:	LowZ REF/HighZ REF/Disabled
TV CT input:	TN3
TV IS1 Set:	0.02In to 1In
TV IS2 Set:	0.1In to 10In
TV IREF K1:	0 to 150.0%
TV IREF K2:	15.00 to 150.0%
TV tREF:	0 to 10.00 s
TV Trans. Bias	Enabled/Disabled
REF Auto status:	LowZ REF/HighZ REF/Disabled
Auto CT input:	TN1
Auto IS1 Set:	0.02In to 1In
Auto IS2 Set:	0.1In to 10In
Auto IREF K1:	0 to 150.0%
Auto IREF K2:	15.00 to 150.0%
Auto tREF:	0 to 10.00 s
Auto Trans. Bias	Enabled/Disabled

17.4 NPS Overcurrent

NPS O/C 1:	T1/T2/T3/T4/T5/HV winding/LV winding/TV winding
I2>1 Status:	Disabled/Enabled
I2>1 Char:	DT / IEC S Inverse / IEC V Inverse / IEC E Inverse / UK LT Inverse / UK Rectifier / RI / IEEE M Inverse / IEEE V Inverse / IEEE E Inverse / US Inverse / US ST Inverse
I2>1 Directional:	Non-directional, Directional Fwd, Directional Rev
I2>1 Current Set:	0.08 to 4.00 In
I2>1 Time Delay:	0.00 to 100.00 s
I2>1 TMS:	0.025 to 1.200
I2>1 Time Dial:	0.01 to 100.00
I2>1 K (RI):	0.10 to10.00
I2>1 Reset Char:	DT/Inverse
I2>1 tRESET:	0.00 to 100.00 s
I2>2 the same as I2>1	
I2>3 Status:	Disabled/Enabled
I2>3 Directional:	Non-directional, Directional Fwd, Directional Rev
I2>3 Current Set:	0.08 to 4.00 In
I2>3 Time Delay:	0.00 to 100.00 s
I2>4 the same as I2>3	
I2> VTS Blocking:	1111
I2> V2pol Set:	0.5 to 25V
I2> Char Angle:	-95° to 95°
NPS O/C 2 and NPS O/C 3 same as NPS O/C 1	

17.5 Phase Overcurrent

Overcurrent1:	T1/T2/T3/T4/T5/HV winding/LV winding/TV winding
I>1 Status:	Enabled/Disabled
I> 1 Char:	DT / IEC S Inverse / IEC V Inverse / IEC E Inverse / UK LT Inverse / UK Rectifier / RI / IEEE M Inverse / IEEE V Inverse / IEEE E Inverse / US Inverse / US ST Inverse
I>1 Direction:	Non-directional, Directional Fwd, Directional Rev
I>1 Current Set:	0.08 to 4.00 In
I>1 Time Delay:	0.00 to 100.00 s
I>1 TMS:	0.025 to 1.200
I>1 Time Dial:	0.01 to 100.00
I>1 K (RI):	0.10 to10.00
I>1 Reset Char:	DT/Inverse
I>1 tRESET:	0.00 to 100.00 s
I>2 the same as I>1	
I>3 Status:	Disabled/Enabled
I>3 Direction:	Non-directional, Directional Fwd, Directional Rev
I>3 Current Set:	0.08 to 32.00 In
I>3 Time Delay:	0.00 to 100.00 s
I>4 the same as I>3	
I> Char Angle:	-95° to 95°
I> Function Link:	1111
Overcurrent2 and Overcurrent3 the same as Overcurrent1	

17.6 V DEPENDANT O/C

V Dep OC>1 Mode:	VCO/VRO
V OC>1:	T1/T2/T3/T4/T5/HV winding/LV winding/TV winding
V OC>1 Char:	DT / IEC S Inverse / IEC V Inverse / IEC E Inverse / UK LT Inverse / UK Rectifier / RI / IEEE M Inverse / IEEE V Inverse / IEEE E Inverse / US Inverse / US ST Inverse
V OC>1 Direction:	Non-directional, Directional Fwd, Directional Rev
V OC>1 Curr' Set:	0.08 to 4.00 In
V OC>1 T Delay:	0.00 to 100.00 s
V OC>1 TMS:	0.025 to 1.200
V OC>1 Time Dial:	0.01 to 100.00
V OC>1 K (RI):	0.10 to10.00
V OC>1 Rst Char:	DT/Inverse
V OC>1 tRESET:	0.00 to 100.00 s
V OC>1 Angle:	-95° to 95°
V OC>1 V<1 Set:	5 V to 120.00 V
V OC>1 K Setting:	0.1 to 1
V OC>1 V<1 Set:	5 V to 120.00 V

V OC>2 the same as VCO>1

17.7 Thermal Overload

Mon't Winding:	HV/LV/TV/Biased Current
Ambient T:	RTD1 / RTD2 / RTD3 / RTD4 / RTD5 / RTD5 / RTD7 / RTD8 / RTD9 / RTD10 / AVERAGE / CLIO1 / CLIO2 / CLIO3 / CLIO4
Amb CLIO Type:	0-1 / 0-10 / 0-20 / 4-20 mA
Amb CLIO Min:	-9999 to +9999
Amb CLIO Max:	-9999 to +9999
Average Amb T:	-25.00 to +75.00 Cel
Top Oil T:	RTD1 / RTD2 / RTD3 / RTD4 / RTD5 / RTD5 / RTD7 / RTD8 / RTD9 / RTD10 / CALCULATED / CLIO1 / CLIO2 / CLIO3 / CLIO4
Top Oil CLIO Typ:	0-1 / 0-10 / 0-20 / 4-20 mA
Top Oil CLIO Min:	-9999 to +9999
Top Oil CLIO Max:	-9999 to +9999
IB:	0.1 to 4.0 PU
Rated NoLoadLoss:	0.1 to 100
Hot Spot overtop:	0.1 to 200.0 Cel
Top Oil overamb:	0.1 to 200.0 Cel
Cooling mode:	Cooling mode 1 / Cooling mode 2 / Cooling mode 3 / Cooling mode 4 / Select Via PSL
Cooling Status:	(data) Cooling mode 1 / Cooling mode 2 / Cooling mode 3 / Cooling mode 4 / Cooling mode 1
Winding exp m:	0.01 to 2.0
Oil exp n:	0.01 to 2.0
	Cooling mode 2, Cooling mode 3 and Cooling mode 4 same as Cooling mode 1
Hot spot rise co:	0.01 to 20.0 min
Top oil rise co:	1.0 to 1000.0 min
TOL Status:	Enabled/Disabled
Hot Spot>1 to 3 Set:	1.0 to 300.0 Cel
tHot Spot>1 to 3 Set:	0 to 60 k min
Top Oil>1 to 3 Set:	1.0 to 300.0 Cel
tTop Oil>1 to 3 Set:	0 to 60k min
tPre-trip Set:	0 to 60 k min
LOL Status:	Enabled/Disabled
Life Hours at HS:	1 to 300 000 hr
Designed HS temp:	1 to 200.0 Cel
Constant B Set:	1 to 100 000
FAA> Set:	0.1 to 30
tFAA> Set:	0 to 60 k min
LOL>1 Set:	0.1 to 300 000hr
tLOL> Set:	0 to 60 k min
Rst Life Hours:	0 to 300 000 hr

17.8 4-Stage Directional Earth Fault

Earth Fault 1:	Enabled, Disabled
EF 1 Input:	Measured / Derived
EF 1 Derived:	(data) T1/T2/T3/T4/T5/HV winding/LV winding/TV winding
EF 1 Measured:	(data) TN1/TN2/TN3
IN>1 Status:	Enabled/Disabled
IN>1 Char:	DT / IEC S Inverse / IEC V Inverse / IEC E Inverse / UK LT Inverse / RI / IEEE M Inverse / IEEE V Inverse / IEEE E Inverse / US Inverse / US ST Inverse / IDG
IN>1 Direction:	Non-directional, Directional Fwd, Directional Rev
IN>1 Current:	0.08 to 4 In
IN>1 IDG Is:	1 to 4 In
IN>1 Time Delay:	0.00 to 200.0 s
IN>1 TMS:	0.025 to 1.200
IN>1 Time Dial:	0.01 to 100.00
IN>1 K(RI):	0.1 to 10.00
IN>1 IDG Time:	1 to 2.00
IN>1 Reset Char:	DT, Inverse
IN>1 tRESET:	0.00 to 100.00 s
IN>2 same as IN>1	
IN>3 Status:	Disabled, DT
IN>3 Current:	0.08 to 32.00 In
IN>3 Time Delay:	0.00 to 200.00 s
IN>4 same as IN>3	

Earth fault 2 and Earth fault 3 same as Earth fault 1

The IDG curve is commonly used for time delayed earth fault protection in the Swedish market. This curve is available in stage 1 of the Earth Fault protection.

The IDG curve is represented by:

$$t = 5.8 - 1.35 \log_e \left(\frac{I}{IN > Setting} \right) \text{ in seconds}$$

Where:

I = Measured current

IN>Setting = An adjustable setting which defines the start point of the characteristic

Although the start point of the characteristic is defined by the "IN>" setting, the actual relay current threshold is a different setting called "IDG Is". The "IDG Is" setting is set as a multiple of "IN>".

An additional setting "IDG Time" is also used to set the minimum operating time at high levels of fault current.

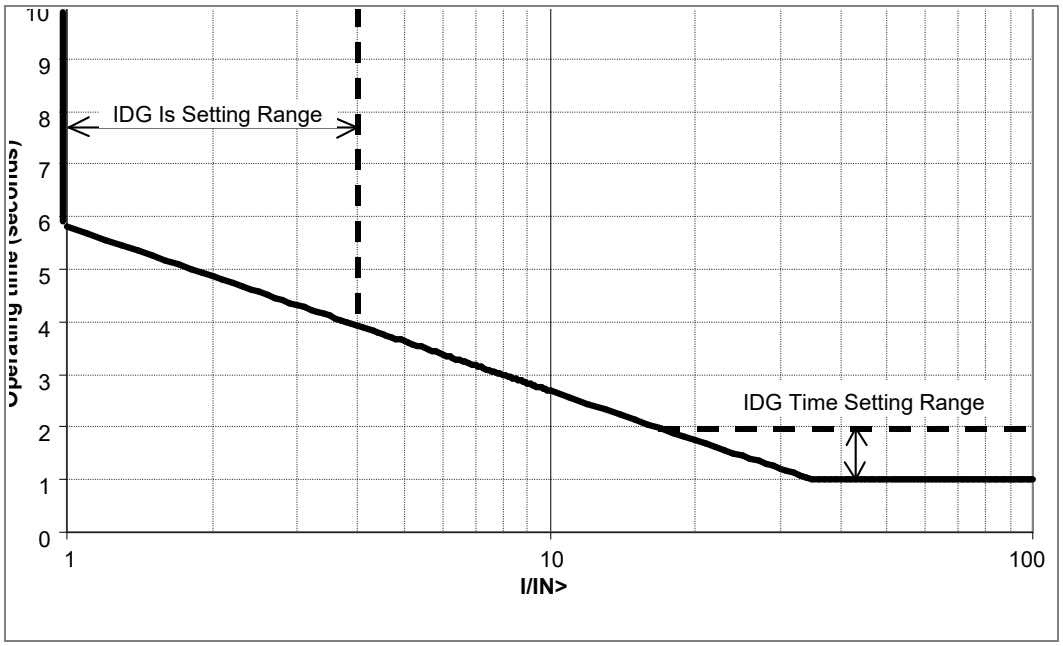


Figure 1 - IDG Characteristic

17.9 Through Fault

Through Fault:	Disabled/Enabled
Monitored Input:	HV / LV / TV
TF I> Trigger:	0.08 to 20.00PU
TF I2t> Alarm:	0 to 500 000 A2 s

17.10 Residual Overvoltage (NVD)

VN>1 Function:	Disabled/DT/IDMT
VN>1 Voltage Set:	1 to 80 V
VN>1 Time Delay:	0 to 100 s
VN>1 TMS:	0.5 to 100
VN>1 tReset:	0 to 100 s
VN>2 Status:	Enabled/Disabled
VN>2 Voltage Set:	1 to 80 V
VN>2 Time Delay:	0 to 100 s

17.11 Overfluxing (Volts/Hz)

Volts/Hz W2

V/Hz Alm Status:	Disabled/Enabled
V/Hz Alarm Set:	1.5 to 3.5 V/Hz
V/Hz Alarm Delay:	0 to 6000 s
V/Hz>1 Status:	Disabled/Enabled
V/Hz>1 Trip Func:	DT / IDMT
V/Hz>1 Trip Set:	1.5 to 3.5 V/Hz
V/Hz>1 Trip TMS:	0.01 to 12
V/Hz>1 Delay:	0 to 6000 s
V/Hz>1 tReset:	0 to 6000 s
V/Hz>2 Status:	Disabled/Enabled
V/Hz>2 Trip Set:	1.5 to 3.5 V/Hz
V/Hz>2 Delay:	0 to 6000 s

V/Hz>3 and 4 same as V/Hz>2

TPre-trip Alarm:	1 to 6000.0 s

Volts/Hz W1 the same as Volts/Hz W2

The inverse time characteristic is given by

$$t = \frac{TMS}{(M - 1)^2}$$

Where:

$$M = \frac{V/f}{(\text{V/f Trip Setting})}$$

V = Measured voltage
F = Measured frequency

17.12 Voltage Protection - Undervoltage

V< Measur't Mode:	Phase-Phase/Phase-Neutral
V< Operate Mode:	Any Phase/Three Phase
V< 1 Function:	Disabled/DT/IDMT
V<1 Voltage Set:	10 to 120 V (100/120 V)
V<1 Time Delay:	0.00 to 00.00 s
V<1 TMS:	0.05 to 100.0
V<1 Poledead Inh:	Disabled/Enabled
V<2 Function:	Disabled/DT
V<2 Status:	Disabled/Enabled
V<2 Voltage Set:	10 to 120 V (100/120 V)
V<2 Time Delay:	0.00 to 100.00 s
V<2 Poledead Inh:	Disabled/Enabled

The inverse characteristic is given by:

$$t = \frac{K}{(1 - M)}$$

Where:
K = Time multiplier setting
t = Operating time in seconds
M = Applied input voltage/ undervoltage setting

17.13 Voltage Protection - Overvoltage

V> Measur't Mode: Phase-Phase/Phase-Neutral
V> Operate Mode: Any Phase/Three Phase
V> 1 Function: Disabled/DT/IDMT
V>1 Voltage Set: 60 to 185 V(100/120 V)
V>1 Time Delay: 0.00 to 100.00 s
V>1 TMS: 0.05 to 100.0
V>2 Status: Disabled/Enabled
V>2 Voltage Set: 60 to 185 V (100/120 V)
V>2 Time Delay: 0.00 to 100.00 s

The inverse characteristic is given by:

$$t = \frac{K}{(M - 1)}$$

Where:
K = Time multiplier setting
t = Operating time in seconds
M = Applied input voltage/overvoltage setting

17.14 Voltage Protection - NPS Overvoltage

V2>1 Status: Enabled/Disabled
V2>1 Voltage Set: 1 to 110 V
V2>1 Time Delay: 0 to 100 s

17.15 Frequency Protection - Underfrequency

F<1 Status: Disabled/Enabled
F<1 Setting: 46.00 to 65.00 Hz
F<1 Time Delay: 0 to 100.0 s
F<2/3/4 the same as F<1

17.16 Frequency Protection - Overfrequency

F>1 Status: Disabled/Enabled
F>1 Setting: 46.00 to 65.00 Hz
F>1 Time Delay: 0 to 100.0 s
F>2 the same as F>1

17.17 RTD Protection

Select RTD: Bit 0 - Select RTD 1, Bit 1 - Select RTD 2 to Bit 9 - Select RTD 10
Binary function link string, selecting which RTDs (1 - 10) are enabled.

RTD 1 Alarm Set: 0°C to 200°C
RTD 1 Alarm Dly: 0 s to 100 s
RTD 1 Trip Set: 0°C to 200°C
RTD 1 Trip Dly: 0 s to 100 s
RTD2/3/4/5/6/7/8/9/10 the same as RTD1

17.18 Current Loop Input

CLIO1 Input 1:	Disabled/Enabled
CLI1 Input Type:	0 – 1 mA 0 – 10 mA 0 – 20 mA 4 – 20 mA
CLI1 Input Label:	16 characters (CLIO input 1)
CLI1 Minimum:	-9999…+9999
CLI1 Maximum:	-9999…+9999
CLI1 Alarm:	Disabled/Enabled
CLI1 Alarm Fn:	Over/Under
CLI1 Alarm Set:	CLI1 min to CLI1 max
CLI1 Alarm Delay:	0.0 to 100.0 s
CLI1 Trip:	Disabled/Enabled
CLI1 Trip Fn:	CLI1 min to CLI1 max
CLI1 Trip Delay:	0.0 to 100.0 s
CLI1 I< Alarm (4 to 20 mA input only):	Disabled/Enabled
CLI1 I< Alm Set (4 to 20 mA input only):	0.0 to 4.0 mA

CLI2/3/4 the same as CLI1

17.19 Current Loop Output

CLO1 Output 1:	Disabled/Enabled
CLO1 Output Type:	0 – 1 mA 0 – 10 mA 0 – 20 mA 4 – 20 mA
CLO1 Set Values:	Primary/Secondary
CLO1 Parameter:	As shown below*
CLO1 Min:	Range, step size and unit corresponds to the selected parameter
CLO1 Max:	Same as CLO1 Min

CLO2/3/4 the same as CLO1

Current Loop Output Parameters:

IA-1 Magnitude	I1-4 Magnitude	VAN Magnitude
IB-1 Magnitude	I2-4 Magnitude	VBN Magnitude
IC-1 Magnitude	I0-4 Magnitude	VCN Magnitude
IA-2 Magnitude	I1-5 Magnitude	Vx Magnitude
IB-2 Magnitude	I2-5 Magnitude	VN Derived Mag
IC-2 Magnitude	I0-5 Magnitude	V1 Magnitude
IA-3 Magnitude	IA HV Magnitude	V2 Magnitude
IB-3 Magnitude	IB HV Magnitude	V0 Magnitude
IC-3 Magnitude	IC HV Magnitude	VAN RMS
IA-4 Magnitude	IN HV Measured Mag	VBN RMS
IB-4 Magnitude	IN HV Derived Mag	VCN RMS
IC-4 Magnitude	IA LV Magnitude	Frequency
IA-5 Magnitude	IB LV Magnitude	RTD 1 through to RTD 10
IB-5 Magnitude	IC LV Magnitude	CL Input 1 through to CL Input 4
IC-5 Magnitude	IN LV Measured Mag	Volts/Hz W1
I1-1 Magnitude	IN LV Derived Mag	V/Hz W1 Thermal
I2-1 Magnitude	IA TV Magnitude	Volts/Hz W2
I0-1 Magnitude	IB TV Magnitude	V/Hz W2 Thermal
I1-2 Magnitude	IC TV Magnitude	Hot Spot T
I2-2 Magnitude	IN TV Measured Mag	Top Oil T
I0-2 Magnitude	IN TV Derived Mag	Ambient T
I1-3 Magnitude	VAB Magnitude	LOL Status
I2-3 Magnitude	VBC Magnitude	
I0-3 Magnitude	VCA Magnitude	

17.20 CB Fail & I<

T1 CBF Status:	Enabled/Disabled
I< Current Set:	5% to 400%
IN< Status:	Enabled/Disabled
IN< Input:	Measured/Derived
IN< Terminal:	TN1/TN2/TN3
IN< Current Set:	5% to 400%
CB Fail 1 Status:	Enabled/Disabled
CB Fail 1 Timer:	0 to 10s
CB Fail 2 Status:	Enabled/Disabled
CB Fail 2 Timer:	0 to 10s
CBF Non I Reset:	I< Only / CB Open & I< / Prot Reset & I<
CBF Ext Reset:	I< Only / CB Open & I < / Prot Reset & I<

T2 CBF, T3 CBF, T4 CBF and T5 CBF the same as T1 CBF

18 LABELS

18.1 Input Labels

Opto Input 1 to 32: Input L1 to Input L32
User-defined text string to describe the function of the particular opto input.

18.2 Output Labels

Relay 1 to 32: Output R1 to Output R32
User-defined text string to describe the function of the particular relay output contact.

18.3 RTD Labels

RTD 1-10: RTD1 to RTD10
User-defined text string to describe the function of the particular RTD.

19 SUPERVISORY FUNCTIONS

19.1 Voltage Transformer Supervision

VTS Status:	Blocking/ Indication/ Disabled
VTS Reset Mode:	Manual/Auto
VTS Time Delay:	1.0 to 10.0 s
VTS I> Inhibit:	0.08 In to 32.0 In
VTS I2> Inhibit:	0.05 In to 0.50 In
Negative phase sequence voltage (V2):	10 V (100/120 V)
Phase overvoltage:	
Pick-up	30 V,
Drop-off	10 V (100/120 V)
Superimposed Current:	0.1 In

19.2 Current Transformer Supervision

Diff CTS:	Enabled/Disabled
CTS Status:	Restrain/Indication
CTS Time Delay:	0 to 10 s
CTS I1:	5 to 100%
CTS I2/I1>1:	5 to 100%
CTS I2/I1>2:	5 to 100%

20 MEASUREMENTS LIST

20.1 Measurements 1

20.1.1 P642

IA-1 Magnitude
IA-1 Phase Angle
IB-1 Magnitude
IB-1 Phase Angle
IC-1 Magnitude
IC-1 Phase Angle
IA-2 Magnitude
IA-2 Phase Angle
IB-2 Magnitude
IB-2 Phase Angle
IC-2 Magnitude
IC-2 Phase Angle
IA-HV Magnitude
IA-HV Phase Ang
IB-HV Magnitude
IB-HV Phase Ang
IC-HV Magnitude
IC-HV Phase Ang
IA-LV Magnitude
IA-LV Phase Ang
IB-LV Magnitude
IB-LV Phase Ang
IC-LV Magnitude
IC-LV Phase Ang
I0-1 Magnitude
I1-1 Magnitude
I2-1 Magnitude
IN-HV Mea Mag
IN-HV Mea Ang
IN-HV Deriv Mag
IN-HV Deriv Ang
I0-2 Magnitude
I1-2 Magnitude
I2-2 Magnitude
IN-LV Mea Mag
IN-LV Mea Ang
IN-LV Deriv Mag
IN-LV Deriv Ang
IA-HV RMS
IB-HV RMS
IC-HV RMS
IA-LV RMS
IB-LV RMS
IC-LV RMS
Vx Magnitude
Vx Phase Angle
V1 Magnitude
V2 Magnitude
VAB Magnitude
VAB Phase Angle
VBC Magnitude
VBC Phase Angle
VCA Magnitude
VCA Phase Angle
Frequency
IN-T1 Deriv Mag
IN-T1 Deriv Ang
IN-T2 Deriv Mag
IN-T2 Deriv Ang
IN-TN1 Mea Mag
IN-TN1 Mea Ang
IN-TN2 Mea Mag
IN-TN2 Mea Ang

20.1.2 P643

IA-1 Magnitude
IA-1 Phase Angle
IB-1 Magnitude
IB-1 Phase Angle
IC-1 Magnitude
IC-1 Phase Angle
IA-2 Magnitude
IA-2 Phase Angle
IB-2 Magnitude
IB-2 Phase Angle
IC-2 Magnitude
IC-2 Phase Angle
IA-3 Magnitude
IA-3 Phase Angle
IB-3 Magnitude
IB-3 Phase Angle
IC-3 Magnitude
IC-3 Phase Angle
IC-TV Phase Ang
I0-1 Magnitude
I1-1 Magnitude
I2-1 Magnitude
IN-HV Mea Mag
IN-HV Mea Ang
IN-HV Deriv Mag
IN-HV Deriv Ang
I0-2 Magnitude
I1-2 Magnitude
I2-2 Magnitude
IN-LV Mea Mag
IN-LV Mea Ang
IN-LV Deriv Mag
IN-LV Deriv Ang
I0-3 Magnitude
I1-3 Magnitude
I2-3 Magnitude
VCN Magnitude
VCN Phase Angle
Vx Magnitude
Vx Phase Angle
V1 Magnitude
V2 Magnitude
V0 Magnitude
VN Derived Mag
VN Derived Angle
VAB Magnitude
VAB Phase Angle
VBC Magnitude
VBC Phase Angle
VCA Magnitude
VCA Phase Angle
VAN RMS
VBN RMS
VCN RMS

IA-HV Magnitude
IA-HV Phase Ang
IB-HV Magnitude
IB-HV Phase Ang
IC-HV Magnitude
IC-HV Phase Ang
IA-LV Magnitude
IA-LV Phase Ang
IB-LV Magnitude
IB-LV Phase Ang
IC-LV Magnitude
IC-LV Phase Ang
IA-TV Magnitude
IA-TV Phase Ang
IB-TV Magnitude
IB-TV Phase Ang
IC-TV Magnitude
IN-TV Mea Mag
IN-TV Mea Ang
IN-TV Deriv Mag
IN-TV Deriv Ang
IA-HV RMS
IB-HV RMS
IC-HV RMS
IA-LV RMS
IB-LV RMS
IC-LV RMS
IA-TV RMS
IB-TV RMS
IC-TV RMS
VAN Magnitude
VAN Phase Angle
VBN Magnitude
VBN Phase Angle
Frequency
IN-T1 Deriv Mag
IN-T1 Deriv Ang
IN-T2 Deriv Mag
IN-T2 Deriv Ang
IN-T3 Deriv Mag
IN-T3 Deriv Ang
IN-TN1 Mea Mag
IN-TN1 Mea Ang
IN-TN2 Mea Mag
IN-TN2 Mea Ang
IN-TN3 Mea Mag
IN-TN3 Mea Ang

20.1.3 P645

IA-1 Magnitude
IA-1 Phase Angle
IB-1 Magnitude
IB-1 Phase Angle
IC-1 Magnitude
IC-1 Phase Angle
IA-2 Magnitude
IA-2 Phase Angle
IB-2 Magnitude
IB-2 Phase Angle
IC-2 Magnitude
IC-2 Phase Angle
IA-3 Magnitude
IA-3 Phase Angle
IB-3 Magnitude
IB-3 Phase Angle
IC-3 Magnitude
IC-3 Phase Angle
IA-4 Magnitude
IA-4 Phase Angle
IB-4 Magnitude
IB-4 Phase Angle
IC-4 Magnitude
IC-4 Phase Angle
IA-5 Magnitude
IA-5 Phase Angle
IB-5 Magnitude
IA-TV Magnitude
IA-TV Phase Ang
IB-TV Magnitude
IB-TV Phase Ang
IC-TV Magnitude
IC-TV Phase Ang
I0-1 Magnitude
I1-1 Magnitude
I2-1 Magnitude
IN-HV Mea Mag
IN-HV Mea Ang
IN-HV Deriv Mag
IN-HV Deriv Ang
I0-2 Magnitude
I1-2 Magnitude
I2-2 Magnitude
IN-LV Mea Mag
IN-LV Mea Ang
IN-LV Deriv Mag
IN-LV Deriv Ang
I0-3 Magnitude
I1-3 Magnitude
I2-3 Magnitude
IN-TV Mea Mag
IN-TV Mea Ang
IN-TV Deriv Mag
IN-TV Deriv Ang
VAN Magnitude
VAN Phase Angle
VBN Magnitude
VBN Phase Angle
VCN Magnitude
VCN Phase Angle
Vx Magnitude
Vx Phase Angle
V1 Magnitude
V2 Magnitude
V0 Magnitude
VN Derived Mag
VN Derived Angle
VAB Magnitude
VAB Phase Angle
VBC Magnitude
VBC Phase Angle
VCA Magnitude
VCA Phase Angle
VAN RMS
VBN RMS
VCN RMS
Frequency
IN-T1 Deriv Mag
IN-T1 Deriv Ang
IN-T2 Deriv Mag
IN-T2 Deriv Ang

IB-5 Phase Angle	I0-4 Magnitude	IN-T3 Deriv Mag
IC-5 Magnitude	I1-4 Magnitude	IN-T3 Deriv Ang
IC-5 Phase Angle	I2-4 Magnitude	IN-T4 Deriv Mag
IA-HV Magnitude	I0-5 Magnitude	IN-T4 Deriv Ang
IA-HV Phase Ang	I1-5 Magnitude	IN-T5 Deriv Mag
IB-HV Magnitude	I2-5 Magnitude	IN-T5 Deriv Ang
IB-HV Phase Ang	IA-HV RMS	IN-TN1 Mea Mag
IC-HV Magnitude	IB-HV RMS	IN-TN1 Mea Ang
IC-HV Phase Ang	IC-HV RMS	IN-TN2 Mea Mag
IA-LV Magnitude	IA-LV RMS	IN-TN2 Mea Ang
IA-LV Phase Ang	IB-LV RMS	IN-TN3 Mea Mag
IB-LV Magnitude	IC-LV RMS	IN-TN3 Mea Ang
IB-LV Phase Ang	IA-TV RMS	
IC-LV Magnitude	IB-TV RMS	
IC-LV Phase Ang	IC-TV RMS	

20.2 Measurements 2

20.2.1 P642

IA Differential	IREF Auto HighZ Op	RTD 1 label
IB Differential	Thermal Overload	RTD 2 label
IC Differential	Hot Spot T	RTD 3 label
IA Bias	Top Oil T	RTD 4 label
IB Bias	Reset Thermal	RTD 5 label
IC Bias	Ambient T	RTD 6 label
IA Diff 2H	TOL Pretrip left	RTD 7 label
IB Diff 2H	LOL status	RTD 8 label
IC Diff 2H	Reset LOL	RTD 9 label
IA Diff 5H	Rate of LOL	RTD 10 label
IB Diff 5H	LOL Aging Factor	RTD Open Cct
IC Diff 5H	Lres at designed	RTD Short Cct
IREF HV LoZ Diff	FAA,m	RTD Data Error
IREF HV LoZ Bias	Lres at FAA,m	Reset RTD Flags
IREF LV LoZ Diff	Volts/Hz	CLIO Input 1
IREF LV LoZ Bias	Volts/Hz W2	CLIO Input 2
IREF Auto LoZ Diff	V/Hz W2 tPretrip	CLIO Input 3
IREF Auto LoZ Bias	V/Hz W2 Thermal	CLIO Input 4
IREF HV HighZ Op	Reset V/Hz W2	
IREF LV HighZ Op		

20.2.2 P643 and P645

A Phase Watts	A Phase VA	3Ph Power Factor
A Phase Watts	A Phase VA	APh Power Factor
A Phase Watts	A Phase VA	BPh Power Factor
B Phase Watts	B Phase VA	CPh Power Factor
B Phase Watts	B Phase VA	3Ph WHours Fwd
B Phase Watts	B Phase VA	3Ph WHours Rev

C Phase Watts	C Phase VA	3Ph VArHours Fwd
C Phase Watts	C Phase VA	3Ph VArHours Rev
C Phase Watts	C Phase VA	3Ph W Fix Demand
A Phase VArs	3 Phase Watts	3Ph VArs Fix Dem
A Phase VArs	3 Phase Watts	3 Ph W Roll Dem
A Phase VArs	3 Phase Watts	3Ph VArs RollDem
B Phase VArs	3 Phase VArs	3Ph W Peak Dem
B Phase VArs	3 Phase VArs	3Ph VAr Peak Dem
B Phase VArs	3 Phase VArs	Reset Demand
C Phase VArs	3 Phase VA	
C Phase VArs	3 Phase VA	
C Phase VArs	3 Phase VA	

20.3 Measurements 3

20.3.1 P643 and P645

IA Differential	IREF TV HighZ Op	V/Hz W2 Thermal
IB Differential	IREF Auto HighZ Op	Reset V/Hz W2
IC Differential	Thermal Overload	RTD 1 label
IA Bias	Hot Spot T	RTD 2 label
IB Bias	Top Oil T	RTD 3 label
IC Bias	Reset Thermal	RTD 4 label
IA Diff 2H	Ambient T	RTD 5 label
IB Diff 2H	TOL Pretrip left	RTD 6 label
IC Diff 2H	LOL status	RTD 7 label
IA Diff 5H	Reset LOL	RTD 8 label
IB Diff 5H	Rate of LOL	RTD 9 label
IC Diff 5H	LOL Aging Factor	RTD 10 label
IREF HV LoZ Diff	Lres at designed	RTD Open Cct
IREF HV LoZ Bias	FAA,m	RTD Short Cct
IREF LV LoZ Diff	Lres at FAA,m	RTD Data Error
IREF LV LoZ Bias	Volts/Hz	Reset RTD Flags
IREF TV LoZ Diff	Volts/Hz W1	CLIO Input 1
IREF TV LoZ Bias	V/Hz W1 tPretrip	CLIO Input 2
IREF Auto LoZ Diff	V/Hz W1 Thermal	CLIO Input 3
IREF Auto LoZ Bias	Reset V/Hz W1	CLIO Input 4
IREF HV HighZ Op	Volts/Hz W2	
IREF LV HighZ Op	V/Hz W2 tPretrip	

Notes:

GETTING STARTED

CHAPTER 3

Date:	07/2018
Products covered by this chapter:	This chapter covers the specific versions of the MiCOM products listed below. This includes ***only*** the following combinations of Software Version and Hardware Suffix.
Hardware Suffix:	L (P642) M (P643/P645)
Software Version:	B4 - P64x (P642, P643 & P645)
Connection Diagrams:	10P642xx (xx = 01 to 10) 10P643xx (xx = 01 to 06) 10P645xx (xx = 01 to 09)

CONTENTS

FIGURES

TABLES

1 INTRODUCTION TO THE RELAY

Warning **Before carrying out any work on the equipment, you should be familiar with the contents of the latest issue of the Safety Guide, Safety Information and Technical Data chapters and the equipment rating label(s).**

1.1 User Interfaces and Menu Structure

The settings and functions of the MiCOM protection relay can be accessed both from the front panel keypad and LCD, and via the front and rear communication ports. Information on each of these methods is given in this section to describe how to start using the relay.

1.2 Front Panel

The following figure shows the front panel of the relay; the hinged covers at the top and bottom of the front panel are shown open. An optional transparent front cover physically protects the front panel. With the cover in place, access to the user interface is read-only. Removing the cover allows access to the relay settings and does not compromise the protection of the product from the environment.

When editing relay settings, full access to the relay keypad is needed. To remove the front cover:

1. Open the top and bottom covers, then unclip and remove the transparent cover. If the lower cover is secured with a wire seal, remove the seal.
2. Using the side flanges of the transparent cover, pull the bottom edge away from the relay front panel until it is clear of the seal tab.
3. Move the cover vertically down to release the two fixing lugs from their recesses in the front panel.

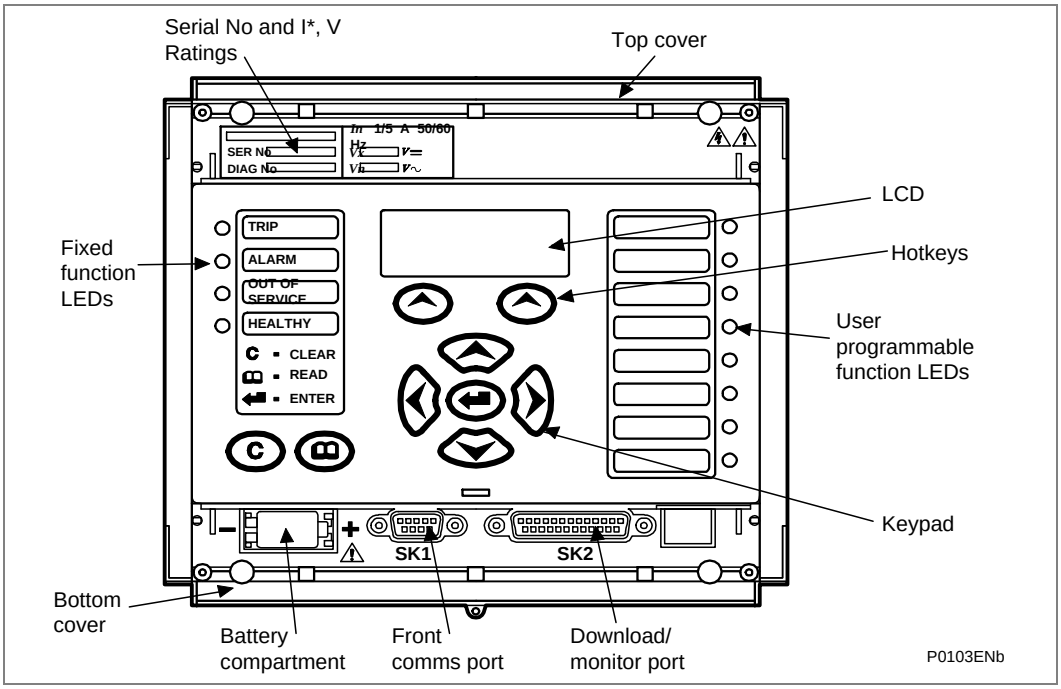


Figure 1 - Relay front view (P642) (40TE)

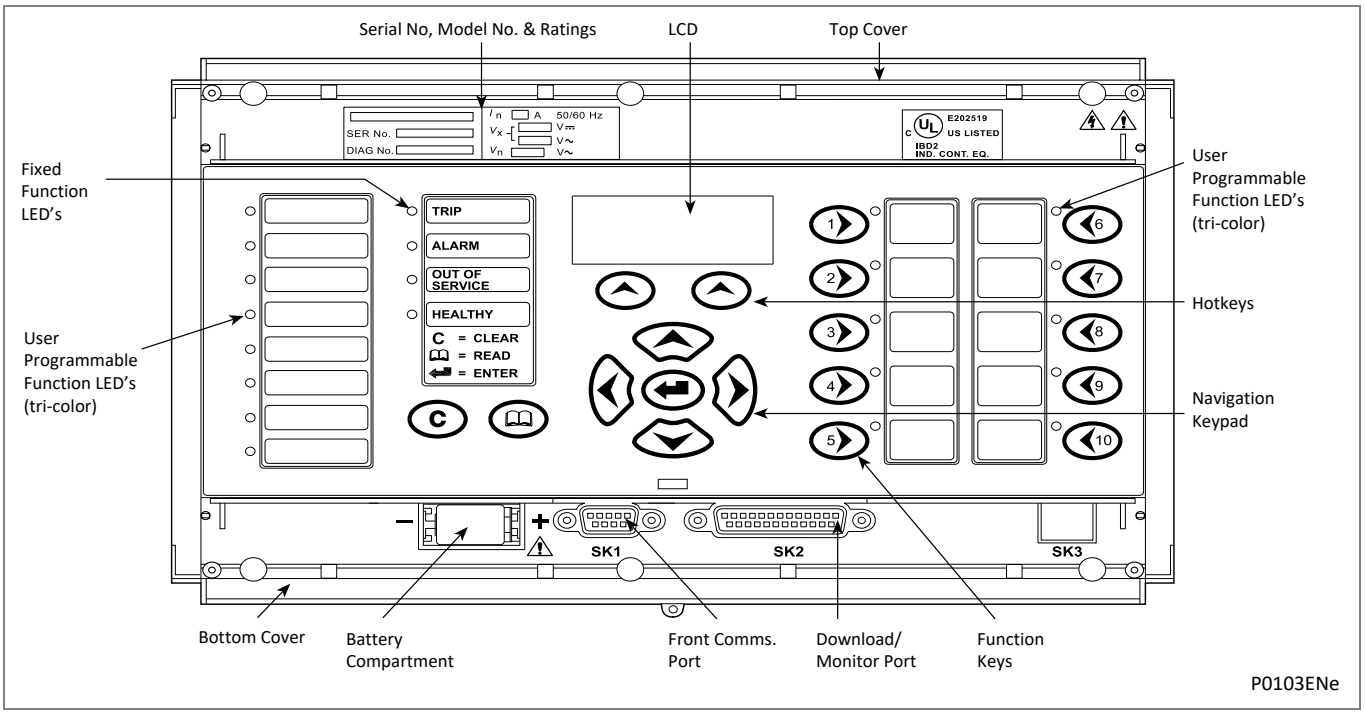


Figure 2 - Relay front view (P643 and P645) (60TE)

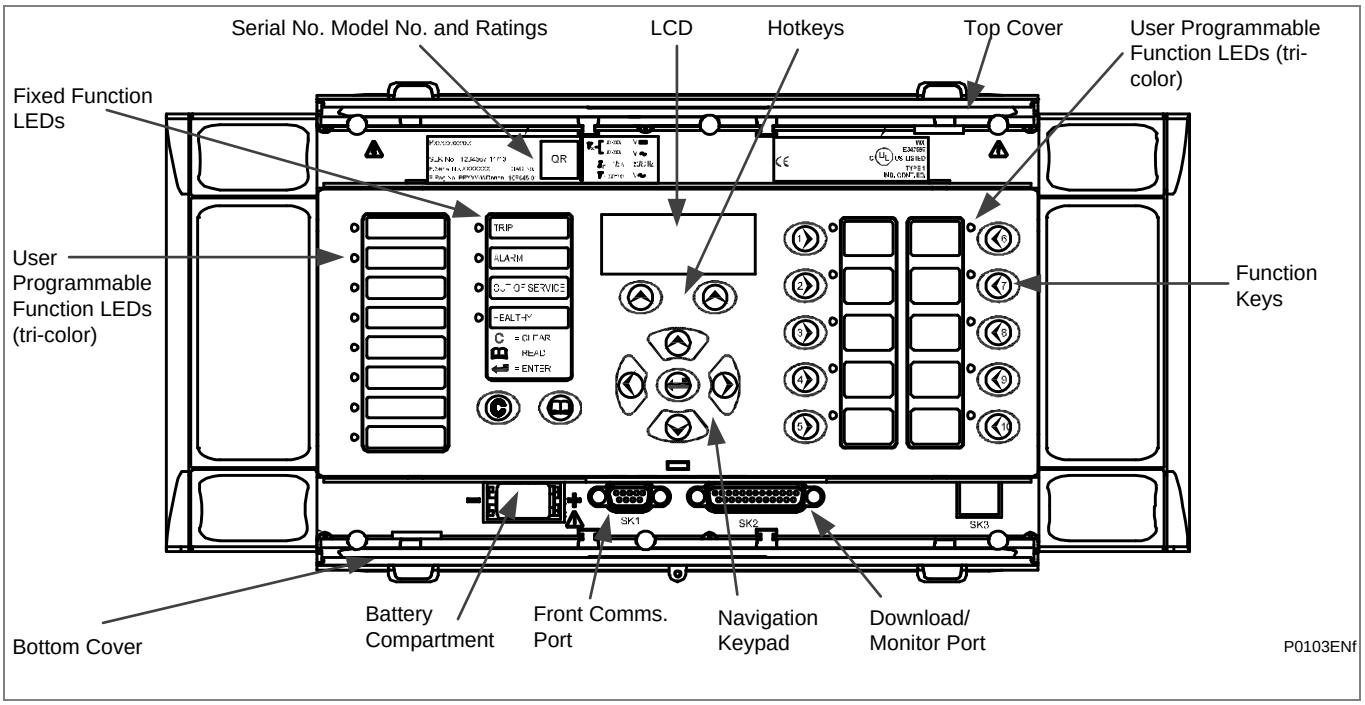


Figure 3 - Relay front view (P645) (80TE)

The front panel of the relay includes the following, as shown in the previous figures:

- A 16-character by 3-line alphanumeric Liquid Crystal Display (LCD).
- A 19-key (P643/P645), 9-key (P643) keypad with 4 arrow keys (⇦, ⇨, ⇧ and ⇩), an enter key (↵), a clear key (C), a read key (📖), 2 hot keys (⇧) and 10 (1 – 10) programmable function keys (P645).

Function Key Functionality (P643/P645):

- The relay front panel has control keys with programmable LEDs for local control. Factory default settings associate specific relay functions with these 10 direct-action keys and LEDs, e.g. Enable or Disable the auto-recloser function. Using programmable scheme logic, the user can change the default functions of the keys and LEDs to fit specific needs.
- Hotkey functionality:
  - **SCROLL** starts scrolling through the various default displays.
  - **STOP** stops scrolling the default display.

For control of setting groups, control inputs and circuit breaker operation:

- 22 LEDs (P643/P645), 12 LEDs (P642); 4 fixed function LEDs, 8 tri-color (P643/P645), 8 red (P642) programmable function LEDs on the left-hand side of the front panel and 10 tri-color programmable function LEDs on the right-hand side associated with the function keys (P643/P645).

Under the top hinged cover:

- The relay serial number, and the relay's current and voltage rating information

Under the bottom hinged cover:

- Battery compartment to hold the 1/2 AA size battery which is used for memory back-up for the real time clock, event, fault and disturbance records
- A 9-pin female D-type front port for communication with a PC locally to the relay (up to 15m distance) via an EIA(RS)232 serial data connection
- A 25-pin female D-type port providing internal signal monitoring and high speed local downloading of software and language text via a parallel data connection

1.2.1 LED Indications

1.2.1.1 Fixed Function

The Fixed Function LEDs on the left-hand side of the front panel show these conditions:

- **Trip (Red)** switches ON when the relay issues a trip signal. It is reset when the associated fault record is cleared from the front display. Also the trip LED can be configured as self-resetting.
- **Alarm (Yellow)** flashes when the relay registers an alarm. This may be triggered by a fault, event or maintenance record. The LED flashes until the alarms have been accepted (read), then changes to constantly ON. When the alarms are cleared, the LED switches OFF.
- **Out of Service (Yellow)** is ON when the relay is not fully operational.
- **Healthy (Green)** is ON when the relay is in correct working order, and should be ON at all times. It goes OFF if the relay's self-tests show there is an error in the relay's hardware or software. The state of the healthy LED is reflected by the watchdog contacts at the back of the relay.

To adjust the LCD contrast, from the **CONFIGURATION** column, select **LCD Contrast**. This is only needed in very hot or cold ambient temperatures.

1.2.1.2 Programmable LEDs

The P642 has eight red programmable LEDs (numbers 1 to 8) used for alarm indications.

The P643 and P645 have eight programmable LEDs (numbers 1 to 8) for alarm conditions and ten programmable LEDs (F1 to F10) to show the status of the function keys. All of the programmable LEDs on the P643 and P645 are tri-color and can be set to red, yellow or green.

The default behaviour and mappings for the programmable LEDs are shown here:

LED No	Default indication	P64x relay
1	Red	Differential trip
2	Red	REF trip - REF HV Trip, REF LV trip, REF TV trip

LED No	Default indication	P64x relay
3	Red	Top oil trip – Top oil 1 trip, Top oil 2 trip, Top oil 3 trip Hot spot trip – Hot spot 1 trip, Hot spot 2 trip, Hot spot 3 trip
4	Red	Overflux trip – W1 V/Hz>1, W1 V/Hz>2, W1 V/Hz>3, W1 V/Hz>4, W2 V/Hz>1, W2 V/Hz>2, W2 V/Hz>3, W2 V/Hz>4 Underfrequency trip – F<1, F<2, F<3, F<4 Overfrequency trip – F>1, F>2 Undervoltage trip – V<1, V<2 Overvoltage trip – V>1, V>2 Residual overvoltage trip - VN>1, VN>2
5	Red	HV overcurrent trip – POC 1I>1, POC 1I>2, POC 1 I>3, POC 1 I>4, HV earth fault trip – EF 1 IN>1, EF 1 IN>2, EF 1 IN>3, EF 1IN>4 HV NPOC trip – NPOC1I2>1, NPOC1 I2>2, NPOC I2>3, NPOC I2>4
6	Red	LV overcurrent trip – POC 2 I>1, POC 2 I>2, POC 2 I>3, POC 2 I>4, LV earth fault trip - EF 2 IN>1, EF 2 IN>2, EF 2 IN>3, EF 2 IN>4 LV NPSOC trip - NPOC2 I2>1, NPOC2 I2>2, NPOC2 I2>3, NPOC2 I2>4
7	Green	TV overcurrent trip – POC 3 I>1, POC 3 I>2, POC 3 I>3, POC 3 I>4 TV earth fault trip - EF 3 IN>1, EF 3 IN>2, EF 3 IN>3, EF 3 IN>4 TV NPOC trip - NPOC3 I2>1, NPOC3 I2>2, NPOC3 I2>3, NPOC3 I2>4
8	Red/Yellow/Green	CB Fail
F1	Red/Yellow/Green	Not used
F2	Red/Yellow/Green	Not used
F3	Red/Yellow/Green	Not used
F4	Red/Yellow/Green	Not used
F5	Red	Setting Group 2 Enabled
F6	Yellow	Overfluxing Reset
F7	Yellow	Thermal overload reset
F8	Yellow	Loss of life reset
F9	Yellow	Relay/LED reset
F10	Yellow	Manual Trigger Disturbance Recorder

Table 1 - Default settings

1.3 Relay Rear Panel

The following diagram shows the rear panel of the relay. Slots A and B are for optional IRIG-B boards providing time-synchronization input and fiber optic communications. Refer to the wiring diagrams in the *Connection Diagrams* chapter for further details.

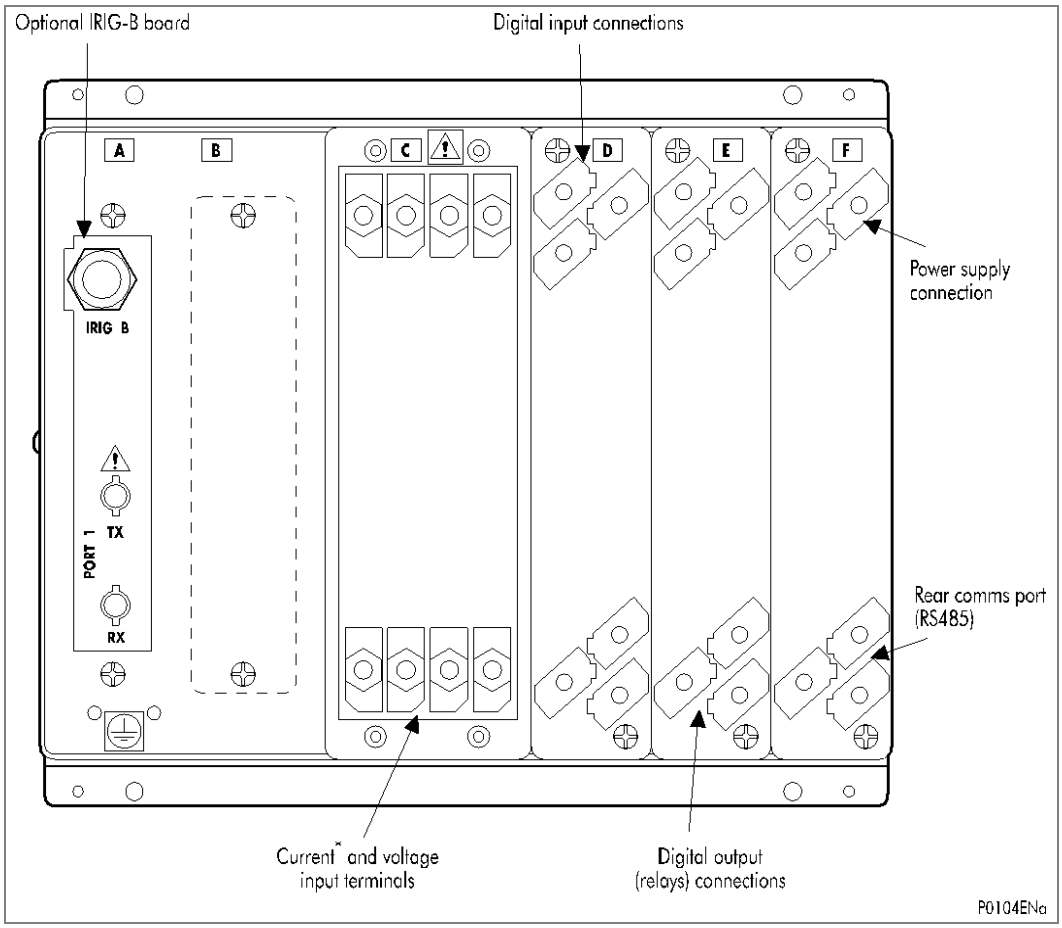


Figure 4 - P642 relay rear view

Note	*This is one example of a case layout. The exact layout will vary depending on model configuration and case size. Refer to the wiring diagrams in the Connection Diagrams chapter for complete connection details.*

1.4 Relay Connection and Power-Up

Before powering-up the relay, confirm that the relay power supply voltage and nominal ac signal magnitudes are appropriate for your application. The relay serial number, and the relay's current and voltage rating, power rating information can be viewed under the top hinged cover. The relay is available in the auxiliary voltage versions shown in this table:

Nominal Ranges		Operative Ranges	
dc	**ac**	**dc**	**ac**
24 – 32 V dc	-	19 - 38 V dc	-
48 – 110 V dc	-	37 - 150 V dc	-
110 – 250 V dc **	100 – 240 V ac rms **	87 - 300 V dc	80 - 265 V ac
** rated for ac or dc operation			

Table 2 - Nominal and Operative dc and ac Ranges

The relay has universal opto isolated logic inputs. These can be programmed for the nominal battery voltage of the circuit where they are used. See *Universal Opto isolated logic inputs* in the *Product Design* chapter for more information on logic input specifications.

Note	*The opto inputs have a maximum input voltage rating of 300 V dc at any setting.*

Once the ratings have been verified for the application, connect external power according to the power requirements specified on the label. See the *Connection Diagrams* chapter for complete installation details, ensuring the correct polarities are observed for the dc supply.

2 USER INTERFACES AND SETTINGS

The relay has these user interfaces:

- The front panel using the LCD and keypad
- The front port which supports Courier communication
- The rear port which supports one of these protocols:
  - Courier
  - MODBUS
  - IEC 60870-5-103
  - DNP3.0
- The optional Ethernet port supports IEC 61850-8-1 and DNP3.0
- A second optional rear port which supports Courier, KBUS communication protocol.

The protocol for the rear port must be specified when the relay is ordered.

	Keypad / LCD	Courier	MODBUS	IEC870-5-103	DNP3.0	IEC 61850
Display and modification of all settings	Yes	Yes				
Digital I/O signal status	Yes	Yes		Yes	Yes	Yes
Display/extraction of measurements	Yes	Yes		Yes	Yes	Yes
Display/extraction of fault records	Yes	Yes		Yes	Yes	Yes
Extraction of disturbance records		Yes		Yes	Yes	Yes
Programmable scheme logic settings		Yes				
Reset of fault and alarm records	Yes	Yes		Yes	Yes	Yes
Clear event and fault records	Yes	Yes			Yes	
Time synchronization		Yes		Yes	Yes	Yes
Control commands	Yes	Yes		Yes	Yes	Yes

Table 3 - User interfaces and settings

3 MENU STRUCTURE

The relay's menu is arranged in a table. Each setting in the menu is referred to as a cell, and each cell in the menu may be accessed using a row and column address. The settings are arranged so that each column contains related settings, for example all the disturbance recorder settings are contained within the same column. As shown in the following diagram, the top row of each column contains the heading that describes the settings contained within that column. Movement between the columns of the menu can only be made at the column heading level.

For a complete list of all of the menu settings see the *Settings* chapter and the *Menu Database* document.

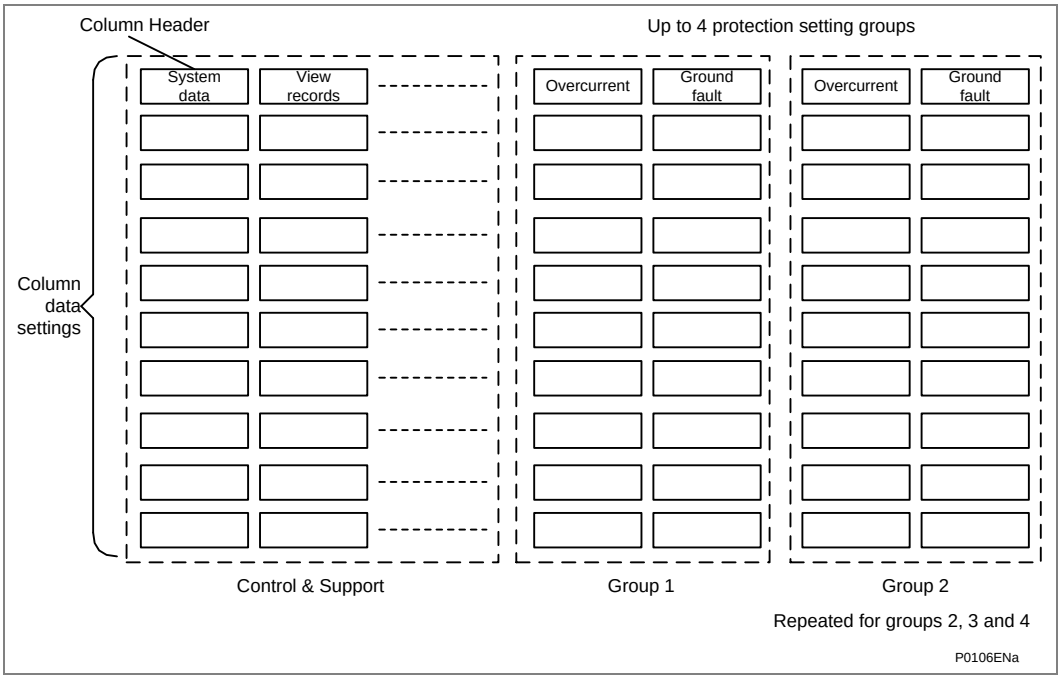


Figure 5 - Menu structure

The settings in the menu fall into one of these categories:

- Protection Settings
- Disturbance Recorder settings
- Control and Support (C&S) settings.

Different methods are used to change a setting depending on which category the setting falls into.

- C&S settings are stored and used by the relay immediately after they are entered.
- For either protection settings or disturbance recorder settings, the relay stores the new setting values in a temporary 'scratchpad'. It activates all the new settings together, but only after it has been confirmed that the new settings are to be adopted. This technique is employed to provide extra security, and so that several setting changes that are made within a group of protection settings will all take effect at the same time.

Additional security settings can now be gained by using Cyber Security. This is now an option for Software Release B2 and later.

3.1 Protection Settings

The protection settings include the following items:

- Protection element settings
- Scheme logic settings

There are four groups of protection settings (only two groups for the P24x), with each group containing the same setting cells. One group of protection settings is selected as the active group, and is used by the protection elements.

3.2 Disturbance Recorder Settings

The Disturbance Recorder (DR) settings include the record duration and trigger position, selection of analogue and digital signals to record, and the signal sources that trigger the recording.
The number of digital channels varies depending on the product and the software version.
For Software Version numbers A0 and B0, the disturbance recorder was enhanced so that the maximum number of digital channels was increased to 128.

There are now four additional ***DDB Group Sig x*** Nodes that can be mapped to individual or multiple DDBs in the PSL. These can then be set to trigger the DR via the DISTURBANCE RECORD menu.

These "Nodes" are general and can also be used to group signals together in the PSL for any other reason. These four nodes are available in each of the four PSL setting groups.

1. For a control input, the DR can be triggered directly by triggering directly from the Individual Control Input (e.g. Low to High (L to H) change)
2. For an input that cannot be triggered directly, or where any one of a number of DDBs are required to trigger a DR, map the DDBs to the new PSL Group sig n and then trigger the DR on this.

e.g. in the PSL:

In the DR Settings:

- Digital Input 1 is triggered by the PSL Group Sig 1 (L to H)
- Digital Input 2 is triggered by Control Input 1 (L to H)

If triggering on both edges is required map another DR channel to the H/L as well

Digital Input 4 is triggered by the PSL Group Sig 1 (H to L)

Digital Input 5 is triggered by Control Input 1 (H to L)

3.3 Control and Support Settings

The control and support settings include:

- Relay configuration settings
- Open/close circuit breaker (may vary according to relay type or model)
- CT & VT ratio settings
- Reset LEDs
- Active protection setting group
- Password & language settings
- Communications settings
- Measurement settings
- Event & fault record settings
- User interface settings
- Commissioning settings
- Circuit breaker control & monitoring settings (may vary according to relay type/model)

4 CYBER SECURITY

4.1 Cyber Security Settings

A detailed description of Schneider Electric Cyber Security features is provided in the *Cyber Security* chapter.

Important	***We would strongly recommend that you understand the contents of the Cyber Security chapter before you use any cyber security features or make any changes to the settings.***

Each MiCOM P40 IED includes a large number of possible settings. These settings are very important in determining how the device works.

A detailed description of the settings is given in the *Cyber Security* chapter.

4.2 Role Based Access Control (RBAC)

The Role Based Access Control (RBAC) is a method to restrict resource access to authorized users. RBAC is an alternative to traditional Mandatory Access Control (MAC) and Discretionary Access Control (DAC).

A key feature of RBAC model is that all access is through roles. A role is essentially a collection of permissions, and all users receive permissions only through the roles to which they are assigned, or through roles they inherit through the role hierarchy.

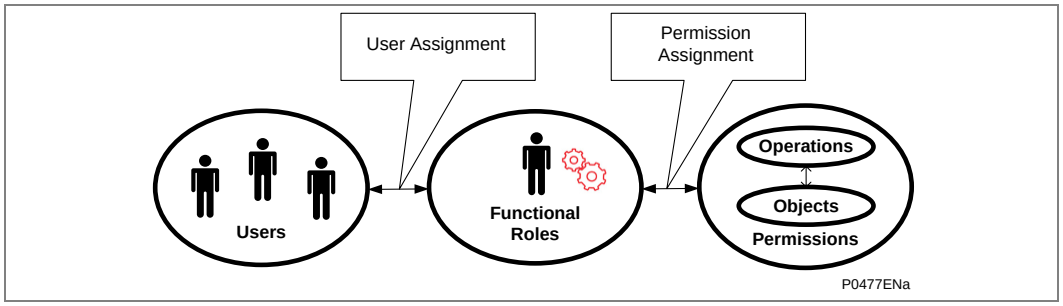


Figure 6 - RBAC Role structure

Roles are created for various job activities. The ***Permissions***, to perform certain operations, are assigned to specific roles. ***Users*** are assigned particular roles, and through those role assignments acquire the computer permissions to perform particular computer-system functions. Since ***users*** are not assigned permissions directly, but only acquire them through their role (or roles), management of individual user rights becomes a matter of simply assigning appropriate roles to the user's account; this simplifies common operations, such as adding a user, or changing user's account.

4.3 User Roles and Rights

Different named roles are associated with different access rights. Roles and Rights are setup in a pre-defined arrangement, according to the IEC62351 standard, but customized to the MiCOM Px4x equipment.

When the user tries to access an IED, they need to login using their own username and their own password. The username/password combination is then checked against the records stored on the IED. If they are allowed to login, a message appears which shows them what Role they have been assigned to. It is the role that defines their access to the relevant parts of the system.

In a similar way in which a set of pre-defined Roles have been created, a pre-defined set of Rights have been created.

These Rights give different permissions to look at what devices may be present, what those devices may contain, manage data within those devices (directly or by using files) and configure rights for other people.

5 RELAY CONFIGURATION

The relay is a multi-function device that supports numerous different protection, control and communication features. To simplify the setting of the relay, there is a configuration settings column which can be used to enable or disable many of the functions of the relay. The settings associated with any function that is disabled are made invisible, i.e. they are not shown in the menu. To disable a function change the relevant cell in the '**Configuration'** column from '**Enabled'** to '**Disabled'**.

The configuration column controls which of the protection settings groups is selected as active through the '**Active settings**' cell. A protection setting group can also be disabled in the configuration column, provided it is not the present active group. Similarly, a disabled setting group cannot be set as the active group.

The column also allows all of the setting values in one group of protection settings to be copied to another group.

To do this firstly set the 'Copy from' cell to the protection setting group to be copied, then set the 'Copy to' cell to the protection group where the copy is to be placed. The copied settings are initially placed in the temporary scratchpad, and will only be used by the relay following confirmation.

To restore the default values to the settings in any protection settings group, set the 'Restore defaults' cell to the relevant group number. Alternatively it is possible to set the 'Restore defaults' cell to 'All settings' to restore the default values to all of the relay's settings, not just the protection groups' settings. The default settings will initially be placed in the scratchpad and will only be used by the relay after they have been confirmed. Note that restoring defaults to all settings includes the rear communication port settings, which may result in communication via the rear port being disrupted if the new (default) settings do not match those of the master station.

6 FRONT PANEL USER INTERFACE (KEYPAD AND LCD)

When the keypad is exposed it provides full access to the menu options of the relay, with the information displayed on the LCD.

The ⟨, ⟩, ⌃ and ⌄ keys which are used for menu navigation and setting value changes include an auto-repeat function that comes into operation if any of these keys are held continually pressed. This can speed up both setting value changes and menu navigation; the longer the key is held depressed, the faster the rate of change or movement becomes.

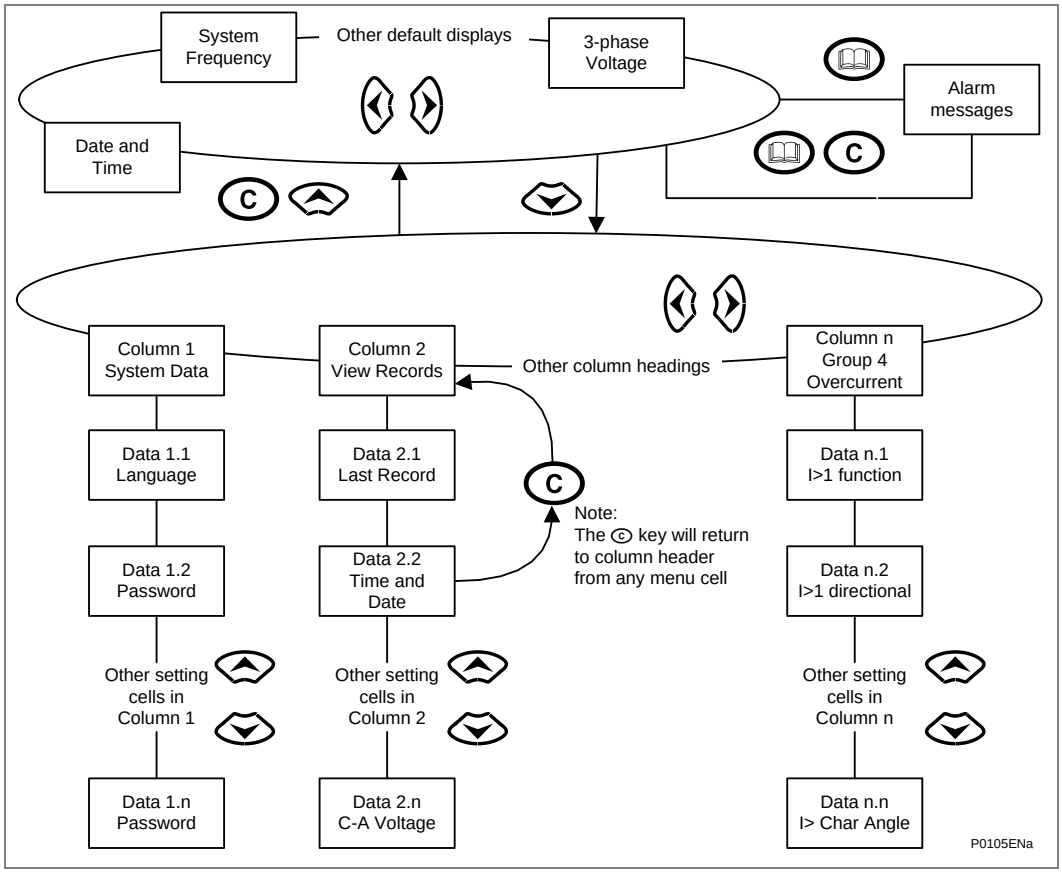


Figure 7 - Front panel user interface

6.1 Default Display and Menu Time-Out

The front panel menu has a default display. To change it, the Engineer Role will be required and the following items can be selected:

- Date and time
- Relay description (user defined)
- Plant reference (user defined)
- System frequency
- 3-phase voltage
- 3-phase and neutral current (P64x)
- Power (P64x)
- Access level
- Check zone bias currents (A, B, C) (P741/P742/P743)
- Check zone differential currents (A, B, C) (P741/P742/P743)

From the default display, the user can switch the default display to other default display items using the ◇ and ◇ keys. The default display will be saved as the last viewed items automatically. If the user tries to change the default display, Engineer Role will be requested (if the current access role is not that of an Engineer).

When user is browsing the relay menu structure with default access right, if there is no keypad activity for the 15 minutes (i.e. the timeout period), the default display will revert from the last viewed menu structure (can be any location from the menu structure) and the LCD backlight will turn off.

When user is logged in with Engineer Role, the menu timeout time may be shorter than 15 minutes. This depends on the value of inactive timer (e.g. if the inactive timer is set to shorter than 15 minutes). If menu timeout happens, any setting changes that have not been confirmed will be lost and the original setting values maintained.

Whenever there is an uncleared alarm present in the relay (e.g. fault record, protection alarm, control alarm etc.) the default display will be replaced by:

```
Alarms/Faults
Present
```

Entry to the menu structure of the relay is made from the default display and is not affected if the display is showing the Alarms/Faults present message.

6.2 Navigating Menus and Browsing the Settings

Use the four arrow keys to browse the menu, following the menu structure shown above.

1. Starting at the default display, press the ◇ key to show the first column heading.
2. Use the ◇ and ◇ keys to select the required column heading.
3. Use the ◇ and ◇ keys to view the setting data in the column.
4. To return to the column header, either hold the ◇ key down or press the clear key C once. It is only possible to move across columns at the column heading level.
5. To return to the default display, press the ◇ key or the clear key C from any of the column headings. If you use the auto-repeat function of the ◇ key, you cannot go straight to the default display from one of the column cells because the auto-repeat stops at the column heading.
6. Press the ◇ key again to go to the default display.

6.3 Navigating the Hotkey Menu

To access the hotkey menu from the default display:

1. Press the key directly below the **HOTKEY** text on the LCD.
2. Once in the hotkey menu, use the ⟨ and ⟩ keys to scroll between the available options, then use the hotkeys to control the function currently displayed.
   If neither the ⟨ or ⟩ keys are pressed within 20 seconds of entering a hotkey sub menu, the relay reverts to the default display.
3. Press the clear key C to return to the default menu from any page of the hotkey menu.

The layout of a typical page of the hotkey menu is as follows:

- The top line shows the contents of the previous and next cells for easy menu navigation
- The center line shows the function
- The bottom line shows the options assigned to the direct access keys

The functions available in the hotkey menu are listed in the following sections.

6.3.1 Setting Group Selection

The user can either scroll using <<NXT GRP>> through the available setting groups or <<SELECT>> the setting group that is currently displayed.

When the SELECT button is pressed a screen confirming the current setting group is displayed for 2 seconds before the user is prompted with the <<NXT GRP>> or <<SELECT>> options again. The user can exit the sub menu by using the left and right arrow keys.

For more information on setting group selection refer to “Setting group selection” section in the Operation chapter.

6.3.2 Control Inputs - User Assignable Functions

The number of control inputs (user assignable functions – USR ASS) represented in the hotkey menu is user configurable in the “CTRL I/P CONFIG” column. The chosen inputs can be SET/RESET using the hotkey menu.

For more information refer to the “Control Inputs” section in the Operation chapter.

6.3.3 CB Control

The CB control functionality varies from one Px40 relay to another. For a detailed description of the CB control via the hotkey menu refer to the “Circuit Breaker Control” section of the Setting chapter.

6.4 How to Login

6.4.1 Local Default Access

If the Local Default Access is enabled, the user may login to the front panel with associated roles.

See Table 4 for the applied cases.

6.4.2 Auto Login

Auto login means the user will login the IED automatically and no need to select the user name and enter the password. In this case, the user will be authorized with relevant rights. The auto login will be applied in these cases:

CS Version	Interface	RBAC/PW Cases	Login Process
CSL1	Front panel	Factory RBAC	Auto login with **EngineerLevel**
		Customized RBAC	Local Default Access Enabled: Login with **Local Default Access** Local Default Access Disabled: Login with **Prompt User List**
	Courier Interface	All cases	Login with **Prompt User List**
CSL0	Front panel	Factory RBAC	Auto login with **EngineerLevel**
		Password changed	**EngineerLevel** password is “AAAA” or is disabled/blank: Auto login with **EngineerLevel** **OperatorLevel** password is “AAAA” or is disabled/blank: Auto login with **OperatorLevel** **EngineerLevel** and **OperatorLevel** password changed: Auto login with **ViewerLevel Access**
	Courier Interface	Factory RBAC	Auto login with **EngineerLevel**
		Password changed	**EngineerLevel** password is “AAAA” or is disabled/blank: Auto login with **EngineerLevel** **OperatorLevel** password is “AAAA” or is disabled/blank: Auto login with **OperatorLevel** **EngineerLevel** and **OperatorLevel** password changed: Login with **Prompt User List**

Table 4 - Auto Login process

For more details about the Factory RBAC, please refer to the Cyber Security chapter.

6.4.3 Login with Prompt User List

This login process will happen if:

- The Auto login process is not applied.
- Or high authorization is required for the current operation.

In this case, the IED will prompt the user list, and the user needs to select proper user name and enter the password to login.

6.5 Reading and Clearing Alarm Messages and Fault Records

One or more alarm messages appear on the default display and the yellow alarm LED flashes. The alarm messages can either be self-resetting or latched, in which case they must be cleared manually.

1. To view the alarm messages, press the read key. When all alarms have been viewed but not cleared, the alarm LED change from flashing to constantly ON and the latest fault record appears (if there is one).
2. Scroll through the pages of the latest fault record, using the key. When all pages of the fault record have been viewed, the following prompt appears.

```
Press clear to
reset alarms
```

3. To clear all alarm messages, press C. To return to the display showing alarms or faults present, and leave the alarms uncleared, press .
4. Depending on the password configuration settings, you may need to enter a password before the alarm messages can be cleared. See the ***How to Access the IED/Relay*** section.
5. When all alarms are cleared, the yellow alarm LED switches OFF; also the red trip LED switches OFF if it was switched ON after a trip.
6. To speed up the procedure, enter the alarm viewer using the key, then press the C key. This goes straight to the fault record display. Press C again to move straight to the alarm reset prompt, then press C again to clear all alarms.

6.6 Setting Changes

1. To change the value of a setting, go to the relevant cell in the menu, then press the enter key to change the cell value. A flashing cursor on the LCD shows the value can be changed. If a password is required to edit the cell value, a password prompt appears.
2. To change the setting value, press the or keys. If the setting to be changed is a binary value or a text string, select the required bit or character to be changed using the and keys.
3. Press to confirm the new setting value or the clear key C to discard it. The new setting is automatically discarded if it is not confirmed in 15 minutes.
4. For protection group settings and disturbance recorder settings, the changes must be confirmed before they are used by the relay.
5. To do this, when all required changes have been entered, return to the column heading level and press the key. Before returning to the default display, the following prompt appears.

```
Update settings?
Enter or clear
```

6. Press to accept the new settings or press C to discard the new settings.

Note	*If the menu time-out occurs before the setting changes have been confirmed, the setting values are also discarded.*

Control and support settings are updated immediately after they are entered, without the **Update settings?** prompt.

6.7 How to Logout

6.7.1 How to Logout at the IED

For security consideration, it would be better to “logout' the IED once the configuration done. You can do this by going up to the default display. When you are at the default display and you press the ‘Cancel’ button, you may be prompted to log out with the following display:

```
ENTER TO LOGOUT
CLEAR TO CANCEL
```

You will be asked this question if you are logged in.

If you confirm, the following message is displayed for 2 seconds:

```
LOGGED OUT
User Name
```

If you decide not to log out (i.e. you cancel), the following message is displayed for 2 seconds.

```
LOGOUT CANCELLED
User Name
```

Note	*The MiCOM IED runs a timer, which logs the user out after a period of inactivity. For more details, refer to the Inactivity Timer section.*

6.7.2 How to Logout at Easergy Studio

- Right-click on the device name and select Log Off.
- In the Log Off confirmation dialog click Yes.

7 FRONT COMMUNICATION PORT USER INTERFACE

The front communication port is provided by a 9-pin female D-type connector located under the bottom hinged cover. It provides EIA(RS)232 serial data communication and is intended for use with a PC locally to the relay (up to 15m distance) as shown in the following diagram. This port supports the Courier communication protocol only. Courier is the communication language developed by Schneider Electric to allow communication with its range of protection relays. The front port is particularly designed for use with the relay settings program Easergy Studio.

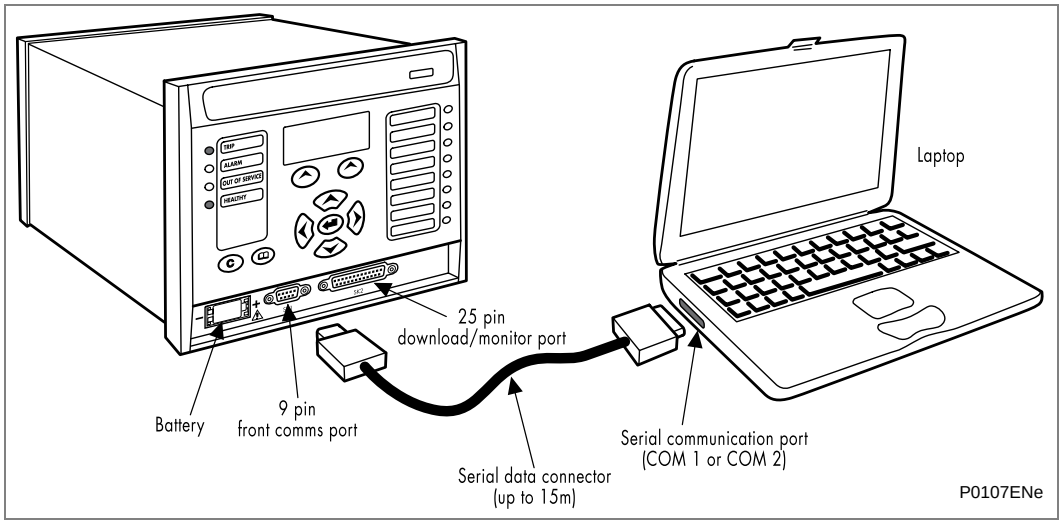


Figure 8 - Front port connection

The IED is a Data Communication Equipment (DCE) device. The pin connections of the 9-pin front port are as follows:

Pin no.	Description
2	Tx Transmit data
3	Rx Receive data
5	0V Zero volts common

Table 5 - Front port DCE pin connections

None of the other pins are connected in the relay. The relay should be connected to the serial port of a PC, usually called COM1 or COM2. PCs are normally Data Terminal Equipment (DTE) devices which have a serial port pin connection as below (if in doubt check your PC manual):

Pin	25 Way	9 Way	Description
Pin no. 2	3	2	Rx Receive data
Pin no. 3	2	3	Tx Transmit data
Pin no. 5	7	5	0V Zero volts common

Table 6 - DTE devices serial port pin connections

For successful data communication, the Tx pin on the relay must be connected to the Rx pin on the PC, and the Rx pin on the relay must be connected to the Tx pin on the PC, as shown in the diagram. Therefore, providing that the PC is a DTE with pin connections as given above, a 'straight through' serial connector is required, i.e. one that connects pin 2 to pin 2, pin 3 to pin 3, and pin 5 to pin 5.

Note	*A common cause of difficulty with serial data communication is connecting Tx to Tx and Rx to Rx. This could happen if a 'cross-over' serial connector is used, i.e. one that connects pin 2 to pin 3, and pin 3 to pin 2, or if the PC has the same pin configuration as the relay.*

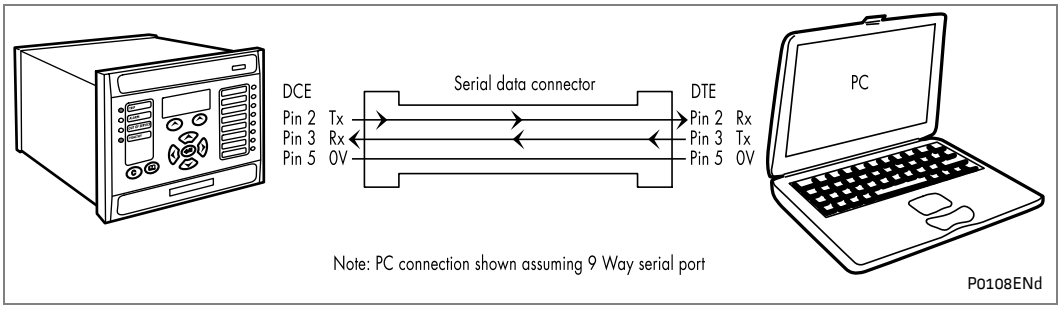


Figure 9 - PC - relay signal connection

Having made the physical connection from the relay to the PC, the PCs communication settings must be configured to match those of the relay. The relays communication settings for the front port are fixed as shown below:

Protocol	Baud rate	Courier address	Message format
Courier	19,200 bits/s	1	11 bit - 1 start bit, 8 data bits, 1 parity bit (even parity), 1 stop bit

Table 7 - Communication settings

7.1 Relay Front Port Settings

The inactivity timer for the front port is set at 15 minutes. This controls how long the relay will maintain its password access on the front port. If no messages are received on the front port for 15 minutes then any password access that has been enabled will be revoked.

7.2 Front Courier Port

The front EIA(RS)232 9-pin port supports the Courier protocol for one to one communication.

Note	*The front port is actually compliant to EIA(RS)574; the 9-pin version of EIA(RS)232, see www.tiaonline.org.*

The front port is designed for use during installation and commissioning/maintenance and is not suitable for permanent connection. Since this interface will not be used to link the relay to a substation communication system, some of the features of Courier are not implemented. These are as follows:

- Automatic Extraction of Event Records:
  - Courier Status byte does not support the Event flag
  - Send Event/Accept Event commands are not implemented
- Automatic Extraction of Disturbance Records:
  - Courier Status byte does not support the Disturbance flag
- Busy Response Layer: Courier Status byte does not support the Busy flag, the only response to a request will be the final data
- Fixed Address: The address of the front courier port is always 1, the Change Device address command is not supported.
- Fixed Baud Rate: 19200 bps

Note	*Although automatic extraction of event and disturbance records is not supported, this data can be manually accessed using the front port.*

8 EASERGY STUDIO RELAY COMMUNICATIONS BASICS

The EIA(RS)232 front communication port is particularly designed for use with the relay settings program Easergy Studio. Easergy Studio is the universal MiCOM IED Support Software and provide users a direct and convenient access to all stored data in any MiCOM IED using the EIA(RS)232 front communication port.

Easergy Studio provides full access to MiCOM Px10, Px20, Px30, Px40 and Mx20 measurements units.

The Easergy Studio product is updated periodically. These updates provide support for new features (such as allowing you to manage new MiCOM products, as well as using new software releases and hardware suffixes). The updates may also include fixes. **Accordingly, we strongly advise customers to use the latest Schneider Electric version of Easergy Studio.**

8.1 PC Requirements

The minimum and recommended hardware requirements for Easergy Studio (v7.0.0) are shown below. These include the Studio application and other tools which are included: UPCT, P746 RHMI, P74x Topology Tool:

Minimum requirements:				
Platform	**Processor**	**RAM**	**HDD (Note 1 & 3)**	**HDD (Note 2 & 3)**
Windows XP x86	1 GHz	512 MB	900 MB	1.5 GB
Windows 7 x86	1 GHz	1 GB	900 MB	1.9 GB
Windows 7 x64	1 GHz	2 GB	900 MB	2.1 GB
Windows Server 2008 x86 Sp1	1 GHz	512 MB	900 MB	1.7 GB

Recommended requirements:				
Platform	**Processor**	**RAM**	**HDD (Note 1 & 3)**	**HDD (Note 2 & 3)**
Windows XP x86	1 GHz	1 GB	900 MB	1.5 GB
Windows 7 x86	1 GHz	2 GB	900 MB	1.9 GB
Windows 7 x64	1 GHz	4 GB	900 MB	2.1 GB
Windows Server 2008 x86 Sp1	1 GHz	4 GB	900 MB	1.7 GB

Note 1	*Operating system with Windows Updates updated on 2015/05.*
Note 2	*Operating system without Windows Updates installed.*
Note 3	*Both configurations do not include Data Models HDD requirements. Data Models typically need from 1 GB to 15 GB of hard disk space.*

Screen resolution for minimum requirements: Super VGA (800 x 600).
Screen resolution for recommended requirements: XGA (1024x768) and higher.
Easergy Studio must be started with Administrator privileges.

Easergy Studio Additional components

The following components are required to run Easergy Studio and are installed by its installation package.

Component Type	Component
Package	.NET Framework 2.0 SP 1 (x64)
Package	.NET Framework 2.0 SP 1 (x86)
Package	.NET Framework 4.0 Client (x64)
Package	.NET Framework 4.0 Client (x86)
Package	Visual C++ 2005 SP1 Redistributable Package (x86)
Package	Visual C++ 2008 SP1 Redistributable Package (x86)
Merge modules	DAO 3.50
Merge modules	MFC 6.0
Merge modules	MFC Unicode 6.0
Merge modules	Microsoft C Runtime Library 6.0
Merge modules	Microsoft C++ Runtime Library 6.0
Merge modules	Microsoft Component Category Manager Library
Merge modules	Microsoft Data Access Components 2.8 (English)
Merge modules	Microsoft Jet Database Engine 3.51 (English)
Merge modules	Microsoft OLE 2.40 for Windows NT and Windows 95
Merge modules	Microsoft Visual Basic Virtual Machine 6.0
Merge modules	MSXML 4.0 - Windows 9x and later
Merge modules	MSXML 4.0 - Windows XP and later
Merge modules	Visual C++ 8.0 MFC (x86) WinSXS MSM
Merge modules	Visual C++ 8.0 MFC.Policy (x86) WinSXS MSM

8.2 Connecting to the Relay using Easergy Studio

This section is a quick start guide to using Easergy Studio and assumes this is installed on your PC. See the Easergy Studio online help for more detailed information.

1. Make sure the EIA(RS)232 serial cable is properly connected between the port on the front panel of the relay and the PC.
2. To start Easergy Studio, select **Start** > **All apps** > **Schneider Electric** > **Easergy Studio**.
3. Click the **Quick Connect** tab and select **Create a New System**.
4. Check the **Path to System file** is correct, then enter the name of the system in the **Name** field. To add a description of the system, use the **Comment** field.
5. Click **OK**.
6. Select the device type.
7. Select the communications port, and open a connection with the device.
8. Once connected, select the language for the settings file, the device name, then click **Finish**. The configuration is updated.
9. In the **Studio Explorer** window, select **Device** > **Supervise Device**… to control the relay directly. (User Login necessary)

8.3 Off-Line Use of Easergy Studio

Easergy Studio can also be used as an off-line tool to prepare settings, without access to the relay.

1. If creating a new system, in the Studio Explorer, select **create new** system. Then right-click the new system and select **New substation**.
2. Right-click the new substation and select **New voltage level**.
3. Then right-click the new voltage level and select **New bay**.
4. Then right-click the new bay and select **New device**.

   You can add a device at any level, whether it is a system, substation, voltage or bay.
5. Select a device type from the list, then enter the relay type. Click **Next**.
6. Enter the full model number and click **Next**.
7. Select the **Language** and **Model**, then click **Next**.
8. If the IEC61850 protocol is selected, and an Ethernet board with hardware option Q, R or S is selected, select IEC 61850 Edition:
   IEC 61850 Edition 2 Mode or
   IEC 61850 Edition 1 Compatible Mode.
9. Enter a unique device name, then click **Finish**.
10. Right-click the **Settings** folder and select **New File**. A default file **000** is added.
11. Right-click file **000** and select click **Open**. You can then edit the settings. See the Easergy Studio program online help for more information.

Notes:

SETTINGS

CHAPTER 4

Date:	07/2018
Products covered by this chapter:	This chapter covers the specific versions of the MiCOM products listed below. This includes ***only*** the following combinations of Software Version and Hardware Suffix.
Hardware Suffix:	L (P642) M (P643/P645)
Software Version:	B4 - P64x (P642, P643 & P645)
Connection Diagrams:	10P642xx (xx = 01 to 10) 10P643xx (xx = 01 to 06) 10P645xx (xx = 01 to 09)

CONTENTS

TABLES

Notes:

1 INTRODUCTION

The IED must be configured to the system and the application by means of appropriate settings.

The sequence in which the settings are listed and described in this chapter will be the protection setting, control and configuration settings and the disturbance recorder settings.

The IED is supplied with a factory-set configuration of default settings.

2 RELAY SETTINGS

The IED is a multi-function device that supports numerous different control and communication features. The settings associated with any function that is disabled are made invisible; i.e. they are not shown in the menu. To disable a function change the relevant cell in the '**Configuration'** column from '**Enabled'** to '**Disabled'**.

To simplify the setting of the IED, there is a configuration settings column, used to enable or disable many of the IED functions. The aim of the configuration column is to allow general configuration from a single point in the menu.

The configuration column controls which of the four settings groups is selected as active through the '**Active settings**' cell. A setting group can also be disabled in the configuration column, provided it is not the present active group. Similarly, a disabled setting group cannot be set as the active group.

The column also allows all of the setting values in one group of settings to be copied to another group.

To do this firstly set the '**Copy from**' cell to the setting group to be copied, then set the '**Copy to**' cell to the group where the copy is to be placed. The copied settings are initially placed in the temporary scratchpad, and will only be used by the IED following confirmation.

2.1 Restore Default Settings

To restore the default values to the settings in any protection settings group, set the 'restore defaults' cell to the relevant group number. Alternatively, it is possible to set the 'restore defaults' cell to 'all settings' to restore the default values to all of the IEDs settings, not just the protection groups' settings. The default settings will initially be placed in the scratchpad and will only be used by the IED after they have been confirmed.

Important	***Restoring defaults to all settings includes the rear communication port settings, which may result in communication via the rear port being disrupted if the new (default) settings do not match those of the master station.***

Important	***If you restore settings, the settings for the IEC 61850 Edition and the Communications Mode will not be restored, even if "Restore All Settings" is set.***

3 CONFIGURATION MENU

Menu Text	Col	Row	Default Setting	Available Setting
Description				
CONFIGURATION	09	00		
This column contains CONFIGURATION parameters.				
Restore Defaults	09	01	No Operation	No operation, All settings, Setting Group 1, Setting Group 2, Setting Group 3, or Setting Group 4
Setting to restore a setting group to factory default settings.				
Setting Group	09	02	Menu	Select from Menu or Select from PSL
Allows setting group changes to be initiated using 2 DDB signals in the programmable scheme logic or from the Menu settings.				
Active Settings	09	03	Group 1	Group 1, Group 2, Group 3 or Group 4
Selects the active setting group.				
Save Changes	09	04	No Operation	No Operation, Save or Abort
Saves all relay settings.				
Copy From	09	05	Group 1	Group 1, Group 2, Group 3 or Group 4
Allows displayed settings to be copied from a selected setting group.				
Copy To	09	06	No Operation	No Operation, Group 1, Group 2, Group 3 or Group 4
Allows displayed settings to be copied to a selected setting group.				
Setting Group 1	09	07	Enabled	Enabled or Disabled
Enables or disables Group 1 settings. If the setting group is disabled from the configuration, all associated settings and signals are hidden, with the exception of this setting.				
Setting Group 2	09	08	Disabled	Enabled or Disabled
Setting Group 2 works in the same way as Setting Group 1.				
Setting Group 3	09	09	Disbaled	Enabled or Disabled
Setting Group 3 works in the same way as Setting Group 1.				
Setting Group 4	09	0A	Disabled	Enabled or Disabled
Setting Group 4 works in the same way as Setting Group 1.				
Diff Protection	09	0C	Enabled	Enabled or Disabled
Enables (activates) or disables (turns off) the differential protection. The unit provides bias differential protection with multiple CT inputs.				
REF Protection	09	0E	Enabled	Enabled or Disabled
Enables (activates) or disables (turns off) the Restricted Earth Fault protection. The unit provides a low impedance REF function per transformer winding.				
Over Current	09	10	Enabled	Enabled or Disabled
Enables (activates) or disables (turns off) the overcurrent protection: ANSI 50/51/67P, 46OC.				
NPS OverCurrent	09	11	Enabled	Enabled or Disabled
Enables (activates) or disables (turns off) the Negative Phase Sequence overcurrent protection: ANSI 50/51/67P, 46OC.				
Thermal Overload	09	12	Enabled	Enabled or Disabled
Enables (activates) or disables (turns off) the Thermal Overload Protection: ANSI 49.				
Earth Fault	09	13	Enabled	Enabled or Disabled
Enables (activates) or disables (turns off) the Earth Fault Protection: ANSI 50N/51N.				
Residual O/V NVD	09	16	Enabled	Enabled or Disabled

Menu Text	Col	Row	Default Setting	Available Setting
Description				
P643 and P645 only. Enables (activates) or disables (turns off) the Residual Overvoltage (Neutral Voltage Displacement) Protection function: ANSI 59N.				
Overfluxing	09	18	Disabled	Enabled or Disabled
Enables (activates) or disables (turns off) the Overfluxing protection: ANSI 24.				
Through Fault	09	1B	Disabled	Enabled or Disabled
Enables (activates) or disables (turns off) the Through Fault function. The Through Fault current monitoring function in the P64x gives the fault current level, the duration of the faulty condition, the date and time.				
Volt Protection	09	1D	Disabled	Enabled or Disabled
Enables (activates) or disables (turns off) the Voltage Protection (Under/Overvoltage and NPS Overvoltage) function: ANSI 27/59/47.				
Freq Protection	09	1E	Enabled	Enabled or Disabled
Enables (activates) or disables (turns off) the Frequency Protection (Under/Overfrequency) function: ANSI 81O/U.				
RTD Inputs	09	1F	Enabled	Enabled or Disabled
Enables (activates) or disables (turns off) the RTD (Resistance Temperature Device) Inputs.				
CB Fail	09	20	Disabled	Enabled or Disabled
Enables (activates) or disables (turns off) the Circuit Breaker Fail Protection function: ANSI 50BF.				
Supervision	09	21	Disabled	Enabled or Disabled
Enables (activates) or disables (turns off) the Supervision (VTS&CTS) functions: ANSI VTS/CTS.				
Input Labels	09	25	Visible	Invisible or Visible
Sets the Input Labels menu visible in the relay settings menu.				
Output Labels	09	26	Visible	Invisible or Visible
NOT USED. Sets the Output Labels menu to visible in the relay settings menu.				
RTD Lables	09	27	Visible	Invisible or Visible
Sets the RTD Labels menu visible in the relay settings menu.				
CT and VT Ratios	09	28	Visible	Invisible or Visible
Sets the Current & Voltage Transformer Ratios menu visible in the relay settings menu.				
Record Control	09	29	Visible	Invisible or Visible
Sets the Record Control menu visible in the relay settings menu.				
Disturb Recorder	09	2A	Visible	Invisible or Visible
Sets the Disturbance Recorder menu visible in the relay settings menu.				
Measure't Setup	09	2B	Visible	Invisible or Visible
Sets the Measurement Setup menu visible in the relay settings menu.				
Comms Settings	09	2C	Visible	Invisible or Visible
Sets the Communications Settings menu visible in the relay settings menu. These are the settings associated with the 1st and 2nd rear communications ports.				
Commission Tests	09	2D	Visible	Invisible or Visible
Sets the Commissioning Tests menu visible in the relay settings menu.				
Setting Values	09	2E	Primary	Primary or Secondary
This affects all protection settings that are dependent on CT and VT ratios.				
Control Inputs	09	2F	Visible	Invisible or Visible
Sets the Control Inputs menu visible in the relay setting menu.				
CLIO Inputs	09	30	Enabled	Enabled or Disabled
Enables (activates) or disables (turns off) the CLIO (Current Loop Input Output) function.				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
CLIO Outputs	09	31	Enabled	Enabled or Disabled
Enables (activates) or disables (turns off) the CLIO (Current Loop Input Output) Outputs function.				
CLIO status (Hidden)	09	32	Hidden	False or True
CLIO status (Hidden). No Courier text. Cell value set to False if CLIO not fitted and Cell value set to True if CLIO is fitted.				
Control I/P Config	09	35	Visible	Invisible or Visible
Sets the Control Input Configuration menu visible in the relay setting menu.				
Ctrl I/P Labels	09	36	Visible	Invisible or Visible
Sets the Control Input Labels menu visible in the relay setting menu.				
Direct Access	09	39	Enabled	Enabled, Disabled or Hotkey Only
Defines what controls are available using the direct access keys - Enabled (Hotkey and CB Control functions) / Hotkey Only (Control Inputs and Setting group selection) / CB Cntrl Only (CB open/close).				
PB CONFIG	09	48	Visible	Invisible or Visible
Sets the PB CONFIG menu visible in the relay setting menu.				
IEC GOOSE	09	49	Visible	Invisible or Visible
Sets the IEC 61850 GOOSE menu visible in the relay setting menu.				
Function Keys	09	50	Visible	Invisible or Visible
Sets the Function Key menu visible in the relay setting menu.				
VIR I/P Labels	09	70	Invisible	Invisible or Visible
VIR I/P Labels Visible/Invisible				
VIR O/P Labels	09	80	Invisible	Invisible or Visible
VIR O/P Labels Visible/Invisible				
Usr Alarm Labels	09	90	Invisible	Invisible or Visible
USR Alarm Labels Visible/Invisible				
RP1 Read Only	09	FB	Disabled	Enabled, Disabled
Visible when comms options are: 1 – Courier 3 – CS103 6 – IEC61850 with 1st Rear Courier, 7 – IEC61850 with 1st Rear CS103.				
RP2 Read Only	09	FC	Disabled	Enabled, Disabled
Visible when comms options are: 1 – Courier, or 3 – CS103; and hardware options are: 7, 8, E or F.				
NIC Read Only	09	FD	Disabled	Enabled, Disabled
Visible when comms options are: 6 – IEC61850 with 1st Rear Courier, 7 – IEC61850 with 1st Rear CS103.				
SettingValueBeh.	09	FE	Independent	0 = Independent or 1 = Locked Mode
Independent: cell [092E] Setting Values will be independent in each interface. For example, the Front Port can have [092E] set to Secondary and a remote port can have [092E] set to Primary. Locked Mode: cell [092E] Setting Values are locked to the same value for all interfaces. All interfaces have the same value for [092E]. Whichever interface selects Locked Mode will have its setting for [092E] applied to all interfaces. Any interface can then change [092E] and it will apply on all interfaces.				
LCD Contrast	09	FF	11	0 to 31 step 1
To confirm the LCD contrast press the right and left arrow keys together instead of Enter. This prevents someone selecting a black or blank contrast setting by accident. Note: The contrast can be set through the FP comms port using the MiCOM software.				

Table 1 - Configuration settings

4 GROUPED PROTECTION SETTINGS

The grouped protection settings include all the following items that become active once enabled in the configuration column of the relay menu database:

- Protection Element Settings.
- Programmable Scheme Logic (PSL).

There are four groups of protection settings, with each group containing the same setting cells. One group of protection settings is selected as the active group, and is used by the protection elements. The settings for group 1 are shown. The settings are discussed in the same order in which they are displayed in the menu.

4.1 System Config

The relay maintains correct operation of all the protection functions through user-configurable settings.

Menu Text	Col	Row	Default Setting	Available Setting
Description				
GROUP 1: SYSTEM CONFIG	30	00		
This column contains GROUP 1 SYSTEM CONFIG parameters				
Winding Config	30	01	HV+LV+TV	HV+LV or HV+LV+TV
P643 and P645 only. This setting indicates if the protected transformer is a two or three winding transformer.				
Winding Type	30	02	Conventional	Conventional or Auto
The winding type may be configured as Conventional or Auto. This setting is just for information.				
HV CT Terminals	30	03	01 (P642)	01 (P642)
Each digit corresponds to a terminal. For further detailed connections refer to the installation section. P642 only - from right to left the current inputs are T1, T2. 0 = disabled, 1 = enabled.				
LV CT Terminals	30	04	10 (P645)	10 (P642)
P642 only. Each digit corresponds to a terminal. From right to left the current inputs are T1, T2. 0 = disabled, 1 = enabled For further detailed connections refer to the installation section.				
TV CT Terminals	30	05	010 (P643)	010 (P643)
P643 only. Each digit corresponds to a terminal. From right to left the current inputs are T1, T2, T3. 0 = disabled, 1 = enabled For further detailed connections refer to the installation section.				
Sref	30	07	100MVA	0.1MVA to 5000MVA step 0.1MVA
Reference power. Used by the differential function to calculate the ratio correction factors. Used by the thermal function when the monitored winding is set to biased current.				
HV Connection	30	08	Y-Wye	Y-Wye, D-Delta or Z-Zigzag
The HV winding connections can be configured as Wye, Delta, or Zigzag.				
HV Grounding	30	09	Grounded	Grounded or Ungrounded
In Simple mode: Grounded = P64x filters zero sequence current on HV side. Ungrounded = no zero sequence filtering is done on HV side. In Advanced mode: Grounding = Information only, and zero sequence filtering depends on Zero seq filt HV setting.				
HV Nominal	30	0A	220kV	100V to 1MV step 1V
Nominal voltage of the HV winding, mid-tap voltage of the on-load tap changer, or no-load tap changer tap voltage.				
HV Rating	30	0B	100MVA	0.1MVA to 5000MVA step 0.1MVA
This rating is used by the thermal overload function if the monitored winding is set to HV.				
% Reactance	30	0C	0.1	1% to 100% step 0.63%

Menu Text	Col	Row	Default Setting	Available Setting
Description				
Transformer leakage reactance.				
LV Vector Group	30	0D	0	0 to 11 step 1
This is used to provide vector correction for phase shift between HV and LV windings.				
LV Connection	30	0E	Y-Wye	Y-Wye, D-Delta or Z-Zigzag
The LV winding connections can be configured as Wye, Delta, or Zigzag.				
LV Grounding	30	0F	Grounded	Grounded or Ungrounded
When set as grounded, the P64x filters the zero sequence current in the LV side. When set as ungrounded, no zero sequence filtering is done in the LV side.				
LV Nominal	30	10	220kV	100V to 1MV step 1V
Nominal voltage of the LV winding, mid-tap voltage of the on-load tap changer, or no-load tap changer tap voltage.				
LV Rating	30	11	100MVA	0.1MVA to 5000MVA step 0.1MVA
This rating is used by the thermal overload function if the monitored winding is set to LV.				
TV Vector Group	30	12	0	0 to 11 step 1
P643 and P645 only. This is used to provide vector correction for phase shift between HV and TV windings.				
TV Connection	30	13	Y-Wye	Y-Wye,D-Delta or Z-Zigzag
P643 and P645 only. The winding connections can be configured as Wye, Delta, or Zigzag.				
TV Grounding	30	14	Grounded	Grounded or Ungrounded
P643 and P645 only. Simple: Grounded = P64x filters zero sequence current on TV side. Ungrounded = no zero sequence filtering is done on LV side. Advanced: Grounding = Information only, and zero sequence filtering depends on Zero seq filt HV setting.				
TV Nominal	30	15	220kV	100V to 1MV step 1V
P643 and P645 only. Nominal voltage of the TV winding.				
TV Rating	30	16	100MVA	0.1MVA to 5000MVA step 0.1MVA
P643 and P645 only. This rating is used by the thermal overload function if the monitored winding is set to TV.				
Match Factor CT1	30	20	Set by relay	Set by relay
CT1 ratio correction factor used by the differential function.				
Match Factor CT2	30	21	Set by relay	Set by relay
CT2 ratio correction factor used by the differential function.				
Match Factor CT3	30	22	Set by relay	Set by relay
P643 and P645 only. CT3 ratio correction factor used by the differential function.				
Match Factor CT4	30	23	Set by relay	Set by relay
P645 only. CT4 ratio correction factor used by the differential function.				
Match Factor CT5	30	24	Set by relay	Set by relay
P645 only. CT5 ratio correction factor used by the differential function.				
MatchFac REF HV	30	25	Set by relay	Set by relay
Ratio correction factor used by REF HV protection.				
MatchFac REF LV	30	26	Set by relay	Set by relay

Menu Text	Col	Row	Default Setting	Available Setting
Description				
Ratio correction factor used by REF LV protection.				
MatchFac REF TV	30	27	Set by relay	Set by relay
P643 and P645 only. Ratio correction factor used by REF TV protection.				
MatchFac REFAuto	30	28	Set by relay	Set by relay
Ratio correction factor used by REF Auto protection.				
Phase Sequence	30	5E	Standard ABC	Standard ABC or Reverse ACB
This sets the phase rotation. It affects the positive and negative sequence quantities calculated by the relay. It also affects functions that are dependent on phase quantities.				
VT Reversal	30	5F	No Swap	No Swap, A-B Swap or C-A Swap
P643 and P645 only. For applications where 2-phase current inputs are swapped.				
CT1 Reversal	30	60	No Swap	No Swap, A-B Swap or C-A Swap
For applications where 2-phase current inputs are swapped.				
CT2 Reversal	30	61	No Swap	No Swap, A-B Swap or C-A Swap
For applications where 2-phase current inputs are swapped.				
CT3 Reversal	30	62	No Swap	No Swap, A-B Swap or C-A Swap
P643 and P645 only. For applications where 2-phase current inputs are swapped.				
CT4 Reversal	30	63	No Swap	No Swap, A-B Swap or C-A Swap
P645 only. For applications where 2-phase current inputs are swapped.				
CT5 Reversal	30	64	No Swap	No Swap, A-B Swap or C-A Swap
P645 only. For applications where 2-phase current inputs are swapped.				

Table 2 - Group 1 system config settings

4.2 Differential Protection

Menu Text	Col	Row	Default Setting	Available Setting
Description				
GROUP 1: DIFF PROTECTION	31	00		
This column contains the GROUP 1 DIFF PROTECTION parameters				
Trans Diff	31	01	Enabled	Enabled or Disabled
This enables or disables differential protection for setting group1.				
Set Mode	31	02	Simple	Simple or Advanced
Defines Simple or Advanced Mode, as per HV/LV/TV Grounding. Advanced = zero sequence filtering enabled/disabled in Zero seq filt HV/LV/TV. Simple = Is-HS1 calculated as 1/Xt (Xt=transformer reactance); and Zero seq filt HV/LV/TV, Is-HS1 and Is-Hs2 hidden				
Is1	31	03	0.2	0.1pu to 2.5pu step 0.01pu
Minimum differential threshold of the low set differential characteristic				
K1	31	04	0.3	0% to 150% step 1%
First slope setting of the low set differential characteristic				
Is2	31	05	1	0.1pu to 10pu step 0.1pu
Bias current threshold for the second slope of the low set differential characteristic				
K2	31	06	0.8	15% to 150% step 1%
Second slope setting of the low set differential characteristic				
tDiff	31	07	0s	0 to 10s step 10ms
Differential time delay				
Is-CTS	31	08	1.5	0.1pu to 2.5pu step 0.01pu
In restrain mode, the differential protection Is1 setting is increased to Is-CTS setting after CT failure is detected. The Is-CTS setting increases the restrain region of the differential characteristic				
Is-HS1	31	10	1/Xt	2.5pu to 32pu step 0.1pu
High set element one. In the simple mode the relay calculates Is-HS1 as 1/Xt. Where Xt is the transformer reactance. This setting is hidden in simple mode. In advance mode Is-HS1 is visible and settable.				
HS2 Status	31	11	Enabled	Enabled or Disabled
Enable or Disabled High set element two				
Is-HS2	31	12	32	2.5pu to 32pu step 0.1pu
High Set element two when HS2 Status is enabled. When HS2 Status is enabled, High set element two. In the simple mode the relay calculates Is-HS2 as 1/Xt. Where Xt is the transformer reactance. This setting is hidden in simple mode. In advance mode Is-HS2 is visible and settable.				
Diff calc remove	31	13	Disabled	Disabled or TV
P643 and P645 only. Disable means diff protection is same as usual, 'TV' means phase currents of the ends which belong to TV are no effect on trans diff protection. This setting is only settable in advance mode.				
Transient Bias	31	14	Enabled	Enabled or Disabled
Default setting 'Enabled' means trans diff protection is same as version B2A, 'Disabled ' means the transient bias is removed from bias current for all cases.				
Zero seq filt HV	31	20	Enabled	Enabled or Disabled
Enables or disables zero sequence filtering on the HV winding. This setting is only visible and settable in advance mode.				
Zero seq filt LV	31	21	Enabled	Enabled or Disabled
Enables or disables zero sequence filtering on the LV winding. This setting is only visible and settable in advance mode.				
Zero seq filt TV	31	22	Enabled	Enabled or Disabled
P643 and P645 only. Enables or disables zero sequence filtering on the TV winding. This setting is only visible and settable in advance mode.				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
2nd harm blocked	31	28	Enabled	Enabled or Disabled
2nd harm blocked				
Ih(2)%>	31	29	0.2	5% to 50% step 1%
Second harmonic blocking threshold				
Cross blocking	31	2A	Enabled	Enabled or Disabled
Enables or disables cross blocking				
CTSat and NoGap	31	2B	Enabled	Enabled or Disabled
Enables or disables CT saturation detection				
5th harm blocked	31	33	Enabled	Enabled or Disabled
Enables or disables 5th harmonic blocking				
Ih(5)%>	31	34	0.35	0% to 100% step 1%
Fifth harmonic blocking threshold				
Circuitry Fail	31	40	Disabled	Enabled or Disabled
Enables or disables the circuitry fail alarm				
Is-cctfail	31	41	0.1	0.03pu to 1pu step 0.01pu
Minimum differential threshold of the circuitry fail alarm				
K-cctfail	31	42	0.1	0% to 50% step 1%
Slope for the circuitry fail alarm function				
CctFail Delay	31	43	5s	0s to 10s step 0.1s
Sets the circuitry fail alarm time delay				

Table 3 - Group 1 DIFF protection settings

4.3 Restricted Earth Fault (REF) Protection

Menu Text	Col	Row	Default Setting	Available Setting
Description				
GROUP 1: REF PROTECTION	32	00		
This column contains GROUP1 REF PROTECTION parameters.				
REF HV status	32	01	LowZ REF	Disabled, LowZ REF or HighZ REF
Select to be HighZ REF or LowZ REF or disable for the HV winding				
Neutral CT Input	32	02	TN1	TN1
HV IS1 Set	32	03	0.09	0.02In to 1In step 0.01In
Minimum differential threshold of the HV restricted earth fault characteristic				
HV IS2 Set	32	04	0.9	0.1In to 10In step 0.1In
Bias current threshold for the second slope of the HV restricted earth fault characteristic				
HV IREF K1	32	05	0	0% to 150% step 1%
First slope setting of the HV REF characteristic. Normally set to 0% to give optimum sensitivity for internal faults				
HV IREF K2	32	06	1.5	15% to 150% step 1%
Second slope setting of the HV REF characteristic. Normally set to 150% to ensure adequate restraint for external faults.				
HV tREF	32	07	0s	0s to 10s step 0.01s
Operating time delay for the HV REF element				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
HV IREF>Is	32	08	0.09	0.02In to 1In step 0.01In
Threshold of the HV HighZ restricted earth fault.				
HV Trans.Bias	32	09	Enabled	Enabled or Disabled
Default setting 'Enabled' means REF protection is same as version B2A, 'Disabled ' means the transient bias is removed from bias current for all cases.				
REF LV status	32	20	Disabled	Disabled, LowZ REF or HighZ REF
Select to be HighZ REF or LowZ REF or disable for the LV winding				
Neutral CT Input	32	21	TN2	TN2
LV IS1 Set	32	22	0.09	0.02In to 1In step 0.01In
Minimum differential threshold of the LV REF characteristic				
LV IS2 Set	32	23	0.9	0.1In to 10In step 0.1In
Bias current threshold for the second slope of the LV REF characteristic				
LV IREF K1	32	24	0	0% to 150% step 1%
First slope setting of the LV REF characteristic. Normally set to 0% to give optimum sensitivity for internal faults				
LV IREF K2	32	25	1.5	15% to 150% step 1%
Second slope setting of the LV REF characteristic. Normally set to 150% to ensure adequate restraint for external faults.				
LV tREF	32	26	0s	0s to 10s step 0.01s
Operating time delay for the LV restricted earth fault element				
LV IREF>Is	32	27	0.09	0.02In to 1In step 0.01In
Threshold of the LV HighZ restricted earth fault.				
LV Trans.Bias	32	28	Enabled	Enabled or Disabled
Default setting 'Enabled' means REF protection is same as version B2A, 'Disabled ' means the transient bias is removed from bias current for all cases.				
REF TV status	32	30	Disabled	Disabled, LowZ REF or HighZ REF
P643 and P645 only. Select to be HighZ REF or LowZ REF or disable for the LV winding				
Neutral CT Input	32	31	TN3	TN3
P643 and P645 only.				
TV IS1 Set	32	32	0.09	0.02In to 1In step 0.01In
P643 and P645 only. Minimum differential threshold of the TV REF characteristic				
TV IS2 Set	32	33	0.9	0.1In to 10In step 0.1In
P643 and P645 only. Bias current threshold for the second slope of the TV REF characteristic				
TV IREF K1	32	34	0	0% to 150% step 1%
P643 and P645 only. First slope setting of the TV REF characteristic. Normally set to 0% to give optimum sensitivity for internal faults				
TV IREF K2	32	35	1.5	15% to 150% step 1%
P643 and P645 only. Second slope setting of the TV REF characteristic. Normally set to 150% to ensure adequate restraint for external faults				
TV tREF	32	36	0s	0s to 10s step 0.01s
P643 and P645 only. Operating time delay for the TV restricted earth fault element				
TV IREF>Is	32	37	0.09	0.02In to 1In step 0.01In

Menu Text	Col	Row	Default Setting	Available Setting
Description				
P643 and P645 only. Threshold of the TV HighZ restricted earth fault.				
TV Trans.Bias	32	38	Enabled	Enabled or Disabled
Default setting 'Enabled' means REF protection is same as version B2A, 'Disabled ' means the transient bias is removed from bias current for all cases.				
REF Auto status	32	40	LowZ REF	Disabled, LowZ REF or HighZ REF
Enables or disables restricted earth fault protection for the Auto				
Neutral CT Input	32	41	TN1	TN1
Indicates which single phase CT is used for Auto REF calculation.				
Auto IS1 Set	32	42	0.09	0.02In to 1In step 0.01In
Minimum differential threshold of the Auto REF characteristic				
Auto IS2 Set	32	43	0.9	0.1In to 10In step 0.1In
Bias current threshold for the second slope of the Auto REF characteristic				
Auto IREF K1	32	44	0	0% to 150% step 1%
First slope setting of the Auto REF characteristic. Normally set to 0% to give optimum sensitivity for internal faults				
Auto IREF K2	32	45	1.5	15% to 150% step 1%
Second slope setting of the Auto REF characteristic. Normally set to 150% to ensure adequate restraint for external faults				
Auto tREF	32	46	0s	0s to 10s step 0.01s
Operating time delay for the Auto restricted earth fault element				
Auto IS1 Set	32	47	0.09	0.02In to 1In step 0.01In
Threshold of the Auto HighZ restricted earth fault.				
Auto Trans.Bias	32	48	Enabled	Enabled or Disabled
Default setting 'Enabled' means REF protection is same as version B2A, 'Disabled ' means the transient bias is removed from bias current for all cases.				

Table 4 - Group 1 REF protection settings

4.4 NPS Overcurrent

Menu Text	Col	Row	Default Setting	Available Setting
Description				
GROUP 1: NPS OVERCURRENT	34	00		
This column contains GROUP 1: NPS OVERCURRENT parameters				
NPS O/C 1	34	01	T1	Disabled, HV Winding, LV Winding, TV Winding, T1, T2, T3, T4 or T5
Negative Sequence Overcurrent 1				
I2>1 Status	34	02	Disabled	Enabled or Disabled
Enables or disables stage 1 of NPS OC 1				
I2>1 Char	34	03	DT (DT)	DT (DT), IEC S Inverse (TMS), IEC V Inverse (TMS), IEC E Inverse (TMS), UK LT Inverse (TMS), Rectifier (TMS), RI (K), IEEE M Inverse (TD), IEEE V Inverse (TD), IEEE E Inverse (TD), US Inverse (TD) or US ST Inverse (TD)
Slelect the stage 1 of NPSOC element 1 time characteristic				
I2>1 Direction	34	04	Non-Directional	Non-directional, Directional Fwd or Directional Rev
Determines the direction of measurement for this element				
I2>1 Current Set	34	05	0.2*I1	0.08*I1 to 4*I1 step 0.01*I1
Current pick-up setting for the stage 1 NPS element 1				
I2>1 Time Delay	34	06	10s	0s to 100s step 0.01s
Operating time delay for the stage 1 NPS overcurrent element 1				
I2>1 TMS	34	07	1s	0.025 to 1.2 step 0.025
Setting for the time multiplier setting to adjust the operating time of IEC IDMT characteristic				
I2>1 Time Dial	34	08	1	0.01 to 100 step 0.01
Setting for the time dial setting to adjust the operating time of IEEE/US IDMT characteristic				
I2>1 K(RI)	34	09	1	0.1 to 10 step 0.05
Setting for the time multiplier setting to adjust the oprating time for the RI IDMT characteristic				
I2>1 Reset Char	34	0A	DT	DT or Inverse
Setting to determine the type of reset/release characteristic of the IEEE/US curves				
I2>1 tReset	34	0B	0s	0s to 100s step 0.01s
Setting that determine the reset/release time for definite time reset characteristic				
I2>2 Status	34	12	Disabled	Enabled or Disabled
Enables or disables stage 2 of NPS OC 1				
I2>2 Char	34	13	DT (DT)	DT (DT), IEC S Inverse (TMS), IEC V Inverse (TMS), IEC E Inverse (TMS), UK LT Inverse (TMS), Rectifier (TMS), RI (K), IEEE M Inverse (TD), IEEE V Inverse (TD), IEEE E Inverse (TD), US Inverse (TD) or US ST Inverse (TD)
Slelect stage 2 of NPSOC element 1 time characteristic				
I2>2 Direction	34	14	Non-Directional	Non-directional, Directional Fwd or Directional Rev
Determines the direction of measurement for this element				
I2>2 Current Set	34	15	0.2*I1	0.08*I1 to 4*I1 step 0.01*I1
Current pick-up setting for the stage 2 NPS element 1				
I2>2 Time Delay	34	16	10s	0s to 100s step 0.01s
Operating time delay for the stage 2 NPS overcurrent element 1				
I2>2 TMS	34	17	1s	0.025 to 1.2 step 0.025

Menu Text	Col	Row	Default Setting	Available Setting
Description				
Setting for the time multiplier setting to adjust the operating time of IEC IDMT characteristic				
I2>2 Time Dial	34	18	1	0.01 to 100 step 0.01
Setting for the time dial setting to adjust the operating time of IEEE/US IDMT characteristic				
I2>2 K(RI)	34	19	1	0.1 to 10 step 0.05
Setting for the time multiplier setting to adjust the oprating time for the RI IDMT characteristic				
I2>2 Reset Char	34	1A	DT	DT or Inverse
Setting to determine the type of reset/release characteristic of the IEEE/US curves				
I2>2 tReset	34	1B	0s	0s to 100s step 0.01s
Setting that determine the reset/release time for definite time reset characteristic				
I2>3 Status	34	21	Disabled	Enabled or Disabled
Enables or disables stage 3 NPS definite time element 1				
I2>3 Direction	34	22	Non-Directional	Non-directional, Directional Fwd or Directional Rev
Determines the direction of measurement for this element				
I2>3 Current Set	34	23	0.2*I1	0.08*I1 to 4*I1 step 0.01*I1
Current pick-up setting for the stage 3 NPS element 1				
I2>3 Time Delay	34	24	10s	0s to 100s step 0.01s
Operating time delay for the stage 3 NPS overcurrent element 1				
I2>4 Status	34	27	Disabled	Enabled or Disabled
Enables or disables stage 4 NPS definite time element 1				
I2>4 Direction	34	28	Non-Directional	Non-directional, Directional Fwd or Directional Rev
Determines the direction of measurement for this element				
I2>4 Current Set	34	29	0.2*I1	0.08*I1 to 4*I1 step 0.01*I1
Current pick-up setting for the stage 4 NPS element 1				
I2>4 Time Delay	34	2A	10s	0s to 100s step 0.01s
Operating time delay for the stage 4 NPS overcurrent element 1				
I2> VTS Block	34	2D	15	4-bit binary setting
Logic settings that determine whether VT supervision will block selected negative sequence overcurrent stages. VTS Block only affects directional overcurrent protection. Setting 0 allows continued non-directional operation				
I2> V2pol Set	34	2E	5*V1	0.5*V1 to 25*V1 step 0.5*V1
The minimum threshold above which the relay must detect a polarizing voltage for the negative phase sequence directional elements to operate				
I2> Char Angle	34	2F	-60°	-95° to 95° step 1°'
Characteristic angle for directionalized NPS fault protection				
NPS O/C 2	34	31	P642: T2 P643: T3 P645: T5	Disabled, HV Winding, LV Winding, TV Winding, T1, T2, T3, T4 or T5
Negative Sequence Overcurrent 2				
I2>1 Status	34	32	Disabled	Enabled or Disabled
Enables or disables stage 1 of NPS OC 2				
I2>1 Char	34	33	DT (DT)	DT (DT), IEC S Inverse (TMS), IEC V Inverse (TMS), IEC E Inverse (TMS), UK LT Inverse (TMS), Rectifier (TMS), RI (K), IEEE M Inverse (TD), IEEE V Inverse (TD), IEEE E Inverse (TD), US Inverse (TD) or US ST Inverse (TD)
Slelect stage 1 of NPSOC element 2 time characteristic				
I2>1 Direction	34	34	Non-Directional	Non-directional, Directional Fwd or Directional Rev

Menu Text	Col	Row	Default Setting	Available Setting
Description				
Determines the direction of measurement for this element				
I2>1 Current Set	34	35	0.2*I1	0.08*I1 to 4*I1 step 0.01*I1
Current pick-up setting for the stage 1 NPS element 2				
I2>1 Time Delay	34	36	10s	0s to 100s step 0.01s
Operating time delay for the stage 1 NPS overcurrent element 2				
I2>1 TMS	34	37	1s	0.025 to 1.2 step 0.025
Setting for the time multiplier setting to adjust the operating time of IEC IDMT characteristic				
I2>1 Time Dial	34	38	1	0.01 to 100 step 0.01
Setting for the time dial setting to adjust the operating time of IEEE/US IDMT characteristic				
I2>1 K(RI)	34	39	1	0.1 to 10 step 0.05
Setting for the time multiplier setting to adjust the oprating time for the RI IDMT characteristic				
I2>1 Reset Char	34	3A	DT	DT or Inverse
Setting to determine the type of reset/release characteristic of the IEEE/US curves				
I2>1 tReset	34	3B	0s	0s to 100s step 0.01s
Setting that determine the reset/release time for definite time reset characteristic				
I2>2 Status	34	42	Disabled	Enabled or Disabled
Enables or disables stage 2 NPS OC 2				
I2>2 Char	34	43	DT (DT)	DT (DT), IEC S Inverse (TMS), IEC V Inverse (TMS), IEC E Inverse (TMS), UK LT Inverse (TMS), Rectifier (TMS), RI (K), IEEE M Inverse (TD), IEEE V Inverse (TD), IEEE E Inverse (TD), US Inverse (TD) or US ST Inverse (TD)
Slelect stage 2 of NPSOC element 2 time characteristic				
I2>2 Direction	34	44	Non-Directional	Non-directional, Directional Fwd or Directional Rev
Determines the direction of measurement for this element				
I2>2 Current Set	34	45	0.2*I1	0.08*I1 to 4*I1 step 0.01*I1
Current pick-up setting for the stage 2 NPS element 2				
I2>2 Time Delay	34	46	10s	0s to 100s step 0.01s
Operating time delay for the stage 2 NPS overcurrent element 2				
I2>2 TMS	34	47	1s	0.025 to 1.2 step 0.025
Setting for the time multiplier setting to adjust the operating time of IEC IDMT characteristic				
I2>2 Time Dial	34	48	1	0.01 to 100 step 0.01
Setting for the time dial setting to adjust the operating time of IEEE/US IDMT characteristic				
I2>2 K(RI)	34	49	1	0.1 to 10 step 0.05
Setting for the time multiplier setting to adjust the oprating time for the RI IDMT characteristic				
I2>2 Reset Char	34	4A	DT	DT or Inverse
Setting to determine the type of reset/release characteristic of the IEEE/US curves				
I2>2 tReset	34	4B	0s	0s to 100s step 0.01s
Setting that determine the reset/release time for definite time reset characteristic				
I2>3 Status	34	51	Disabled	Enabled or Disabled
Enables or disables stage 3 NPS OC 2				
I2>3 Direction	34	52	Non-Directional	Non-directional, Directional Fwd or Directional Rev
Determines the direction of measurement for this element				
I2>3 Current Set	34	53	0.2	24A to 1200A step 3A
Current pick-up setting for the stage 3 NPS OC 2				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
I2>3 Time Delay	34	54	10	0s to 100s step 0.01s
Operating time delay for the stage 3 NPS OC 2				
I2>4 Status	34	57	Disabled	Enabled or Disabled
Enables or disables stage 4 NPS OC 2				
I2>4 Direction	34	58	Non-Directional	Non-directional, Directional Fwd or Directional Rev
Determines the direction of measurement for this element				
I2>4 Current Set	34	59	0.2*I1	0.08*I1 to 4*I1 step 0.01*I1
Current pick-up setting for the stage 4 OC 2				
I2>4 Time Delay	34	5A	10s	0s to 100s step 0.01s
Operating time delay for the stage 4 NPS OC2				
I2> VTS Block	34	5D	15	4-bit binary setting
Logic settings that determine whether VT supervision will block selected negative sequence overcurrent stages. VTS Block only affects directional overcurrent protection. Setting 0 allows continued non-directional operation				
I2> V2pol Set	34	5E	5*V1	0.5*V1 to 25*V1 step 0.5*V1
The minimum threshold above which the relay must detect a polarizing voltage for the negative phase sequence directional elements to operate				
I2> Char Angle	34	5F	-60°	-95° to 95° step 1°
Characteristic angle for directionalized NPS fault protection				
NPS O/C 3	34	61	P643: T2 P645: T3	Disabled, HV Winding, LV Winding, TV Winding, T1, T2, T3, T4 or T5
P643 and P645 only. Negetive Sequence Overcurrent 3				
I2>1 Status	34	62	Disabled	Enabled or Disabled
P643 and P645 only. Enables or disables stage 1 of NPS OC 3				
I2>1 Char	34	63	DT (DT)	DT (DT), IEC S Inverse (TMS), IEC V Inverse (TMS), IEC E Inverse (TMS), UK LT Inverse (TMS), Rectifier (TMS), RI (K), IEEE M Inverse (TD), IEEE V Inverse (TD), IEEE E Inverse (TD), US Inverse (TD) or US ST Inverse (TD)
P643 and P645 only. Slelect stage 1 of NPSOC element 3 time characteristic				
I2>1 Direction	34	64	Non-Directional	Non-directional, Directional Fwd or Directional Rev
P643 and P645 only. Determines the direction of measurement for this element				
I2>1 Current Set	34	65	0.2*I1	0.08*I1 to 4*I1 step 0.01*I1
P643 and P645 only. Current pick-up setting for the stage 1 NPS element 3				
I2>1 Time Delay	34	66	10s	0s to 100s step 0.01s
P643 and P645 only. Operating time delay for the stage 1 NPS overcurrent element 3				
I2>1 TMS	34	67	1s	0.025 to 1.2 step 0.025
P643 and P645 only. Setting for the time multiplier setting to adjust the operating time of IEC IDMT characteristic				
I2>1 Time Dial	34	68	1	0.01 to 100 step 0.01
P643 and P645 only. Setting for the time dial setting to adjust the operating time of IEEE/US IDMT characteristic				
I2>1 K(RI)	34	69	1	0.1 to 10 step 0.05

Menu Text	Col	Row	Default Setting	Available Setting
Description				
P643 and P645 only. Setting for the time multiplier setting to adjust the oprating time for the RI IDMT characteristic				
I2>1 Reset Char	34	6A	DT	DT or Inverse
P643 and P645 only. Setting to determine the type of reset/release characteristic of the IEEE/US curves				
I2>1 tReset	34	6B	0s	0s to 100s step 0.01s
P643 and P645 only. Setting that determine the reset/release time for definite time reset characteristic				
I2>2 Status	34	72	Disabled	Enabled or Disabled
P643 and P645 only. Enables or disables stage 2 of NPS OC 3				
I2>2 Char	34	73	DT (DT)	DT (DT), IEC S Inverse (TMS), IEC V Inverse (TMS), IEC E Inverse (TMS), UK LT Inverse (TMS), Rectifier (TMS), RI (K), IEEE M Inverse (TD), IEEE V Inverse (TD), IEEE E Inverse (TD), US Inverse (TD) or US ST Inverse (TD)
P643 and P645 only. Slelect stage 2 of NPSOC element 3 time characteristic				
I2>2 Direction	34	74	Non-Directional	Non-directional, Directional Fwd or Directional Rev
P643 and P645 only. Determines the direction of measurement for this element				
I2>2 Current Set	34	75	0.2*I1	0.08*I1 to 4*I1 step 0.01*I1
P643 and P645 only. Current pick-up setting for the stage 2 NPS element 3				
I2>2 Time Delay	34	76	10s	0s to 100s step 0.01s
P643 and P645 only. Operating time delay for the stage 2 NPS overcurrent element 3				
I2>2 TMS	34	77	1s	0.025 to 1.2 step 0.025
P643 and P645 only. Setting for the time multiplier setting to adjust the operating time of IEC IDMT characteristic				
I2>2 Time Dial	34	78	1	0.01 to 100 step 0.01
P643 and P645 only. Setting for the time dial setting to adjust the operating time of IEEE/US IDMT characteristic				
I2>2 K(RI)	34	79	1	0.1 to 10 step 0.05
P643 and P645 only. Setting for the time multiplier setting to adjust the oprating time for the RI IDMT characteristic				
I2>2 Reset Char	34	7A	DT	DT or Inverse
P643 and P645 only. Setting to determine the type of reset/release characteristic of the IEEE/US curves				
I2>2 tReset	34	7B	0s	0s to 100s step 0.01s
P643 and P645 only. Setting that determine the reset/release time for definite time reset characteristic				
I2>3 Status	34	81	Disabled	Enabled or Disabled
P643 and P645 only. Enables or disables stage 3 NPS OC 3				
I2>3 Direction	34	82	Non-Directional	Non-directional, Directional Fwd or Directional Rev
P643 and P645 only. Determines the direction of measurement for this element				
I2>3 Current Set	34	83	0.2*I1	0.08*I1 to 4*I1 step 0.01*I1

Menu Text	Col	Row	Default Setting	Available Setting
Description				
P643 and P645 only. Current pick-up setting for the stage 3 NPS OC 3				
I2>3 Time Delay	34	84	10s	0s to 100s step 0.01s
P643 and P645 only. Operating time delay for the stage 3 NPS OC 3				
I2>4 Status	34	87	Disabled	Enabled or Disabled
P643 and P645 only. Enables or disables stage 4 NPS OC 3				
I2>4 Direction	34	88	Non-Directional	Non-directional, Directional Fwd or Directional Rev
P643 and P645 only. Determines the direction of measurement for this element				
I2>4 Current Set	34	89	0.2*I1	0.08*I1 to 4*I1 step 0.01*I1
P643 and P645 only. Current pick-up setting for the stage 4 NPS OC 3				
I2>4 Time Delay	34	8A	10s	0s to 100s step 0.01s
P643 and P645 only. Operating time delay for the stage 4 NPS OC 3				
I2> VTS Block	34	8D	15	4-bit binary setting
P643 and P645 only. Logic settings that determine whether VT supervision will block selected negative sequence overcurrent stages. VTS Block only affects directional overcurrent protection. Setting 0 allows continued non-directional operation				
I2> V2pol Set	34	8E	5*V1	0.5*V1 to 25*V1 step 0.5*V1
P643 and P645 only. The minimum threshold above which the relay must detect a polarizing voltage for the negative phase sequence directional elements to operate				
I2> Char Angle	34	8F	-60°	-95° to 95° step 1°
P643 and P645 only. Characteristic angle for directionalized NPS fault protection				

Table 5 - Group 1 NPS overcurrent settings

4.5 Overcurrent

Menu Text	Col	Row	Default Setting	Available Setting
Description				
GROUP 1: OVERCURRENT 1	35	00		
This column contains GROUP 1: OVERCURRENT 1 parameters				
Overcurrent 1	35	01	T1	Disabled, HV Winding, LV Winding, TV Winding, T1, T2, T3, T4 or T5
Overcurrent 1				
I>1 Status	35	02	Disabled	Enabled or Disabled
Setting to enable or disable the first stage overcurrent element				
I>1 Char	35	03	IEC S Inverse	DT (DT), IEC S Inverse (TMS), IEC V Inverse (TMS), IEC E Inverse (TMS), UK LT Inverse (TMS), Rectifier (TMS), RI (K), IEEE M Inverse (TD), IEEE V Inverse (TD), IEEE E Inverse (TD), US Inverse (TD) or US ST Inverse (TD)
Setting for the tripping characteristic for the first stage overcurrent element				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
I>1 Direction	35	04	Non-Directional	Non-directional, Directional Fwd or Directional Rev
This setting determines the direction of measurement for the first stage element				
I>1 Current Set	35	05	1	24A to 1200A step 3A
Pick-up setting for the first stage overcurrent element				
I>1 Time Delay	35	06	1s	0s to 100s step 0.01s
Setting for the time delay for the definite time setting if selected for the first stage element				
I>1 TMS	35	07	1	0.025 to 1.2 step 0.025
Setting for the time multiplier setting to adjust the operating time of the IEC IDMT characteristic				
I>1 Time Dial	35	08	1	0.01 to 100 step 0.01
Setting for the time multiplier setting to adjust the operating time of the IEEE/US IDMT curves				
I>1 K (RI)	35	09	1	0.1 to 10 step 0.05
Setting for the time multiplier to adjust the operating time for the RI curve				
I>1 Reset Char	35	0A	DT	DT or Inverse
Setting to determine the type of reset/release characteristic of the IEEE/US curves				
I>1 tRESET	35	0B	0	0s to 100s step 0.01s
Setting that determines the reset/release time for definite time reset characteristic				
I>2 Status	35	12	Disabled	Enabled or Disabled
Setting to enable or disable the first stage overcurrent element				
I>2 Char	35	13	DT (DT)	DT (DT), IEC S Inverse (TMS), IEC V Inverse (TMS), IEC E Inverse (TMS), UK LT Inverse (TMS), Rectifier (TMS), RI (K), IEEE M Inverse (TD), IEEE V Inverse (TD), IEEE E Inverse (TD), US Inverse (TD) or US ST Inverse (TD)
Setting for the tripping characteristic for the second stage overcurrent element				
I>2 Direction	35	14	Non-Directional	Non-directional, Directional Fwd or Directional Rev
This setting determines the direction of measurement for the second stage element				
I>2 Current Set	35	15	1	24A to 1200A step 3A
Pick-up setting for the second stage overcurrent element				
I>2 Time Delay	35	16	1s	0s to 100s step 0.01s
Setting for the time delay for the definite time setting if selected for the second stage element.				
I>2 TMS	35	17	1s	0.025 to 1.2 step 0.025
Setting for the time multiplier setting to adjust the operating time of the IEC IDMT characteristic				
I>2 Time Dial	35	18	1	0.01 to 100 step 0.01
Setting for the time multiplier setting to adjust the operating time of the IEEE/US IDMT curves				
I>2 K (RI)	35	19	1	0.1 to 10 step 0.05
Setting for the time multiplier to adjust the operating time for the RI curve				
I>2 Reset Char	35	1A	DT	DT or Inverse
Setting to determine the type of reset/release characteristic of the IEEE/US curves				
I>2 tRESET	35	1B	0s	0s to 100s step 0.01s
Setting that determines the reset/release time for definite time reset characteristic				
I>3 Status	35	21	Disabled	Enabled or Disabled
Setting to enable or disable the third stage overcurrent element				
I>3 Direction	35	22	Non-Directional	Non-directional, Directional Fwd or Directional Rev
This setting determines the direction of measurement for the third stage element				
I>3 Current Set	35	23	10A	24A to 3840A step 3A

Menu Text	Col	Row	Default Setting	Available Setting
Description				
Pick-up setting for the third stage overcurrent element				
I>3 Time Delay	35	24	0s	0s to 100s step 0.01s
Setting for the time delay for the definite time setting if selected for the third stage element				
I>4 Status	35	27	Disabled	Enabled or Disabled
Setting to enable or disable the fourth stage overcurrent element				
I>4 Direction	35	28	Non-Directional	Non-directional, Directional Fwd or Directional Rev
This setting determines the direction of measurement for the fourth stage element				
I>4 Current Set	35	29	10	24A to 3840A step 3A
Pick-up setting for the fourth stage overcurrent element				
I>4 Time Delay	35	2A	0s	0s to 100s step 0.01s
Setting for the time delay for the definite time setting if selected for the fourth stage element.				
I> Char Angle	35	2D	30°	-95°' to 95° step '1°'
Setting for the relay characteristic angle used for the directional decision				
I> Function Link	35	2E	15	4-bit binary setting
Logic Settings that determine whether blocking signals from VT supervision affect certain overcurrent stages				
Overcurrent 2	35	31	P642: T2 P643: T3 P645: T5	Disabled, HV Winding, LV Winding, TV Winding, T1, T2, T3, T4 or T5
Overcurrent 2				
I>1 Status	35	32	Disabled	Enabled or Disabled
Setting to enable or disable the first stage overcurrent element				
I>1 Char	35	33	IEC S Inverse	DT (DT), IEC S Inverse (TMS), IEC V Inverse (TMS), IEC E Inverse (TMS), UK LT Inverse (TMS), Rectifier (TMS), RI (K), IEEE M Inverse (TD), IEEE V Inverse (TD), IEEE E Inverse (TD), US Inverse (TD) or US ST Inverse (TD)
Setting for the tripping characteristic for the first stage overcurrent element				
I>1 Direction	35	34	Non-Directional	Non-directional, Directional Fwd or Directional Rev
This setting determines the direction of measurement for the first stage element				
I>1 Current Set	35	35	1	24A to 1200A step 3A
Pick-up setting for the first stage overcurrent element				
I>1 Time Delay	35	36	1s	0s to 100s step 0.01s
Setting for the time delay for the definite time setting if selected for the first stage element				
I>1 TMS	35	37	1	0.025 to 1.2 step 0.025
Setting for the time multiplier setting to adjust the operating time of the IEC IDMT characteristic				
I>1 Time Dial	35	38	1	0.01 to 100 step 0.01
Setting for the time multiplier setting to adjust the operating time of the IEEE/US IDMT curves				
I>1 K (RI)	35	39	1	0.1 to 10 step 0.05
Setting for the time multiplier to adjust the operating time for the RI curve				
I>1 Reset Char	35	3A	DT	DT or Inverse
Setting to determine the type of reset/release characteristic of the IEEE/US curves				
I>1 tRESET	35	3B	0s	0s to 100s step 0.01s
Setting that determines the reset/release time for definite time reset characteristic				
I>2 Status	35	42	Disabled	Enabled or Disabled
Setting to enable or disable the second stage overcurrent element				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
I>2 Char	35	43	IEC S Inverse	DT (DT), IEC S Inverse (TMS), IEC V Inverse (TMS), IEC E Inverse (TMS), UK LT Inverse (TMS), Rectifier (TMS), RI (K), IEEE M Inverse (TD), IEEE V Inverse (TD), IEEE E Inverse (TD), US Inverse (TD) or US ST Inverse (TD)
Setting for the tripping characteristic for the first stage overcurrent element				
I>2 Direction	35	44	Non-Directional	Non-directional, Directional Fwd or Directional Rev
This setting determines the direction of measurement for the second stage element				
I>2 Current Set	35	45	1	24A to 1200A step 3A
Pick-up setting for the second stage overcurrent element				
I>2 Time Delay	35	46	1	0s to 100s step 0.01s
Setting for the time delay for the definite time setting if selected for the second stage element.				
I>2 TMS	35	47	1	0.025 to 1.2 step 0.025
Setting for the time multiplier setting to adjust the operating time of the IEC IDMT characteristic				
I>2 Time Dial	35	48	1	0.01 to 100 step 0.01
Setting for the time multiplier setting to adjust the operating time of the IEEE/US IDMT curves				
I>2 K (RI)	35	49	1	0.1 to 10 step 0.05
Setting for the time multiplier to adjust the operating time for the RI curve				
I>2 Reset Char	35	4A	DT	DT or Inverse
Setting to determine the type of reset/release characteristic of the IEEE/US curves				
I>2 tRESET	35	4B	0	0s to 100s step 0.01s
Setting that determines the reset/release time for definite time reset characteristic				
I>3 Status	35	51	Disabled	Enabled or Disabled
Setting to enable or disable the third stage overcurrent element				
I>3 Direction	35	52	Non-Directional	Non-directional, Directional Fwd or Directional Rev
This setting determines the direction of measurement for the third stage element				
I>3 Current Set	35	53	10	24A to 3840A step 3A
Pick-up setting for the third stage overcurrent element				
I>3 Time Delay	35	54	0	0s to 100s step 0.01s
Setting for the time delay for the definite time setting if selected for the third stage element				
I>4 Status	35	57	Disabled	Enabled or Disabled
Setting to enable or disable the fourth stage overcurrent element				
I>4 Direction	35	58	Non-Directional	Non-directional, Directional Fwd or Directional Rev
This setting determines the direction of measurement for the fourth stage element				
I>4 Current Set	35	59	10	24A to 3840A step 3A
Pick-up setting for the fourth stage overcurrent element				
I>4 Time Delay	35	5A	0s	0s to 100s step 0.01s
Setting for the time delay for the definite time setting if selected for the fourth stage element.				
I> Char Angle	35	5D	30°	-95° to 95° step 1°
Setting for the relay characteristic angle used for the directional decision				
I> Function Link	35	5E	15	4-bit binary setting
Logic Settings that determine whether blocking signals from VT supervision affect certain overcurrent stages				
Overcurrent 3	35	61	P643: T2 P645: T3	P643 and P645 only. Disabled, HV Winding, LV Winding, TV Winding, T1, T2, T3, T4 or T5

Menu Text	Col	Row	Default Setting	Available Setting
Description				
P643 and P645 only. Overcurrent 3				
I>1 Status	35	62	Disabled	Enabled or Disabled
P643 and P645 only. Setting to enable or disable the first stage overcurrent element				
I>1 Char	35	63	IEC S Inverse	DT (DT), IEC S Inverse (TMS), IEC V Inverse (TMS), IEC E Inverse (TMS), UK LT Inverse (TMS), Rectifier (TMS), RI (K), IEEE M Inverse (TD), IEEE V Inverse (TD), IEEE E Inverse (TD), US Inverse (TD) or US ST Inverse (TD)
P643 and P645 only. Setting for the tripping characteristic for the first stage overcurrent element				
I>1 Direction	35	64	Non-Directional	Non-directional, Directional Fwd or Directional Rev
P643 and P645 only. This setting determines the direction of measurement for the first stage element				
I>1 Current Set	35	65	1	24A to 1200A step 3A
P643 and P645 only. Pick-up setting for the first stage overcurrent element				
I>1 Time Delay	35	66	1	0s to 100s step 0.01s
P643 and P645 only. Setting for the time delay for the definite time setting if selected for the first stage element				
I>1 TMS	35	67	1	0.025 to 1.2 step 0.025
P643 and P645 only. Setting for the time multiplier setting to adjust the operating time of the IEC IDMT characteristic				
I>1 Time Dial	35	68	1	0.01 to 100 step 0.01
P643 and P645 only. Setting for the time multiplier setting to adjust the operating time of the IEEE/US IDMT curves				
I>1 K (RI)	35	69	1	0.1 to 10 step 0.05
P643 and P645 only. Setting for the time multiplier to adjust the operating time for the RI curve				
I>1 Reset Char	35	6A	DT	DT or Inverse
P643 and P645 only. Setting to determine the type of reset/release characteristic of the IEEE/US curves				
I>1 tRESET	35	6B	0	0s to 100s step 0.01s
P643 and P645 only. Setting that determines the reset/release time for definite time reset characteristic				
I>2 Status	35	72	Disabled	Enabled or Disabled
P643 and P645 only. Setting to enable or disable the second stage overcurrent element				
I>2 Char	35	73	DT (DT)	DT (DT), IEC S Inverse (TMS), IEC V Inverse (TMS), IEC E Inverse (TMS), UK LT Inverse (TMS), Rectifier (TMS), RI (K), IEEE M Inverse (TD), IEEE V Inverse (TD), IEEE E Inverse (TD), US Inverse (TD) or US ST Inverse (TD)
P643 and P645 only. Setting for the tripping characteristic for the second stage overcurrent element				
I>2 Direction	35	74	Non-Directional	Non-directional, Directional Fwd or Directional Rev
P643 and P645 only. This setting determines the direction of measurement for the second stage element				
I>2 Current Set	35	75	1	24A to 1200A step 3A
P643 and P645 only. Pick-up setting for the second stage overcurrent element				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
I>2 Time Delay	35	76	1	0s to 100s step 0.01s
P643 and P645 only. Setting for the time delay for the definite time setting if selected for the second stage element.				
I>2 TMS	35	77	1	0.025 to 1.2 step 0.025
P643 and P645 only. Setting for the time multiplier setting to adjust the operating time of the IEC IDMT characteristic				
I>2 Time Dial	35	78	1	0.01 to 100 step 0.01
P643 and P645 only. Setting for the time multiplier setting to adjust the operating time of the IEEE/US IDMT curves				
I>2 K (RI)	35	79	1	0.1 to 10 step 0.05
P643 and P645 only. Setting for the time multiplier to adjust the operating time for the RI curve				
I>2 Reset Char	35	7A	DT	DT or Inverse
P643 and P645 only. Setting to determine the type of reset/release characteristic of the IEEE/US curves				
I>2 tRESET	35	7B	0	0s to 100s step 0.01s
P643 and P645 only. Setting that determines the reset/release time for definite time reset characteristic				
I>3 Status	35	81	Disabled	Enabled or Disabled
P643 and P645 only. Setting to enable or disable the third stage overcurrent element				
I>3 Direction	35	82	Non-Directional	Non-directional, Directional Fwd or Directional Rev
P643 and P645 only. This setting determines the direction of measurement for the third stage element				
I>3 Current Set	35	83	10	24A to 3840A step 3A
P643 and P645 only. Pick-up setting for the third stage overcurrent element				
I>3 Time Delay	35	84	0	0s to 100s step 0.01s
P643 and P645 only. Setting for the time delay for the definite time setting if selected for the third stage element				
I>4 Status	35	87	Disabled	Enabled or Disabled
P643 and P645 only. Setting to enable or disable the fourth stage overcurrent element				
I>4 Direction	35	88	Non-Directional	Non-directional, Directional Fwd or Directional Rev
P643 and P645 only. This setting determines the direction of measurement for the fourth stage element				
I>4 Current Set	35	89	10	24A to 3840A step 3A
P643 and P645 only. Pick-up setting for the fourth stage overcurrent element				
I>4 Time Delay	35	8A	0s	0s to 100s step 0.01s
P643 and P645 only. Setting for the time delay for the definite time setting if selected for the fourth stage element.				
I> Char Angle	35	8D	30°	-95° to 95° step 1°
P643 and P645 only. Setting for the relay characteristic angle used for the directional decision				
I> Function Link	35	8E	15	4-bit binary setting
P643 and P645 only. Logic Settings that determine whether blocking signals from VT supervision affect certain overcurrent stages				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
V DEPENDANT O/C	35	90	Sub-Heading	Sub-Heading
Sub-Heading for voltage dependant over current				
V Dep OC>1 Mode	35	91	VCO	0 = VCO, 1 = VRO
Voltage dependant overcurrent stage 1 mode				
V OC>1	35	92	Disabled	Disabled, HV Winding, LV Winding, TV Winding, T1, T2, T3, T4 or T5
Enable or disable Voltage dependant overcurrent stage 1				
V OC>1 Char	35	93	IEC S Inverse	DT (DT), IEC S Inverse (TMS), IEC V Inverse (TMS), IEC E Inverse (TMS), UK LT Inverse (TMS), Rectifier (TMS), RI (K), IEEE M Inverse (TD), IEEE V Inverse (TD), IEEE E Inverse (TD), US Inverse (TD) or US ST Inverse (TD)
Setting for the tripping characteristic for the first stage voltage dependant overcurrent element				
V OC>1 Direction	35	94	Non-Directional	Non-directional, Directional Fwd or Directional Rev
This setting determines the direction of measurement for the first stage element				
V OC>1 Curr' Set	35	95	1	24A to 1200A step 3A
Current pick-up setting for first stage the voltage dependant over current				
V OC>1 T Delay	35	96	1	0s to 100s step 0.01s
Setting for the time delay for the definite time setting if selected for the first stage element				
V OC>1 TMS	35	97	1	0.025 to 1.2 step 0.025
Setting for the time multiplier setting to adjust the operating time of the IEC IDMT characteristic				
V OC>1 Time Dial	35	98	1	0.01 to 100 step 0.01
Setting for the time multiplier setting to adjust the operating time of the IEEE/US IDMT curves				
V OC>1 k (RI)	35	99	1	0.1 to 10 step 0.05
Setting for the time multiplier to adjust the operating time for the RI curve				
V OC>1 Rst Char	35	9A	DT	DT or Inverse
Setting to determine the type of reset/release characteristic of the IEEE/US curves				
V OC>1 tRESET	35	9B	0s	0s to 100s step 0.01s
Setting that determines the reset/release time for definite time reset characteristic				
V OC>1 Angle	35	9C	30°	-95° to 95° step 1°
Setting for the relay characteristic angle used for the directional decision				
V OC>1 V<1 Set	35	9D	80	5V to 120V step 1V
Sets the voltage V1 threshold at which the current setting of the overcurrent stage/stages becomes reduced, noting that this occurs on a per phase basis.				
V OC>1 K Set	35	9E	0.25	0.1 to 1 step 0.25
Sets to determine the overcurrent multiplier factor used to reduce the pick-up overcurrent setting.				
V OC>1 V<2 Set	35	9F	60	5V to 120V step 1V
Sets the voltage V2 threshold at which the current setting of the overcurrent stage/stages becomes reduced, noting that this occurs on a per phase basis.				
V Dep OC>2 Mode	35	A1	VCO	0 = VCO, 1 = VRO
Allows selection of whether voltage control or voltage restrained should be applied.				
V OC>2	35	A2	Disabled	Disabled, HV Winding, LV Winding, TV Winding, T1, T2, T3, T4 or T5
Enable or disable Voltage dependant overcurrent stage 2				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
V OC>2 Char	35	A3	IEC S Inverse	DT (DT), IEC S Inverse (TMS), IEC V Inverse (TMS), IEC E Inverse (TMS), UK LT Inverse (TMS), Rectifier (TMS), RI (K), IEEE M Inverse (TD), IEEE V Inverse (TD), IEEE E Inverse (TD), US Inverse (TD) or US ST Inverse (TD)
Setting for the tripping characteristic for the second stage voltage dependant overcurrent element				
V OC>2 Direction	35	A4	Non-Directional	Non-directional, Directional Fwd or Directional Rev
This setting determines the direction of measurement for the second stage element				
V OC>2 Curr' Set	35	A5	1	24A to 1200A step 3A
Current pick-up setting for second stage the voltage dependant over current				
V OC>2 T Delay	35	A6	1	0s to 100s step 0.01s
Setting for the time delay for the definite time setting if selected for the second stage element				
V OC>2 TMS	35	A7	1	0.025 to 1.2 step 0.025
Setting for the time multiplier setting to adjust the operating time of the IEC IDMT characteristic				
V OC>2 Time Dial	35	A8	1	0.01 to 100 step 0.01
Setting for the time multiplier setting to adjust the operating time of the IEEE/US IDMT curves				
V OC>2 k (RI)	35	A9	1	0.1 to 10 step 0.05
Setting for the time multiplier to adjust the operating time for the RI curve				
V OC>2 Rst Char	35	AA	DT	DT or Inverse
Setting to determine the type of reset/release characteristic of the IEEE/US curves				
V OC>2 tRESET	35	AB	0s	0s to 100s step 0.01s
Setting that determines the reset/release time for definite time reset characteristic				
V OC>2 Angle	35	AC	30°	-95° to 95° step 1°
Setting for the relay characteristic angle used for the directional decision				
V OC>2 V<1 Set	35	AD	80	5V to 120V step 1V
Sets the voltage V1 threshold at which the current setting of the overcurrent stage/stages becomes reduced, noting that this occurs on a per phase basis.				
V OC>2 K Set	35	AE	0.25	0.1 to 1 step 0.25
Sets to determine the overcurrent multiplier factor used to reduce the pick-up overcurrent setting.				
V OC>2 V<2 Set	35	AF	60	5V to 120V step 1V
Sets the voltage V2 threshold at which the current setting of the overcurrent stage/stages becomes reduced, noting that this occurs on a per phase basis.				

Table 6 - Group 1 overcurrent settings

4.6 Thermal Overload

Menu Text	Col	Row	Default Setting	Available Setting
Description				
GROUP 1: THERMAL OVERLOAD	37	00		
This column contains GROUP1: THERMAL OVERLOAD parameters				
Monit'd winding	37	11	HV	HV, LV, TV or Biased Current
An overall through loading picture of the transformer is provided when the monitor winding is set to Biased Current				
Ambient T	37	12	AVERAGE	RTD 1 to 10, CLIO 1 to 4 or Average
Ambient temperature				
CLI Input Type	37	15	4-20mA	0-1 mA, 0-10m/a, 0-20mA or 4-20mA
This setting is available when Ambient T is set to CLIOx				
CLI Minimum	37	16	0	-9999 to 9999 step 0.1
This setting is available when Ambient T is set to CLIOx				
CLI Maximum	37	17	100	-9999 to 9999 step 0.1
This setting is available when Ambient T is set to CLIOx				
Average Amb T	37	18	25	-25°C to 75°C step 0.1°C
This setting is available when Ambient T is set to Average				
Top Oil Temp	37	21	CALCULATED	RTD 1 to 10, CLIO 1 to 4 or Calculated
The top oil temperature may be calculated by the relay, or it may be measured using RTD or CLIO inputs				
CLI Input Type	37	24	4-20mA	0 to 3 step 1
This setting is available when Top Oil T is set to CLIOx				
CLI Minimum	37	25	0	-9999 to 9999 step 0.1
This setting is available when Top Oil T is set to CLIOx				
CLI Maximum	37	26	100	-9999 to 9999 step 0.1
This setting is available when Top Oil T is set to CLIOx				
IB	37	29	1	0.1pu to 4pu step 0.01pu
The relay uses this setting to calculate the ratio of ultimate load to rated load				
Rated NoLoadLoss	37	2A	3	0.1 to 100 step 0.1
Ratio of load loss at rated load to no-load loss (iron loss). The transformer manufacturer should provide this parameter				
Hot Spot Overtop	37	2B	25	0.1°C to 200°C step 0.1°C
Hottest spot temperature over top oil temperature setting. The transformer manufacturer should provide this parameter				
Top Oil Overamb	37	2C	55	0.1°C to 200°C step 0.1°C
Top oil temperature over ambient temperature setting. The transformer manufacturer should provide this parameter				
Cooling Mode	37	2D	Cooling Mode 1	Cooling Mode 1, Cooling Mode 2, Cooling Mode 3, Cooling Mode 4 or Select via PSL
This setting is uesed to select the cooling Mode				
Cooling Mode 1	37	2F	Sub-Heading	Sub-Heading
This is the Sub-Heading for cooling mode 1. It is visible when cooling mode is selected to be cooling mode 1 or to be select from PSL				
Winding exp m	37	30	0.8	0.01 to 2 step 0.01
Winding exponient m for cooling mode 1, available when cooling mode is selected to be cooling mode 1 or select from PSL				
Oil exp n	37	31	0.8	0.01 to 2 step 0.01
oil exponient n for cooling mode 1, available when cooling mode is selected to be cooling mode 1 or select from PSL				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
Cooling Mode 2	37	32	Sub-Heading	Sub-Heading
This is the Sub-Heading for cooling mode 2. It is visible when cooling mode is selected to be cooling mode 2 or to be select from PSL				
Winding exp m	37	33	0.8	0.01 to 2 step 0.01
Winding exponient m for cooling mode 2, available when cooling mode is selected to be cooling mode 2 or select from PSL				
Oil exp n	37	34	0.8	0.01 to 2 step 0.01
oil exponient n for cooling mode 2, available when cooling mode is selected to be cooling mode 2 or select from PSL				
Cooling Mode 3	37	35	Sub-Heading	Sub-Heading
This is the Sub-Heading for cooling mode 3. It is visible when cooling mode is selected to be cooling mode 3 or to be select from PSL				
Winding exp m	37	36	0.8	0.01 to 2 step 0.01
Winding exponient m for cooling mode 3, available when cooling mode is selected to be cooling mode 3 or select from PSL				
Oil exp n	37	37	0.8	0.01 to 2 step 0.01
oil exponient n for cooling mode 3, available when cooling mode is selected to be cooling mode 3 or select from PSL				
Cooling Mode 4	37	38	Sub-Heading	Sub-Heading
This is the Sub-Heading for cooling mode 4. It is visible when cooling mode is selected to be cooling mode 4 or to be select from PSL				
Winding exp m	37	39	0.8	0.01 to 2 step 0.01
Winding exponient m for cooling mode 4, available when cooling mode is selected to be cooling mode 4 or select from PSL				
Oil exp n	37	3A	0.8	0.01 to 2 step 0.01
oil exponient n for cooling mode 4, available when cooling mode is selected to be cooling mode 4 or select from PSL				
Hot spot rise co	37	3B	1	0.01 min to 20 min step 0.01 min
Hot spot rise co parameters used to calculate the hot spot temperature				
Top oil rise co	37	3C	120	1 min to 1000 min step 1 min
Top oil reis co parameters used to calculate the top oil temperature				
Tol Status	37	40	Enabled	Enabled or Disabled
This setting enables or disables the three hot spot and the three top oil thermal stages				
Hot Spot>1 Set	37	5E	110 deg C	1°C to 300°C step 0.1°C
Hot spot first stage setting. The suggested temperature limits given by IEEE Std. C57.91-1995 may be used to set it. See the application chapter for suggested values				
tHot Spot>1 Set	37	5F	10 mins	0 min to 60000 min step 1 min
Hot spot first stage time delay setting				
Hot Spot>2 Set	37	60	130 deg C	1°C to 300°C step 0.1°C
Hot spot second stage setting. The suggested temperature limits given by IEEE Std. C57.91-1995 may be used to set it. See the application chapter for suggested values				
tHot Spot>2 Set	37	61	10 mins	0 min to 60000 min step 0.1 min
Hot spot second stage time delay setting				
Hot Spot>3 Set	37	62	150 deg C	1°C to 300°C step 0.1°C
Hot spot third stage setting. The suggested temperature limits given by IEEE Std. C57.91-1995 may be used to set it. See the application chapter for suggested values				
tHot Spot>3 Set	37	63	10 mins	0 min to 60000 min step 1 min
Hot spot third stage time delay setting				
Top Oil>1 Set	37	64	70 deg C	1°C to 300°C step 0.1°C
Top oil first stage setting. The suggested temperature limits given by IEEE Std. C57.91-1995 may be used to set it. See the application chapter for suggested values.				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
tTop Oil>1 Set	37	65	10 mins	0 min to 60000 min step 1 min
Top oil second stage setting. The suggested temperature limits given by IEEE Std. C57.91-1995 (may be used to set it. See the application chapter for suggested values				
Top Oil>2 Set	37	66	80 deg C	1°C to 300°C step 0.1°C
Top oil second stage setting. The suggested temperature limits given by IEEE Std. C57.91-1995 (may be used to set it. See the application chapter for suggested values				
tTop Oil>2 Set	37	67	10 mins	0 min to 60000 min step 1 min
Top oil second stage time delay setting				
Top Oil>3 Set	37	68	90 deg C	1°C to 300°C step 0.1°C
Top oil third stage setting. The suggested temperature limits given by IEEE Std. C57.91-1995 may be used to set it. See the application chapter for suggested values				
tTop Oil>3 Set	37	69	10 mins	0 min to 60000 min step 1 min
Top oil third stage time delay setting				
tPre-trip Set	37	6A	5 mins	0 min to 60000 min step 1 min
After the tpre-trip timer has expired, a pre-trip alarm is given. This alarm indicates that if the load remains unchanged a thermal trip will be asserted after the stage timer has expired				
LOL Status	37	80	Enable	Enabled or Disabled
Enables or disables the loss of life function				
Life Hours at HS	37	81	180000 hrs	1 hr to 300000 hrs step 1hr
Life hours at the reference hottest spot temperature. Advice from the transformer manufacturer may be required				
Designed HS temp	37	82	110 deg C	1°C to 200°C step 0.1°C
The designed hottest spot temperature is 110°C for a transformer rated 65°C average winding rise, and 95°C for a transformer rated 55°C average winding rise				
Constant B Set	37	83	15000	1 to 100000 step 1
Constant B is associated to the life expectancy curve. It is based on modern experimental data, and it may be set to 15000 as suggested by IEEE Std. C57.91-1995				
FAA> Set	37	84	2	0.1 to 30 step 0.01
Aging acceleration factor setting. If the aging acceleration factor calculated by the relay is above this setting and tFAA has expired, an FAA alarm would be asserted. FAA calculation depends on constant B and the hottest temperature calculated by the thermal element				
tFAA> Set	37	85	10 mins	0 min to 60000 min step 1 min
Aging acceleration factor timer				
LOL>1 Set	37	86	135000 hrs	1 hr to 300000 hrs step 1hr
Transformer loss of life setting. If the life already lost by the transformer is above this threshold, an LOL alarm would be asserted after tLOL has expired. LOL calculation depends on the life hours at design hot spot temperature and the calculated residual life				
tLOL> Set	37	87	10 mins	0 min to 60000 min step 1 min
Loss of life timer				
Reset Life Hours	37	88	0 hr	1 hr to 300000 hrs step 1hr
Resets the LOL status parameter to the set value when the loss of life reset command is executed. For new transformers Reset Life Hours is zero, so that when the commissioning of the thermal element is over, the loss of life statistics calculations are reset to zero. For old transformers this setting should indicate how much life the transformer has already lost; therefore, it should be set to the transformer loss of life				

Table 7 - Group 1 thermal overload settings

4.7 Earth Fault Protection

The standard Earth Fault (EF) protection elements are duplicated within the relay and are referred to in the relay menu as "**Earth Fault 1**" (EF1) and "**Earth Fault 2**" (EF2). EF1 operates from earth fault current that is measured directly from the system; either by means of a separate CT located in a power system earth connection or via a residual connection of the three line CTs. The EF2 element operates from a residual current quantity that is derived internally from the summation of the three phase currents.

EF1 and EF2 are identical elements, each having four stages. The first and second stages have selectable IDMT or DT characteristics, whilst the third and fourth stages are DT only. Each stage is selectable to be either non-directional, directional forward or directional reverse. The timer hold facility, previously described for the overcurrent elements, is available on each of the first two stages.

The following table shows the relay menu for "**Earth Fault 1**" protection, including the available setting ranges and factory defaults. The menu for "**Earth Fault 2**" is identical to that for EF1 and so is not shown here.

Menu Text	Col	Row	Default Setting	Available Setting
Description				
GROUP 1: EARTH FAULT	38	00		
This colunm contains GROUP1 : EARTH FAULT parameters				
Earth Fault 1	38	01	Enabled	Enabled or Disabled
Enable or Disable Earth Fault 1				
EF 1 Input	38	02	Measured	Measured or Derived
Selects measured neutral current or derived neutral current				
EF 1 Derived	38	03	T1	HV Winding, LV Winding, TV Winding, T1, T2, T3, T4 or T5
This is available when earth fault is selected to be derived for stage 1 to detemine the derived current source				
EF 1 Measured	38	04	TN1	TN1, TN2 or TN3
This is available when earth fault is selected to be measured for stage 1 to determine the measured current source				
IN>1 Status	38	05	Enabled	Enabled or Disabled
Setting to enable or disable the first stage definite time element. If the function is disabled, all associated settings with the exception of this setting, are hidden				
IN>1 Char	38	06	IEC S Inverse	DT (DT), IEC S Inverse (TMS), IEC V Inverse (TMS), IEC E Inverse (TMS), UK LT Inverse (TMS), Rectifier (TMS), RI (K), IEEE M Inverse (TD), IEEE V Inverse (TD), IEEE E Inverse (TD), US Inverse (TD) or US ST Inverse (TD)
Tripping characteristic for the first stage earth fault element 1				
IN>1 Direction	38	07	Non-Directional	Non-directional, Directional Fwd or Directional Rev
Direction setting for the first stage earth fault protection 1				
IN>1 Current	38	08	0.2*In	24A to 1200A step 3A
Pick-up setting for the first stage earth fault element 1				
IN>1 IDG Is	38	09	1.5	1 to 4 step 0.1
Multiple of IN>1 setting for the IDG curve (Scandinavia), determines the actual relay current threshold at which the element starts				
IN>1 Time Delay	38	0A	1	0s to 200s step 0.01s
Operating time delay setting for the first stage definite time element				
IN>1 TMS	38	0B	1	0.025 to 1.2 step 0.025
Time multiplier setting to adjust the operating time of the IEC IDMT characteristic				
IN>1 Time Dial	38	0C	1	0.01 to 100 step 0.01
Time multiplier setting to adjust the operating time of the IEEE/US IDMT curves				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
IN>1 K (RI)	38	0D	1	0.1 to 10 step 0.05
Time multiplier to adjust the operating time for the RI curve				
IN>1 IDG Time	38	0E	1.2	1 to 2 step 0.01
Minimum operating time at high levels of fault current for the IDG curve				
IN>1 Reset Char	38	0F	DT	DT or Inverse
Type of reset/release characteristic of the IEEE/US curves				
IN>1 tRESET	38	10	0	0s to 100s step 0.01s
Reset/release time setting for definite time reset characteristic				
IN>2 Status	38	15	Disabled	Enabled or Disabled
Setting to enable or disable the second stage definite time element. If the function is disabled, all associated settings with the exception of this setting, are hidden				
IN>2 Char	38	16	DT	Disabled, DT (DT), IEC S Inverse (TMS), IEC V Inverse (TMS), IEC E Inverse (TMS), UK LT Inverse (TMS), Rectifier (TMS), RI (K), IEEE M Inverse (TD), IEEE V Inverse (TD), IEEE E Inverse (TD), US Inverse (TD) or US ST Inverse (TD)
Tripping characteristic for the second stage earth fault protection 1				
IN>2 Direction	38	17	Non-Directional	Non-directional, Directional Fwd or Directional Rev
Direction setting for the second stage earth fault protection 1				
IN>2 Current	38	18	0.2	24A to 1200A step 3A
Pick-up setting for the second stage earth fault element 1				
IN>2 IDG Is	38	19	1.5	1 to 4 step 0.1
Multiple of IN>2 setting for the IDG curve (Scandinavia), determines the actual relay current threshold at which the element starts				
IN>2 Time Delay	38	1A	1	0s to 200s step 0.01s
Operating time delay setting for the second stage definite time element				
IN>2 TMS	38	1B	1	0.025 to 1.2 step 0.025
Time multiplier setting to adjust the operating time of the IEC IDMT characteristic				
IN>2 Time Dial	38	1C	1	0.01 to 100 step 0.01
Time multiplier setting to adjust the operating time of the IEEE/US IDMT curves				
IN>2 K (RI)	38	1D	1	0.1 to 10 step 0.05
Time multiplier to adjust the operating time for the RI curve				
IN>2 IDG Time	38	1E	1.2	1s to 2s step 0.01s
Minimum operating time at high levels of fault current for the IDG curve				
IN>2 Reset Char	38	1F	DT	DT or Inverse
Type of reset/release characteristic of the IEEE/US curves				
IN>2 tRESET	38	20	0	0s to 100s step 0.01s
Reset/release time setting for definite time reset characteristic				
IN>3 Status	38	25	Disabled	Enabled or Disabled
Setting to enable or disable the third stage definite time element. If the function is disabled, all associated settings with the exception of this setting, are hidden				
IN>3 Direction	38	26	Non-Directional	Non-directional, Directional Fwd or Directional Rev
Direction setting for the third stage earth fault protection 1				
IN>3 Current	38	27	0.5	24A to 9600A step 3A
Pick-up setting for the third stage earth fault element 1				
IN>3 Time Delay	38	28	0	0s to 200s step 0.01s

Menu Text	Col	Row	Default Setting	Available Setting
Description				
Operating time delay setting for the third stage definite time element				
IN>4 Status	38	2C	Disabled	Enabled or Disabled
Setting to enable or disable the fourth stage definite time element. If the function is disabled, all associated settings with the exception of this setting, are hidden				
IN>4 Direction	38	2D	Non-Directional	Non-directional, Directional Fwd or Directional Rev
Direction setting for the fourth stage earth fault protection 1				
IN>4 Current	38	2E	0.5	24A to 9600A step 3A
Pick-up setting for the fourth stage earth fault element 1				
IN>4 Time Delay	38	2F	0	0s to 200s step 0.01s
Operating time delay setting for the fourth stage definite time element				
IN> Func Link	38	33	15	4-bit binary setting
Settings that determine whether VT supervision logic signals block selected earth fault stages. When set to 1, the VTS operation will block the stage if directionalized. When set to 0, the stage will revert to non-directional on the operation of the VTS				
IN> DIRECTIONAL	38	34	Sub-Heading	Sub-Heading
Sub-Heading for IN directional				
IN> Char Angle	38	35	-60	-95° to 95° step 1°
Setting for the relay characteristic angle used for the directional decision				
IN> Pol	38	36	Zero Sequence	Zero sequence or Neg sequence
Setting that determines whether the directional function uses zero sequence or negative sequence voltage polarizing				
IN> VNpol Set	38	37	5	0.5V to 80V step 0.5V
P643 and P645 only. Setting for the minimum zero sequence voltage polarizing quantity for directional decision				
IN> V2pol Set	38	38	5	0.5V to 80V step 0.5V
Setting for the minimum negative sequence voltage polarizing quantity for directional decision				
IN> I2pol Set	38	39	0.08	24A to 300A step 3A
Setting for the minimum negative sequence current polarizing quantity for directional decision				
Earth Fault 2	38	41	Enabled	Enabled or Disabled
Enable or Disable Earth Fault 2				
EF 2 Input	38	42	Measured	Measured or Derived
Selects measured neutral current or derived neutral current				
EF 2 Derived	38	43	P642: T2 P643: T3 P645: T5	HV Winding, LV Winding, TV Winding, T1, T2, T3, T4 or T5
The setting is avaliable when earth fault input is derived to select the derived neural current source				
EF 2 Measured	38	44	TN2	TN1, TN2 or TN3
The setting is avaliable when earth fault input is measured to select the measured neural curernt source				
IN>1 Status	38	45	Enabled	Enabled or Disabled
Setting to enable or disable the first stage definite time element. If the function is disabled, all associated settings with the exception of this setting, are hidden				
IN>1 Char	38	46	IEC S Inverse	DT (DT), IEC S Inverse (TMS), IEC V Inverse (TMS), IEC E Inverse (TMS), UK LT Inverse (TMS), Rectifier (TMS), RI (K), IEEE M Inverse (TD), IEEE V Inverse (TD), IEEE E Inverse (TD), US Inverse (TD) or US ST Inverse (TD)
Tripping characteristic for the first stage earth fault protection 2				
IN>1 Direction	38	47	Non-Directional	Non-directional, Directional Fwd or Directional Rev

Menu Text	Col	Row	Default Setting	Available Setting
Description				
Direction setting for the first stage earth fault protection 2				
IN>1 Current	38	48	0.2*In	24A to 1200A step 3A
Pick-up setting for the first stage earth fault element 2				
IN>1 IDG Is	38	49	1.5	1 to 4 step 0.1
Multiple of IN>1 setting for the IDG curve (Scandinavia), determines the actual relay current threshold at which the element starts				
IN>1 Time Delay	38	4A	1	0s to 200s step 0.01s
Operating time delay setting for the first stage definite time element				
IN>1 TMS	38	4B	1	0.025 to 1.2 step 0.025
Time multiplier setting to adjust the operating time of the IEC IDMT characteristic				
IN>1 Time Dial	38	4C	1	0.01 to 100 step 0.01
Time multiplier setting to adjust the operating time of the IEEE/US IDMT curves				
IN>1 K (RI)	38	4D	1	0.1 to 10 step 0.05
Time multiplier setting to adjust the operating time for the RI curve				
IN>1 IDG Time	38	4E	1.2	1s to 2s step 0.01s
Minimum operating time at high levels of fault current for the IDG curve				
IN>1 Reset Char	38	4F	DT	DT or Inverse
Type of reset/release characteristic of the IEEE/US curves				
IN>1 tRESET	38	50	0	0s to 100s step 0.01s
Reset/release time setting for definite time reset characteristic				
IN>2 Status	38	55	Disabled	Enabled or Disabled
Setting to enable or disable the second stage definite time element. If the function is disabled, all associated settings with the exception of this setting, are hidden				
IN>2 Char	38	56	DT	DT (DT), IEC S Inverse (TMS), IEC V Inverse (TMS), IEC E Inverse (TMS), UK LT Inverse (TMS), Rectifier (TMS), RI (K), IEEE M Inverse (TD), IEEE V Inverse (TD), IEEE E Inverse (TD), US Inverse (TD) or US ST Inverse (TD)
Tripping characteristic for the second stage earth fault protection 2				
IN>2 Direction	38	57	Non-Directional	Non-directional, Directional Fwd or Directional Rev
Direction setting for the second stage earth fault protection 2				
IN>2 Current	38	58	0.2	24A to 1200A step 3A
Pick-up setting for the second stage earth fault element 2				
IN>2 IDG Is	38	59	1.5	1 to 4 step 0.1
Multiple of IN>2 setting for the IDG curve (Scandinavia), determines the actual relay current threshold at which the element starts				
IN>2 Time Delay	38	5A	1	0s to 200s step 0.01s
Operating time delay setting for the second stage definite time element				
IN>2 TMS	38	5B	1	0.025 to 1.2 step 0.025
Time multiplier setting to adjust the operating time of the IEC IDMT characteristic				
IN>2 Time Dial	38	5C	1	0.01 to 100 step 0.01
Time multiplier setting to adjust the operating time of the IEEE/US IDMT curves				
IN>2 K (RI)	38	5D	1	0.1 to 10 step 0.05
Time multiplier to adjust the operating time for the RI curve				
IN>2 IDG Time	38	5E	1.2	1s to 2s step 0.01s
Minimum operating time at high levels of fault current for the IDG curve				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
IN>2 Reset Char	38	5F	DT	DT or Inverse
Type of reset/release characteristic of the IEEE/US curves				
IN>2 tRESET	38	60	0	0s to 100s step 0.01s
Reset/release time setting for definite time reset characteristic				
IN>3 Status	38	65	Disabled	Enabled or Disabled
Setting to enable or disable the third stage definite time element. If the function is disabled, all associated settings with the exception of this setting, are hidden				
IN>3 Direction	38	66	Non-Directional	Non-directional, Directional Fwd or Directional Rev
Direction setting for the third stage earth fault protection 2				
IN>3 Current	38	67	0.5	24A to 9600A step 3A
Pick-up setting for the third stage earth fault element 2				
IN>3 Time Delay	38	68	0	0s to 200s step 0.01s
Operating time delay setting for the third stage definite time element				
IN>4 Status	38	6C	Disabled	Enabled or Disabled
Setting to enable or disable the fourth stage definite time element. If the function is disabled, all associated settings with the exception of this setting, are hidden				
IN>4 Direction	38	6D	Non-Directional	Non-directional, Directional Fwd or Directional Rev
Direction setting for the fourth stage earth fault protection 2				
IN>4 Current	38	6E	0.5	24A to 9600A step 3A
Pick-up setting for the fourth stage earth fault element 2				
IN>4 Time Delay	38	6F	0	0s to 200s step 0.01s
Operating time delay setting for the fourth stage definite time element				
IN> Func Link	38	73	15	4-bit binary setting
Settings that determine whether VT supervision logic signals block selected earth fault stages. When set to 1, the VTS operation will block the stage if directionalized. When set to 0, the stage will revert to non-directional on the operation of the VTS				
IN> DIRECTIONAL	38	74	Sub-Heading	Sub-Heading
Sub-Heading for IN directional				
IN> Char Angle	38	75	-60	-95° to 95° step 1°
Setting for the relay characteristic angle used for the directional decision				
IN> Pol	38	76	Zero Sequence	Zero sequence or Neg sequence
Setting that determines whether the directional function uses zero sequence or negative sequence voltage polarizing				
IN> VNpol Set	38	77	5	0.5V to 80V step 0.5V
P643 and P645 only. Setting for the minimum zero sequence voltage polarizing quantity for directional decision				
IN> V2pol Set	38	78	5	0.5V to 25V step 0.5V
Setting for the minimum negative sequence voltage polarizing quantity for directional decision				
IN> I2pol Set	38	79	0.08	24A to 300A step 3A
Setting for the minimum negative sequence current polarizing quantity for directional Decision				
Earth Fault 3	38	81	Enabled	Enabled or Disabled
P643 and P645 only. Earth Fault 3				
EF 3 Input	38	82	Measured	Measured or Derived
P643 and P645 only. Selects measured neutral current or derived neutral current				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
EF 3 Derived	38	83	P643: T2 P645: T3	HV Winding, LV Winding, TV Winding, T1, T2, T3, T4 or T5
P643 and P645 only.				
EF 3 Measured	38	84	TN3	TN1, TN2 or TN3
P643 and P645 only.				
IN>1 Status	38	85	Enabled	Enabled or Disabled
P643 and P645 only. Setting to enable or disable the first stage definite time element. If the function is disabled, all associated settings with the exception of this setting, are hidden				
IN>1 Char	38	86	IEC S Inverse	DT (DT), IEC S Inverse (TMS), IEC V Inverse (TMS), IEC E Inverse (TMS), UK LT Inverse (TMS), Rectifier (TMS), RI (K), IEEE M Inverse (TD), IEEE V Inverse (TD), IEEE E Inverse (TD), US Inverse (TD) or US ST Inverse (TD)
P643 and P645 only. Tripping characteristic for the first stage earth fault protection				
IN>1 Direction	38	87	Non-Directional	Non-directional, Directional Fwd or Directional Rev
P643 and P645 only. Direction setting for the first stage earth fault protection 3				
IN>1 Current	38	88	0.2*In	24A to 1200A step 3A
P643 and P645 only. Pick-up setting for the first stage earth fault element 3				
IN>1 IDG Is	38	89	1.5	1 to 4 step 0.1
P643 and P645 only. Multiple of IN>1 setting for the IDG curve (Scandinavia), determines the actual relay current threshold at which the element starts				
IN>1 Time Delay	38	8A	1	0s to 200s step 0.01s
P643 and P645 only. Operating time delay setting for the first stage definite time element				
IN>1 TMS	38	8B	1	0.025 to 1.2 step 0.025
P643 and P645 only. Time multiplier setting to adjust the operating time of the IEC IDMT characteristic				
IN>1 Time Dial	38	8C	1	0.01 to 100 step 0.01
P643 and P645 only. Time multiplier setting to adjust the operating time of the IEEE/US IDMT curves				
IN>1 K (RI)	38	8D	1	0.1 to 10 step 0.05
P643 and P645 only. Time multiplier to adjust the operating time for the RI curve				
IN>1 IDG Time	38	8E	1.2	1s to 2s step 0.01s
P643 and P645 only. Minimum operating time at high levels of fault current for the IDG curve				
IN>1 Reset Char	38	8F	DT	DT or Inverse
P643 and P645 only. Type of reset/release characteristic of the IEEE/US curves				
IN>1 tRESET	38	90	0	0s to 100s step 0.01s
P643 and P645 only. Reset/release time setting for definite time reset characteristic				
IN>2 Status	38	95	Disabled	Enabled or Disabled

Menu Text	Col	Row	Default Setting	Available Setting
Description				
P643 and P645 only. Setting to enable or disable the second stage definite time element. If the function is disabled, all associated settings with the exception of this setting, are hidden				
IN>2 Char	38	96	DT	DT (DT), IEC S Inverse (TMS), IEC V Inverse (TMS), IEC E Inverse (TMS), UK LT Inverse (TMS), Rectifier (TMS), RI (K), IEEE M Inverse (TD), IEEE V Inverse (TD), IEEE E Inverse (TD), US Inverse (TD) or US ST Inverse (TD)
P643 and P645 only. Tripping characteristic for the second stage earth fault protection				
IN>2 Direction	38	97	Non-Directional	Non-directional, Directional Fwd or Directional Rev
P643 and P645 only. Direction setting for the second stage earth fault protection 2				
IN>2 Current	38	98	0.2	24A to 1200A step 3A
P643 and P645 only. Pick-up setting for the second stage earth fault element 2				
IN>2 IDG Is	38	99	1.5	1 to 4 step 0.1
P643 and P645 only. Multiple of IN>2 setting for the IDG curve (Scandinavia), determines the actual relay current threshold at which the element starts				
IN>2 Time Delay	38	9A	1	0s to 200s step 0.01s
P643 and P645 only. Operating time delay setting for the second stage definite time element				
IN>2 TMS	38	9B	1	0.025 to 1.2 step 0.025
P643 and P645 only. Time multiplier setting to adjust the operating time of the IEC IDMT characteristic				
IN>2 Time Dial	38	9C	1	0.01 to 100 step 0.01
P643 and P645 only. Time multiplier setting to adjust the operating time of the IEEE/US IDMT curves				
IN>2 K (RI)	38	9D	1	0.1 to 10 step 0.05
P643 and P645 only. Time multiplier to adjust the operating time for the RI curve				
IN>2 IDG Time	38	9E	1.2	1s to 2s step 0.01s
P643 and P645 only. Minimum operating time at high levels of fault current for the IDG curve				
IN>2 Reset Char	38	9F	DT	DT or Inverse
P643 and P645 only. Type of reset/release characteristic of the IEEE/US curves				
IN>2 tRESET	38	A0	0	0s to 100s step 0.01s
P643 and P645 only. Reset/release time setting for definite time reset characteristic				
IN>3 Status	38	A5	Disabled	Enabled or Disabled
P643 and P645 only. Setting to enable or disable the third stage definite time element. If the function is disabled, all associated settings with the exception of this setting, are hidden				
IN>3 Direction	38	A6	Non-Directional	Non-directional, Directional Fwd or Directional Rev
P643 and P645 only. Direction setting for the third stage earth fault protection 3				
IN>3 Current	38	A7	0.5	24A to 9600A step 3A
P643 and P645 only. Pick-up setting for the third stage earth fault element 3				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
IN>3 Time Delay	38	A8	0	0s to 200s step 0.01s
P643 and P645 only. Operating time delay setting for the third stage definite time element				
IN>4 Status	38	AC	Disabled	Enabled or Disabled
P643 and P645 only. Setting to enable or disable the fourth stage definite time element. If the function is disabled, all associated settings with the exception of this setting, are hidden				
IN>4 Direction	38	AD	Non-Directional	Non-directional, Directional Fwd or Directional Rev
P643 and P645 only. Direction setting for the fourth stage TV winding earth fault protection				
IN>4 Current	38	AE	0.5	24A to 9600A step 3A
P643 and P645 only. Pick-up setting for the fourth stage earth fault element on the TV winding				
IN>4 Time Delay	38	AF	0	0s to 200s step 0.01s
P643 and P645 only. Operating time delay setting for the fourth stage definite time element				
IN> Func Link	38	B3	15	4-bit binary setting
P643 and P645 only. Settings that determine whether VT supervision logic signals block selected earth fault stages. When set to 1, the VTS operation will block the stage if directionalized. When set to 0, the stage will revert to non-directional on the o				
IN> DIRECTIONAL	38	B4	Sub-Heading	Sub-Heading
P643 and P645 only.				
IN> Char Angle	38	B5	-60	-95° to 95° step 1°
P643 and P645 only. Setting for the relay characteristic angle used for the directional decision				
IN> Pol	38	B6	Zero Sequence	Zero sequence or Neg sequence
P643 and P645 only. Setting that determines whether the directional function uses zero sequence or negative sequence voltage polarizing				
IN> VNpol Set	38	B7	5	0.5V to 80V step 0.5V
P643 and P645 only. Setting for the minimum zero sequence voltage polarizing quantity for directional decision				
IN> V2pol Set	38	B8	5	0.5V to 25V step 0.5V
P643 and P645 only. Setting for the minimum negative sequence voltage polarizing quantity for directional decision				
IN> I2pol Set	38	B9	0.08	24A to 300A step 3A
P643 and P645 only. Setting for the minimum negative sequence current polarizing quantity for directional decision				

Table 8 - Group 1 earth fault settings

4.8 Through Fault (TF) Monitoring Protection

Menu Text	Col	Row	Default Setting	Available Setting
Description				
GROUP 1: TF MONITORING	39	00		
This column contains GROUP1: THROUGH FAULT parameters				
Through Fault	39	01	Enabled	Enabled or Disabled

Menu Text	Col	Row	Default Setting	Available Setting
Description				
Enables or disables monitoring of through faults				
Monitored Input	39	02	HV	HV, LV, TV or Biased Current
Selects the input winding to be monitored				
TF I> Trigger	39	03	3.85pu	0.08pu to 20pu step 0.01pu
A through fault event is recorded if any of the phase currents is larger than this setting				
TF I2t> Alarm	39	04	100 pu	0 to 1600pu step 0.1pu
An alarm is asserted if the maximum cumulative I2t in the three phases exceeds this setting				

Table 9 - Group 1 TF monitoring settings

4.9 Residual Overvoltage (Neutral Voltage Displacement)

The Neutral Voltage Displacement (NVD) element within the relay is of two-stage design, each stage having separate voltage and time delay settings. Stage 1 may be set to operate on either an IDMT or DT characteristic, whilst stage 2 may be set to DT only.

Menu Text	Col	Row	Default Setting	Available Setting
Description				
GROUP 1: RESIDUAL O/V NVD	3B	00		
P643 and P645 only. This column contains GROUP 1: RESIDUAL O/V NVD parameters				
VN>1 Function	3B	14	DT	Disabled, DT or IDMT
P643 and P645 only. Setting for the tripping characteristic of the first stage residual overvoltage element				
VN>1 Voltage Set	3B	16	5*V1	1*V1 to 80*V1 step 1*V1
P643 and P645 only. Pick-up setting for the first stage residual overvoltage characteristic				
VN>1 Time Delay	3B	18	5s	0 to 100s step 0.01s
P643 and P645 only. Operating time delay setting for the first stage definite time residual overvoltage element				
VN>1 TMS	3B	1A	1	0.5 to 100 step 0.5
P643 and P645 only. TMS to adjust the operating time of the IDMT characteristic. The characteristic is defined as follows: t = K / (M – 1) where: K = TMS t = Operating time in seconds M = Derived residual voltage/relay setting voltage (VN> Voltage Set)				
VN>1 tReset	3B	1C	0s	0 to 100s step 0.01s
P643 and P645 only. Setting to determine the reset or release definite time for the first stage characteristic				
VN>2 Status	3B	20	Disabled	Enabled or Disabled
P643 and P645 only. Setting to enable or disable the second stage definite time residual overvoltage element				
VN>2 Voltage Set	3B	26	10*V1	1*V1 to 80*V1 step 1*V1
P643 and P645 only. Pick-up setting for the second stage residual overvoltage element				
VN>2 Time Delay	3B	28	10s	0 to 100s step 0.01s
P643 and P645 only. Operating time delay for the second stage residual overvoltage element				

Table 10 - Group 1 residual overvoltage NVD settings

4.10 Overfluxing

The P64x relays have four-stage overfluxing elements. The P642 has one overfluxing element and the P643 and P645 may have up to two overfluxing elements.

The element measures the ratio of voltage, (VAB), to frequency i.e. (V/Hz) and operates when this ratio exceeds the setting. The higher the voltage-to-frequency ratio, the greater the magnetizing current that would lead to heating and possible isolation failure. One stage can be set to operate with a Definite Time (DT) or Inverse Definite Time Delay (IDMT), this stage can be used to provide the protection trip output. When the flux level drops below pickup, the reset timer starts. The different stages can be combined to create a multi-stage V/Hz trip characteristic using PSL.

Menu Text	Col	Row	Default Setting	Available Setting
Description				
GROUP 1: OVERFLUXING	3D	00		
This column contains GROUP 1: OVERFLUXING parameters				
Volts/Hz W1	3D	01	Sub-Heading	Sub-Heading
Volts/Hz Overfluxing element W1. P643 and P645 only if the optional three-phase VT is available.				
V/HZ Alm Status	3D	02	Enabled	Enabled or Disabled
P643 and P645 only. Enables or disables the V/Hz alarm element				
V/HZ Alm Set	3D	03	2.31 V/HZ	1.5V/Hz to 3.5V/Hz step 0.01V/Hz
P643 and P645 only. Pick-up setting for the V/Hz element				
V/Hz Alarm Delay	3D	04	10s	0s to 6000s step 0.1s
P643 and P645 only. Operating time delay setting of the V/Hz alarm element				
V/Hz>1 Status	3D	10	Enabled	Enabled or Disabled
P643 and P645 only. Enables or disables the V/Hz first stage trip element				
V/Hz>1 Function	3D	13	DT	DT or IDMT
P643 and P645 only. Tripping characteristic setting of the V/Hz first stage trip element				
V/Hz>1 Trip Set	3D	16	2.42 V/HZ	1.5V/Hz to 3.5V/Hz step 0.01V/Hz
P643 and P645 only. Pick-up setting for the V/Hz first stage trip element				
V/Hz>1 Trip TMS	3D	19	0.1	0.01 to 12 step 0.01
P643 and P645 only. Setting for the Time Multiplier Setting (TMS) to adjust the operating time of the IDMT characteristic				
V/Hz>1 Delay	3D	1A	60s	0s to 6000s step 0.1s
P643 and P645 only. Operating time-delay setting of the V/Hz first stage trip element				
V/Hz>1 tReset	3D	1B	60s	0s to 6000s step 0.1s
P643 and P645 only. Reset function so the user can reset overfluxing after injection testing				
V/Hz>2 Status	3D	20	Enabled	Enabled or Disabled
P643 and P645 only. Enables or disables the V/Hz second stage trip element				
V/Hz>2 Trip Set	3D	25	2.64 V/HZ	1.5V/Hz to 3.5V/Hz step 0.01V/Hz

Menu Text	Col	Row	Default Setting	Available Setting
Description				
P643 and P645 only. Pick-up setting for the V/Hz second stage trip element				
V/Hz>2 Delay	3D	2A	3s	0s to 6000s step 0.1s
P643 and P645 only. Operating time delay setting of the V/Hz alarm element				
V/Hz>3 Status	3D	30	Enabled	Enabled or Disabled
P643 and P645 only. Enables or disables the V/Hz third stage trip element				
V/Hz>3 Trip Set	3D	35	2.86 V/HZ	1.5V/Hz to 3.5V/Hz step 0.01V/Hz
P643 and P645 only. Pick-up setting for the V/Hz third stage trip element				
V/Hz>3 Delay	3D	3A	2.00s	0s to 6000s step 0.1s
P643 and P645 only. Operating time delay setting of the V/Hz alarm element				
V/Hz>4 Status	3D	40	Enabled	Enabled or Disabled
P643 and P645 only. Enables or disables the V/Hz fourth stage trip element				
V/Hz>4 Trip Set	3D	45	3.08 V/HZ	1.5V/Hz to 3.5V/Hz step 0.01V/Hz
P643 and P645 only. Pick-up setting for the V/Hz fourth stage trip element				
V/Hz>4 Delay	3D	4A	1.00s	0s to 6000s step 0.1s
P643 and P645 only. Operating time delay setting of the V/Hz alarm element				
TPre-trip Alarm	3D	4F	200s	0s to 6000s step 0.1s
P643 and P645 only. Pre-trip alarm time delay				
Volts/Hz W2	3D	50		
Volts/Hz Overfluxing element W2.				
V/HZ Alm Status	3D	51	Enabled	Enabled or Disabled
Enables or disables the V/Hz alarm element				
V/HZ Alm Set	3D	52	2.31 V/HZ	1.5V/Hz to 3.5V/Hz step 0.01V/Hz
Pick-up setting for the V/Hz element				
V/Hz Alarm Delay	3D	53	10s	0s to 6000s step 0.1s
Operating time delay setting of the V/Hz alarm element				
V/Hz>1 Status	3D	60	Enabled	Enabled or Disabled
Enables or disables the V/Hz first stage trip element				
V/Hz>1 Function	3D	63	DT	DT or IDMT
Tripping characteristic setting of the V/Hz first stage trip element				
V/Hz>1 Trip Set	3D	66	2.42 V/HZ	1.5V/Hz to 3.5V/Hz step 0.01V/Hz
Pick-up setting for the V/Hz first stage trip element				
V/Hz>1 Trip TMS	3D	69	0.1 s	0.01 to 12 step 0.01
Setting for the time multiplier setting to adjust the operating time of the IDMT characteristic.				
V/Hz>1 Delay	3D	6A	60s	0s to 6000s step 0.1s
Operating time delay setting of the V/Hz alarm element				
V/Hz>1 tReset	3D	6B	0s	0s to 6000s step 0.1s
Reset function so the user can reset overfluxing after injection testing				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
V/Hz>2 Status	3D	70	Enabled	Enabled or Disabled
Enables or disables the V/Hz second stage trip element				
V/Hz>2 Trip Set	3D	75	2.64 V/HZ	1.5V/Hz to 3.5V/Hz step 0.01V/Hz
Pick-up setting for the V/Hz second stage trip element				
V/Hz>2 Delay	3D	7A	3s	0s to 6000s step 0.1s
Operating time delay setting of the V/Hz alarm element				
V/Hz>3 Status	3D	80	Enabled	Enabled or Disabled
Enables or disables the V/Hz third stage trip element				
V/Hz>3 Trip Set	3D	85	2.86 V/HZ	1.5V/Hz to 3.5V/Hz step 0.01V/Hz
Pick-up setting for the V/Hz third stage trip element				
V/Hz>3 Delay	3D	8A	2.00s	0s to 6000s step 0.1s
Operating time delay setting of the V/Hz alarm element				
V/Hz>4 Status	3D	90	Enabled	Enabled or Disabled
Enables or disables the V/Hz fourth stage trip element				
V/Hz>4 Trip Set	3D	95	3.08 V/HZ	1.5V/Hz to 3.5V/Hz step 0.01V/Hz
Pick-up setting for the V/Hz fourth stage trip element				
V/Hz>4 Delay	3D	9A	1.00s	0s to 6000s step 0.1s
Operating time delay setting of the V/Hz alarm element				
TPre-trip alarm	3D	9F	200s	0s to 6000s step 0.1s
Pre-trip alarm time delay				

Table 11 - Group 1 overfluxing settings

4.11 Voltage Protection

One two-stage undervoltage and one two-stage overvoltage functions are available in the P643 and P645. These can be configured to measure either phase-to-phase or phase-to-neutral voltages. Stage 1 has inverse time-delayed characteristics and can be selected as IDMT, DT or Disabled. Stage 2 is DT only and is enabled or disabled in the **V<2 status** cell. The undervoltage stages can be blocked by a Poledead Inh setting.

One single stage negative phase sequence overvoltage function is available in the P642, P643 and P645.

Menu Text	Col	Row	Default Setting	Available Setting
Description				
GROUP 1: VOLT PROTECTION	42	00		
This column contains GROUP 1: VOLT PROTECTION parameters				
UNDER VOLTAGE	42	01	Sub-Heading	Sub-Heading
P643 and P645 only. UNDER VOLTAGE				
V< Measur't Mode	42	02	Phase-Neutral	Phase-Phase or Phase-Neutral
P643 and P645 only. Sets the measured input voltage used for the undervoltage elements				
V< Operate Mode	42	03	Any Phase	Any-Phase or Three-phase
P643 and P645 only. Determines whether any phase or all three phases must satisfy the undervoltage criteria before a decision is made				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
V<1 Function	42	04	DT	IDMT or DT or Disabled
P643 and P645 only. Tripping characteristic for the first stage undervoltage function. The characteristic is defined by: t = K / (1 - M) Where: K = TMS t = Operating time in seconds M = Measured voltage/relay setting voltage (V< Voltage Set)				
V<1 Voltage Set	42	05	50V	10V to 120V step 1V
P643 and P645 only. Sets the pick-up setting for the first stage undervoltage element				
V<1 Time Delay	42	06	10s	0s to 100s step 0.01s
P643 and P645 only. Sets the operating time-delay for the first stage definite time undervoltage element				
V<1 TMS	42	07	1	0.05 to 100 step 0.05
P643 and P645 only. Sets the time multiplier setting to adjust the operating time of the IEC IDMT characteristic				
V<1 Poledead Inh	42	08	Enabled	Enabled or Disabled
P643 and P645 only. If the setting is enabled, the relevant stage is inhibited by the pole dead logic. This logic produces an output when it detects either an open circuit breaker through auxiliary contacts feeding the relay opto inputs, or it detects a combination of both undercurrent and undervoltage on any one phase. It allows the undervoltage protection to reset when the circuit breaker opens to cater for line or bus side VT applications.				
V<2 Status	42	09	Disabled	Enabled or Disabled
P643 and P645 only. Enables or disables the second stage undervoltage element				
V<2 Voltage Set	42	0A	38V	10V to 120V step 1V
P643 and P645 only. Sets the pick-up setting for the second stage undervoltage element				
V<2 Time Delay	42	0B	5s	0s to 100s step 0.01s
P643 and P645 only. Sets the operating time-delay for the second stage definite time undervoltage element				
V<2 Poledead Inh	42	0C	Enabled	Enabled or Disabled
P643 and P645 only. This works in the same way as V<1 Poledead Inh but for V<2 Poledead Inh instead.				
OVERVOLTAGE	42	20	Sub-Heading	Sub-Heading
P643 and P645 only. OVERVOLTAGE				
V> Measur't Mode	42	21	Phase-Phase	Phase-Phase or Phase-Neutral
P643 and P645 only. Sets the measured input voltage used for the overvoltage elements				
V> Operate Mode	42	22	Any Phase	Any-Phase or Three-phase
P643 and P645 only. Determines whether any phase or all three phases must satisfy the overvoltage criteria before a decision is made				
V>1 Function	42	23	DT	IDMT or DT or Disabled

Menu Text	Col	Row	Default Setting	Available Setting
Description				
P643 and P645 only. Tripping characteristic for the first stage overvoltage function. The characteristic is defined by: t = K / (M - 1) Where: K = TMS t = Operating time in seconds M = Measured voltage/relay setting voltage (V<> Voltage Set)				
V>1 Voltage Set	42	24	130V	60V to 185V step 1V
P643 and P645 only. Sets the pick-up setting for the first stage overvoltage element				
V>1 Time Delay	42	25	10s	0s to 100s step 0.01s
P643 and P645 only. Sets the operating time-delay for the first stage definite time overvoltage element				
V>1 TMS	42	26	1	0.05 to 100 step 0.05
P643 and P645 only. Sets the time multiplier to adjust the operating time of the IEC IDMT characteristic				
V>2 Status	42	27	Disabled	Enabled or Disabled
P643 and P645 only. Enables or disables the second stage overvoltage element				
V>2 Voltage Set	42	28	150V	60V to 185V step 1V
P643 and P645 only. Sets the pick-up setting for the second stage overvoltage element				
V>2 Time Delay	42	29	0.5	0s to 100s step 0.01s
P643 and P645 only. Sets the operating time-delay for the second stage definite time overvoltage element				
NPS O/V	42	40	Sub-Heading	Sub-Heading
Negative phase sequence over voltage				
V2> Status	42	41	Disabled	Enabled or Disabled
Enable or disable the NPS OV				
V2> Voltage Set	42	42	15V	1V to 110V step 1V
Set up the pick up setting for Negative phase sequence over voltage				
V2> Time Delay	42	43	5s	0s to 100s step 0.01s
Set the operating time delay for the definite time stage				

Table 12 - Group 1 voltage protection settings

4.12 Frequency Protection

The relay includes four stages of underfrequency and two stages of overfrequency protection to facilitate load shedding and subsequent restoration. The underfrequency stages may be optionally blocked by a pole dead (CB Open) condition.

Menu Text	Col	Row	Default Setting	Available Setting
Description				
GROUP 1: FREQ PROTECTION	43	00		
This column contains GROUP 1: FREQ PROTECTION parameters				
UNDER FREQUENCY	43	01	Sub-Heading	Sub-Heading
UNDER FREQUENCY				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
F<1 Status	43	02	Enabled	Enabled or Disabled
Enables or disables the first stage underfrequency element				
F<1 Setting	43	03	49.5Hz	46Hz to 65Hz step 0.01Hz
Determines the pick-up threshold for the first stage underfrequency element				
F<1 Time Delay	43	04	4s	0s to 100s step 0.01s
Determines the minimum operating time-delay for the first stage underfrequency element				
F<2 Status	43	05	Disabled	Enabled or Disabled
Enables or disables the second stage underfrequency element				
F<2 Setting	43	06	49Hz	46Hz to 65Hz step 0.01Hz
Determines the pick-up threshold for the second stage underfrequency element				
F<2 Time Delay	43	07	3s	0s to 100s step 0.01s
Determines the minimum operating time-delay for the second stage underfrequency element				
F<3 Status	43	08	Disabled	Enabled or Disabled
Enables or disables the third stage underfrequency element				
F<3 Setting	43	09	48.5Hz	46Hz to 65Hz step 0.01Hz
Determines the pick-up threshold for the third stage underfrequency element				
F<3 Time Delay	43	0A	2s	0s to 100s step 0.01s
Determines the minimum operating time-delay for the third stage underfrequency element				
F<4 Status	43	0B	Disabled	Enabled or Disabled
Determines the pick-up threshold for the fourth stage underfrequency element				
F<4 Setting	43	0C	48Hz	46Hz to 65Hz step 0.01Hz
Enables or disables the fourth stage underfrequency element				
F<4 Time Delay	43	0D	1s	0s to 100s step 0.01s
Determines the minimum operating time-delay for the fourth stage underfrequency element				
OVER FREQUENCY	43	0F	Sub-Heading	Sub-Heading
OVER FREQUENCY				
F>1 Status	43	10	Enabled	Enabled or Disabled
Enables or disables the first stage overfrequency element				
F>1 Setting	43	11	50.5Hz	46Hz to 65Hz step 0.01Hz
Determines the pick-up threshold for the first stage overfrequency element				
F>1 Time Delay	43	12	2s	0s to 100s step 0.01s
Determines the minimum operating time-delay for the first stage overfrequency element				
F>2 Status	43	13	Disabled	Enabled or Disabled
Enables or disables the second stage overfrequency element				
F>2 Setting	43	14	51Hz	46Hz to 65Hz step 0.01Hz
Determines the pick-up threshold for the second stage overfrequency element				
F>2 Time Delay	43	15	1s	0s to 100s step 0.01s
Determines the minimum operating time-delay for the second stage overfrequency element				

Table 13 - Group 1 FREQ protection settings

4.13 Resistor Temperature Device (RTD) Protection

The relays can optionally provide temperature protection from 10 PT100 Resistor Temperature Devices (RTD). Each RTD has a definite time trip and alarm stage.

Menu Text	Col	Row	Default Setting	Available Setting
Description				
GROUP 1: RTD PROTECTION	44	00		
This column contains GROUP 1: RTD PROTECTION parameters				
Select RTD	44	01	0	10-bit binary setting: Bit 0 - Select RTD 1, Bit 1 - Select RTD 2, Bit 2 - Select RTD 3 through to Bit 9 - Select RTD 10
10-bit setting to enable or disable the 10 RTDs. For each bit 1 = Enabled, 0 = Disabled				
RTD1 PROTECTION	44	02	Sub-Heading	Sub-Heading
RTD1 PROTECTION				
RTD Alarm Set	44	03	80°C	0° to 200°C step 1°C
Temperature setting for the RTD 1 alarm element				
RTD Alarm Dly	44	04	10 s	0s to 100s step 1s
Operating time delay setting for the RTD 1 alarm element				
RTD Trip Set	44	05	85°C	0° to 200°C step 1°C
Operating time delay setting for the RTD 1 alarm element				
RTD Trip Dly	44	06	1 s	0s to 100s step 1s
Operating time delay setting for the RTD 1 alarm element				
RTD2 PROTECTION	44	07	Sub-Heading	Sub-Heading
RTD2 PROTECTION				
RTD Alarm Set	44	08	80°C	0° to 200°C step 1°C
This setting works in the same way as the RTD 1 alarm element, but for RTD 2 instead				
RTD Alarm Dly	44	09	10 s	0s to 100s step 1s
This setting works in the same way as the RTD 1 alarm element, but for RTD 2 instead				
RTD Trip Set	44	0A	85°C	0° to 200°C step 1°C
This setting works in the same way as the RTD 1 alarm element, but for RTD 2 instead				
RTD Trip Dly	44	0B	1 s	0s to 100s step 1s
This setting works in the same way as the RTD 1 alarm element, but for RTD 2 instead				
RTD3 PROTECTION	44	0C	Sub-Heading	Sub-Heading
RTD3 PROTECTION				
RTD Alarm Set	44	0D	80°C	0° to 200°C step 1°C
This setting works in the same way as the RTD 1 alarm element, but for RTD 2 instead				
RTD Alarm Dly	44	0E	10 s	0s to 100s step 1s
This setting works in the same way as the RTD 1 alarm element, but for RTD 2 instead				
RTD Trip Set	44	0F	85°C	0° to 200°C step 1°C
This setting works in the same way as the RTD 1 alarm element, but for RTD 2 instead				
RTD Trip Dly	44	10	1 s	0s to 100s step 1s
This setting works in the same way as the RTD 1 alarm element, but for RTD 2 instead				
RTD4 PROTECTION	44	11	Sub-Heading	Sub-Heading
RTD4 PROTECTION				
RTD Alarm Set	44	12	80°C	0° to 200°C step 1°C

Menu Text	Col	Row	Default Setting	Available Setting
Description				
This setting works in the same way as the RTD 1 alarm element, but for RTD 2 instead				
RTD Alarm Dly	44	13	10 s	0s to 100s step 1s
This setting works in the same way as the RTD 1 alarm element, but for RTD 2 instead				
RTD Trip Set	44	14	85°C	0° to 200°C step 1°C
This setting works in the same way as the RTD 1 alarm element, but for RTD 2 instead				
RTD Trip Dly	44	15	1 s	0s to 100s step 1s
This setting works in the same way as the RTD 1 alarm element, but for RTD 2 instead				
RTD5 PROTECTION	44	16	Sub-Heading	Sub-Heading
RTD5 PROTECTION				
RTD Alarm Set	44	17	80°C	0° to 200°C step 1°C
This setting works in the same way as the RTD 1 alarm element, but for RTD 2 instead				
RTD Alarm Dly	44	18	10 s	0s to 100s step 1s
This setting works in the same way as the RTD 1 alarm element, but for RTD 2 instead				
RTD Trip Set	44	19	85°C	0° to 200°C step 1°C
This setting works in the same way as the RTD 1 alarm element, but for RTD 2 instead				
RTD Trip Dly	44	1A	1 s	0s to 100s step 1s
This setting works in the same way as the RTD 1 alarm element, but for RTD 2 instead				
RTD6 PROTECTION	44	1B	Sub-Heading	Sub-Heading
RTD6 PROTECTION				
RTD Alarm Set	44	1C	80°C	0° to 200°C step 1°C
This setting works in the same way as the RTD 1 alarm element, but for RTD 2 instead				
RTD Alarm Dly	44	1D	10 s	0s to 100s step 1s
This setting works in the same way as the RTD 1 alarm element, but for RTD 2 instead				
RTD Trip Set	44	1E	85°C	0° to 200°C step 1°C
This setting works in the same way as the RTD 1 alarm element, but for RTD 2 instead				
RTD Trip Dly	44	1F	1 s	0s to 100s step 1s
This setting works in the same way as the RTD 1 alarm element, but for RTD 2 instead				
RTD7 PROTECTION	44	20	Sub-Heading	Sub-Heading
RTD7 PROTECTION				
RTD Alarm Set	44	21	80°C	0° to 200°C step 1°C
This setting works in the same way as the RTD 1 alarm element, but for RTD 2 instead				
RTD Alarm Dly	44	22	10 s	0s to 100s step 1s
This setting works in the same way as the RTD 1 alarm element, but for RTD 2 instead				
RTD Trip Set	44	23	85°C	0° to 200°C step 1°C
This setting works in the same way as the RTD 1 alarm element, but for RTD 2 instead				
RTD Trip Dly	44	24	1 s	0s to 100s step 1s
This setting works in the same way as the RTD 1 alarm element, but for RTD 2 instead				
RTD8 PROTECTION	44	25	Sub-Heading	Sub-Heading
RTD8 PROTECTION				
RTD Alarm Set	44	26	80°C	0° to 200°C step 1°C
This setting works in the same way as the RTD 1 alarm element, but for RTD 2 instead				
RTD Alarm Dly	44	27	10 s	0s to 100s step 1s
This setting works in the same way as the RTD 1 alarm element, but for RTD 2 instead				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
RTD Trip Set	44	28	85°C	0° to 200°C step 1°C
This setting works in the same way as the RTD 1 alarm element, but for RTD 2 instead				
RTD Trip Dly	44	29	1 s	0s to 100s step 1s
This setting works in the same way as the RTD 1 alarm element, but for RTD 2 instead				
RTD9 PROTECTION	44	2A	Sub-Heading	Sub-Heading
RTD9 PROTECTION				
RTD Alarm Set	44	2B	80°C	0° to 200°C step 1°C
This setting works in the same way as the RTD 1 alarm element, but for RTD 2 instead				
RTD Alarm Dly	44	2C	10 s	0s to 100s step 1s
This setting works in the same way as the RTD 1 alarm element, but for RTD 2 instead				
RTD Trip Set	44	2D	85°C	0° to 200°C step 1°C
This setting works in the same way as the RTD 1 alarm element, but for RTD 2 instead				
RTD Trip Dly	44	2E	1 s	0s to 100s step 1s
This setting works in the same way as the RTD 1 alarm element, but for RTD 2 instead				
RTD 10 PROTECTION	44	2F	Sub-Heading	Sub-Heading
RTD 10 PROTECTION				
RTD Alarm Set	44	30	80°C	0° to 200°C step 1°C
This setting works in the same way as the RTD 1 alarm element, but for RTD 2 instead				
RTD Alarm Dly	44	31	10 s	0s to 100s step 1s
This setting works in the same way as the RTD 1 alarm element, but for RTD 2 instead				
RTD Trip Set	44	32	85°C	0° to 200°C step 1°C
This setting works in the same way as the RTD 1 alarm element, but for RTD 2 instead				
RTD Trip Dly	44	33	1 s	0s to 100s step 1s
This setting works in the same way as the RTD 1 alarm element, but for RTD 2 instead				

Table 14 - Group 1 RTD protection settings

4.14 Circuit Breaker (CB) Failure

Current-based protection: the reset condition depends on undercurrent to determine whether the CB has opened.

Non current-based protection: the reset criteria can be selected from a setting to determine a CB Failure.

Menu Text	Col	Row	Default Setting	Available Setting
Description				
GROUP 1: CB FAIL	45	00		
GROUP 1: CB FAIL				
T1 CBF	45	01	Disabled	Enabled or Disabled
BREAKER FAIL for CT1				
I< Current Set	45	02	0.1	5% to 400% step 1%
Set the CT1 under current setting				
IN< Status	45	03	Disabled	Enabled or Disabled
Enable or Disabel the IN<				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
IN< Input	45	04	Measured	Measured or Derived
Set the IN input, derived or measured				
IN< Terminal	45	05	TN1	TN1, TN2 or TN3
If for IN is measured, set the measured netrual current source				
IN< Current Set	45	06	0.1	5% to 400% step 1%
Set IN under current setting				
CB Fail 1 Status	45	07	Disabled	Enabled or Disabled
Enables or disables the first stage of the circuit breaker function				
CB Fail 1 Timer	45	08	0.05s	0s to 10s step 0.001s
Circuit breaker fail timer setting for stage 1, for which the initiating condition must be valid				
CB Fail 2 Status	45	09	Enabled	Enabled or Disabled
Enables or disables the second stage of the circuit breaker function				
CB Fail 2 Timer	45	0A	0.2s	0s to 10s step 0.001s
Circuit breaker fail timer setting for stage 2, for which the initiating condition must be valid				
CBF Non I Reset	45	0C	CB Open & I<	I< Only, CB Open & I< or Prot Reset & I
Setting which determines the elements that reset the circuit breaker fail time for non current-based protection functions (such as voltage and frequency) initiating circuit breaker fail conditions				
CBF Ext Reset	45	0D	CB Open & I<	I< Only, CB Open & I< or Prot Reset & I
Setting which determines the elements that reset the circuit breaker fail time for external protection functions initiating circuit breaker fail conditions				
T2 CBF	45	11	Disabled	Enabled or Disabled
I< Current Set	45	12	0.1	5% to 400% step 1%
IN< Status	45	13	Disabled	Enabled or Disabled
IN< Input	45	14	Measured	Measured or Derived
IN< Terminal	45	15	TN1	TN1, TN2 or TN3
IN< Current Set	45	16	0.1	5% to 400% step 1%
CB Fail 1 Status	45	17	Disabled	Enabled or Disabled
CB Fail 1 Timer	45	18	0.05s	0s to 10s step 0.001s
CB Fail 2 Status	45	19	Enabled	Enabled or Disabled
CB Fail 2 Timer	45	1A	0.2s	0s to 10s step 0.001s
CBF Non I Reset	45	1C	CB Open & I<	I< Only, CB Open & I< or Prot Reset & I
CBF Ext Reset	45	1D	CB Open & I<	I< Only, CB Open & I< or Prot Reset & I

Menu Text	Col	Row	Default Setting	Available Setting
Description				
T3 CBF	45	21	Disabled	Enabled or Disabled
P643 and P645 only.				
I< Current Set	45	22	0.1	5% to 400% step 1%
P643 and P645 only.				
IN< Status	45	23	Disabled	Enabled or Disabled
P643 and P645 only.				
IN< Input	45	24	Measured	Measured or Derived
P643 and P645 only.				
IN< Terminal	45	25	TN1	TN1, TN2 or TN3
P643 and P645 only.				
IN< Current Set	45	26	0.1	5% to 400% step 1%
P643 and P645 only.				
CB Fail 1 Status	45	27	Disabled	Enabled or Disabled
P643 and P645 only.				
CB Fail 1 Timer	45	28	0.05s	0s to 10s step 0.001s
P643 and P645 only.				
CB Fail 2 Status	45	29	Enabled	Enabled or Disabled
P643 and P645 only.				
CB Fail 2 Timer	45	2A	0.2s	0s to 10s step 0.001s
P643 and P645 only.				
CBF Non I Reset	45	2C	CB Open & I<	I< Only, CB Open & I< or Prot Reset & I
P643 and P645 only.				
CBF Ext Reset	45	2D	CB Open & I<	I< Only, CB Open & I< or Prot Reset & I
P643 and P645 only.				
T4 CBF	45	31	Disabled	Enabled or Disabled
P645 only.				
I< Current Set	45	32	0.1	5% to 400% step 1%
P645 only.				
IN< Status	45	33	Disabled	Enabled or Disabled
P645 only.				
IN< Input	45	34	Measured	Measured or Derived
P645 only.				
IN< Terminal	45	35	TN1	TN1, TN2 or TN3
P645 only.				
IN< Current Set	45	36	0.1	5% to 400% step 1%
P645 only.				
CB Fail 1 Status	45	37	Disabled	Enabled or Disabled
P645 only.				
CB Fail 1 Timer	45	38	0.05s	0s to 10s step 0.001s
P645 only.				
CB Fail 2 Status	45	39	Enabled	Enabled or Disabled
P645 only.				
CB Fail 2 Timer	45	3A	0.2s	0s to 10s step 0.001s

Menu Text	Col	Row	Default Setting	Available Setting
Description				
P645 only.				
CBF Non I Reset	45	3C	CB Open & I<	I< Only, CB Open & I< or Prot Reset & I
P645 only.				
CBF Ext Reset	45	3D	CB Open & I<	I< Only, CB Open & I< or Prot Reset & I
P645 only.				
T5 CBF	45	41	Disabled	Enabled or Disabled
P645 only.				
I< Current Set	45	42	0.1	5% to 400% step 1%
P645 only.				
IN< Status	45	43	Disabled	Enabled or Disabled
P645 only.				
IN< Input	45	44	Measured	Measured or Derived
P645 only.				
IN< Terminal	45	45	TN1	TN1, TN2 or TN3
P645 only.				
IN< Current Set	45	46	0.1	5% to 400% step 1%
P645 only.				
CB Fail 1 Status	45	47	Disabled	Enabled or Disabled
P645 only.				
CB Fail 1 Timer	45	48	0.05s	0s to 10s step 0.001s
P645 only.				
CB Fail 2 Status	45	49	Enabled	Enabled or Disabled
P645 only.				
CB Fail 2 Timer	45	4A	0.2s	0s to 10s step 0.001s
P645 only.				
CBF Non I Reset	45	4C	CB Open & I<	I< Only, CB Open & I< or Prot Reset & I
P645 only.				
CBF Ext Reset	45	4D	CB Open & I<	I< Only, CB Open & I< or Prot Reset & I
P645 only.				

Table 15 - Group 1 CB fail settings

4.15 VT and CT Supervision

The VTS feature in the relay operates when it detects a Negative Phase Sequence (NPS) voltage when there is no NPS current. This gives operation for the loss of one or two-phase voltages. Stability of the VTS function is assured during system fault conditions by the presence of the NPS current. The use of negative sequence quantities ensures correct operation even where 3-limb or V-connected VTs are used.

If all 3-phase voltages to the relay are lost, there are no NPS quantities to operate the VTS function, and the 3-phase voltages collapse. If this is detected without a corresponding change in any of the phase current signals (which would indicate a fault), a VTS condition is raised. In practice, the relay detects superimposed current signals, which are changes in the current applied to the relay.

If a VT is inadvertently left isolated before line energization, voltage-dependent elements may operate incorrectly. The previous VTS element detected 3-phase VT failure due to the absence of all 3-phase voltages with no corresponding change in current. However, on-line energization there is a change in current, for example, due to load or line charging current. An alternative method of detecting 3-phase VT failure is therefore required on line energization.

The absence of measured voltage on all three phases on line energization can be as a result of two conditions. The first is a 3-phase VT failure and the second is a close-up 3-phase fault. The first condition would require blocking of the voltage dependent function and the second would require tripping. To differentiate between these two conditions an overcurrent level detector (VTS I> Inhibit) is used to prevent a VTS block from being issued if it operates. This element should be set in excess of any non-fault based currents on line energization (load, line charging current, transformer inrush current if applicable) but below the level of current produced by a close-up 3-phase fault. If the line is closed where a 3-phase VT failure is present, the overcurrent detector does not operate and a VTS block is applied. Closing onto a 3-phase fault results in operation of the overcurrent detector and prevents a VTS block from being applied.

This logic is only enabled during a live line condition to prevent operation under dead system conditions. A live line condition is indicated by the relay's pole dead logic. Dead system conditions are where no voltage is present and the VTS I> Inhibit overcurrent element is not picked up.

Differential CTS is based on measurement of the ratio of I2 and I1 at all ends. When this ratio is not zero, either the system has an unbalanced fault or there is a 1 or 2 phase CT problem. In both cases, both I2 and I1 are non-zero.

If the ratio of I2 and I1 is detected at all ends, it is almost certainly a genuine fault condition and CTS is prevented from operating. If this ratio is detected at only one end, it could be either a CT problem or a single end-fed fault condition. I1 is therefore detected to determine whether it is a CT problem or not.

If I1 is detected at all ends, it must be CT problem and CTS is allowed to operate. If I1 is detected at only one end, it is either an inrush condition or a single end-fed internal fault, therefore the CTS operation is blocked.

Menu Text	Col	Row	Default Setting	Available Setting
Description				
GROUP 1: SUPERVISION	46	00		
This column contains GROUP 1: SUPERVISION parameters				
VT SUPERVISION	46	01	Sub-Heading	Sub-Heading
VT Supervision does not apply to P642 when the optional three-phase VT input is available. Only visible if Main VT is fitted or P642 model with 2 VT inputs.				
VTS Status	46	02	Indication	Blocking or Indication or Disabled

Menu Text	Col	Row	Default Setting	Available Setting
Description				
Determines whether on detection of VTS. • VTS logic is Disabled. • VTS alarm is Indication only. • Voltage-dependent protection elements are Blocked. Optional conversion of directional overcurrent to non-directional protection (blocking mode only).				
VTS Reset Mode	46	03	Manual	Manual or Auto
VTS block is latched after user-settable VTS Time Delay. Once latched, the reset methods are: Manual using the front panel interface (or remote communications). Auto provided VTS condition has been removed and 3-phase voltages have been restored above ph				
VTS Time Delay	46	04	5s	1s to 10s step 0.1s
Operating time delay setting of the VTS element on detection of a voltage supervision condition.				
VTS I> Inhibit	46	05	10	0.08pu to 32pu step 0.01pu
The overcurrent setting inhibits VT supervision if all 3-phase voltages are lost, due to a close-up 3-phase fault after CB is closed. In P643, CT1/CT2/CT3 if the VT is in the HV, TV or LV. In P645, CT1/CT3/CT5 if the VT is in HV, TV or LV.				
VTS I2> Inhibit	46	06	0.05	0.05pu to 0.5pu step 0.01pu
NPS overcurrent setting inhibits VT supervision if a fault occurs with excess negative sequence current. In P643, always referred to CT1/CT2/CT3 if the VT is in the HV, TV or LV. In P645, always referred to CT1/CT3/CT5 if the VT is in HV, TV or LV.				
CT SUPERVISION	46	20	Sub-Heading	Sub-Heading
CT Supervision applies to P642, P643, P645 and P746 when the optional CT input is available.				
Diff CTS	46	21	Enable	Enabled or Disabled
Enables or disables the CTS function				
CTS Status	46	22	Restrain	Indication or Restrain
In Indication mode, the CTS alarm is issued without delay when a CT failure is detected. In restrain mode, the differential protection is desensitised to the Is-CTS setting				
CTS Tdelay	46	23	2s	0s to 10s step 0.1s
Determines the operating time delay of the element on detection of a current transformer supervision condition				
CTS I1	46	24	0.1	5% to 100% step 1%
Set release threshold				
CTS I2/I1>1	46	25	0.05	5% to 100% step 1%
Low set ratio of negative to positive sequence current				
CTS I2/I1>2	46	26	0.4	5% to 100% step 1%
High set ratio of negative to positive sequence current				

Table 16 - Group 1 supervision settings

4.16 Input Labels

The column **GROUP x INPUT LABELS** is used to individually label each opto input that is available in the relay. The text is restricted to 16 characters and is available if 'Input Labels' are set visible under CONFIGURATION column.

Menu Text	Col	Row	Default Setting	Available Setting
Description				
GROUP 1: INPUT LABELS	4A	00		
This column contains GROUP 1: INPUT LABELS parameters				
Opto Input 1	4A	01	Input L1	16-character text string (32 to 163)
Text label to describe each individual opto input				
Opto Input 2	4A	02	Input L2	16-character text string (32 to 163)
Text label to describe each individual opto input				
Opto Input 3	4A	03	Input L3	16-character text string (32 to 163)
Text label to describe each individual opto input				
Opto Input 4	4A	04	Input L4	16-character text string (32 to 163)
Text label to describe each individual opto input				
Opto Input 5	4A	05	Input L5	16-character text string (32 to 163)
Text label to describe each individual opto input				
Opto Input 6	4A	06	Input L6	16-character text string (32 to 163)
Text label to describe each individual opto input				
Opto Input 7	4A	07	Input L7	16-character text string (32 to 163)
Text label to describe each individual opto input				
Opto Input 8	4A	08	Input L8	16-character text string (32 to 163)
Text label to describe each individual opto input				
Opto Input 9	4A	09	Input L9	16-character text string (32 to 163)
Text label to describe each individual opto input				
Opto Input 10	4A	0A	Input L10	16-character text string (32 to 163)
Text label to describe each individual opto input				
Opto Input 11	4A	0B	Input L11	16-character text string (32 to 163)
Text label to describe each individual opto input				
Opto Input 12	4A	0C	Input L12	16-character text string (32 to 163)
Text label to describe each individual opto input				
Opto Input 13	4A	0D	Input L13	16-character text string (32 to 163)
Text label to describe each individual opto input				
Opto Input 14	4A	0E	Input L14	16-character text string (32 to 163)
Text label to describe each individual opto input				
Opto Input 15	4A	0F	Input L15	16-character text string (32 to 163)
Text label to describe each individual opto input				
Opto Input 16	4A	10	Input L16	16-character text string (32 to 163)
Text label to describe each individual opto input				
Opto Input 17	4A	11	Input L17	16-character text string (32 to 163)
Text label to describe each individual opto input				
Opto Input 18	4A	12	Input L18	16-character text string (32 to 163)

Menu Text	Col	Row	Default Setting	Available Setting
Description				
Text label to describe each individual opto input				
Opto Input 19	4A	13	Input L19	16-character text string (32 to 163)
Text label to describe each individual opto input				
Opto Input 20	4A	14	Input L20	16-character text string (32 to 163)
Text label to describe each individual opto input				
Opto Input 21	4A	15	Input L21	16-character text string (32 to 163)
Text label to describe each individual opto input				
Opto Input 22	4A	16	Input L22	16-character text string (32 to 163)
Text label to describe each individual opto input				
Opto Input 23	4A	17	Input L23	16-character text string (32 to 163)
Text label to describe each individual opto input				
Opto Input 24	4A	18	Input L24	16-character text string (32 to 163)
Text label to describe each individual opto input				
Opto Input 25	4A	19	Input L25	16-character text string (32 to 163)
Text label to describe each individual opto input				
Opto Input 26	4A	1A	Input L26	16-character text string (32 to 163)
Text label to describe each individual opto input				
Opto Input 27	4A	1B	Input L27	16-character text string (32 to 163)
Text label to describe each individual opto input				
Opto Input 28	4A	1C	Input L28	16-character text string (32 to 163)
Text label to describe each individual opto input				
Opto Input 29	4A	1D	Input L29	16-character text string (32 to 163)
Text label to describe each individual opto input				
Opto Input 30	4A	1E	Input L30	16-character text string (32 to 163)
Text label to describe each individual opto input				
Opto Input 31	4A	1F	Input L31	16-character text string (32 to 163)
Text label to describe each individual opto input				
Opto Input 32	4A	20	Input L32	16-character text string (32 to 163)
Text label to describe each individual opto input				

Table 17 - Input label settings

4.17 Output Labels

The column **GROUP x OUTPUT LABELS** is used to individually label each output relay that is available in the relay. The text is restricted to 16 characters and is available if 'Output Labels' are set visible under CONFIGURATION column.

Menu Text	Col	Row	Default Setting	Available Setting
Description				
GROUP 1: OUTPUT LABELS	4B	00		
This column contains GROUP 1: OUTPUT LABELS parameters				
Relay 1	4B	01	Output R1 Not Used	16-character text string (32 to 163)

Menu Text	Col	Row	Default Setting	Available Setting
Description				
P642, P643, P645 and P746. Text label to describe each individual relay output contact. This text is displayed in the programmable scheme logic and event record description of the relay output contact				
Relay 2	4B	02	Output R2 Not Used	16-character text string (32 to 163)
This works in the same way as Relay 1.				
Relay 3	4B	03	Output R3 Not Used	16-character text string (32 to 163)
This works in the same way as Relay 1.				
Relay 4	4B	04	Output R4 Not Used	16-character text string (32 to 163)
This works in the same way as Relay 1.				
Relay 5	4B	05	Output R5 Not Used	16-character text string (32 to 163)
This works in the same way as Relay 1.				
Relay 6	4B	06	Output R6 Not Used	16-character text string (32 to 163)
This works in the same way as Relay 1.				
Relay 7	4B	07	Output R7 Not Used	16-character text string (32 to 163)
This works in the same way as Relay 1.				
Relay 8	4B	08	Output R8 Not Used	16-character text string (32 to 163)
This works in the same way as Relay 1.				
Relay 9	4B	09	Output R9 Not Used	16-character text string (32 to 163)
This works in the same way as Relay 1.				
Relay 10	4B	0A	Output R10 Not Used	16-character text string (32 to 163)
This works in the same way as Relay 1.				
Relay 11	4B	0B	Output R11 Not Used	16-character text string (32 to 163)
This works in the same way as Relay 1.				
Relay 12	4B	0C	Output R12 Not Used	16-character text string (32 to 163)
This works in the same way as Relay 1.				
Relay 13	4B	0D	Output R13 Not Used	16-character text string (32 to 163)
P643, P645 and P746 only. Text label to describe each individual relay output contact. This text is displayed in the programmable scheme logic and event record description of the relay output contact				
Relay 14	4B	0E	Output R14 Not Used	16-character text string (32 to 163)
P643, P645 and P746 only. This works in the same way as Relay 12.				
Relay 15	4B	0F	Output R15 Not Used	16-character text string (32 to 163)
P643, P645 and P746 only. This works in the same way as Relay 12.				
Relay 16	4B	10	Output R16 Not Used	16-character text string (32 to 163)
P643, P645 and P746 only. This works in the same way as Relay 12.				
Relay 17	4B	11	Output R17 Not Used	16-character text string (32 to 163)
P643, P645 and P746 only. This works in the same way as Relay 12.				
Relay 18	4B	12	Output R18 Not Used	16-character text string (32 to 163)
P643, P645 and P746 only. This works in the same way as Relay 12.				
Relay 19	4B	13	Output R19 Not Used	16-character text string (32 to 163)

Menu Text	Col	Row	Default Setting	Available Setting
Description				
P643, P645 and P746 only. This works in the same way as Relay 12.				
Relay 20	4B	14	Output R20 Not Used	16-character text string (32 to 163)
P643, P645 and P746 only. This works in the same way as Relay 12.				
Relay 21	4B	15	Output R21 Not Used	16-character text string (32 to 163)
P643, P645 and P746 only. This works in the same way as Relay 12.				
Relay 22	4B	16	Output R22 Not Used	16-character text string (32 to 163)
P643, P645 and P746 only. This works in the same way as Relay 12.				
Relay 23	4B	17	Output R23 Not Used	16-character text string (32 to 163)
P643, P645 and P746 only. This works in the same way as Relay 12.				
Relay 24	4B	18	Output R24 Not Used	16-character text string (32 to 163)
P643, P645 and P746 only. This works in the same way as Relay 12.				
Relay 25	4B	19	Output R25 Not Used	16-character text string (32 to 163)
P645 and P746 only. Text label to describe each individual relay output contact. This text is displayed in the programmable scheme logic and event record description of the relay output contact				
Relay 26	4B	1A	Output R26 Not Used	16-character text string (32 to 163)
P645 and P746 only. This works in the same way as Relay 19.				
Relay 27	4B	1B	Output R27 Not Used	16-character text string (32 to 163)
P645 and P746 only. This works in the same way as Relay 19.				
Relay 28	4B	1C	Output R28 Not Used	16-character text string (32 to 163)
P645 and P746 only. This works in the same way as Relay 19.				
Relay 29	4B	1D	Output R29 Not Used	16-character text string (32 to 163)
P645 and P746 only. This works in the same way as Relay 19.				
Relay 30	4B	1E	Output R30 Not Used	16-character text string (32 to 163)
P645 and P746 only. This works in the same way as Relay 19.				
Relay 31	4B	1F	Output R31 Not Used	16-character text string (32 to 163)
P645 and P746 only. This works in the same way as Relay 19.				
Relay 32	4B	20	Output R32 Not Used	16-character text string (32 to 163)
P645 and P746 only. This works in the same way as Relay 19.				

Table 18 - Output label settings

4.18 RTD Labels

Menu Text	Col	Row	Default Setting	Available Setting
Description				
GROUP 1: RTD LABELS	4C	00		
This column contains GROUP 1: RTD LABELS parameters				
RTD 1	4C	01	RTD 1	16-character text string (32 to 163)
Text label to describe each individual RTD. This text is displayed in the Measurements 3 menu and fault records for the description of the RTDs.				
RTD 2	4C	02	RTD 2	16-character text string (32 to 163)
This works in the same way as RTD 1.				
RTD 3	4C	03	RTD 3	16-character text string (32 to 163)
This works in the same way as RTD 1.				
RTD 4	4C	04	RTD 4	16-character text string (32 to 163)
This works in the same way as RTD 1.				
RTD 5	4C	05	RTD 5	16-character text string (32 to 163)
This works in the same way as RTD 1.				
RTD 6	4C	06	RTD 6	16-character text string (32 to 163)
This works in the same way as RTD 1.				
RTD 7	4C	07	RTD 7	16-character text string (32 to 163)
This works in the same way as RTD 1.				
RTD 8	4C	08	RTD 8	16-character text string (32 to 163)
This works in the same way as RTD 1.				
RTD 9	4C	09	RTD 9	16-character text string (32 to 163)
This works in the same way as RTD 1.				
RTD 10	4C	0A	RTD 10	16-character text string (32 to 163)
This works in the same way as RTD 1.				

Table 19 - RTD label settings

4.19 Current Loop Inputs and Outputs (CLIO) Protection

Four analog or current loop inputs are optionally provided for transducers with ranges of 0 to 1 mA, 0 to 10 mA, 0 to 20 mA or 4 to 20 mA. The analog inputs can be used for various transducers such as vibration monitors, tachometers, pressure and temperature transducers. Associated with each input there are two protection stages, one for alarm and one for trip. Each stage can be individually enabled or disabled, and each stage has a Definite Time delay setting. The Alarm and Trip stages can be set for operation when the input value falls below the Alarm/Trip threshold **Under** or when the input current is above the input value **Over**. The 4 to 20 mA input has an undercurrent alarm element which can be used to indicate a fault with the transducer or wiring.

There are four analog current outputs with ranges of 0 to 1 mA, 0 to 10 mA, 0 to 20 mA or 4 to 20 mA, which can reduce the need for separate transducers. These outputs can be fed to standard moving coil ammeters for analog measurements or to a SCADA system using an existing analog RTU.

Menu Text	Col	Row	Default Setting	Available Setting
Description				
GROUP 1: CLIO PROTECTION	4D	00		
This column contains GROUP 1: CLIO PROTECTION parameters				
CLI1 PROTECTION	4D	01	Sub-Heading	Sub-Heading
CLI1 PROTECTION				
CLI Input Status	4D	02	Enabled	Enabled or Disabled
Enables or disables the current loop (transducer) input 1 element				
CLI Input Type	4D	04	4-20mA	0 to 1mA, 0 to 10mA, 0 to 20mA or 4 to 20mA
Current loop 1 input type				
CLI Input Label	4D	06	CLIO Input 1	16-character text string (32 to 163)
Current loop 1 input description. The minimum and maximum settings define the range but they have no units. The user can use the label to enter the transducer function and unit of measurement				
CLI Minimum	4D	08	0	-9999 to 9999 step 0.1
Current loop input 1 minimum setting. Defines the lower range of the physical or electrical quantity measured by the transducer				
CLI Maximum	4D	0A	100	-9999 to 9999 step 0.1
Current loop input 1 maximum setting. Defines the upper range of the physical or electrical quantity measured by the transducer				
CLI Alarm	4D	0C	Disabled	Enabled or Disabled
Enables or disables the current loop input 1 alarm element				
CLI Alarm Fn	4D	0E	Over	Over or Under
Operating mode of the current loop input 1 alarm element				
CLI Alarm Set	4D	10	50	From "MIN(CLI1Min, Max)" to "MAX(CLI1Min, Max))" step 0.1
Pick-up setting for the current loop input 1 alarm element				
CLI Alarm Delay	4D	12	1	0s to 100s step 0.1s
Operating time-delay setting of current loop input 1 alarm element				
CLI Trip	4D	14	Disabled	Enabled or Disabled
Pick-up setting for the current loop input 1 trip element				
CLI Trip Fn	4D	16	Over	Over or Under
Operating mode of the current loop input 1 alarm element				
CLI Trip Set	4D	18	60	From "MIN(CLI1Min, Max)" to "MAX(CLI1Min, Max))" step 0.1

Menu Text	Col	Row	Default Setting	Available Setting
Description				
Pick-up setting for the current loop input 1 trip element				
CLI Trip Delay	4D	1A	0	0s to 100s step 0.1s
Operating mode of the current loop input 1 trip element				
CLI I< Alarm	4D	1C	Disabled	Enabled or Disabled
Enables or disables the current loop input 1 undercurrent element used to supervise the 4-20 mA input only				
CLI I< Alm Set	4D	1E	0.0035	0mA to 4mA step 0.1mA
Pick-up setting for the current loop input 1 undercurrent element. (4 - 20 mA input only)				
CLI2 PROTECTION	4D	21	Sub-Heading	Sub-Heading
CLI2 PROTECTION				
CLI Input Status	4D	22	Enabled	Enabled or Disabled
Enables or disables the current loop (transducer) input 1 element				
CLI Input Type	4D	24	4-20mA	0 to 1mA, 0 to 10mA, 0 to 20mA or 4 to 20mA
Current loop 1 input type				
CLI Input Label	4D	26	CLIO Input 2	16-character text string (32 to 163)
Current loop 1 input description. The minimum and maximum settings define the range but they have no units. The user can use the label to enter the transducer function and unit of measurement				
CLI Minimum	4D	28	0	-9999 to 9999 step 0.1
Current loop input 1 minimum setting. Defines the lower range of the physical or electrical quantity measured by the transducer				
CLI Maximum	4D	2A	100	-9999 to 9999 step 0.1
Current loop input 1 maximum setting. Defines the upper range of the physical or electrical quantity measured by the transducer				
CLI Alarm	4D	2C	Disabled	Enabled or Disabled
Enables or disables the current loop input 1 alarm element				
CLI Alarm Fn	4D	2E	Over	Over or Under
Operating mode of the current loop input 1 alarm element				
CLI Alarm Set	4D	30	50	From "MIN(CLI2Min, Max)" to "MAX(CLI2Min, Max))" step 0.1
Pick-up setting for the current loop input 1 alarm element				
CLI Alarm Delay	4D	32	1s	0s to 100s step 0.1s
Operating time-delay setting of current loop input 1 alarm element				
CLI Trip	4D	34	Disabled	Enabled or Disabled
Pick-up setting for the current loop input 1 trip element				
CLI Trip Fn	4D	36	Over	Over or Under
Operating mode of the current loop input 1 alarm element				
CLI Trip Set	4D	38	60	From "MIN(CLI2Min, Max)" to "MAX(CLI2Min, Max))" step 0.1
Pick-up setting for the current loop input 1 trip element				
CLI Trip Delay	4D	3A	0s	0s to 100s step 0.1s
Operating mode of the current loop input 1 trip element				
CLI I< Alarm	4D	3C	Disabled	Enabled or Disabled
Enables or disables the current loop input 1 undercurrent element used to supervise the 4-20 mA input only				
CLI I< Alm Set	4D	3E	0.0035	0mA to 4mA step 0.1mA
Pick-up setting for the current loop input 1 undercurrent element. (4 - 20 mA input only)				
CLI3 PROTECTION	4D	41	Sub-Heading	Sub-Heading

Menu Text	Col	Row	Default Setting	Available Setting
Description				
CLI3 PROTECTION				
CLI Input Status	4D	42	Enabled	Enabled or Disabled
Enables or disables the current loop (transducer) input 1 element				
CLI Input Type	4D	44	4-20mA	0 to 1mA, 0 to 10mA, 0 to 20mA or 4 to 20mA
Current loop 1 input type				
CLI Input Label	4D	46	CLIO Input 3	16-character text string (32 to 163)
Current loop 1 input description. The minimum and maximum settings define the range but they have no units. The user can use the label to enter the transducer function and unit of measurement				
CLI Minimum	4D	48	0	-9999 to 9999 step 0.1
Current loop input 1 minimum setting. Defines the lower range of the physical or electrical quantity measured by the transducer				
CLI Maximum	4D	4A	100	-9999 to 9999 step 0.1
Current loop input 1 maximum setting. Defines the upper range of the physical or electrical quantity measured by the transducer				
CLI Alarm	4D	4C	Disabled	Enabled or Disabled
Enables or disables the current loop input 1 alarm element				
CLI Alarm Fn	4D	4E	Over	Over or Under
Operating mode of the current loop input 1 alarm element				
CLI Alarm Set	4D	50	50	From "MIN(CLI3Min, Max)" to "MAX(CLI3Min, Max))" step 0.1
Pick-up setting for the current loop input 1 alarm element				
CLI Alarm Delay	4D	52	1s	0s to 100s step 0.1s
Operating time-delay setting of current loop input 1 alarm element				
CLI Trip	4D	54	Disabled	Enabled or Disabled
Pick-up setting for the current loop input 1 trip element				
CLI Trip Fn	4D	56	Over	Over or Under
Operating mode of the current loop input 1 alarm element				
CLI Trip Set	4D	58	60	From "MIN(CLI3Min, Max)" to "MAX(CLI3Min, Max))" step 0.1
Pick-up setting for the current loop input 1 trip element				
CLI Trip Delay	4D	5A	0s	0s to 100s step 0.1s
Operating mode of the current loop input 1 trip element				
CLI I< Alarm	4D	5C	Disabled	Enabled or Disabled
Enables or disables the current loop input 1 undercurrent element used to supervise the 4-20 mA input only				
CLI I< Alm Set	4D	5E	0.0035	0mA to 4mA step 0.1mA
Pick-up setting for the current loop input 1 undercurrent element. (4 - 20 mA input only)				
CLI4 PROTECTION	4D	61	Sub-Heading	Sub-Heading
CLI4 PROTECTION				
CLI Input Status	4D	62	Enabled	Enabled or Disabled
Enables or disables the current loop (transducer) input 1 element				
CLI Input Type	4D	64	4-20mA	0 to 1mA, 0 to 10mA, 0 to 20mA or 4 to 20mA
Current loop 1 input type				
CLI Input Label	4D	66	CLIO Input 4	16-character text string (32 to 163)
Current loop 1 input description. The minimum and maximum settings define the range but they have no units. The user can use the label to enter the transducer function and unit of measurement				
CLI Minimum	4D	68	0	-9999 to 9999 step 0.1

Menu Text	Col	Row	Default Setting	Available Setting
Description				
Current loop input 1 minimum setting. Defines the lower range of the physical or electrical quantity measured by the transducer				
CLI Maximum	4D	6A	100	-9999 to 9999 step 0.1
Current loop input 1 maximum setting. Defines the upper range of the physical or electrical quantity measured by the transducer				
CLI Alarm	4D	6C	Disabled	Enabled or Disabled
Enables or disables the current loop input 1 alarm element				
CLI Alarm Fn	4D	6E	Over	Over or Under
Operating mode of the current loop input 1 alarm element				
CLI Alarm Set	4D	70	50	From "MIN(CLI4Min, Max)" to "MAX(CLI4Min, Max))" step 0.1
Pick-up setting for the current loop input 1 alarm element				
CLI Alarm Delay	4D	72	1s	0s to 100s step 0.1s
Operating time-delay setting of current loop input 1 alarm element				
CLI Trip	4D	74	Disabled	Enabled or Disabled
Pick-up setting for the current loop input 1 trip element				
CLI Trip Fn	4D	76	Over	Over or Under
Operating mode of the current loop input 1 alarm element				
CLI Trip Set	4D	78	60	From "MIN(CLI4Min, Max)" to "MAX(CLI4Min, Max))" step 0.1
Pick-up setting for the current loop input 1 trip element				
CLI Trip Delay	4D	7A	0s	0s to 100s step 0.1s
Operating mode of the current loop input 1 trip element				
CLI I< Alarm	4D	7C	Disabled	Enabled or Disabled
Enables or disables the current loop input 1 undercurrent element used to supervise the 4-20 mA input only				
CLI I< Alm Set	4D	7E	0.0035	0mA to 4mA step 0.1mA
Pick-up setting for the current loop input 1 undercurrent element. (4 - 20 mA input only)				
CLO OUTPUT1	4D	9F	Sub-Heading	Sub-Heading
CLO OUTPUT1				
CLO Status	4D	A0	Disabled	Enabled or Disabled
Enable or disables the current loop (transducer) output 1 element				
CLO Type	4D	A2	4-20mA	0 to 1mA, 0 to 10mA, 0 to 20mA or 4 to 20mA
Current loop 1 output type				
CLO Set Values	4D	A4	Primary	Primary or Secondary
This setting controls if the measured values from current loop output 1 are Primary or Secondary values				
CLO Parameter	4D	A6	IA Magnitude	See CLIO measurement table
This setting defines the measured quantity assigned to current loop output 1				
CLO Minimum	4D	A8	See G155 table	See CLIO measurement table
Current loop output 1 minimum setting. Defines the lower range of the measurement				
CLO Maximum	4D	AA	See G155 table	See CLIO measurement table
Current loop output 1 maximum setting. Defines the upper range of the measurement				
CLO OUTPUT2	4D	AF	Sub-Heading	Sub-Heading
CLO OUTPUT2				
CLO Status	4D	B0	Disabled	Enabled or Disabled
Enable or disables the current loop (transducer) output 1 element				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
CLO Type	4D	B2	4-20mA	0 to 1mA, 0 to 10mA, 0 to 20mA or 4 to 20mA
Current loop 1 output type				
CLO Set Values	4D	B4	Primary	Primary or Secondary
This setting controls if the measured values from current loop output 1 are Primary or Secondary values				
CLO Parameter	4D	B6	IB Magnitude	See CLIO measurement table
This setting defines the measured quantity assigned to current loop output 1				
CLO Minimum	4D	B8	See G155 table	See CLIO measurement table
Current loop output 1 minimum setting. Defines the lower range of the measurement				
CLO Maximum	4D	BA	See G155 table	See CLIO measurement table
Current loop output 1 maximum setting. Defines the upper range of the measurement				
CLO OUTPUT3	4D	BF	Sub-Heading	Sub-Heading
CLO OUTPUT3				
CLO Status	4D	C0	Disabled	Enabled or Disabled
Enable or disables the current loop (transducer) output 1 element				
CLO Type	4D	C2	4-20mA	0 to 1mA, 0 to 10mA, 0 to 20mA or 4 to 20mA
Current loop 1 output type				
CLO Set Values	4D	C4	Primary	Primary or Secondary
This setting controls if the measured values from current loop output 1 are Primary or Secondary values				
CLO Parameter	4D	C6	IC Magnitude	See CLIO measurement table
This setting defines the measured quantity assigned to current loop output 1				
CLO Minimum	4D	C8	See G155 Table	See CLIO measurement table
Current loop output 1 minimum setting. Defines the lower range of the measurement				
CLO Maximum	4D	CA	See G155 Table	See CLIO measurement table
Current loop output 1 maximum setting. Defines the upper range of the measurement				
CLO OUTPUT4	4D	CF	Sub-Heading	Sub-Heading
CLO OUTPUT4				
CLO Status	4D	D0	Disabled	Enabled or Disabled
Enable or disables the current loop (transducer) output 1 element				
CLO Type	4D	D2	4-20mA	0 to 1mA, 0 to 10mA, 0 to 20mA or 4 to 20mA
Current loop 1 output type				
CLO Set Values	4D	D4	Primary	Primary or Secondary
This setting controls if the measured values from current loop output 1 are Primary or Secondary values				
CLO Parameter	4D	D6	IN Measured Mag	See CLIO measurement table
This setting defines the measured quantity assigned to current loop output 1				
CLO Parameter	4D	D6	IN Derived Mag	See CLIO measurement table
P642 only. This setting defines the measured quantity assigned to current loop output 1				
CLO Minimum	4D	D8	See G155 Table	See CLIO measurement table
Current loop output 1 minimum setting. Defines the lower range of the measurement				
CLO Maximum	4D	DA	See G155 Table	See CLIO measurement table
Current loop output 1 maximum setting. Defines the upper range of the measurement				

Table 20 - Group 1 CLIO Protection Settings

The CLIO output measurements are updated using a software timer every 50 ms. The CLIO protection is called every cycle (20 ms).
Current loop output parameters are shown in the following table:

Current loop output measurement	Unit	Min.	Max.	Step	Default min.	Default max.
IA-1 Magnitude	A	0	16 In	0.01 In	0	1.2 In
IB-1 Magnitude	A	0	16 In	0.01 In	0	1.2 In
IC-1 Magnitude	A	0	16 In	0.01 In	0	1.2 In
IA-2 Magnitude	A	0	16 In	0.01 In	0	1.2 In
IB-2 Magnitude	A	0	16 In	0.01 In	0	1.2 In
IC-2 Magnitude	A	0	16 In	0.01 In	0	1.2 In
IA-3 Magnitude	A	0	16 In	0.01 In	0	1.2 In
IB-3 Magnitude	A	0	16 In	0.01 In	0	1.2 In
IC-3 Magnitude	A	0	16In	0.01 In	0	1.2 In
IA-4 Magnitude	A	0	16In	0.01 In	0	1.2 In
IB-4 Magnitude	A	0	16In	0.01 In	0	1.2 In
IC-4 Magnitude	A	0	16In	0.01 In	0	1.2 In
IA-5 Magnitude	A	0	16In	0.01 In	0	1.2 In
IB-5 Magnitude	A	0	16In	0.01 In	0	1.2 In
IC-5 Magnitude	A	0	16In	0.01 In	0	1.2 In
I1-1 Magnitude	A	0	16In	0.01 In	0	1.2 In
I2-1 Magnitude	A	0	16In	0.01 In	0	1.2 In
I0-1 Magnitude	A	0	16In	0.01 In	0	1.2 In
I1-2 Magnitude	A	0	16 In	0.01 In	0	1.2 In
I2-2 Magnitude	A	0	16 In	0.01 In	0	1.2 In
I0-2 Magnitude	A	0	16In	0.01 In	0	1.2 In
I1-3 Magnitude	A	0	16In	0.01 In	0	1.2 In
I2-3 Magnitude	A	0	16In	0.01 In	0	1.2 In
I0-3 Magnitude	A	0	16In	0.01 In	0	1.2 In
I1-4 Magnitude	A	0	16In	0.01 In	0	1.2 In
I2-4 Magnitude	A	0	16In	0.01 In	0	1.2 In
I0-4 Magnitude	A	0	16In	0.01 In	0	1.2 In
I1-5 Magnitude	A	0	16In	0.01 In	0	1.2 In
I2-5 Magnitude	A	0	16In	0.01 In	0	1.2 In
I0-5 Magnitude	A	0	16In	0.01 In	0	1.2 In
IA HV Magnitude	A	0	16In	0.01 In	0	1.2 In
IB HV Magnitude	A	0	16In	0.01 In	0	1.2 In
IC HV Magnitude	A	0	16In	0.01 In	0	1.2 In
IN HV Measured Mag	A	0	16In	0.01 In	0	1.2 In
IN HV Derived Mag	A	0	16In	0.01 In	0	1.2 In
IA LV Magnitude	A	0	16In	0.01 In	0	1.2 In
IB LV Magnitude	A	0	16In	0.01 In	0	1.2 In
IC LV Magnitude	A	0	16In	0.01 In	0	1.2 In
IN LV Measured Mag	A	0	16In	0.01 In	0	1.2 In
IN LV Derived Mag	A	0	16In	0.01 In	0	1.2 In
IA TV Magnitude	A	0	16In	0.01 In	0	1.2 In

Current loop output measurement	Unit	Min.	Max.	Step	Default min.	Default max.
IB TV Magnitude	A	0	16In	0.01 In	0	1.2 In
IC TV Magnitude	A	0	16In	0.01 In	0	1.2 In
IN TV Measured Mag	A	0	16In	0.01 In	0	1.2 In
IN TV Derived Mag	A	0	16In	0.01 In	0	1.2 In
VAB Magnitude	V	0	200 Vn	0.1 Vn	0	140 Vn
VBC Magnitude	V	0	200 Vn	0.1 Vn	0	140 Vn
VCA Magnitude	V	0	200 Vn	0.1 Vn	0	140 Vn
VAN Magnitude	V	0	200 Vn	0.1 Vn	0	80 Vn
VBN Magnitude	V	0	200 Vn	0.1 Vn	0	80 Vn
VCN Magnitude	V	0	200 Vn	0.1 Vn	0	80 Vn
Vx Magnitude	V	0	200 Vn	0.1 Vn	0	80 Vn
VN Derived Mag	V	0	200 Vn	0.1 Vn	0	80 Vn
V1 Magnitude	V	0	200 Vn	0.1 Vn	0	80 Vn
V2 Magnitude	V	0	200 Vn	0.1 Vn	0	80 Vn
V0 Magnitude	V	0	200 Vn	0.1 Vn	0	80 Vn
VAN RMS	V	0	200 Vn	0.1 Vn	0	80 Vn
VBN RMS	V	0	200 Vn	0.1 Vn	0	80 Vn
VCN RMS	V	0	200 Vn	0.1 Vn	0	80 Vn
Frequency	Hz	0	70	0.01	45	65
RTD 1	°C	-40	300	0.1	0	200
RTD 2	°C	-40	300	0.1	0	200
RTD 3	°C	-40	300	0.1	0	200
RTD 4	°C	-40	300	0.1	0	200
RTD 5	°C	-40	300	0.1	0	200
RTD 6	°C	-40	300	0.1	0	200
RTD 7	°C	-40	300	0.1	0	200
RTD 8	°C	-40	300	0.1	0	200
RTD 9	°C	-40	300	0.1	0	200
RTD 10	°C	-40	300	0.1	0	200
CL Input 1		-9999	9999	0.1	0	9999
CL Input 2		-9999	9999	0.1	0	9999
CL Input 3		-9999	9999	0.1	0	9999
CL Input 4		-9999	9999	0.1	0	9999
Volts/Hz W1	V/Hz	0	20	0.01	0	4
V/Hz W1 Thermal	%	0	200	0.01	0	120
Volts/Hz W2	V/Hz	0	20	0.01	0	4
V/Hz W2 Thermal	%	0	200	0.01	0	120
Hot Spot T	°C	-40	300	0.1	0	200
Top Oil T	°C	-40	300	0.1	0	200
Ambient T	°C	-40	300	0.1	0	200
LOL Status	Hr	1	300000	1	1	300000
Note These settings are for nominal 1A and 100/120 V versions only. For other nominal versions they need to be multiplied accordingly.						

Table 21 - Current loop output measurements

5 CONTROL AND SUPPORT SETTINGS

The control and support settings are part of the main menu and are used to configure the global configuration for the relay. It includes submenu settings as shown here.

- Relay function configuration settings
- Open/close circuit breaker
- CT & VT ratio settings
- Reset LEDs
- Active protection setting group
- Password & language settings
- Circuit breaker control & monitoring settings
- Communications settings
- Measurement settings
- Event & fault record settings
- User interface settings
- Commissioning settings

5.1 System Data

This menu provides information for the device and general status of the relay.

Menu Text	Col	Row	Default Setting	Available Setting
Description				
SYSTEM DATA	00	00		
This column contains general system settings				
Language	00	01	English	English, Français, Deutsch or Español
The default language used by the device. Selectable as English, French, German, Spanish.				
Sys Fn Links	00	03	0 = Latched	0 = latched or 1 = self-reset
Setting to allow the fixed function trip LED to be self resetting (set to 1 to extinguish the LED after a period of healthy restoration of load current).				
Description	00	04	MiCOM P	MiCOM P64x
Editable 16-character description of the unit				
Plant Reference	00	05	MiCOM	MiCOM
Plant description: Can be edited				
Model Number	00	06	Model Number	<Model number>
Displays the model number (e.g. P643?11???0010K). This can not be edited				
Serial Number	00	08	Serial Number	<Serial number>
Displays the serial number (e.g. 149188B). This can not be edited.				
Frequency	00	09	50	50Hz or 60Hz
Sets the mains frequency				
Comms Level	00	0A	2	<conformance level displayed>
Displays the conformance of the relay to the Courier Level 2 comms				
Relay Address	00	0B	255	<Unit address>
Sets the first rear port relay address of the unit				
Plant Status	00	0C	0	16-bit binary data: 0 = Energised or 1 = de-energized
Displays the circuit breaker plant status for up to 8 circuit breakers. The P64x relay supports only a single circuit breaker configuration				
Control Status	00	0D	0	Not Used

Menu Text	Col	Row	Default Setting	Available Setting
Description				
Not used				
Active Group	00	0E	1	1, 2, 3 or 4
Displays the active settings group				
Software Ref. 1	00	11	<Software Ref. 1>	<Software Ref. 1>
Displays the relay software version including the protocol and relay model				
Software Ref. 2	00	12	<Software Ref. 2>	<Software Ref. 1>
Displays the relay software version including the protocol and relay model. This is displayed for those units which are used with theIEC 61850 protocol only and displays the software version of the Ethernet card.				
Software Ref. 3	00	13	<Software Ref. 2>	<Software Ref. 1>
Displays the relay software version including the protocol and relay model. This is displayed for those units which are used with theIEC 61850 protocol only and displays the software version of the Ethernet card.				
NIC Platform Ref	00	14		<NIC platform reference>
IEC61850 Edition	00	15	2	Edition 1, Edition 2
Set the IEC61850 version (edition 1 or edition 2)				
ETH COMM Mode	00	16	Dual IP	Duanl IP, PRP, HSR, RSTP
Set the FPGA type for Ethernet board (substaion bord)				
PB COMM Mode	00	17	Dual IP	Duanl IP, PRP
Set the FPGA type for process board				
Opto I/P Status	00	30	0	16-bit binary data: 1 = Energised or 0 = de-energized
Displays the status of the relay's opto-isolated inputs as a binary string. 1 indicates an energized opto-isolated input and 0 a de-energized one				
Relay O/P Status	00	40	0	16-bit binarydata: 1 = Operated state or 0 = non-operated state
Displays the status of the relay's output contacts as a binary string. 1 indicates an operated state and 0 a non-operated state				
Alarm Status 1	00	50	00000000000000000000000000000000	32-bit binary data: 0 = Off or 1=On
This menu cell displays the status of the first 32 alarms as a binary string. 1 indicates an ON state and 0 an OFF state. Includes fixed and user settable alarms. See Data Type G96 in the Menu Database document, P64x/EN/MD for details.				
Alarm Status 2	00	51	00000000000000000000000000000000	32-bit binary data: 0 = Off or 1=On
This menu cell displays the status of the second 32 alarms as a binary string.1 indicates an ON state and 0 an OFF state. See Data Type G128 in the Menu Database document, P64x/EN/MD for details.				
Alarm Status 3	00	52	00000000000000000000000000000000	32-bit binary data: 0 = Off or 1=On
This menu cell displays the status of the third 32 alarms as a binary string. 1 indicates an ON state and 0 an OFF state. Assigned specifically for platform alarms. See Data Type G228 in the Menu Database document, P64x/EN/MD for details.				
Usr Alarm Status	00	53	00000000000000000000000000000000	32-bit binary data: 0 = Off or 1=On
This menu cell displays the status of the fourth 32 alarms as a binary string. 1 indicates an ON state and 0 an OFF state. Assigned specifically for platform alarms. See Data Type G228 in the Menu Database document, P64x/EN/MD for details.				
Access Level	00	D0		
Display the Role(s) of the current logged in user, if no one logged in, it shall be "NONE".				
New Eng.Level PW	00	D3		ASCII 33 to 122
Common Engineer level password for all interfaces				
New Op.Level PW	00	D4		ASCII 33 to 122

Menu Text	Col	Row	Default Setting	Available Setting
Description				
Common Operator level password for all interfaces				
Security Features	00	DF	3	
Displays the level of cyber security implemented				
Password	00	E1		ASCII 33 to 122
Common password for all interfaces				
Encryption Salt	00	E5		
Enter username	00	F1		
Number of users	00	F2		
New UI pwd	00	F3		
Cells reserved for second password modification. Not in use currently.				
New password	00	F4		

Table 22 - System data settings

5.2 View Records

This menu provides information on fault and maintenance records. The relay records the last five fault records and the last ten maintenance records.

Menu Text	Col	Row	Default Setting	Available Setting
Description				
VIEW RECORDS	01	00		
This column contains View Records settings				
Select Event	01	01	0	0 to 511 step 1
Setting range from 0 to 511. This selects the required event record from the possible 512 that can be stored. A value of 0 corresponds to the latest event				
Menu Cell Ref	01	02	(From Record)	Latched alarm active, Latched alarm inactive, Self reset alarm active, Self reset alarm inactive, Relay contact event, Opto-isolated input event, Protection event, General event, Fault record event, Maintenance record event
Indicates the type of event				
Time & Date	01	03	(From Record)	From record
Time & Date Stamp for the event given by the internal Real Time Clock				
Event Text	01	04	32-character string	32 character string
Up to 32 Character description of the Event. See the event sheet in the Measurements and Recording chapter, P64x/EN MR or the Menu Database document, P64x/EN/MD for details.				
Event Value	01	05	32-bit binary string	32-bit binary string - ON (1) or OFF (0) for status of relay contact or opto input or alarm or protection event depending on event type.
Unsigned integer is used for maintenance records. See the event sheet in the Measurements and Recording chapter, P64x/EN MR or the Menu Database document, P64x/EN/MD for details.				
Select Fault	01	06	0	0 to 19 step 1
Setting range from 0 to 19. This selects the required fault record from the possible 20 that can be stored. A value of 0 corresponds to the latest fault				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
Faulted Phase	01	07	00000000	8-bit binary string
Displays the faulted phase as a binary string, bits 0 – 8 = Start A/B/C/N Trip A/B/C/N				
Start Elements1	01	08	00000000000000000000000000000000	32-bit binary string
32-bit binary string gives status of first 32 start signals. See Data type G84 in the Menu Database document, P64x/EN/MD for details.				
Start Elements2	01	09	00000000000000000000000000000000	32-bit binary string
32-bit binary string gives status of second 32 start signals. See Data type G107 in the Menu Database document, P64x/EN/MD for details.				
Start Elements3	01	0A	00000000000000000000000000000000	32-bit binary string
32-bit binary string gives status of third 32 start signals. See Data type G129 in the Menu Database document, P64x/EN/MD for details.				
Trip Elements1	01	10	00000000000000000000000000000000	32-bit binary string
32-bit binary string gives status of first 32 trip signals. See Data Type G85 in the Menu Database document, P64x/EN/MD for details.				
Trip Elements2	01	11	00000000000000000000000000000000	32-bit binary string
32-bit binary string gives status of second 32 trip signals. See Data Type G86 in the Menu Database document, P64x/EN/MD for details.				
Trip Elements3	01	12	00000000000000000000000000000000	32-bit binary string
32-bit binary string gives status of third 32 trip signals. See Data Type G130 in the Menu Database document, P64x/EN/MD for details.				
Fault Alarms	01	50	00000000000000000000000000000000	32-bit binary string
32-bit binary string gives status of fault alarm signals. See Data Type G87 in the Menu Database document, P64x/EN/MD for details.				
Fault Time	01	51	(From Record)	From record
Displays the Fault Time and Date.				
Fault Type	01	52	Data	Internal or External
Displays the Fault Type (internal or external).				
Active Group	01	53	Data	<Active group>
Displays the Active setting group 1-4.				
System Frequency	01	54	Data	<System frequency>
Displays the System frequency.				
Fault Duration	01	55	Data	<Fault duration>
Fault duration: Time from the start or trip until the undercurrent elements indicate the CB is open				
CB Operate Time	01	56	Data	<CB Operate time>
Circuit Breaker Operate Time: Time from protection trip to undercurrent elements indicating the CB is open				
Relay Trip Time	01	60	Data	<relay trip time>
Relay Trip Time: Time from protection start to protection trip				
IA-1 Magnitude	01	62		Not settable
This provides measurement information about the fault.				
IB-1 Magnitude	01	64		Not settable
This provides measurement information about the fault.				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
IC-1 Magnitude	01	66		Not settable
This provides measurement information about the fault.				
IA-2 Magnitude	01	68		Not settable
This provides measurement information about the fault.				
IB-2 Magnitude	01	6A		Not settable
This provides measurement information about the fault.				
IC-2 Magnitude	01	6C		Not settable
This provides measurement information about the fault.				
IA-3 Magnitude	01	6E		Not settable
P643, P645 and P746 only. This provides measurement information about the fault.				
IB-3 Magnitude	01	70		Not settable
P643, P645 and P746 only. This provides measurement information about the fault.				
IC-3 Magnitude	01	72		Not settable
P643, P645 and P746 only. This provides measurement information about the fault.				
IA-4 Magnitude	01	74		Not settable
P645 and P746 only. This provides measurement information about the fault.				
IB-4 Magnitude	01	76		Not settable
P645 and P746 only. This provides measurement information about the fault.				
IC-4 Magnitude	01	78		Not settable
P645 and P746 only. This provides measurement information about the fault.				
IA-5 Magnitude	01	7A		Not settable
P645 and P746 only. This provides measurement information about the fault.				
IB-5 Magnitude	01	7C		Not settable
P645 and P746 only. This provides measurement information about the fault.				
IC-5 Magnitude	01	7E		Not settable
P645 and P746 only. This provides measurement information about the fault.				
IA-HV Magnitude	01	90		Not settable
This provides measurement information about the fault.				
IB-HV Magnitude	01	91		Not settable
This provides measurement information about the fault.				
IC-HV Magnitude	01	92		Not settable
This provides measurement information about the fault.				
IA-LV Magnitude	01	93		Not settable
This provides measurement information about the fault.				
IB-LV Magnitude	01	94		Not settable
This provides measurement information about the fault.				
IC-LV Magnitude	01	95		Not settable

Menu Text	Col	Row	Default Setting	Available Setting
Description				
This provides measurement information about the fault.				
IA-TV Magnitude	01	96		Not settable
P643 and P645 only. This provides measurement information about the fault.				
IB-TV Magnitude	01	97		Not settable
P643 and P645 only. This provides measurement information about the fault.				
IC-TV Magnitude	01	98		Not settable
P643 and P645 only. This provides measurement information about the fault.				
I2-HV Magnitude	01	99		Not settable
This provides measurement information about the fault.				
I2-LV Magnitude	01	9A		Not settable
This provides measurement information about the fault.				
I2-TV Magnitude	01	9B		Not settable
P643 and P645 only. This provides measurement information about the fault.				
IN-HV Mea Mag	01	9C		Not settable
This provides measurement information about the fault.				
IN-LV Mea Mag	01	9D		Not settable
This provides measurement information about the fault.				
IN-TV Mea Mag	01	9E		Not settable
P643 and P645 only. This provides measurement information about the fault.				
VAN Magnitude	01	A0		Not settable
P643, P645 and P746 only. This provides measurement information about the fault.				
VBN Magnitude	01	A1		Not settable
P643, P645 and P746 only. This provides measurement information about the fault.				
VCN Magnitude	01	A2		Not settable
P643, P645 and P746 only. This provides measurement information about the fault.				
Vx Magnitude	01	A3		Not settable
This provides measurement information about the fault.				
V1 Magnitude	01	A4		Not settable
This provides measurement information about the fault.				
V2 Magnitude	01	A5		Not settable
This provides measurement information about the fault.				
VN Derived Mag	01	A6		Not settable
P643, P645 and P746 only. This provides measurement information about the fault.				
VAB Magnitude	01	A7		Not settable
This provides measurement information about the fault.				
VBC Magnitude	01	A8		Not settable
This provides measurement information about the fault.				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
VCA Magnitude	01	A9		Not settable
This provides measurement information about the fault.				
IN-TN1 Mea Mag	01	AA		Not settable
This provides measurement information about the fault.				
IN-TN2 Mea Mag	01	AB		Not settable
This provides measurement information about the fault.				
IN-TN3 Mea Mag	01	AC		Not settable
P643 and P645 only. This provides measurement information about the fault.				
IA Differential	01	B0		Not settable
This provides measurement information about the fault.				
IB Differential	01	B1		Not settable
This provides measurement information about the fault. IB Differential Current fault.				
IC Differential	01	B2		Not settable
This provides measurement information about the fault. IC Differential Current fault.				
IA Bias	01	B3		Not settable
This provides measurement information about the fault. IA Bias Current fault.				
IB Bias	01	B4		Not settable
This provides measurement information about the fault. IB Bias Current fault.				
IC Bias	01	B5		Not settable
This provides measurement information about the fault. IC Bias Current fault.				
IREF HV LoZ Diff	01	B9		Not settable
This provides measurement information about the fault. IREF HV LoZ Differential Current fault.				
IREF HV LoZ Bias	01	BA		Not settable
This provides measurement information about the fault. IREF HV LoZ Bias Current fault.				
IREF LV LoZ Diff	01	BB		Not settable
This provides measurement information about the fault. IREF LV LoZ Differential Current fault.				
IREF LV LoZ Bias	01	BC		Not settable
This provides measurement information about the fault. IREF LV LoZ Bias Current fault.				
IREF TV LoZ Diff	01	BD		Not settable
P643 and P645 only. This provides measurement information about the IREF TV LoZ Differential Current fault.				
IREF TV LoZ Bias	01	BE		Not settable
P643 and P645 only. This provides measurement information about the IREF TV LoZ Bias Current fault.				
IREF Auto LoZ Diff	01	BF		Not settable
This provides measurement information about the IREF Auto Loz Differential Current fault				
IREF Auto LoZ Bias	01	C0		Not settable
This provides measurement information about the IREF Auto Loz Bias Current fault				
IREF HV HighZ Op	01	C1		Not settable
This provides measurement information about the IREF HV HighZ Operation Current fault				
IREF LV HighZ Op	01	C2		Not settable
This provides measurement information about the IREF LV HighZ Operation Current fault				
IREF TV HighZ Op	01	C3		Not settable

Menu Text	Col	Row	Default Setting	Available Setting
Description				
This provides measurement information about the IREF TV TighZ Operation Current fault				
IREF Auto HighZ Op	01	C4		Not settable
This provides measurement information about the IREF Auto TighZ Operation Current fault				
IA Peak Mag	01	C5		Not settable
This provides measurement information about the IA Peak Magnitude fault.				
IB Peak Mag	01	C6		Not settable
This provides measurement information about the IB Peak Magnitude fault.				
IC Peak Mag	01	C7		Not settable
This provides measurement information about the IC Peak Magnitude fault.				
I2t Phase A	01	C8		Not settable
This provides measurement information about the I2t Phase A fault.				
I2t Phase B	01	C9		Not settable
This provides measurement information about the I2t Phase B fault.				
I2t Phase C	01	CA		Not settable
This provides measurement information about the I2t Phase C fault.				
RTD 1	01	D0		Not settable
This provides measurement information about the RTD 1 fault.				
RTD 2	01	D1		Not settable
This provides measurement information about the RTD 2 fault.				
RTD 3	01	D2		Not settable
This provides measurement information about the RTD 3 fault.				
RTD 4	01	D3		Not settable
This provides measurement information about the RTD 4 fault.				
RTD 5	01	D4		Not settable
This provides measurement information about the RTD 5 fault.				
RTD 6	01	D5		Not settable
This provides measurement information about the RTD 6 fault.				
RTD 7	01	D6		Not settable
This provides measurement information about the RTD 7 fault.				
RTD 8	01	D7		Not settable
This provides measurement information about the RTD 8 fault.				
RTD 9	01	D8		Not settable
This provides measurement information about the RTD 9 fault.				
RTD 10	01	D9		Not settable
This provides measurement information about the RTD 10 fault.				
CLIO Input 1	01	DA		Not settable
This provides measurement information about the CLIO Input 1 fault.				
CLIO Input 2	01	DB		Not settable
This provides measurement information about the CLIO Input 2 fault.				
CLIO Input 3	01	DC		Not settable
This provides measurement information about the CLIO Input 3 fault.				
CLIO Input 4	01	DD		Not settable
This provides measurement information about the CLIO Input 4 fault.				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
Evt Iface Source	01	FA		
Evt Access Level	01	FB		
Evt Extra Info	01	FC		
Evt Unique Id	01	FE		
Reset Indication	01	FF	No	No or Yes
Resets latched LEDs and latched relay contacts provided the relevant protection element has reset				

Table 23 - View records settings

5.3 Measurements 1

This menu provides measurement information.

Menu Text	Col	Row	Default Setting	Available Setting
Description				
MEASUREMENTS 1	02	00		
Measurement 1 group for P642, P643, P645				
IA-1 Magnitude	02	01	Data	Not settable
This records the IA-1 Magnitude measurement				
IA-1 Phase Angle	02	02	Data	Not settable
This records the IA-1 Phase Angle measurement				
IB-1 Magnitude	02	03	Data	Not settable
This records the IB-1 Magnitude measurement				
IB-1 Phase Angle	02	04	Data	Not settable
This records the IB-1 Phase Angle measurement				
IC-1 Magnitude	02	05	Data	Not settable
This records the IC-1 Magnitude measurement				
IC-1 Phase Angle	02	06	Data	Not settable
This records the IC-1 Phase Angle measurement				
IA-2 Magnitude	02	07	Data	Not settable
This records the IA-2 Magnitude measurement				
IA-2 Phase Angle	02	08	Data	Not settable
This records the IA-2 Phase Angle measurement				
IB-2 Magnitude	02	09	Data	Not settable
This records the IB-2 Magnitude measurement				
IB-2 Phase Angle	02	0A	Data	Not settable
This records the IB-2 Phase Angle measurement				
IC-2 Magnitude	02	0B	Data	Not settable
This records the IC-2 Magnitude measurement				
IC-2 Phase Angle	02	0C	Data	Not settable
This records the IC-2 Phase Angle measurement				
IA-3 Magnitude	02	0D	Data	Not settable

Menu Text	Col	Row	Default Setting	Available Setting
Description				
P643, P645 and P746 only. This records the IA-3 Magnitude measurement				
IA-3 Phase Angle	02	0E	Data	Not settable
P643, P645 and P746 only. This records the IA-3 Phase Angle measurement				
IB-3 Magnitude	02	0F	Data	Not settable
P643, P645 and P746 only. This records the IB-3 Magnitude measurement				
IB-3 Phase Angle	02	10	Data	Not settable
P643, P645 and P746 only. This records the IB-3 Phase Angle measurement				
IC-3 Magnitude	02	11	Data	Not settable
P643, P645 and P746 only. This records the IC-3 Magnitude measurement				
IC-3 Phase Angle	02	12	Data	Not settable
P643, P645 and P746 only. This records the IC-3 Phase Angle measurement				
IA-4 Magnitude	02	13	Data	Not settable
P645 and P746 only. This records the IA-4 Magnitude measurement				
IA-4 Phase Angle	02	14	Data	Not settable
P645 and P746 only. This records the IA-4 Phase Angle measurement				
IB-4 Magnitude	02	15	Data	Not settable
P645 and P746 only. This records the IB-4 Magnitude measurement				
IB-4 Phase Angle	02	16	Data	Not settable
P645 and P746 only. This records the IB-4 Phase Angle measurement				
IC-4 Magnitude	02	17	Data	Not settable
P645 and P746 only. This records the IC-4 Magnitude measurement				
IC-4 Phase Angle	02	18	Data	Not settable
P645 and P746 only. This records the IC-4 Phase Angle measurement				
IA-5 Magnitude	02	19	Data	Not settable
P645 and P746 only. This records the IA-5 Magnitude measurement				
IA-5 Phase Angle	02	1A	Data	Not settable
P645 and P746 only. This records the IA-5 Phase Angle measurement				
IB-5 Magnitude	02	1B	Data	Not settable
P645 and P746 only. This records the IB-5 Magnitude measurement				
IB-5 Phase Angle	02	1C	Data	Not settable
P645 and P746 only. This records the IB-5 Phase Angle measurement				
IC-5 Magnitude	02	1D	Data	Not settable

Menu Text	Col	Row	Default Setting	Available Setting
Description				
P645 and P746 only. This records the IC-5 Magnitude measurement				
IC-5 Phase Angle	02	1E	Data	Not settable
P645 and P746 only. This records the IC-5 Phase Angle measurement				
IA-HV Magnitude	02	50	Data	Not settable
This records the IA-HV Magnitude measurement				
IA-HV Phase Ang	02	51	Data	Not settable
This records the IA-HV Phase Ang measurement				
IB-HV Magnitude	02	52	Data	Not settable
This records the IB-HV Magnitude measurement				
IB-HV Phase Ang	02	53	Data	Not settable
This records the IB-HV Phase Ang measurement				
IC-HV Magnitude	02	54	Data	Not settable
This records the IC-HV Magnitude measurement				
IC-HV Phase Ang	02	55	Data	Not settable
This records the IC-HV Phase Ang measurement				
IA-LV Magnitude	02	56	Data	Not settable
This records the IA-LV Magnitude measurement				
IA-LV Phase Ang	02	57	Data	Not settable
This records the IA-LV Phase Ang measurement				
IB-LV Magnitude	02	58	Data	Not settable
This records the IB-LV Magnitude measurement				
IB-LV Phase Ang	02	59	Data	Not settable
This records the IB-LV Phase Ang measurement				
IC-LV Magnitude	02	5A	Data	Not settable
This records the IC-LV Magnitude measurement				
IC-LV Phase Ang	02	5B	Data	Not settable
This records the IC-LV Phase Ang measurement				
IA-TV Magnitude	02	5C	Data	Not settable
P643 and P645 only. This records the IA-TV Magnitude measurement				
IA-TV Phase Ang	02	5D	Data	Not settable
P643 and P645 only. This records the IA-TV Phase Ang measurement				
IB-TV Magnitude	02	5E	Data	Not settable
P643 and P645 only. This records the IB-TV Magnitude measurement				
IB-TV Phase Ang	02	5F	Data	Not settable
P643 and P645 only. This records the IB-TV Phase Ang measurement				
IC-TV Magnitude	02	60	Data	Not settable
P643 and P645 only. This records the IC-TV Magnitude measurement				
IC-TV Phase Ang	02	61	Data	Not settable

Menu Text	Col	Row	Default Setting	Available Setting
Description				
P643 and P645 only. This records the IC-TV Phase Ang measurement				
I0-1 Magnitude	02	62	Data zero sequence current	Not settable
This records the I0-1 Magnitude measurement				
I1-1 Magnitude	02	63	Data positive sequence current	Not settable
This records the I1-1 Magnitude measurement				
I2-1 Magnitude	02	64	Data negative sequence current	Not settable
This records the I2-1 Magnitude measurement				
IN-HV Mea Mag	02	65	Data	Not settable
This records the IN-HV Mea Mag measurement				
IN-HV Mea Ang	02	66	Data	Not settable
This records the IN-HV Mea Ang measurement				
IN-HV Deriv Mag	02	67	Data	Not settable
This records the IN-HV Deriv Mag measurement				
IN-HV Deriv Ang	02	68	Data	Not settable
This records the IN-HV Deriv Ang measurement				
I0-2 Magnitude	02	69	Data zero sequence current	Not settable
This records the I0-2 Magnitude measurement				
I1-2 Magnitude	02	6A	Data positive sequence current	Not settable
This records the I1-2 Magnitude measurement				
I2-2 Magnitude	02	6B	Data negative sequence current	Not settable
This records the I2-2 Magnitude measurement				
IN-LV Mea Mag	02	6C	Data	Not settable
This records the IN-LV Mea Mag measurement				
IN-LV Mea Ang	02	6D	Data	Not settable
This records the IN-LV Mea Ang measurement				
IN-LV Deriv Mag	02	6E	Data	Not settable
This records the IN-LV Deriv Mag measurement				
IN-LV Deriv Ang	02	6F	Data	Not settable
This records the IN-LV Deriv Ang measurement				
I0-3 Magnitude	02	70	Data zero sequence current. P643,P645 and P746 only	Not settable
P643, P645 and P746 only. This records the I0-3 Magnitude measurement				
I1-3 Magnitude	02	71	Data positive sequence current. P643,P645 and P746 only	Not settable
P643, P645 and P746 only. This records the I1-3 Magnitude measurement				
I2-3 Magnitude	02	72	Data negative sequence current . P643, P645 and P746 only	Not settable
P643, P645 and P746 only. This records the I2-3 Magnitude measurement				
IN-TV Mea Mag	02	73	Data	Not settable
P643 and P645 only. This records the IN-TV Mea Mag measurement				
IN-TV Mea Ang	02	74	Data	Not settable

Menu Text	Col	Row	Default Setting	Available Setting
Description				
P643 and P645 only. This records the IN-TV Mea Ang measurement				
IN-TV Deriv Mag	02	75	Data	Not settable
P643 and P645 only. This records the IN-TV Deriv Mag measurement				
IN-TV Deriv Ang	02	76	Data	Not settable
P643 and P645 only. This records the IN-TV Deriv Ang measurement				
I0-4 Magnitude	02	77	Data zero sequence current. P645 and P746 only	Not settable
P645 and P746 only. This records the I0-4 Magnitude measurement				
I1-4 Magnitude	02	78	Data positive sequence current. P645 and P746 only	Not settable
P645 and P746 only. This records the I1-4 Magnitude measurement				
I2-4 Magnitude	02	79	Data negative sequence current . P645 and P746 only	Not settable
P645 and P746 only. This records the I2-4 Magnitude measurement				
I0-5 Magnitude	02	7C	Data zero sequence current. P645 and P746 only.	Not settable
P645 and P746 only. This records the I0-5 Magnitude measurement				
I1-5 Magnitude	02	7D	Data positive sequence current. P645 and P746 only.	Not settable
P645 and P746 only. This records the I1-5 Magnitude measurement				
I2-5 Magnitude	02	7E	Data negative sequence current . P645 and P746 only.	Not settable
P645 and P746 only. This records the I2-5 Magnitude measurement				
IA-HV RMS	02	86	Data	Not settable
This records the IA-HV RMS measurement				
IB-HV RMS	02	87	Data	Not settable
This records the IB-HV RMS measurement				
IC-HV RMS	02	88	Data	Not settable
This records the IC-HV RMS measurement				
IA-LV RMS	02	89	Data	Not settable
This records the IA-LV RMS measurement				
IB-LV RMS	02	8A	Data	Not settable
This records the IB-LV RMS measurement				
IC-LV RMS	02	8B	Data	Not settable
This records the IC-LV RMS measurement				
IA-TV RMS	02	8C	Data	Not settable
P643 and P645 only. This records the IA-TV RMS measurement				
IB-TV RMS	02	8D	Data	Not settable

Menu Text	Col	Row	Default Setting	Available Setting
Description				
P643 and P645 only. This records the IB-TV RMS measurement				
IC-TV RMS	02	8E	Data	Not settable
P643 and P645 only. This records the IC-TV RMS measurement				
VAN Magnitude	02	8F	Data	Not settable
P643, P645 and P746 only. This records the VAN Magnitude measurement				
VAN Phase Angle	02	90	Data	Not settable
P643, P645 and P746 only. This records the VAN Phase Angle measurement				
VBN Magnitude	02	91	Data	Not settable
P643, P645 and P746 only. This records the VBN Magnitude measurement				
VBN Phase Angle	02	92	Data	Not settable
P643, P645 and P746 only. This records the VBN Phase Angle measurement				
VCN Magnitude	02	93	Data	Not settable
P643, P645 and P746 only. This records the VCN Magnitude measurement				
VCN Phase Angle	02	94	Data	Not settable
P643, P645 and P746 only. This records the VCN Phase Angle measurement				
Vx Magnitude	02	95	Data	Not settable
This records the Vx Magnitude measurement				
Vx Phase Angle	02	96	Data	Not settable
This records the Vx Phase Angle measurement				
V1 Magnitude	02	97	Data. Positive sequence Voltage	Not settable
This records the V1 Magnitude measurement				
V2 Magnitude	02	98	Data Negative sequence Voltage	Not settable
This records the V2 Magnitude measurement				
V0 Magnitude	02	99	Data Zero sequence voltage	Not settable
P643, P645 and P746 only. This records the V0 Magnitude measurement				
VN Derived Mag	02	9A	Data	Not settable
P643, P645 and P746 only. This records the VN Derived Mag measurement				
VN Derived Angle	02	9B	Data	Not settable
P643, P645 and P746 only. This records the VN Derived Angle measurement				
VAB Magnitude	02	9C	Data	Not settable
This records the VAB Magnitude measurement				
VAB Phase Angle	02	9D	Data	Not settable
This records the VAB Phase Angle measurement				
VBC Magnitude	02	9E	Data	Not settable
This records the VBC Magnitude measurement				
VBC Phase Angle	02	9F	Data	Not settable

Menu Text	Col	Row	Default Setting	Available Setting
Description				
This records the VBC Phase Angle measurement				
VCA Magnitude	02	A0	Data	Not settable
This records the VCA Magnitude measurement				
VCA Phase Angle	02	A1	Data	Not settable
This records the VCA Phase Angle measurement				
VAN RMS	02	A2	Data	Not settable
P643, P645 and P746 only. This records the VAN RMS measurement				
VBN RMS	02	A3	Data	Not settable
P643, P645 and P746 only. This records the VBN RMS measurement				
VCN RMS	02	A4	Data	Not settable
P643, P645 and P746 only. This records the VCN RMS measurement				
Frequency	02	AA	Data	Not settable
This records the Frequency measurement				
IN-T1 Deriv Mag	02	AB	Data	Not settable
P642, P643 and P645 only. This records the IN-T1 Derived Mag measurement.				
IN-T1 Deriv Ang	02	AC	Data	Not settable
P642, P643 and P645 only. This records the IN-T1 Derived Ang measurement.				
IN-T2 Deriv Mag	02	AD	Data	Not settable
P642, P643 and P645 only. This records the IN-T2 Derived Mag measurement.				
IN-T2 Deriv Ang	02	AE	Data	Not settable
P642, P643 and P645 only. This records the IN-T2 Derived Ang measurement.				
IN-T3 Deriv Mag	02	AF	Data	Not settable
P643 and P645 only. This records the IN-T3 Derived Mag measurement.				
IN-T3 Deriv Ang	02	B0	Data	Not settable
P643 and P645 only. This records the IN-T3 Derived Ang measurement.				
IN-T4 Deriv Mag	02	B1	Data	Not settable
P645 only. This records the IN-T4 Derived Mag measurement.				
IN-T4 Deriv Ang	02	B2	Data	Not settable
P645 only. This records the IN-T4 Derived Ang measurement.				
IN-T5 Deriv Mag	02	B3	Data	Not settable
P645 only. This records the IN-T5 Derived Mag measurement.				
IN-T5 Deriv Ang	02	B4	Data	Not settable
P645 only. This records the IN-T5 Derived Ang measurement.				
IN-TN1 Mea Mag	02	B5	Data	Not settable

Menu Text	Col	Row	Default Setting	Available Setting
Description				
This records the IN-TN1 Mea Mag measurement				
IN-TN1 Mea Ang	02	B6	Data	Not settable
This records the IN-TN1 Mea Ang measurement				
IN-TN2 Mea Mag	02	B7	Data	Not settable
This records the IN-TN2 Mea Mag measurement				
IN-TN2 Mea Ang	02	B8	Data	Not settable
This records the IN-TN2 Mea Ang measurement				
IN-TN3 Mea Mag	02	B9	Data	Not settable
P643 and P645 only. This records the IN-TN3 Mea Mag measurement				
IN-TN3 Mea Ang	02	BA	Data	Not settable
P643 and P645 only. This records the IN-TN3 Mea Ang measurement				

Table 24 - Measurements 1 settings

5.4 Measurements 2

This menu provides measurement information.

Menu Text	Col	Row	Default Setting	Available Setting
Description				
MEASUREMENTS 2	03	00		
P643 and P645 only. Measurement 2 Group.				
A Phase Watts	03	01	Data	Not settable
P643 and P645 only. This records the A Phase Watts measurement				
A Phase Watts	03	02	Data	Not settable
P643 and P645 only. This records the A Phase Watts measurement				
A Phase Watts	03	03	Data	Not settable
P643 and P645 only. This records the A Phase Watts measurement				
B Phase Watts	03	04	Data	Not settable
P643 and P645 only. This records the B Phase Watts measurement				
B Phase Watts	03	05	Data	Not settable
P643 and P645 only. This records the B Phase Watts measurement				
B Phase Watts	03	06	Data	Not settable
P643 and P645 only. This records the B Phase Watts measurement				
C Phase Watts	03	07	Data	Not settable
P643 and P645 only. This records the C Phase Watts measurement				
C Phase Watts	03	08	Data	Not settable
P643 and P645 only. This records the C Phase Watts measurement				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
C Phase Watts	03	09	Data	Not settable
P643 and P645 only. This records the C Phase Watts measurement				
A Phase VArs	03	0A	Data	Not settable
P643 and P645 only. This records the A Phase VArs measurement				
A Phase VArs	03	0B	Data	Not settable
P643 and P645 only. This records the A Phase VArs measurement				
A Phase VArs	03	0C	Data	Not settable
P643 and P645 only. This records the A Phase VArs measurement				
B Phase VArs	03	0D	Data	Not settable
P643 and P645 only. This records the B Phase VArs measurement				
B Phase VArs	03	0E	Data	Not settable
P643 and P645 only. This records the B Phase VArs measurement				
B Phase VArs	03	0F	Data	Not settable
P643 and P645 only. This records the B Phase VArs measurement				
C Phase VArs	03	10	Data	Not settable
P643 and P645 only. This records the C Phase VArs measurement				
C Phase VArs	03	11	Data	Not settable
P643 and P645 only. This records the C Phase VArs measurement				
C Phase VArs	03	12	Data	Not settable
P643 and P645 only. This records the C Phase VArs measurement				
A Phase VA	03	13	Data	Not settable
P643 and P645 only. This records the A Phase VA measurement				
A Phase VA	03	14	Data	Not settable
P643 and P645 only. This records the A Phase VA measurement				
A Phase VA	03	15	Data	Not settable
P643 and P645 only. This records the A Phase VA measurement				
B Phase VA	03	16	Data	Not settable
P643 and P645 only. This records the B Phase VA measurement				
B Phase VA	03	17	Data	Not settable
P643 and P645 only. This records the B Phase VA measurement				
B Phase VA	03	18	Data	Not settable
P643 and P645 only. This records the B Phase VA measurement				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
C Phase VA	03	19	Data	Not settable
P643 and P645 only. This records the C Phase VA measurement				
C Phase VA	03	1A	Data	Not settable
P643 and P645 only. This records the C Phase VA measurement				
C Phase VA	03	1B	Data	Not settable
P643 and P645 only. This records the C Phase VA measurement				
3 Phase Watts	03	1C	Data	Not settable
P643 and P645 only. This records the 3 Phase Watts measurement				
3 Phase Watts	03	1D	Data	Not settable
P643 and P645 only. This records the 3 Phase Watts measurement				
3 Phase Watts	03	1E	Data	Not settable
P643 and P645 only. This records the 3 Phase Watts measurement				
3 Phase VArs	03	1F	Data	Not settable
P643 and P645 only. This records the 3 Phase VArs measurement				
3 Phase VArs	03	20	Data	Not settable
P643 and P645 only. This records the 3 Phase VArs measurement				
3 Phase VArs	03	21	Data	Not settable
P643 and P645 only. This records the 3 Phase VArs measurement				
3 Phase VA	03	22	Data	Not settable
P643 and P645 only. This records the 3 Phase VA measurement				
3 Phase VA	03	23	Data	Not settable
P643 and P645 only. This records the 3 Phase VA measurement				
3 Phase VA	03	24	Data	Not settable
P643 and P645 only. This records the 3 Phase VA measurement				
3Ph Power Factor	03	25	Data	Not settable
P643 and P645 only. This records the 3Ph Power Factor measurement				
APh Power Factor	03	26	Data	Not settable
P643 and P645 only. This records the APh Power Factor measurement				
BPh Power Factor	03	27	Data	Not settable
P643 and P645 only. This records the BPh Power Factor measurement				
CPh Power Factor	03	28	Data	Not settable
P643 and P645 only. This records the CPh Power Factor measurement				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
3Ph WHours Fwd	03	29	Data	Not settable
P643 and P645 only. This records the 3Ph WHours Fwd measurement				
3Ph WHours Rev	03	2A	Data	Not settable
P643 and P645 only. This records the 3Ph WHours Rev measurement				
3Ph VArHours Fwd	03	2B	Data	Not settable
P643 and P645 only. This records the 3Ph VArHours Fwd measurement				
3Ph VArHours Rev	03	2C	Data	Not settable
P643 and P645 only. This records the 3Ph VArHours Rev measurement				
3Ph W Fix Demand	03	2D	Data	Not settable
P643 and P645 only. This records the 3Ph W Fix Demand measurement				
3Ph VArs Fix Dem	03	2E	Data	Not settable
P643 and P645 only. This records the 3Ph VArs Fix Dem measurement				
3 Ph W Roll Dem	03	2F	Data	Not settable
P643 and P645 only. This records the 3 Ph W Roll Dem measurement				
3Ph VArs RollDem	03	30	Data	Not settable
P643 and P645 only. This records the 3Ph VArs RollDem measurement				
3Ph W Peak Dem	03	31	Data	Not settable
P643 and P645 only. This records the 3Ph W Peak Dem measurement				
3Ph VAr Peak Dem	03	32	Data	Not settable
P643 and P645 only. This records the 3Ph VAr Peak Dem measurement				
Reset Demand	03	50	No	No or Yes
P643 and P645 only. Reset Demand				

Table 25 - Measurements 2 settings

5.5 Measurements 3

This menu provides measurement information.

Menu Text	Col	Row	Default Setting	Available Setting
Description				
MEASUREMENTS 3	04	00		
P643 and P645 only. Measurement 3 Group.				
IA Differential	04	01	Data	Not settable
This records the IA Differential measurement				
IB Differential	04	02	Data	Not settable
This records the IB Differential measurement				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
IC Differential	04	03	Data	Not settable
This records the IC Differential measurement				
IA Bias	04	04	Data	Not settable
This records the IA Bias measurement				
IB Bias	04	05	Data	Not settable
This records the IB Bias measurement				
IC Bias	04	06	Data	Not settable
This records the IC Bias measurement				
IA Diff 2H	04	07	Data	Not settable
This records the IA Diff 2H measurement				
IB Diff 2H	04	08	Data	Not settable
This records the IB Diff 2H measurement				
IC Diff 2H	04	09	Data	Not settable
This records the IC Diff 2H measurement				
IA Diff 5H	04	0A	Data	Not settable
This records the IA Diff 5H measurement				
IB Diff 5H	04	0B	Data	Not settable
This records the IB Diff 5H measurement				
IC Diff 5H	04	0C	Data	Not settable
This records the IC Diff 5H measurement				
IREF HV LoZ Diff	04	0D	Data	Not settable
This records the IREF HV LoZ Diff measurement				
IREF HV LoZ Bias	04	0E	Data	Not settable
This records the IREF HV LoZ Bias measurement				
IREF LV LoZ Diff	04	0F	Data	Not settable
This records the IREF LV LoZ Diff measurement				
IREF LV LoZ Bias	04	10	Data	Not settable
This records the IREF LV LoZ Bias measurement				
IREF TV LoZ Diff	04	11	Data.	Not settable
P643 and P645 only. This records the IREF TV LoZ Diff measurement				
IREF TV LoZ Bias	04	12	Data	Not settable
P643 and P645 only. This records the IREF TV LoZ Bias measurement				
IREF Auto LoZ Diff	04	13	Data	Not settable
This records the IREF Auto LoZ Diff measurement				
IREF Auto LoZ Bias	04	14	Data	Not settable
This records the IREF Auto LoZ Bias measurement				
IREF HV HighZ Op	04	15	Data	Not settable
This records the HV High measurement				
IREF LV HighZ Op	04	16	Data	Not settable
This records the LV HighZ measurement				
IREF TV HighZ Op	04	17	Data	Not settable

Menu Text	Col	Row	Default Setting	Available Setting
Description				
P643 and P645 only. This records the IREF TV HighZ Operation measurement				
IREF Auto HighZ Op	04	18	Data	Not settable
This records the IREF Auto measurement				
Thermal Overload	04	27	Sub-Heading	Sub-Heading
Sub-Heading				
Hot Spot T	04	28	Data	Not settable
This records the Hot Spot T measurement				
Top Oil T	04	2A	Data	Not settable
This records the Top Oil T measurement				
Reset Thermal	04	2B	No	No or Yes
Reset Thermal Overload command. Resets thermal state to 0.				
Ambient T	04	2C	Data	Not settable
This records the Ambient T measurement				
TOL Pretrip left	04	2D	Data	Not settable
Thermal OverLoad pre-trip time left. This records the TOL Pretrip left measurement				
LOL status	04	2F	Data	Not settable
Accumulated Loss Of Life. Invisible only when the turbine abnormal frequency protection is not enabled.				
Reset LOL	04	30	No	No or Yes
Reset Loss Of Life (LOL) command. Resets state to 0.				
Rate of LOL	04	31	Data	Not settable
This records the Rate of LOL (ROLOL) measurement				
LOL Aging Factor	04	32	Data	Not settable
Aging Acceleration Factor (FAA). This records the LOL Aging Factor measurement				
Lres at designed	04	33	Data	Not settable
Residual life hours at design temperature QH,r. This records the Lres at designed measurement				
FAA,m	04	34	Data	Not settable
Mean Aging Acceleration Factor (FAA,m). This records the FAA,m measurement				
Lres at FAA,m	04	35	Data	Not settable
Residual life hours at FAA,m (LRES(FAA,m)). This records the Lres at FAA,m measurement				
Volts/Hz	04	38	Sub-Heading	Sub-Heading
Sub-Heading				
Volts/Hz W1	04	39	Data	Not settable
P643 and P645 only. This records the Volts/Hz W1 measurement				
V/Hz W1 tPretrip	04	3A	Data	Not settable
P643 and P645 only. This records the V/Hz W1 tPretrip measurement				
V/Hz W1 Thermal	04	3B	Data	Not settable
P643 and P645 only. This records the V/Hz W1 Thermal measurement				
Reset V/Hz W1	04	3C	No	No or Yes
P643 and P645 only. Reset V/Hz W1				
Volts/Hz W2	04	3D	Data	Not settable

Menu Text	Col	Row	Default Setting	Available Setting
Description				
This records the Volts/Hz W2 measurement				
V/Hz W2 tPretrip	04	3E	Data	Not settable
This records the V/Hz W2 tPretrip measurement				
V/Hz W2 Thermal	04	3F	Data	Not settable
This records the V/Hz W2 Thermal measurement				
Reset V/Hz W2	04	40	No	No or Yes
Reset V/Hz W2				
RTD 1 label	04	60	Data	Not settable
This records the RTD 1 label measurement				
RTD 2 label	04	61	Data	Not settable
This records the RTD 2 label measurement				
RTD 3 label	04	62	Data	Not settable
This records the RTD 3 label measurement				
RTD 4 label	04	63	Data	Not settable
This records the RTD 4 label measurement				
RTD 5 label	04	64	Data	Not settable
This records the RTD 5 label measurement				
RTD 6 label	04	65	Data	Not settable
This records the RTD 6 label measurement				
RTD 7 label	04	66	Data	Not settable
This records the RTD 7 label measurement				
RTD 8 label	04	67	Data	Not settable
This records the RTD 8 label measurement				
RTD 9 label	04	68	Data	Not settable
This records the RTD 9 label measurement				
RTD 10 label	04	69	Data	Not settable
This records the RTD 10 label measurement				
RTD Open Cct	04	6A	0000000000	Not settable
Displays the status of the eight RTDs as a binary string. 0 = No Open Circuit, 1 = Open Circuit. The Open Cct alarms are latched.				
RTD Short Cct	04	6B	0000000000	Not settable
Displays the status of the eight RTDs as a binary string. 0 = No Short Circuit, 1 = Short Circuit. The Short Cct alarms are latched.				
RTD Data Error	04	6C	0000000000	Not settable
Displays the status of the eight RTDs as a binary string. 0 = No Data Error, 1 = Data Error. The Data Error alarms are latched.				
Reset RTD Flags	04	6D	No	No or Yes
Reset RTD alarms command. Resets latched RTD Open Cct, Short Cct, Data Error alarms.				
CLIO Input 1	04	70	Data	Not settable
This records the CLIO Input 1 measurement				
CLIO Input 2	04	71	Data	Not settable
This records the CLIO Input 2 measurement				
CLIO Input 3	04	72	Data	Not settable
This records the CLIO Input 3 measurement				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
CLIO Input 4	04	73	Data	Not settable
This records the CLIO Input 4 measurement				

Table 26 - Measurements 3 settings

5.6 Date and Time

Displays the date and time as well as the battery condition.

Menu Text	Col	Row	Default Setting	Available Setting
Description				
DATE AND TIME	08	00		
This column contains DATE AND TIME parameters.				
Date/Time	08	01		
Displays the relay's date and time				
Date 12/01/1998	08	N/A		<Date>
Displays the relay's date				
Time 12:00:00	08	N/A		<Time>
Displays the relay's time				
IRIG-B Sync	08	04	Disabled	Enabled or Disabled
Enables or disables the IRIG-B time synchronization				
IRIG-B Status	08	05		Card not fitted, Card failed, signal healthy or No signal
Displays the status of IRIG-B				
Battery Status	08	06		Dead or Healthy
Displays whether the battery is healthy or not				
Battery Alarm	08	07	Enabled	Enabled or Disabled
Enables or disables battery alarm. The battery alarm needs to be disabled when a battery is removed or not used				
SNTP Status	08	13		Disabled, Trying Server1, Trying Server 2, Server 1 OK, Server 2 OK, No response or No Valid Clock
Displays information about the SNTP time synchronization status				
LocalTime Enable	08	20	Flexible	Disabled, Fixed or Flexible
LocalTime Enable				
LocalTime Offset	08	21	0	-720 mins to +720 mins step 15 mins
LocalTime Offset				
DST Enable	08	22	Enabled	Enabled or Disabled
Daylight Saving Time(DST) Enbale				
DST Offset	08	23	60	30 mins to 60 mins step 30mins
DST Offset				
DST Start	08	24	Last	First, Second, Third, Fourth or Last
DST Start				
DST Start Day	08	25	Sunday	Monday, Tuesday, Wednesday, Thursday, Friday, Saturday or Sunday

Menu Text	Col	Row	Default Setting	Available Setting
Description				
DST Start Day				
DST Start Month	08	26	March	Any of the 12 months
DST Start Month				
DST Start Mins	08	27	60	0mins to 1425 mins step 15mins
DST Start Mins				
DST End	08	28	Last	First, Second, Third, Fourth or Last
DST End				
DST End Day	08	29	Sunday	Monday, Tuesday, Wednesday, Thursday, Friday, Saturday or Sunday
DST End Day				
DST End Month	08	2A	October	Any of the 12 months
DST End Month				
DST End Mins	08	2B	60	0mins to 1425 mins step 15mins
DST End Mins				
RP1 Time Zone	08	30	UTC	UTC or Local
RP1 Time Zone				
RP2 Time Zone	08	31	UTC	UTC or Local
RP2 Time Zone				
DNPOE Time Zone	08	32	UTC	UTC or Local
DNPOE Time Zone				
Tunnel Time Zone	08	33	UTC	UTC or Local
Tunnel Time Zone				
1588 Sync	08	40	DISABLE	0 = Disabled or 1 = Intfc 1 Enabled or 2 = Intfc 2 Enabled or 3 = Intfc 1 & 2 Enabled
The setting that indicate the 1588 enable or the Intfc 1,Intfc 2 OR Both.				
1588 DomainNum	08	41	0	0 to 255 step 1
The domian number of 1588 which define the scope of PTP message communication, state, operations, data sets, and timescale.				
1588 PdelInterv	08	42	0	From 0 to 5 step 1
The initialization value is implementation-specific consistent				
1588 KP	08	43	1.2	From 0 to 5 step 0.01
The coefficient Kp value that use calculate the sync time				
1588 Status	08	50		Not Settable
Indication the status of 1588				
InterfaceNum	08	51		Not Settable
The value of the port number				
OffsetFromMaster	08	52		Not Settable
An implementation-specific representation of the current value of the time difference between a master and a slave as computed by the slave				
PeerMeanPDelay	08	53		Not Settable
An estimate of the current one-way propagation delay on the link				
StepsRemoved	08	54		Not Settable
The number of communication paths traversed between the local clock and the grandmaster clock.				
ParentClockId	08	55		Not Settable

Menu Text	Col	Row	Default Setting	Available Setting
Description				
The clock clockIdentity of the parent clock.				
ParentPortNum	08	56		Not Settable
The value of parent port number				
ParentClockClass	08	57		Not Settable
The parent clock class which is the attribute defining a clock's TAI traceability				
ParentClockAcc	08	58		Not Settable
The parent clock accuracy which is the attribute defining the accuracy of a clock				
ParentClockVar	08	59		Not Settable
The parent clock variance which is the attribute defining the stability of a clock				
ParentPriority1	08	5A		Not Settable
A user configurable designation that a clock belongs to an ordered set of clocks from which a master is selected				
ParentPriority2	08	5B		Not Settable
A user configurable designation that provides finer grained ordering among otherwise equivalent clocks				

Table 27 - Date and time settings

5.7 CT and VT Ratios

Menu Text	Col	Row	Default Setting	Available Setting
Description				
CT AND VT RATIOS	0A	00		
This column contains CT AND VT RATIOS parameter values for multipliers used elsewhere				
Main VT Location	0A	01	HV/LV/TV	HV, LV or TV
SMF for P643 and P645 only. Sets main VT location				
Aux' VT Location	0A	02	HV	HV or LV
P642 only. Sets Auxiliary VT Location				
Main VT Primary	0A	03	110	100V to 1MV step 1V
P643 and P645 only. Main voltage transformer input, primary voltage setting				
Main VT Sec'y	0A	04	110	0*V1 to 140*V1 step 1*V1
P643 and P645 only. Main voltage transformer input, secondary voltage setting				
Aux' VT Primary	0A	07	110	100V to 1MV step 1V
Single phase VT primary voltage used for W2 overfluxing				
Aux' VT Sec'y	0A	08	110	0*V1 to 140*V1 step 1*V1
Single phase VT secondary voltage used for W2 overfluxing				
T1 CT	0A	10	Sub-Heading	Sub-Heading
Terminal 1 CT				
Polarity	0A	11	Standard	Standard or Inverted
Polarity with respect to the other CTs				
Primary	0A	12	300	1A to 60000A step 1A
CT primary nominal current				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
Secondary	0A	13	1	1A to 5A step 4A
Secondary				
T2 CT	0A	14	Sub-Heading	Sub-Heading
Terminal 2 CT				
Polarity	0A	15	Standard	Standard or Inverted
Polarity with respect to the other CTs				
Primary	0A	16	300	1A to 60000A step 1A
CT primary nominal current				
Secondary	0A	17	1	1A to 5A step 4A
Secondary				
T3 CT	0A	18	Sub-Heading	Sub-Heading
P643, P645 and P746 only. Terminal 3 CT				
Polarity	0A	19	Standard	Standard or Inverted
P643, P645 and P746 only. Polarity with respect to the other CTs				
Primary	0A	1A	300	1A to 60000A step 1A
P643 and P645 only. CT primary nominal current				
Secondary	0A	1B	1	1A to 5A step 4A
P643, P645 and P746 only. CT secondary nominal current				
T4 CT	0A	1C	Sub-Heading	Sub-Heading
P645 and P746 only. Terminal 4 CT				
Polarity	0A	1D	Standard	Standard or Inverted
P645 and P746 only. Polarity with respect to the other CTs				
Primary	0A	1E	300	1A to 60000A step 1A
P645 only. CT primary nominal current				
Secondary	0A	1F	1	1A to 5A step 4A
P645 and P746 only. CT secondary nominal current				
T5 CT	0A	20	Sub-Heading	Sub-Heading
P645 and P746 only. Terminal 5 CT				
Polarity	0A	21	Standard	Standard or Inverted
P645 and P746 only. Polarity with respect to the other CTs				
Primary	0A	22	300	1A to 60000A step 1A
P645 only. CT primary nominal current				
Secondary	0A	23	1	1A to 5A step 4A
P645 and P746 only. CT secondary nominal current				
TN1 CT	0A	58	Sub-Heading	Sub-Heading

Menu Text	Col	Row	Default Setting	Available Setting
Description				
HV E/F CT				
Polarity	0A	59	Standard	Standard or Inverted
Polarity with respect to the other CTs				
Primary	0A	5A	300	1A to 60000A step 1A
Earth fault CT primary nominal current				
Secondary	0A	5B	1	1A to 5A step 4A
Earth fault CT secondary nominal current				
TN2 CT	0A	5D	Sub-Heading	Sub-Heading
LV E/F CT				
Polarity	0A	5E	Standard	Standard or Inverted
Polarity with respect to the other CTs				
Primary	0A	5F	300	1A to 60000A step 1A
Earth fault CT primary nominal current				
Secondary	0A	60	1	1A to 5A step 4A
Earth fault CT secondary nominal current				
TN3 CT	0A	62	Sub-Heading	Sub-Heading
P643 and P645 only. TV E/F CT				
Polarity	0A	63	Standard	Standard or Inverted
P643 and P645 only. Polarity with respect to the other CTs				
Primary	0A	64	300	1A to 60000A step 1A
P643 and P645 only. Earth fault CT primary nominal current				
Secondary	0A	65	1	1A to 5A step 4A
P643 and P645 only. Earth fault CT secondary nominal current				

Table 28 - CT and VT ratio settings

5.8 Record Control

It is possible to disable the reporting of events from all interfaces that support setting changes. The settings that control the various types of events are in the Record Control column. The effect of setting each to disabled is as follows:

Menu Text	Col	Row	Default Setting	Available Setting
Description				
RECORD CONTROL	0B	00		
This column contains RECORD CONTROL parameter				
Clear Events	0B	01	No	0 = No or 1 = Yes
Clear Event records				
Clear Faults	0B	02	No	0 = No or 1 = Yes
Clear Fault records				
Clear Maint	0B	03	No	0 = No or 1 = Yes
Clear Maintenance records				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
Alarm Event	0B	04	Enabled	Enabled or Disabled
Disabling this setting means that no event is generated for all alarms				
Relay O/P Event	0B	05	Enabled	Enabled or Disabled
Disabling this setting means that no event is generated for any change in relay output contact state				
Opto Input Event	0B	06	Enabled	Enabled or Disabled
Disabling this setting means that no event is generated for any change in logic input state				
General Event	0B	07	Enabled	Enabled or Disabled
Disabling this setting means that no General Events is generated				
Fault Rec Event	0B	08	Enabled	Enabled or Disabled
Disabling this setting means that no event is generated for any fault that produces a fault record.				
Maint Rec Event	0B	09	Enabled	Enabled or Disabled
Disabling this setting means that no event is generated for any maintenance records				
Protection Event	0B	0A	Enabled	Enabled or Disabled
Disabling this setting means that no event is generated for any operation of the protection elements				
Clear Dist Recs	0B	30	No	0 = No or 1 = Yes
Clear Disturbance records				
Security Event	0B	31	Enabled	Enabled or Disabled
Disabling this setting means that any operation of security elements will not be logged as an event				
DDB 31 - 0	0B	40	0xFFFFFFFF	32-bit binary setting
Digital Data Bus (DDB) 1 = event recording Enabled, 0 = event recording Disabled				
DDB 63 - 32	0B	41	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 63 - 32 instead				
DDB 95 - 64	0B	42	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 95 - 64 instead				
DDB 127 - 96	0B	43	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 127 - 96 instead				
DDB 159 - 128	0B	44	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 159 - 128 instead				
DDB 191 - 160	0B	45	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 191 - 160 instead				
DDB 223 - 192	0B	46	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 223 - 192 instead				
DDB 255 - 224	0B	47	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 255 - 224 instead				
DDB 287 - 256	0B	48	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 287 - 256 instead				
DDB 319 - 288	0B	49	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 319 - 288 instead				
DDB 351 - 320	0B	4A	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 351 - 320 instead				
DDB 383 - 352	0B	4B	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 383 - 352 instead				
DDB 415 - 384	0B	4C	0xFFFFFFFF	32-bit binary setting

Menu Text	Col	Row	Default Setting	Available Setting
Description				
This setting works in the same way as DDB 31 - 0 but for DDB 415 - 384 instead				
DDB 447 - 416	0B	4D	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 447 - 416 instead				
DDB 479 - 448	0B	4E	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 479 - 448 instead				
DDB 511 - 480	0B	4F	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 511 - 480 instead				
DDB 543 - 512	0B	50	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 543 - 512 instead				
DDB 575 - 544	0B	51	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 575 - 544 instead				
DDB 607 - 576	0B	52	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 607 - 576 instead				
DDB 639 - 608	0B	53	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 639 - 608 instead				
DDB 671 - 640	0B	54	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 671 - 640 instead				
DDB 703 - 672	0B	55	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 703 - 672 instead				
DDB 735 - 704	0B	56	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 735 - 704 instead				
DDB 767 - 736	0B	57	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 767 - 736 instead				
DDB 799 - 768	0B	58	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 799 - 768 instead				
DDB 831 - 800	0B	59	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 831 - 800 instead				
DDB 863 - 832	0B	5A	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 863 - 832 instead				
DDB 895 - 864	0B	5B	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 895 - 864 instead				
DDB 927 - 896	0B	5C	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 927 - 896 instead				
DDB 959 - 928	0B	5D	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 959 - 928 instead				
DDB 991 - 960	0B	5E	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 991 - 960 instead				
DDB 1023 - 992	0B	5F	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1023 - 992 instead				
DDB 1055-1024	0B	60	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1055-1024 instead				
DDB 1087-1056	0B	61	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1087-1056 instead				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
DDB 1119-1088	0B	62	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1119-1088 instead				
DDB 1151-1120	0B	63	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1151-1120 instead				
DDB 1183-1152	0B	64	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1183-1152 instead				
DDB 1215-1184	0B	65	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1215-1184 instead				
DDB 1247-1216	0B	66	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1247-1216 instead				
DDB 1279-1248	0B	67	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1279-1248 instead				
DDB 1311-1280	0B	68	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1311-1280 instead				
DDB 1343-1312	0B	69	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1343-1312 instead				
DDB 1375-1344	0B	6A	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1375-1344 instead				
DDB 1407-1376	0B	6B	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1407-1376 instead				
DDB 1439-1408	0B	6C	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1439-1408 instead				
DDB 1471-1440	0B	6D	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1471-1440 instead				
DDB 1503-1472	0B	6E	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1503-1472 instead				
DDB 1535-1504	0B	6F	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1535-1504 instead				
DDB 1567-1536	0B	70	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1567-1536 instead				
DDB 1599-1568	0B	71	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1599-1568 instead				
DDB 1631-1600	0B	72	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1631-1600 instead				
DDB 1663-1632	0B	73	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1663-1632 instead				
DDB 1695-1664	0B	74	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1695-1664 instead				
DDB 1727-1696	0B	75	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1727-1696 instead				
DDB 1759-1728	0B	76	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1759-1728 instead				
DDB 1791-1760	0B	77	0xFFFFFFFF	32-bit binary setting

Menu Text	Col	Row	Default Setting	Available Setting
Description				
This setting works in the same way as DDB 31 - 0 but for DDB 1791-1760 instead				
DDB 1823-1792	0B	78	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1823-1792 instead				
DDB 1855-1824	0B	79	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1855-1824 instead				
DDB 1887-1856	0B	7A	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1887-1856 instead				
DDB 1919-1888	0B	7B	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1919-1888 instead				
DDB 1951-1920	0B	7C	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1951-1920 instead				
DDB 1983-1952	0B	7D	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1983-1952 instead				
DDB 2015-1984	0B	7E	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 2015-1984 instead				
DDB 2047-2016	0B	7F	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 2047-2016 instead				

Table 29 - Record control settings

5.9 Disturbance Recorder Settings

The disturbance recorder settings include the record duration and trigger position, selection of analog and digital signals to record, and the signal sources that trigger the recording.

The precise event recorder column (“Disturb. Recorder” menu) is visible when the “Disturb recorder” setting (“Configuration” column) = “visible”.

Menu Text	Col	Row	Default Setting	Available Setting
Description				
DISTURB RECORDER	0C	00		
This column contains DISTURBANCE RECORDER paramaters				
Duration	0C	52	1.5	0.1s to 10.5s step 0.01s
Overall recording time setting				
Trigger Position	0C	54	33.3	0% to 100% step 0.1%
Trigger point setting as a percentage of the duration. For example, the default settings show the overall recording time is set to 1.5 s with the trigger point being at 33.3% of this, giving 0.5 s pre-fault and 1 s post fault recording times				
Trigger Mode	0C	56	Single	Single or Extended
If set to single mode, and if a further trigger occurs while a recording is taking place, the recorder ignores the trigger. However, if this is set to Extended, the post trigger timer is reset to zero, extending the recording time				
Analog Channel 1	0C	58	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
Selects any available analog input to be assigned to this channel				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
Analog Channel 2	0C	59	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
This works in the same way as Analog Channel 1 but for Analog Channel 2 instead.				
Analog Channel 3	0C	5A	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
This works in the same way as Analog Channel 1 but for Analog Channel 3 instead.				
Analog Channel 4	0C	5B	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
This works in the same way as Analog Channel 1 but for Analog Channel 4 instead.				
Analog Channel 5	0C	5C	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
This works in the same way as Analog Channel 1 but for Analog Channel 5 instead.				
Analog Channel 6	0C	5D	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
This works in the same way as Analog Channel 1 but for Analog Channel 6 instead.				
Analog Channel 7	0C	5E	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
This works in the same way as Analog Channel 1 but for Analog Channel 7 instead.				
Analog Channel 8	0C	5F	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
This works in the same way as Analog Channel 1 but for Analog Channel 8 instead.				
Analog Channel 9	0C	60	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC

Menu Text	Col	Row	Default Setting	Available Setting
Description				
This works in the same way as Analog Channel 1 but for Analog Channel 9 instead.				
AnalogChannel 10	0C	61	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
This works in the same way as Analog Channel 1 but for AnalogChannel 10 instead.				
AnalogChannel 11	0C	62	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
This works in the same way as Analog Channel 1 but for AnalogChannel 11 instead.				
AnalogChannel 12	0C	63	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
This works in the same way as Analog Channel 1 but for AnalogChannel 12 instead.				
AnalogChannel 13	0C	64	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
This works in the same way as Analog Channel 1 but for AnalogChannel 13 instead.				
AnalogChannel 14	0C	65	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
This works in the same way as Analog Channel 1 but for AnalogChannel 14 instead.				
AnalogChannel 15	0C	66	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
This works in the same way as Analog Channel 1 but for AnalogChannel 15 instead.				
AnalogChannel 16	0C	67	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
This works in the same way as Analog Channel 1 but for AnalogChannel 16 instead.				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
AnalogChannel 17	0C	68	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
This works in the same way as Analog Channel 1 but for AnalogChannel 17 instead.				
AnalogChannel 18	0C	69	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
This works in the same way as Analog Channel 1 but for AnalogChannel 18 instead.				
AnalogChannel 19	0C	6A	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
This works in the same way as Analog Channel 1 but for AnalogChannel 19 instead.				
AnalogChannel 20	0C	6B	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
P643, P645 and P746 only. This works in the same way as Analog Channel 1 but for AnalogChannel 20 instead.				
AnalogChannel 21	0C	6C	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
P643, P645 and P746 only. This works in the same way as Analog Channel 1 but for AnalogChannel 21 instead.				
AnalogChannel 22	0C	6D	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
P643 and P645 only. This works in the same way as Analog Channel 1 but for AnalogChannel 22 instead.				
AnalogChannel 23	0C	6E	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
P643 and P645 only. This works in the same way as Analog Channel 1 but for AnalogChannel 23 instead.				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
AnalogChannel 24	0C	6F	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
P643 and P645 only. This works in the same way as Analog Channel 1 but for AnalogChannel 24 instead.				
AnalogChannel 25	0C	70	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
P643 and P645 only. This works in the same way as Analog Channel 1 but for AnalogChannel 25 instead.				
AnalogChannel 26	0C	71	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
P643 and P645 only. This works in the same way as Analog Channel 1 but for AnalogChannel 26 instead.				
AnalogChannel 27	0C	72	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
P645 only. This works in the same way as Analog Channel 1 but for AnalogChannel 27 instead.				
AnalogChannel 28	0C	73	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
P645 only. This works in the same way as Analog Channel 1 but for AnalogChannel 28 instead.				
AnalogChannel 29	0C	74	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
P645 only. This works in the same way as Analog Channel 1 but for AnalogChannel 29 instead.				
AnalogChannel 30	0C	75	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC

Menu Text	Col	Row	Default Setting	Available Setting
Description				
P645 only. This works in the same way as Analog Channel 1 but for AnalogChannel 30 instead.				
Digital Input 1	0C	80	Output R1	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
The digital channels can be mapped to any of the opto isolated inputs or output contacts, in addition to several internal relay digital signals such as protection starts and LEDs				
Input 1 Trigger	0C	81	No Trigger	No trigger, Trigger L/H or Trigger H/L
Any of the digital channels can be selected to trigger the disturbance recorder on either a low-to-high (L/H) or a high-to-low (H/L) transition				
Digital Input 2	0C	82	Output R2	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 2 instead.				
Input 2 Trigger	0C	83	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 2 Trigger instead.				
Digital Input 3	0C	84	Output R3	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 3 instead.				
Input 3 Trigger	0C	85	Trigger L/H	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 3 Trigger instead.				
Digital Input 4	0C	86	Output R4	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 4 instead.				
Input 4 Trigger	0C	87	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 4 Trigger instead.				
Digital Input 5	0C	88	Output R5	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 5 instead.				
Input 5 Trigger	0C	89	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 5 Trigger instead.				
Digital Input 6	0C	8A	Output R6	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 6 instead.				
Input 6 Trigger	0C	8B	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 6 Trigger instead.				
Digital Input 7	0C	8C	Output R7	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 7 instead.				
Input 7 Trigger	0C	8D	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 7 Trigger instead.				
Digital Input 8	0C	8E	Output R8	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 8 instead.				
Input 8 Trigger	0C	8F	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 8 Trigger instead.				
Digital Input 9	0C	90	Output R9	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals

Menu Text	Col	Row	Default Setting	Available Setting
Description				
This works in the same way as Digital Input 1 but for Digital Input 9 instead.				
Input 9 Trigger	0C	91	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 9 Trigger instead.				
Digital Input 10	0C	92	Input L3	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 10 instead.				
Input 10 Trigger	0C	93	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 10 Trigger instead.				
Digital Input 11	0C	94	Input L4	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 11 instead.				
Input 11 Trigger	0C	95	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 11 Trigger instead.				
Digital Input 12	0C	96	Input L5	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 12 instead.				
Input 12 Trigger	0C	97	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 12 Trigger instead.				
Digital Input 13	0C	98	Input L6	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 13 instead.				
Input 13 Trigger	0C	99	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 13 Trigger instead.				
Digital Input 14	0C	9A	Input L7	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 14 instead.				
Input 14 Trigger	0C	9B	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 14 Trigger instead.				
Digital Input 15	0C	9C	Input L8	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 15 instead.				
Input 15 Trigger	0C	9D	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 15 Trigger instead.				
Digital Input 16	0C	9E	Unused	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 16 instead.				
Input 16 Trigger	0C	9F	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 16 Trigger instead.				
Digital Input 17	0C	A0	Unused	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 17 instead.				
Input 17 Trigger	0C	A1	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 17 Trigger instead.				
Digital Input 18	0C	A2	Unused	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals

Menu Text	Col	Row	Default Setting	Available Setting
Description				
This works in the same way as Digital Input 1 but for Digital Input 18 instead.				
Input 18 Trigger	0C	A3	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 18 Trigger instead.				
Digital Input 19	0C	A4	Unused	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 19 instead.				
Input 19 Trigger	0C	A5	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 19 Trigger instead.				
Digital Input 20	0C	A6	Unused	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 20 instead.				
Input 20 Trigger	0C	A7	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 20 Trigger instead.				
Digital Input 21	0C	A8	Unused	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 21 instead.				
Input 21 Trigger	0C	A9	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 21 Trigger instead.				
Digital Input 22	0C	AA	Unused	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 22 instead.				
Input 22 Trigger	0C	AB	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 22 Trigger instead.				
Digital Input 23	0C	AC	Unused	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 23 instead.				
Input 23 Trigger	0C	AD	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 23 Trigger instead.				
Digital Input 24	0C	AE	Unused	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 24 instead.				
Input 24 Trigger	0C	AF	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 24 Trigger instead.				
Digital Input 25	0C	B0	Unused	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 25 instead.				
Input 25 Trigger	0C	B1	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 25 Trigger instead.				
Digital Input 26	0C	B2	Unused	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 26 instead.				
Input 26 Trigger	0C	B3	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 26 Trigger instead.				
Digital Input 27	0C	B4	Unused	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals

Menu Text	Col	Row	Default Setting	Available Setting
Description				
This works in the same way as Digital Input 1 but for Digital Input 27 instead.				
Input 27 Trigger	0C	B5	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 27 Trigger instead.				
Digital Input 28	0C	B6	Unused	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
P746 only. This works in the same way as Digital Input 1 but for Digital Input 28 instead.				
Input 28 Trigger	0C	B7	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 28 Trigger instead.				
Digital Input 29	0C	B8	Unused	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 29 instead.				
Input 29 Trigger	0C	B9	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 29 Trigger instead.				
Digital Input 30	0C	BA	Unused	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 30 instead.				
Input 30 Trigger	0C	BB	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 30 Trigger instead.				
Digital Input 31	0C	BC	Unused	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 31 instead.				
Input 31 Trigger	0C	BD	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 31 Trigger instead.				
Digital Input 32	0C	BE	Unused	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 32 instead.				
Input 32 Trigger	0C	BF	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 32 Trigger instead.				

Table 30 - Disturbance recorder settings

5.10 Measurement Setup

Menu Text	Col	Row	Default Setting	Available Setting
Description				
MEASURE'T SETUP	0D	00		
This column contains MEASUREMENT SETTINGS				
Default Display	0D	01	User Banner	
Used to select the default display from a range of options				
Local Values	0D	02	Primary	Primary or Secondary
Controls whether measured local values from the rear communication port are displayed as primary or secondary quantities				
Remote Values	0D	03	Primary	Primary or Secondary
Controls whether measured remote values are displayed as primary or secondary quantities				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
Measurement Ref	0D	04	IA1	Vx, VA, VB, VC, IA1, IB1, IC1, IA2, IB2, IC2, IA3, IB3, IC3, IA4, IB4, IC4, IA5, IB5, IC5, VAB or VBC
Measurement Ref				
Measurement Mode	0D	05	0	0, 1, 2 or 3
This setting is used to control the signing of the real and reactive power quantities				

Table 31 - Measure't setup settings

5.11 Communications

The communications settings apply to the rear communications ports only and will depend upon the particular protocol being used. Further details are given in the SCADA Communications chapter.

Depending on the values stored, the available settings may change too. The applicability of each setting is given in the description or available setting cell. These settings are available in the menu '**Communications'** column and are displayed.

These settings potentially cover a variety of different protocols and ports, including:

- Courier
- MODBUS
- IEC60870-5-103
- DNP3.0

These can apply to the following ports:

- Ethernet Port
- Rear Port 2

Menu Text	Col	Row	Default Setting	Available Setting
Description				
COMMUNICATIONS	0E	00		
This column contains COMMUNICATIONS parameters				
RP1 Protocol	0E	01		<Protocol>
Indicates the communications protocol used on the rear communications port RP1				
RP1 Address	0E	02	255	0 to 255 (Courier)
Sets the relay address (protocol dependent). Build = Courier,Rear Port 1 Courier Protocol device address				
RP1 Address	0E	02	1	0 to 247 (Modbus)
Sets the relay address (protocol dependent). Build = Modbus Default Modbus address is 1,Rear Port 1 Modbus Protocol device address				
RP1 Address	0E	02	1	0 to 255 (IEC60870)
Sets the relay address (protocol dependent). Build = IEC60870-5-103,Rear Port 1 IEC60870-5-103 Protocol device address				
RP1 Address	0E	02	1	0 to 65534 (DNP3.0)
Sets the relay address (protocol dependent). Build=DNP 3.0,Rear Port 1 DNP 3.0 Protocol device address				
RP1 InactivTimer	0E	03	15	1 min to 30 min step 1 min (Courier)
Defines the period of inactivity before relay reverts to its default state. Build = Courier,Rear Port 1 Courier Protocol inactivity timer				
RP1 InactivTimer	0E	03	15	1 min to 30 min step 1 min (Modbus)

Menu Text	Col	Row	Default Setting	Available Setting
Description				
Defines the period of inactivity before relay reverts to its default state. Build = Modbus,Rear Port 1 Modbus Protocol inactivity timer				
RP1 InactivTimer	0E	03	15	1 min to 30 min step 1 min (IEC60870)
Defines the period of inactivity before relay reverts to its default state. Build = IEC60870-5-103,Rear Port 1 IEC60870-5-103 Protocol inactivity timer				
RP1 Baud Rate	0E	04	19200 bits/s	9600 bps, 19200 bps or 38400 bps (Modbus)
Defines the Baud rate for RP1. Build = Modbus,Rear Port 1 Modbus Protcol serial bit/baud rate				
RP1 Baud Rate	0E	04	19200 bits/s	9600 bps, 19200 bps or 38400 bps (IEC60870)
Defines the Baud rate for RP1. Build = IEC60870-5-103,Rear Port 1 IEC60870-5-103 Protcol serial bit/baud rate				
RP1 Baud Rate	0E	04	19200 bits/s	9600 bps, 19200 bps or 38400 bps (DNP3.0)
Defines the Baud rate for RP1. Build = DNP 3.0,Rear Port 1 DNP 3.0 Protcol serial bit/baud rate				
RP1 Parity	0E	05	None	Odd, Even or None (Modbus)
The parity type for error correction. Build = Modbus,Rear Port 1 Modbus Protocol parity				
RP1 Parity	0E	05	None	Odd, Even or None (DNP3.0)
The parity type for error correction. Build = DNP 3.0,Rear Port 1 DNP 3.0 Protocol parity				
RP1 Meas Period	0E	06	15	1s to 60s step 1s (IEC60870)
Defines the measurement period for the cyclic measurements. Build = IEC60870-5-103,Rear Port 1 IEC60870-5-103 Protocol measurement period				
RP1 PhysicalLink	0E	07	Copper	Copper, fiber Optic or Kbus
Defines whether an electrical EIA(RS)485, fiber optic or KBus connection is being used for communication between the master station and relay. If Fiber Optic is selected, the optional fiber optic communications board is required. Visible if ((CPU2 or (CPU1 and cs103)) and Fibre Optic Communications card specified by model number),Rear Port 1 Physical link selector, Available when Fibre Optic Comms card is specified by model number				
RP1 Time Sync	0E	08	Disabled	Enabled or Disabled (DNP3.0)
If set to Enabled the master station can be used to synchronize the time on the relay. If set to Disabled either the internal free running clock or IRIG-B input are used. Build=DNP 3.0 Visible when IRIG-B is disabled,Rear Port 1 DNP 3.0 Protocol time sync configuration NB Not available when IRIG-B option fitted and enabled				
Modbus IEC Time	0E	09	Standard	Standard or Reverse (IEC60870)
When Standard is selected, the time format complies with IEC60870-5-4 requirements so that byte 1 of the information is transmitted first, followed by bytes 2 through to 7. If Reverse is selected the transmission of information is reversed. Build = Modbus,Controls the format of the time-date G12 data type. Modbus Only				
RP1 CS103Blcking	0E	0A	Disabled	Disabled, Monitor blocking or Command Blocking (IEC60870)
Sets the blocking type*. Build=IEC60870-5-103,Rear Port 1 IEC60870-5-103 Protocol blocking configuration				
RP1 Card Status	0E	0B		K-Bus OK, EIA485 OK or Fiber Optic OK (Courier)
Displays the status of the card in RP1. Build = Courier,Rear Port 1 Courier Protocol Status				
RP1 Port Config	0E	0C	K-Bus	Kbus or EIA485 (Courier)
Defines communications configuration type for RP1. Build = Courier,Rear Port 1 Courier Protocol copper port configuration; K-Bus or EIA485				
RP1 Comms Mode	0E	0D	IEC60870 FT1.2	IEC60870 FT1.2 Frame or 10-bit No parity

Menu Text	Col	Row	Default Setting	Available Setting
Description				
Defines communications mode for RP1. Build = Courier,Rear Port 1 Courier Protocol EIA485 mode				
RP1 Baud Rate	0E	0E	19200 bits/s	9600 bps, 19200 bps or 38400 bps (Courier)
Defines the Baud rate for RP1. Build = Courier,Rear Port 1 Courier Protocol EIA485 bit/baud rate				
DNP Need Time	0E	11	10	1 to 30 step 1 (DNP3.0)
The duration of time waited before requesting another time sync from the master				
DNP App Fragment	0E	12	2048	100 to 2048 step 1 (DNP3.0)
The maximum message length (application fragment size) transmitted by the relay				
DNP App Timeout	0E	13	2	1 to 120 step 1 (DNP3.0)
Duration of time waited, after sending a message fragment and awaiting a confirmation from the master				
DNP SBO Timeout	0E	14	10	1 to 10 step 1 (DNP3.0)
Duration of time waited, after receiving a select command and awaiting an operate confirmation from the master				
DNP Link Timeout	0E	15	0	0s to 120s step 1s
Duration of time that the unit will wait for a Data Link Confirmation from the master				
ETH Protocol	0E	1F	IEC61850	IEC61850 (Ethernet)
Indicates the protocol used on the Network Interface Card. Build=IEC61850				
MAC Addr 1	0E	22	Ethernet MAC Addr	MAC address (Ethernet)
Shows the MAC address of the rear Ethernet port. Build=IEC61850				
MAC Addr 2	0E	23	Ethernet MAC Addr	MAC address (Ethernet)
Shows the MAC address of the rear Ethernet port. Build=IEC61850				
PB MAC Addr 1	0E	24	PB MAC Addr	MAC address (Ethernet)
Shows the MAC address of the process bus port. Build=IEC61850				
PB MAC Addr 2	0E	25	PB MAC Addr	MAC address (Ethernet)
Shows the MAC address of the process bus port Build=IEC61850				
ETH Tunl Timeout	0E	64	15.00 min	1 min to 30 min step 1 min (Ethernet)
Time waited before an inactive tunnel to MiCOM S1 Studio is reset. Build=IEC61850				
RSTPPriority	0E	75	32768	From 0 to 61440 step 4096
The manageable component of the Bridge Identifier, also known as the Bridge Priority				
RSTPMaxAge	0E	76	20	From 6 to 40 step 1
The maximum age of the information transmitted by the Bridge when it is the Root Bridge				
RSTPFwdDelay	0E	77	15	From 4 to 30 step 1
The delay used by STP Bridges to transition Root and Designated Ports to Forwarding				
RSTPHelloTime	0E	78	2	From 1 to 2 step 1
The interval between periodic transmissions of Configuration Messages by Designated Ports				
RSTPPortAStatus	0E	7E		Not Settable
Indication the status of port A.				
RSTPPortBStatus	0E	7F		Not Settable
Indication the status of port B.				
RP2 Protocol	0E	81	Courier	<Protocol>

Menu Text	Col	Row	Default Setting	Available Setting
Description				
Indicates the communications protocol used on the rear communications port RP2. Visible when Model no. Hardware option (Field 7) = 7 or 8 Implemented as datatype G71,Rear Port 2 Protocol - "Courier"				
RP2 Card Status	0E	84		Unsupported, Card not fitted, EIA232 OK, EIA485 OK or Kbus OK
Displays the status of the card in RP2. Visible when Model no. Hardware option (Field 7) = 7 or 8,Rear Port 2 Courier Protocol Status				
RP2 Port Config	0E	88	EIA232 (RS232)	EIA232, EIA485 or Kbus
Defines communications configuration type for RP2. Visible if RP2 Card status = OK,Rear Port 2 Courier Protocol port configuration; K-Bus or EIA485				
RP2 Comms Mode	0E	8A	IEC60870 FT1.2	IEC60870 FT1.2 Frame or 10-bit No parity
Defines communications mode for RP2. Visible if RP2 Card status = OK and 0E88<2,Rear Port 2 Courier Protocol EIA485 mode				
RP2 Address	0E	90	255	0 to 255
Sets the relay address (protocol dependent). Visible if RP2 Card status = OK,Rear Port 2 Courier Protocol device address				
RP2 InactivTimer	0E	92	15	1 min to 30 min step 1 min
Defines the period of inactivity before relay reverts to its default state. Visible if RP2 Card status = OK,Rear Port 2 Courier Protocol inactivity timer				
RP2 Baud Rate	0E	94	19200 bits/s	9600 bps, 19200 bps or 38400 bps
Defines the Baud rate for RP2. Visible if RP2 Card status = OK and 0E88<2,Rear Port 2 Courier Protocol EIA485 bit/baud rate				
DNP Need Time	0E	B1	10	1 to 30 step 1
The duration of time waited before requesting another time sync from the master				
DNP App Fragment	0E	B2	2048	100 to 2048 step 1 (DNP3.0)
The maximum message length (application fragment size) transmitted by the relay				
DNP App Timeout	0E	B3	2	1 to 120 step 1 (DNP3.0)
Duration of time waited, after sending a message fragment and awaiting a confirmation from the master				
DNP SBO Timeout	0E	B4	10	1 to 10 step 1 (DNP3.0)
Duration of time waited, after receiving a select command and awaiting an operate confirmation from the master				

Table 32 - Communications settings

5.12 Commissioning Tests

To help minimising the time required to test MiCOM relays the relay provides several test facilities under the 'COMMISSION TESTS' menu heading.

There are menu cells which allow the status of the opto-isolated inputs, output relay contacts, internal Digital Data Bus (DDB) signals and user-programmable LEDs to be monitored. Additionally there are cells to test the operation of the output contacts, user-programmable LEDs.

This column is visible when the "Commission tests" setting ("Configuration" column) = "visible".

Menu Text	Col	Row	Default Setting	Available Setting
Description				
COMMISSION TESTS	0F	00		
This column contains COMMISSION TESTS parameters				
Opto I/P Status	0F	01		16-bit binary string: 1 = energized or 0 = de-energized
This displays the status of the relay's opto-isolated inputs as a binary string: 1 = energized, 0 = de-energized				
Relay O/P Status	0F	03		16-bit binary string: 1 = energized or 0 = de-energized
This displays the status of the relay's opto-isolated inputs as a binary string: 1 = operational 0 = unoperational				
Test Port Status	0F	05		8-bit binary string
Displays the status of the eight digital data bus (DDB) signals				
LED Status	0F	06		8-bit binary string
8-bit binary string that indicates which of the LEDs are ON				
Monitor Bit 1	0F	07	64	0 = LED off or 1 = LED on
LED 1 monitor bit				
Monitor Bit 2	0F	08	65	0 = LED off or 1 = LED on
LED 2 monitor bit				
Monitor Bit 3	0F	09	66	0 = LED off or 1 = LED on
LED 3 monitor bit				
Monitor Bit 4	0F	0A	67	0 = LED off or 1 = LED on
LED 4 monitor bit				
Monitor Bit 5	0F	0B	68	0 = LED off or 1 = LED on
LED 5 monitor bit				
Monitor Bit 6	0F	0C	69	0 = LED off or 1 = LED on
LED 6 monitor bit				
Monitor Bit 7	0F	0D	70	0 = LED off or 1 = LED on
LED 7 monitor bit				
Monitor Bit 8	0F	0E	71	0 = LED off or 1 = LED on
LED 8 monitor bit				
Test Mode	0F	0F	Disabled	Disabled, Test Mode or Contacts Blocked
Allows the setting of a Test mode				
Test Pattern	0F	10	0	32 bit binary string
Used to select the output relay contacts tested				
Contact Test	0F	11	No Operation	No Operation, Apply Test or Remove Test
See*				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
Test LEDs	0F	12	No Operation	No Operation or Apply Test
When the Apply Test command is issued, the LEDs are ON for approximately 2 seconds. When they go OFF, the command text on the LCD reverts to No Operation				
Red LED Status	0F	15		18-bit binary string
Binary string that indicates which of the user-programmable LEDs on the relay are ON				
Green LED Status	0F	16		18-bit binary string
Binary string that indicates which of the user-programmable LEDs on the relay are ON				
DDB 31 - 0	0F	20		32-bit binary string
Displays the status of DDB signals				
DDB 63 - 32	0F	21		32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 63 - 32 instead.				
DDB 95 - 64	0F	22		32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 95 - 64 instead.				
DDB 127 - 96	0F	23		32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 127 - 96 instead.				
DDB 159 - 128	0F	24		32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 159 - 128 instead.				
DDB 191 - 160	0F	25		32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 191 - 160 instead.				
DDB 223 - 192	0F	26		32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 223 - 192 instead.				
DDB 255 - 224	0F	27		32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 255 - 224 instead.				
DDB 287 - 256	0F	28		32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 287 - 256 instead.				
DDB 319 - 288	0F	29		32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 319 - 288 instead.				
DDB 351 - 320	0F	2A		32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 351 - 320 instead.				
DDB 383 - 352	0F	2B		32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 383 - 352 instead.				
DDB 415 - 384	0F	2C		32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 415 - 384 instead.				
DDB 447 - 416	0F	2D		32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 447 - 416 instead.				
DDB 479 - 448	0F	2E		32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 479 - 448 instead.				
DDB 511 - 480	0F	2F		32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 511 - 480 instead.				
DDB 543 - 512	0F	30		32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 543 - 512 instead.				
DDB 575 - 544	0F	31		32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 575 - 544 instead.				
DDB 607 - 576	0F	32		32-bit binary string

Menu Text	Col	Row	Default Setting	Available Setting
Description				
This works in the same way as DDB 31 - 0 but for DDB 607 - 576 instead.				
DDB 639 - 608	0F	33		32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 639 - 608 instead.				
DDB 671 - 640	0F	34		32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 671 - 640 instead.				
DDB 703 - 672	0F	35		32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 703 - 672 instead.				
DDB 735 - 704	0F	36		32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 735 - 704 instead.				
DDB 767 - 736	0F	37		32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 767 - 736 instead.				
DDB 799 - 768	0F	38		32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 799 - 768 instead.				
DDB 831 - 800	0F	39		32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 831 - 800 instead.				
DDB 863 - 832	0F	3A		32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 863 - 832 instead.				
DDB 895 - 864	0F	3B		32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 895 - 864 instead.				
DDB 927 - 896	0F	3C		32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 927 - 896 instead.				
DDB 959 - 928	0F	3D		32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 959 - 928 instead.				
DDB 991 - 960	0F	3E		32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 991 - 960 instead.				
DDB 1023 - 992	0F	3F		32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 1023 - 992 instead.				
DDB 1055-1024	0F	40		32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 1055-1024 instead.				
DDB 1087-1056	0F	41		32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 1087-1056 instead.				
DDB 1119-1088	0F	42		32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 1119-1088 instead.				
DDB 1151-1120	0F	43		32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 1151-1120 instead.				
DDB 1183-1152	0F	44		32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 1183-1152 instead.				
DDB 1215-1184	0F	45		32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 1215-1184 instead.				
DDB 1247-1216	0F	46		32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 1247-1216 instead.				
DDB 1279-1248	0F	47		32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 1279-1248 instead.				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
DDB 1311-1280	0F	48		32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 1311-1280 instead.				
DDB 1343-1312	0F	49		32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 1343-1312 instead.				
DDB 1375-1344	0F	4A		32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 1375-1344 instead.				
DDB 1407-1376	0F	4B		32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 1407-1376 instead.				
DDB 1439-1408	0F	4C	0xFFFFFFFF	32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 1439-1408 instead.				
DDB 1471-1440	0F	4D	0xFFFFFFFF	32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 1471-1440 instead.				
DDB 1503-1472	0F	4E	0xFFFFFFFF	32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 1503-1472 instead.				
DDB 1535-1504	0F	4F	0xFFFFFFFF	32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 1535-1504 instead.				
DDB 1567-1536	0F	50	0xFFFFFFFF	32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 1567-1536 instead.				
DDB 1599-1568	0F	51	0xFFFFFFFF	32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 1599-1568 instead.				
DDB 1631-1600	0F	52	0xFFFFFFFF	32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 1631-1600 instead.				
DDB 1663-1632	0F	53	0xFFFFFFFF	32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 1663-1632 instead.				
DDB 1695-1664	0F	54	0xFFFFFFFF	32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 1695-1664 instead.				
DDB 1727-1696	0F	55	0xFFFFFFFF	32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 1727-1696 instead.				
DDB 1759-1728	0F	56	0xFFFFFFFF	32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 1759-1728 instead.				
DDB 1791-1760	0F	57	0xFFFFFFFF	32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 1791-1760 instead.				
DDB 1823-1792	0F	58	0xFFFFFFFF	32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 1823-1792 instead.				
DDB 1855-1824	0F	59	0xFFFFFFFF	32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 1855-1824 instead.				
DDB 1887-1856	0F	5A	0xFFFFFFFF	32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 1887-1856 instead.				
DDB 1919-1888	0F	5B	0xFFFFFFFF	32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 1919-1888 instead.				
DDB 1951-1920	0F	5C	0xFFFFFFFF	32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 1951-1920 instead.				
DDB 1983-1952	0F	5D	0xFFFFFFFF	32-bit binary string

Menu Text	Col	Row	Default Setting	Available Setting
Description				
This works in the same way as DDB 31 - 0 but for DDB 1983-1952 instead.				
DDB 2015-1984	0F	5E	0xFFFFFFFF	32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 2015-1984 instead.				
DDB 2047-2016	0F	5F	0xFFFFFFFF	32-bit binary string
This works in the same way as DDB 31 - 0 but for DDB 2047-2016 instead.				

Table 33 - Commission tests

5.13 Opto Configuration

Menu Text	Col	Row	Default Setting	Available Setting
Description				
OPTO CONFIG	11	00		
This column contains OPTO CONFIG parameters				
Global Nominal V	11	01	48-54V	24-27, 30-34, 48-54, 110-125, 220-250 or custom
Sets the nominal battery voltage for all opto inputs by selecting one of the five standard ratings in the Global Nominal V settings. If Custom is selected, each opto input can be set individually to a nominal voltage value				
Opto Input 1	11	02	48-54V	24-27, 30-34, 48-54, 110-125 or 220-250
Each opto input can be set individually to a nominal voltage value if custom is selected for the global setting				
Opto Input 2	11	03	48-54V	24-27, 30-34, 48-54, 110-125 or 220-250
This setting works in the same way as Opto Input 1 but for Opto Input 2 instead.				
Opto Input 3	11	04	48-54V	24-27, 30-34, 48-54, 110-125 or 220-250
This setting works in the same way as Opto Input 1 but for Opto Input 3 instead.				
Opto Input 4	11	05	48-54V	24-27, 30-34, 48-54, 110-125 or 220-250
This setting works in the same way as Opto Input 1 but for Opto Input 4 instead.				
Opto Input 5	11	06	48-54V	24-27, 30-34, 48-54, 110-125 or 220-250
This setting works in the same way as Opto Input 1 but for Opto Input 5 instead.				
Opto Input 6	11	07	48-54V	24-27, 30-34, 48-54, 110-125 or 220-250
This setting works in the same way as Opto Input 1 but for Opto Input 6 instead.				
Opto Input 7	11	08	48-54V	24-27, 30-34, 48-54, 110-125 or 220-250
This setting works in the same way as Opto Input 1 but for Opto Input 7 instead.				
Opto Input 8	11	09	48-54V	24-27, 30-34, 48-54, 110-125 or 220-250
This setting works in the same way as Opto Input 1 but for Opto Input 8 instead.				
Opto Input 9	11	0A	48-54V	24-27, 30-34, 48-54, 110-125 or 220-250
This setting works in the same way as Opto Input 1 but for Opto Input 9 instead.				
Opto Input 10	11	0B	48-54V	24-27, 30-34, 48-54, 110-125 or 220-250
This setting works in the same way as Opto Input 1 but for Opto Input 10 instead.				
Opto Input 11	11	0C	48-54V	24-27, 30-34, 48-54, 110-125 or 220-250
This setting works in the same way as Opto Input 1 but for Opto Input 11 instead.				
Opto Input 12	11	0D	48-54V	24-27, 30-34, 48-54, 110-125 or 220-250
This setting works in the same way as Opto Input 1 but for Opto Input 12 instead.				
Opto Input 13	11	0E	48-54V	24-27, 30-34, 48-54, 110-125 or 220-250

Menu Text	Col	Row	Default Setting	Available Setting
Description				
This setting works in the same way as Opto Input 1 but for Opto Input 13 instead.				
Opto Input 14	11	0F	48-54V	24-27, 30-34, 48-54, 110-125 or 220-250
This setting works in the same way as Opto Input 1 but for Opto Input 14 instead.				
Opto Input 15	11	10	48-54V	24-27, 30-34, 48-54, 110-125 or 220-250
This setting works in the same way as Opto Input 1 but for Opto Input 15 instead.				
Opto Input 16	11	11	48-54V	24-27, 30-34, 48-54, 110-125 or 220-250
This setting works in the same way as Opto Input 1 but for Opto Input 16 instead.				
Opto Input 17	11	12	48-54V	24-27, 30-34, 48-54, 110-125 or 220-250
This setting works in the same way as Opto Input 1 but for Opto Input 17 instead.				
Opto Input 18	11	13	48-54V	24-27, 30-34, 48-54, 110-125 or 220-250
This setting works in the same way as Opto Input 1 but for Opto Input 18 instead.				
Opto Input 19	11	14	48-54V	24-27, 30-34, 48-54, 110-125 or 220-250
This setting works in the same way as Opto Input 1 but for Opto Input 19 instead.				
Opto Input 20	11	15	48-54V	24-27, 30-34, 48-54, 110-125 or 220-250
This setting works in the same way as Opto Input 1 but for Opto Input 20 instead.				
Opto Input 21	11	16	48-54V	24-27, 30-34, 48-54, 110-125 or 220-250
This setting works in the same way as Opto Input 1 but for Opto Input 21 instead.				
Opto Input 22	11	17	48-54V	24-27, 30-34, 48-54, 110-125 or 220-250
This setting works in the same way as Opto Input 1 but for Opto Input 22 instead.				
Opto Input 23	11	18	48-54V	24-27, 30-34, 48-54, 110-125 or 220-250
This setting works in the same way as Opto Input 1 but for Opto Input 23 instead.				
Opto Input 24	11	19	48-54V	24-27, 30-34, 48-54, 110-125 or 220-250
This setting works in the same way as Opto Input 1 but for Opto Input 24 instead.				
Opto Input 25	11	1A	48-54V	24-27, 30-34, 48-54, 110-125 or 220-250
P645 and P746 only. This setting works in the same way as Opto Input 1 but for Opto Input 25 instead.				
Opto Input 26	11	1B	48-54V	24-27, 30-34, 48-54, 110-125 or 220-250
P645 and P746 only. This setting works in the same way as Opto Input 1 but for Opto Input 26 instead.				
Opto Input 27	11	1C	48-54V	24-27, 30-34, 48-54, 110-125 or 220-250
P645 and P746 only. This setting works in the same way as Opto Input 1 but for Opto Input 27 instead.				
Opto Input 28	11	1D	48-54V	24-27, 30-34, 48-54, 110-125 or 220-250
P645 and P746 only. This setting works in the same way as Opto Input 1 but for Opto Input 28 instead.				
Opto Input 29	11	1E	48-54V	24-27, 30-34, 48-54, 110-125 or 220-250
P645 and P746 only. This setting works in the same way as Opto Input 1 but for Opto Input 29 instead.				
Opto Input 30	11	1F	48-54V	24-27, 30-34, 48-54, 110-125 or 220-250
P645 and P746 only. This setting works in the same way as Opto Input 1 but for Opto Input 30 instead.				
Opto Input 31	11	20	48-54V	24-27, 30-34, 48-54, 110-125 or 220-250
P645 and P746 only. This setting works in the same way as Opto Input 1 but for Opto Input 31 instead.				
Opto Input 32	11	21	48-54V	24-27, 30-34, 48-54, 110-125 or 220-250

Menu Text	Col	Row	Default Setting	Available Setting
Description				
P645 and P746 only. This setting works in the same way as Opto Input 1 but for Opto Input 32 instead.				
OptoFilter Ctrl1	11	50	0xFFFFFFFF	16-bit binary string: 0=disable filtering or 1=enable filtering
A binary string is used to represent the opto inputs available. A 1 or 0 is used to enable or disable for each input a pre-set filter of ½ cycle that renders the input immune to induced ac noise on the wiring				
Characteristic	11	80	Standard 60%-80%	60-80% or 50-70%
Selects the pick-up and drop-off characteristics of the optos. The standard setting means the optos nominally provide a Logic 1 or ON value for voltages ³80% of the set lower nominal voltage, and a Logic 0 or OFF value for the voltages £60% of the set higher nominal voltage				

Table 34 - Opto Config

5.14 Control Input Labels

Each custom input can be set or reset from a Bit Field or separate enable/disable selection.

There are many of these inputs. These are all recorded in blocks of settings within the MiCOM relay. They all have the same Default and Available Settings and the same Description applies to all of them. The following table shows the first and last inputs in the sequence(s).

Menu Text	Col	Row	Default Setting	Available Setting
Description				
CONTROL INPUTS	12	00		
This column contains CONTROL INPUTS parameters				
Ctrl I/P Status	12	01		32-bit binary string: Set = 1 or Reset = 0
Setting to allow the control inputs to be individually assigned to the Hotkey menu by setting 1 in the appropriate bit in the Hotkey Enabled cell. The hotkey menu allows the control inputs to be set, reset or pulsed without the need to enter the CONTROL INPUTS column.				
Control Input 1	12	02	No Operation	No Operation, Set or Reset
Configures the control inputs as either latched or pulsed				
Control Input 2	12	03	No Operation	No Operation, Set or Reset
Configures the control inputs as either latched or pulsed				
Control Input 3	12	04	No Operation	No Operation, Set or Reset
Configures the control inputs as either latched or pulsed				
Control Input 4	12	05	No Operation	No Operation, Set or Reset
Configures the control inputs as either latched or pulsed				
Control Input 5	12	06	No Operation	No Operation, Set or Reset
Configures the control inputs as either latched or pulsed				
Control Input 6	12	07	No Operation	No Operation, Set or Reset
Configures the control inputs as either latched or pulsed				
Control Input 7	12	08	No Operation	No Operation, Set or Reset
Configures the control inputs as either latched or pulsed				
Control Input 8	12	09	No Operation	No Operation, Set or Reset
Configures the control inputs as either latched or pulsed				
Control Input 9	12	0A	No Operation	No Operation, Set or Reset

Menu Text	Col	Row	Default Setting	Available Setting
Description				
Configures the control inputs as either latched or pulsed				
Control Input 10	12	0B	No Operation	No Operation, Set or Reset
Configures the control inputs as either latched or pulsed				
Control Input 11	12	0C	No Operation	No Operation, Set or Reset
Configures the control inputs as either latched or pulsed				
Control Input 12	12	0D	No Operation	No Operation, Set or Reset
Configures the control inputs as either latched or pulsed				
Control Input 13	12	0E	No Operation	No Operation, Set or Reset
Configures the control inputs as either latched or pulsed				
Control Input 14	12	0F	No Operation	No Operation, Set or Reset
Configures the control inputs as either latched or pulsed				
Control Input 15	12	10	No Operation	No Operation, Set or Reset
Configures the control inputs as either latched or pulsed				
Control Input 16	12	11	No Operation	No Operation, Set or Reset
Configures the control inputs as either latched or pulsed				
Control Input 17	12	12	No Operation	No Operation, Set or Reset
Configures the control inputs as either latched or pulsed				
Control Input 18	12	13	No Operation	No Operation, Set or Reset
Configures the control inputs as either latched or pulsed				
Control Input 19	12	14	No Operation	No Operation, Set or Reset
Configures the control inputs as either latched or pulsed				
Control Input 20	12	15	No Operation	No Operation, Set or Reset
Configures the control inputs as either latched or pulsed				
Control Input 21	12	16	No Operation	No Operation, Set or Reset
Configures the control inputs as either latched or pulsed				
Control Input 22	12	17	No Operation	No Operation, Set or Reset
Configures the control inputs as either latched or pulsed				
Control Input 23	12	18	No Operation	No Operation, Set or Reset
Configures the control inputs as either latched or pulsed				
Control Input 24	12	19	No Operation	No Operation, Set or Reset
Configures the control inputs as either latched or pulsed				
Control Input 25	12	1A	No Operation	No Operation, Set or Reset
Configures the control inputs as either latched or pulsed				
Control Input 26	12	1B	No Operation	No Operation, Set or Reset
Configures the control inputs as either latched or pulsed				
Control Input 27	12	1C	No Operation	No Operation, Set or Reset
Configures the control inputs as either latched or pulsed				
Control Input 28	12	1D	No Operation	No Operation, Set or Reset
Configures the control inputs as either latched or pulsed				
Control Input 29	12	1E	No Operation	No Operation, Set or Reset
Configures the control inputs as either latched or pulsed				
Control Input 30	12	1F	No Operation	No Operation, Set or Reset
Configures the control inputs as either latched or pulsed				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
Control Input 31	12	20	No Operation	No Operation, Set or Reset
Configures the control inputs as either latched or pulsed				
Control Input 32	12	21	No Operation	No Operation, Set or Reset
Configures the control inputs as either latched or pulsed				

Table 35 - Control Inputs Labels

5.15 Control Input Configuration

The control inputs function as software switches that can be set or reset either locally or remotely. These inputs can be used to trigger any function that they are connected to as part of the PSL.
This column is visible when the “Control I/P Config” setting (“Configuration” column) = “visible”.

There are many of these inputs. These are all recorded in blocks of settings within the MiCOM relay. They all have the same Default and Available Settings and the same Description applies to all of them. The following table shows the first and last inputs in the sequence(s).

Menu Text	Col	Row	Default Setting	Available Setting
Description				
CTRL I/P CONFIG	13	00		
This column contains CTRL I/P CONFIG parameters				
Hotkey Enabled	13	01	0xFFFFFFFF	32-bit binary string: Enabled = 1 or Disabled = 0
Setting to allow the control inputs to be individually assigned to the Hotkey menu .				
Control Input 1	13	10	Latched	Latched or Pulsed
Configures the control inputs as either latched or pulsed				
Ctrl Command 1	13	11	SET/RESET	Set/Reset, In/Out, Enabled/Disabled or On/Off
Defines the control command text (SET / RESET, In/Out, On/Off, Enabled/Disabled)				
Control Input 2	13	14	Latched	Latched or Pulsed
This setting works in the same way as Control Input 1.				
Ctrl Command 2	13	15	SET/RESET	Set/Reset, In/Out, Enabled/Disabled or On/Off
This setting works in the same way as Ctrl Command 1.				
Control Input 3	13	18	Latched	Latched or Pulsed
This setting works in the same way as Control Input 1.				
Ctrl Command 3	13	19	SET/RESET	Set/Reset, In/Out, Enabled/Disabled or On/Off
This setting works in the same way as Ctrl Command 1.				
Control Input 4	13	1C	Latched	Latched or Pulsed
This setting works in the same way as Control Input 1.				
Ctrl Command 4	13	1D	SET/RESET	Set/Reset, In/Out, Enabled/Disabled or On/Off
This setting works in the same way as Ctrl Command 1.				
Control Input 5	13	20	Latched	Latched or Pulsed
This setting works in the same way as Control Input 1.				
Ctrl Command 5	13	21	SET/RESET	Set/Reset, In/Out, Enabled/Disabled or On/Off
This setting works in the same way as Ctrl Command 1.				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
Control Input 6	13	24	Latched	Latched or Pulsed
This setting works in the same way as Control Input 1.				
Ctrl Command 6	13	25	SET/RESET	Set/Reset, In/Out, Enabled/Disabled or On/Off
This setting works in the same way as Ctrl Command 1.				
Control Input 7	13	28	Latched	Latched or Pulsed
This setting works in the same way as Control Input 1.				
Ctrl Command 7	13	29	SET/RESET	Set/Reset, In/Out, Enabled/Disabled or On/Off
This setting works in the same way as Ctrl Command 1.				
Control Input 8	13	2C	Latched	Latched or Pulsed
This setting works in the same way as Control Input 1.				
Ctrl Command 8	13	2D	SET/RESET	Set/Reset, In/Out, Enabled/Disabled or On/Off
This setting works in the same way as Ctrl Command 1.				
Control Input 9	13	30	Latched	Latched or Pulsed
This setting works in the same way as Control Input 1.				
Ctrl Command 9	13	31	SET/RESET	Set/Reset, In/Out, Enabled/Disabled or On/Off
This setting works in the same way as Ctrl Command 1.				
Control Input 10	13	34	Latched	Latched or Pulsed
This setting works in the same way as Control Input 1.				
Ctrl Command 10	13	35	SET/RESET	Set/Reset, In/Out, Enabled/Disabled or On/Off
This setting works in the same way as Ctrl Command 1.				
Control Input 11	13	38	Latched	Latched or Pulsed
This setting works in the same way as Control Input 1.				
Ctrl Command 11	13	39	SET/RESET	Set/Reset, In/Out, Enabled/Disabled or On/Off
This setting works in the same way as Ctrl Command 1.				
Control Input 12	13	3C	Latched	Latched or Pulsed
This setting works in the same way as Control Input 1.				
Ctrl Command 12	13	3D	SET/RESET	Set/Reset, In/Out, Enabled/Disabled or On/Off
This setting works in the same way as Ctrl Command 1.				
Control Input 13	13	40	Latched	Latched or Pulsed
This setting works in the same way as Control Input 1.				
Ctrl Command 13	13	41	SET/RESET	Set/Reset, In/Out, Enabled/Disabled or On/Off
This setting works in the same way as Ctrl Command 1.				
Control Input 14	13	44	Latched	Latched or Pulsed
This setting works in the same way as Control Input 1.				
Ctrl Command 14	13	45	SET/RESET	Set/Reset, In/Out, Enabled/Disabled or On/Off
This setting works in the same way as Ctrl Command 1.				
Control Input 15	13	48	Latched	Latched or Pulsed
This setting works in the same way as Control Input 1.				
Ctrl Command 15	13	49	SET/RESET	Set/Reset, In/Out, Enabled/Disabled or On/Off
This setting works in the same way as Ctrl Command 1.				
Control Input 16	13	4C	Latched	Latched or Pulsed
This setting works in the same way as Control Input 1.				
Ctrl Command 16	13	4D	SET/RESET	Set/Reset, In/Out, Enabled/Disabled or On/Off

Menu Text	Col	Row	Default Setting	Available Setting
Description				
This setting works in the same way as Ctrl Command 1.				
Control Input 17	13	50	Latched	Latched or Pulsed
This setting works in the same way as Control Input 1.				
Ctrl Command 17	13	51	SET/RESET	Set/Reset, In/Out, Enabled/Disabled or On/Off
This setting works in the same way as Ctrl Command 1.				
Control Input 18	13	54	Latched	Latched or Pulsed
This setting works in the same way as Control Input 1.				
Ctrl Command 18	13	55	SET/RESET	Set/Reset, In/Out, Enabled/Disabled or On/Off
This setting works in the same way as Ctrl Command 1.				
Control Input 19	13	58	Latched	Latched or Pulsed
This setting works in the same way as Control Input 1.				
Ctrl Command 19	13	59	SET/RESET	Set/Reset, In/Out, Enabled/Disabled or On/Off
This setting works in the same way as Ctrl Command 1.				
Control Input 20	13	5C	Latched	Latched or Pulsed
This setting works in the same way as Control Input 1.				
Ctrl Command 20	13	5D	SET/RESET	Set/Reset, In/Out, Enabled/Disabled or On/Off
This setting works in the same way as Ctrl Command 1.				
Control Input 21	13	60	Latched	Latched or Pulsed
This setting works in the same way as Control Input 1.				
Ctrl Command 21	13	61	SET/RESET	Set/Reset, In/Out, Enabled/Disabled or On/Off
This setting works in the same way as Ctrl Command 1.				
Control Input 22	13	64	Latched	Latched or Pulsed
This setting works in the same way as Control Input 1.				
Ctrl Command 22	13	65	SET/RESET	Set/Reset, In/Out, Enabled/Disabled or On/Off
This setting works in the same way as Ctrl Command 1.				
Control Input 23	13	68	Latched	Latched or Pulsed
This setting works in the same way as Control Input 1.				
Ctrl Command 23	13	69	SET/RESET	Set/Reset, In/Out, Enabled/Disabled or On/Off
This setting works in the same way as Ctrl Command 1.				
Control Input 24	13	6C	Latched	Latched or Pulsed
This setting works in the same way as Control Input 1.				
Ctrl Command 24	13	6D	SET/RESET	Set/Reset, In/Out, Enabled/Disabled or On/Off
This setting works in the same way as Ctrl Command 1.				
Control Input 25	13	70	Latched	Latched or Pulsed
This setting works in the same way as Control Input 1.				
Ctrl Command 25	13	71	SET/RESET	Set/Reset, In/Out, Enabled/Disabled or On/Off
This setting works in the same way as Ctrl Command 1.				
Control Input 26	13	74	Latched	Latched or Pulsed
This setting works in the same way as Control Input 1.				
Ctrl Command 26	13	75	SET/RESET	Set/Reset, In/Out, Enabled/Disabled or On/Off
This setting works in the same way as Ctrl Command 1.				
Control Input 27	13	78	Latched	Latched or Pulsed
This setting works in the same way as Control Input 1.				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
Ctrl Command 27	13	79	SET/RESET	Set/Reset, In/Out, Enabled/Disabled or On/Off
This setting works in the same way as Ctrl Command 1.				
Control Input 28	13	7C	Latched	Latched or Pulsed
This setting works in the same way as Control Input 1.				
Ctrl Command 28	13	7D	SET/RESET	Set/Reset, In/Out, Enabled/Disabled or On/Off
This setting works in the same way as Ctrl Command 1.				
Control Input 29	13	80	Latched	Latched or Pulsed
This setting works in the same way as Control Input 1.				
Ctrl Command 29	13	81	SET/RESET	Set/Reset, In/Out, Enabled/Disabled or On/Off
This setting works in the same way as Ctrl Command 1.				
Control Input 30	13	84	Latched	Latched or Pulsed
This setting works in the same way as Control Input 1.				
Ctrl Command 30	13	85	SET/RESET	Set/Reset, In/Out, Enabled/Disabled or On/Off
This setting works in the same way as Ctrl Command 1.				
Control Input 31	13	88	Latched	Latched or Pulsed
This setting works in the same way as Control Input 1.				
Ctrl Command 31	13	89	SET/RESET	Set/Reset, In/Out, Enabled/Disabled or On/Off
This setting works in the same way as Ctrl Command 1.				
Control Input 32	13	8C	Latched	Latched or Pulsed
This setting works in the same way as Control Input 1.				
Ctrl Command 32	13	8D	SET/RESET	Set/Reset, In/Out, Enabled/Disabled or On/Off
This setting works in the same way as Ctrl Command 1.				

Table 36 - Control input config

5.16 Function Keys

Menu Text	Col	Row	Default Setting	Available Setting
Description				
FUNCTION KEYS	17	00		
P643, P645 and P746 only. This column contains FUNCTION KEYS parameters				
Fn Key Status	17	01	0	8-bit binary string
P643, P645 and P746 only. Displays the status of each function key				
Fn Key 1	17	02	Unlocked	Disable, Lock or Unlock
P643, P645 and P746 only. This setting is used to activate the function key. The ‘Lock’ setting allows a function key output that is set to toggle mode to be locked in its current active state.				
Fn Key 1 Mode	17	03	Toggled	Toggle or Normal
P643, P645 and P746 only. Sets FKey in toggle/normal mode. In Toggle, 1st keypress latches FKey DDB output signal ON and next keypress resets FKey DDB output to OFF. This enables/disables relay functions. In Normal, DDB signal remains ON/ ‘high’ as long as FKey is pressed.				
Fn Key 1 Label	17	04	Function Key 1	16-character text string
P643, P645 and P746 only. This setting allows the text of the function key to be changed to something more suitable for the application.				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
Fn Key 2	17	05	Unlocked	Disable, Lock or Unlock
P643, P645 and P746 only. This setting works in the same way as Fn Key 1				
Fn Key 2 Mode	17	06	Normal	Toggle or Normal
P643 and P645 only. This setting works in the same way as Fn Key 1 Mode				
Fn Key 2 Label	17	07	Function Key 2	Toggle or Normal
P643, P645 and P746 only. This setting works in the same way as Fn Key 1 Label				
Fn Key 3	17	08	Unlocked	Disable, Lock or Unlock
P643, P645 and P746 only. This setting works in the same way as Fn Key 1				
Fn Key 3 Mode	17	09	Normal	Toggle or Normal
P643, P645 and P746 only. This setting works in the same way as Fn Key 1 Mode				
Fn Key 3 Label	17	0A	Function Key 3	16-character text string
P643, P645 and P746 only. This setting works in the same way as Fn Key 1 Label				
Fn Key 4	17	0B	Unlocked	Disable, Lock or Unlock
P643, P645 and P746 only. This setting works in the same way as Fn Key 1				
Fn Key 4 Mode	17	0C	Normal	Toggle or Normal
P643, P645 and P746 only. This setting works in the same way as Fn Key 1 Mode				
Fn Key 4 Label	17	0D	Function Key 4	16-character text string
P643, P645 and P746 only. This setting works in the same way as Fn Key 1 Label				
Fn Key 5	17	0E	Unlocked	Disable, Lock or Unlock
P643, P645 and P746 only. This setting works in the same way as Fn Key 1				
Fn Key 5 Mode	17	0F	Normal	Toggle or Normal
P643, P645 and P746 only. This setting works in the same way as Fn Key 1 Mode				
Fn Key 5 Label	17	10	Function Key 5	16-character text string
P643, P645 and P746 only. This setting works in the same way as Fn Key 1 Label				
Fn Key 6	17	11	Unlocked	Disable, Lock or Unlock
P643, P645 and P746 only. This setting works in the same way as Fn Key 1				
Fn Key 6 Mode	17	12	Normal	Toggle or Normal
P643, P645 and P746 only. This setting works in the same way as Fn Key 1 Mode				
Fn Key 6 Label	17	13	Function Key 6	16-character text string
P643, P645 and P746 only. This setting works in the same way as Fn Key 1 Label				
Fn Key 7	17	14	Unlocked	Disable, Lock or Unlock
P643, P645 and P746 only. This setting works in the same way as Fn Key 1				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
Fn Key 7 Mode	17	15	Normal	Toggle or Normal
P643 and P645 only. This setting works in the same way as Fn Key 1 Mode				
Fn Key 7 Label	17	16	Function Key 7	16-character text string
P643, P645 and P746 only. This setting works in the same way as Fn Key 1 Label				
Fn Key 8	17	17	Locked	Disable, Lock or Unlock
P643 and P645 only. This setting works in the same way as Fn Key 1				
Fn Key 8 Mode	17	18	Normal	Toggle or Normal
P643, P645 and P746 only. This setting works in the same way as Fn Key 1 Mode				
Fn Key 8 Label	17	19	Function Key 8	16-character text string
P643, P645 and P746 only. This setting works in the same way as Fn Key 1 Label				
Fn Key 9	17	1A	Unlocked	Disable, Lock or Unlock
P643, P645 and P746 only. This setting works in the same way as Fn Key 1				
Fn Key 9 Mode	17	1B	Normal	Toggle or Normal
P643, P645 and P746 only. his setting works in the same way as Fn Key 1 Mode				
Fn Key 9 Label	17	1C	Function Key 9	16-character text string
This setting works in the same way as Fn Key 1 Label				
Fn Key 10	17	1D	Unlocked	Disable, Lock or Unlock
P643, P645 and P746 only. This setting works in the same way as Fn Key 1				
Fn Key 10 Mode	17	1E	Normal	Toggle or Normal
P643, P645 and P746 only. This setting works in the same way as Fn Key 1 Mode				
Fn Key 10 Label	17	1F	Function Key 10	16 character text string
P643, P645 and P746 only. This setting works in the same way as Fn Key 1 Label				

Table 37 - Function keys

5.17 Process Bus (PB) Config

Menu Text	Col	Row	Default Setting	Available Setting
Description				
PB CONFIG	18	00		
This column contains settings and status parameters relative to process bus				
MU OOS CONFIG	18	01	00000000(bin)	8 bits setting, 0 = MU OOS Disabled, 1 = MU OOS Enabled
Used to set one or more Merging Units to be run in Out of Service mode .				
AntiAlais Filter	18	02	Disabled	0 = Disabled, 1 = Enabled
This cell activates or deactivates the anti-aliasing filter, which conditions the Sampled Values from the Process Bus network.				
SMV Version	18	03	IEC61850-9-2LE	0=IEC61850-9-2LE, 1 = IEC61869

Menu Text	Col	Row	Default Setting	Available Setting
Description				
This cell selects which version of sampled values are used, if it is set to IEC61850-9-2LE, device will subscribe the sampled value compliant with IEC61850-9-2LE, otherwise, device will subscribe the sampled value compliant with IEC61869. If the MU device is configured to published IEC61850-9-2 compatible frames, the setting should be set to IEC61850-9-2LE.				
MUs Delay Offset	18	04	0s	From 0s to 3ms step 250us
This cell adjusts the maximum time-delay offset starting at the reception of the Ethernet message from the “first” Merging Unit (MU) to the reception of the Ethernet message from the “last” Merging Unit (MU). This time-delay should be adjusted to ensure all MU samples for the same time instant are received before sending to the relay processor.				
Mon Delay Offset	18	05	No	0 = No, 1 = Yes
When sampled values are received at the IED from different Merging Units, they do not arrive simultaneously due to differences in Merging Unit performance or different network path delays. After this setting is set to Yes, a command to monitor the maximum time-delay will be sent to Process Bus board. After Process Bus board has calculated a delay, it will send the delay time to main board for users to set a proper MUs Delay Offset.				
Max Delay Offset	18	06		
This setting specifies the maximum time-delay supervised, supervision starting at the reception of the sampled value frame from the "first" Merging Unit to the reception of the sampled value frame from the last Merging Unit for each sample count. If >3ms, a -1 will be displayed.				
Synchro Mode	18	30	No SYNC CLK	0 = No SYNC CLK, 1 = Local Clock 2 = Global Clock
This setting specifies the type of Sampled Value synchronization expected by the IED, depending on the application. Global Clock: The Sampled Values are synchronized with a global area clock (GPS like clock). Local Clock: The Sampled Values are synchronized with a local area clock signal at the substation. Sampled Value frames received with Global or Local synchronization are acceptable with this setting. No SYNC CLK: The Sampled Values do not need to be synchronized. With this setting the IED ignores the synchronization flag in the Sampled Value frames.				
SV Absence Alm	18	31	00000000(bin)	
This is a data cell with 8 binary flags. It indicates the presence or absence of Sampled Values from each of the Merging Units the IED is communicating with. The cell data for each Merging Unit is continuously refreshed. Unused MUs will indicate a 0. 0: Sampled Values being received from the Merging Unit. 1: No Sampled Values being received from the Merging Unit.				
SV SmpSynch Alm	18	32	00000000(bin)	
This is a data cell with 8 binary flags. It indicates whether the Sampled Values being received from each of the Merging Units has the Synchro as required by 1830 above. Unused MUs will indicate a 0 0: Sampled Values received are synchronized. 1: Sampled Values received are not synchronized.				
SV Test Alm	18	33	0000000000(bin)	
This is a data cell with a binary flag for each of the analogue groups within the relays. It indicates the status of the IEC 61850 Quality attribute ‘Test’ in the Sampled Value frame used for that channel. If a channel is marked Test then functions associated with that channel are blocked unless the relay is in ‘Test Mode’ or ‘Contacts Blocked’				
SV Test Alm	18	33	00000000(bin)	
This is a data cell with a binary flag for each of the analogue groups within the relays. It indicates the status of the IEC 61850 Quality attribute ‘Test’ in the Sampled Value frame used for that channel. If a channel is marked Test then functions associated with that channel are blocked unless the relay is in ‘Test Mode’ or ‘Contacts Blocked’				
SV Test Alm	18	33	00000(bin)	
This is a data cell with a binary flag for each of the analogue groups within the relays. It indicates the status of the IEC 61850 Quality attribute ‘Test’ in the Sampled Value frame used for that channel. If a channel is marked Test then functions associated with that channel are blocked unless the relay is in ‘Test Mode’ or ‘Contacts Blocked’				
SV Invalid Alm	18	34	0000000000(bin)	
This is a data cell with a binary flag for each of the analogue groups within the relay. It indicates the status of the IEC 61850 Quality attribute ‘Invalid’ in the Sampled Value frame used for that channel. If a channel is marked Invalid then functions associated with that channel are blocked.				
SV Invalid Alm	18	34	00000000(bin)	

Menu Text	Col	Row	Default Setting	Available Setting
Description				
This is a data cell with a binary flag for each of the analogue groups within the relay. It indicates the status of the IEC 61850 Quality attribute 'Invalid' in the Sampled Value frame used for that channel. If a channel is marked Invalid then functions associated with that channel are blocked.				
SV Invalid Alm	18	34	00000(bin)	
This is a data cell with a binary flag for each of the analogue groups within the relay. It indicates the status of the IEC 61850 Quality attribute 'Invalid' in the Sampled Value frame used for that channel. If a channel is marked Invalid then functions associated with that channel are blocked.				
SV Quest Alm	18	35	0000000000(bin)	
This is a data cell with a binary flag for each of the analogue groups within the relay. It indicates the status of the IEC 61850 Quality attribute 'Questionable' in the Sampled Value frame used for that channel. If a channel is marked Questionable then functions associated with that channel are blocked.				
SV Quest Alm	18	35	00000000(bin)	
This is a data cell with a binary flag for each of the analogue groups within the relay. It indicates the status of the IEC 61850 Quality attribute 'Questionable' in the Sampled Value frame used for that channel. If a channel is marked Questionable then functions associated with that channel are blocked.				
SV Quest Alm	18	35	00000(bin)	
This is a data cell with a binary flag for each of the analogue groups within the relay. It indicates the status of the IEC 61850 Quality attribute 'Questionable' in the Sampled Value frame used for that channel. If a channel is marked Questionable then functions associated with that channel are blocked.				

Table 38 – Process Bus (PB) Config

5.18 IED Configurator (for IEC 61850 Configuration)

The contents of the IED CONFIGURATOR column (for IEC 61850 configuration) are mostly data cells, displayed for information but not editable. To edit the configuration, you need to use the IED (Intelligent Electronic Device) configurator tool within the Schneider Electric MiCOM S1 Studio software.

Menu Text	Col	Row	Default Setting	Available Setting
Description				
IED CONFIGURATOR	19	00		
This column contains IED CONFIGURATION parameters				
Switch Conf.Bank	19	05	No Action	No action or Switch Banks
Setting which allows the user to switch between the current configuration, held in the Active Memory Bank, to the configuration sent to and held in the Inactive Memory Bank				
Restore Conf.	19	0A	No Action (0)	No Action or Restore MCL
Restore IEC 61850 Configuration				
Active Conf.Name	19	10	Not Available	<Active configuration name>
The name of the configuration in the Active Memory Bank, usually taken from the SCL file				
Active Conf.Rev	19	11	Not Available	<Active configuration revision>
Configuration Revision number of the configuration in the Active Memory Bank, usually taken from the SCL file				
Inact.Conf.Name	19	20	Not Available	<Inactive configuration name
The name of the configuration in the Inactive Memory Bank, usually taken from the SCL file				
Inact.Conf.Rev	19	21	Not Available	<Inactive configuration revision>
Configuration Revision number of the configuration in the Inactive Memory Bank, usually taken from the SCL file				
IP PARAMETERS	19	30	Sub-Heading	Sub-Heading
IP PARAMETERS				
IP Address 1	19	31	0.0.0.0	<IP address of relay>

Menu Text	Col	Row	Default Setting	Available Setting
Description				
Displays the unique network IP address that identifies the relay				
Subnet Mask 1	19	32	0.0.0.0	<Subnet mask of relay>
Displays the sub-network the relay is connected to				
Gateway 1	19	33	0.0.0.0	<Gateway address>
Displays the IP address of the gateway (proxy) the relay is connected to, if any				
IP Address 2	19	34	0.0.0.0	<IP address of relay>
2nd IP address for MPC8313				
Subnet Mask 2	19	35	0.0.0.0	<Subnet mask of relay>
2nd sub-network for MPC8313				
Gateway 2	19	36	0.0.0.0	<Gateway address>
2nd Gateway for MPC8313				
SNTP PARAMETERS	19	40	Sub-Heading	Sub-Heading
SNTP PARAMETERS				
SNTP Server 1	19	41	0.0.0.0	<IP address of SNTP server 1>
Displays the IP address of the primary SNTP server				
SNTP Server 2	19	42	0.0.0.0	<IP address of SNTP server 2>
Displays the IP address of the secondary SNTP server				
IEC 61850 SCL	19	50	Sub-Heading	Sub-Heading
IEC 61850 SCL				
IED Name	19	51	Not Available	<8 character IED name>
8 character IED name, which is the unique name on the IEC 61850 network for the IED, usually taken from the SCL file				
IEC 61850 GOOSE	19	60	Sub-Heading	Sub-Heading
IEC 61850 GOOSE				
GoEna	19	70	0000000000000000(bin)	0000000000000000(bin) to 1111111111111111(bin)
Setting to enable GOOSE publisher settings				
Pub.Simul.Goose	19	71	0000000000000000(bin)	0000000000000000(bin) to 1111111111111111(bin)
Setting to enable simulation GOOSE publish for Ed.2 (in Ed.1 mode, this setting is to enable test GOOSE publish).				
Sub.Simul.Goose	19	73	No	Yes or No
On Ed.2 mode, when set to Yes, both normal GOOSE (subscribed) and simulation GOOSE (subscribed) possible to be processed as standard defined. When set to No, only the normal GOOSE will be processed. On Ed.1 mode, when set to Yes, both normal GOOSE (subscribed) and test GOOSE (subscribed) will be processed synchronously. When set to No, only the normal GOOSE will be processed.				

Table 39 - IED configurator

5.19 Virtual Input Labels

There are many of these labels. These are all recorded in a block of settings within the MiCOM relay. They all have the same Default and Available Settings and the same Description applies to all of them. The following table shows the labels in the sequence.

Menu Text	Col	Row	Default Setting	Available Setting
Description				
VIR I/P LABELS	26	00		
This column contains VIR I/P parameters				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
Virtual Input 1	26	01	Virtual Input 1	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 2	26	02	Virtual Input 2	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 3	26	03	Virtual Input 3	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 4	26	04	Virtual Input 4	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 5	26	05	Virtual Input 5	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 6	26	06	Virtual Input 6	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 7	26	07	Virtual Input 7	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 8	26	08	Virtual Input 8	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 9	26	09	Virtual Input 9	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 10	26	0A	Virtual Input 10	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 11	26	0B	Virtual Input 11	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 12	26	0C	Virtual Input 12	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 13	26	0D	Virtual Input 13	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 14	26	0E	Virtual Input 14	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 15	26	0F	Virtual Input 15	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 16	26	10	Virtual Input 16	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 17	26	11	Virtual Input 17	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 18	26	12	Virtual Input 18	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 19	26	13	Virtual Input 19	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 20	26	14	Virtual Input 20	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 21	26	15	Virtual Input 21	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 22	26	16	Virtual Input 22	16 character text string

Menu Text	Col	Row	Default Setting	Available Setting
Description				
Text label to describe each individual Virtual input				
Virtual Input 23	26	17	Virtual Input 23	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 24	26	18	Virtual Input 24	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 25	26	19	Virtual Input 25	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 26	26	1A	Virtual Input 26	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 27	26	1B	Virtual Input 27	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 28	26	1C	Virtual Input 28	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 29	26	1D	Virtual Input 29	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 30	26	1E	Virtual Input 30	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 31	26	1F	Virtual Input 31	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 32	26	20	Virtual Input 32	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 33	26	21	Virtual Input 33	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 34	26	22	Virtual Input 34	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 35	26	23	Virtual Input 35	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 36	26	24	Virtual Input 36	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 37	26	25	Virtual Input 37	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 38	26	26	Virtual Input 38	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 39	26	27	Virtual Input 39	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 40	26	28	Virtual Input 40	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 41	26	29	Virtual Input 41	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 42	26	2A	Virtual Input 42	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 43	26	2B	Virtual Input 43	16 character text string
Text label to describe each individual Virtual input				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
Virtual Input 44	26	2C	Virtual Input 44	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 45	26	2D	Virtual Input 45	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 46	26	2E	Virtual Input 46	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 47	26	2F	Virtual Input 47	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 48	26	30	Virtual Input 48	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 49	26	31	Virtual Input 49	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 50	26	32	Virtual Input 50	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 51	26	33	Virtual Input 51	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 52	26	34	Virtual Input 52	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 53	26	35	Virtual Input 53	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 54	26	36	Virtual Input 54	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 55	26	37	Virtual Input 55	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 56	26	38	Virtual Input 56	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 57	26	39	Virtual Input 57	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 58	26	3A	Virtual Input 58	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 59	26	3B	Virtual Input 59	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 60	26	3C	Virtual Input 60	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 61	26	3D	Virtual Input 61	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 62	26	3E	Virtual Input 62	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 63	26	3F	Virtual Input 63	16 character text string
Text label to describe each individual Virtual input				
Virtual Input 64	26	40	Virtual Input 64	16 character text string
Text label to describe each individual Virtual input				

Table 40 – Virtual Input Labels

5.20 Virtual Output Labels

There are many of these labels. These are all recorded in a block of settings within the MiCOM relay. They all have the same Default and Available Settings and the same Description applies to all of them. The following table shows the labels in the sequence.

Menu Text	Col	Row	Default Setting	Available Setting
Description				
Virtual Output 1	27	01	Virtual Output 1	16 character text string
Text label to describe each individual Virtual output				
Virtual Output 2	27	02	Virtual Output 2	16 character text string
Text label to describe each individual Virtual output				
Virtual Output 3	27	03	Virtual Output 3	16 character text string
Text label to describe each individual Virtual output				
Virtual Output 4	27	04	Virtual Output 4	16 character text string
Text label to describe each individual Virtual output				
Virtual Output 5	27	05	Virtual Output 5	16 character text string
Text label to describe each individual Virtual output				
Virtual Output 6	27	06	Virtual Output 6	16 character text string
Text label to describe each individual Virtual output				
Virtual Output 7	27	07	Virtual Output 7	16 character text string
Text label to describe each individual Virtual output				
Virtual Output 8	27	08	Virtual Output 8	16 character text string
Text label to describe each individual Virtual output				
Virtual Output 9	27	09	Virtual Output 9	16 character text string
Text label to describe each individual Virtual output				
Virtual Output 10	27	0A	Virtual Output 10	16 character text string
Text label to describe each individual Virtual output				
Virtual Output 11	27	0B	Virtual Output 11	16 character text string
Text label to describe each individual Virtual output				
Virtual Output 12	27	0C	Virtual Output 12	16 character text string
Text label to describe each individual Virtual output				
Virtual Output 13	27	0D	Virtual Output 13	16 character text string
Text label to describe each individual Virtual output				
Virtual Output 14	27	0E	Virtual Output 14	16 character text string
Text label to describe each individual Virtual output				
Virtual Output 15	27	0F	Virtual Output 15	16 character text string
Text label to describe each individual Virtual output				
Virtual Output 16	27	10	Virtual Output 16	16 character text string
Text label to describe each individual Virtual output				
Virtual Output 17	27	11	Virtual Output 17	16 character text string
Text label to describe each individual Virtual output				
Virtual Output 18	27	12	Virtual Output 18	16 character text string
Text label to describe each individual Virtual output				
Virtual Output 19	27	13	Virtual Output 19	16 character text string

Menu Text	Col	Row	Default Setting	Available Setting
Description				
Text label to describe each individual Virtual output				
Virtual Output 20	27	14	Virtual Output 20	16 character text string
Text label to describe each individual Virtual output				
Virtual Output 21	27	15	Virtual Output 21	16 character text string
Text label to describe each individual Virtual output				
Virtual Output 22	27	16	Virtual Output 22	16 character text string
Text label to describe each individual Virtual output				
Virtual Output 23	27	17	Virtual Output 23	16 character text string
Text label to describe each individual Virtual output				
Virtual Output 24	27	18	Virtual Output 24	16 character text string
Text label to describe each individual Virtual output				
Virtual Output 25	27	19	Virtual Output 25	16 character text string
Text label to describe each individual Virtual output				
Virtual Output 26	27	1A	Virtual Output 26	16 character text string
Text label to describe each individual Virtual output				
Virtual Output 27	27	1B	Virtual Output 27	16 character text string
Text label to describe each individual Virtual output				
Virtual Output 28	27	1C	Virtual Output 28	16 character text string
Text label to describe each individual Virtual output				
Virtual Output 29	27	1D	Virtual Output 29	16 character text string
Text label to describe each individual Virtual output				
Virtual Output 30	27	1E	Virtual Output 30	16 character text string
Text label to describe each individual Virtual output				
Virtual Output 31	27	1F	Virtual Output 31	16 character text string
Text label to describe each individual Virtual output				
Virtual Output 32	27	20	Virtual Output 32	16 character text string
Text label to describe each individual Virtual output				

Table 41 - Virtual Output Labels

5.21 User Alarms

There are many of these labels. These are all recorded in a block of settings within the MiCOM relay. They all have the same Default and Available Settings and the same Description applies to all of them. The following table shows the labels in the sequence.

Menu Text	Col	Row	Default Setting	Available Setting
Description				
USER ALARMS	28	00		
This column contains USER ALARM parameters				
Manual Reset	28	01	0x00000000	32 bit binary string (0 self-reset, 1 manual reset)
Set the user alarm is maunal reset or self reset				
Labels	28	10	Sub-Heading	Sub-Heading

Menu Text	Col	Row	Default Setting	Available Setting
Description				
User Alarm 1	28	11	User Alarm 1	16 character text string
Text label to describe each individual user alarm				
User Alarm 2	28	12	User Alarm 2	16 character text string
This setting works in the same way as user alarm 1				
User Alarm 3	28	13	User Alarm 3	16 character text string
This setting works in the same way as user alarm 1				
User Alarm 4	28	14	User Alarm 4	16 character text string
This setting works in the same way as user alarm 1				
User Alarm 5	28	15	User Alarm 5	16 character text string
This setting works in the same way as user alarm 1				
User Alarm 6	28	16	User Alarm 6	16 character text string
This setting works in the same way as user alarm 1				
User Alarm 7	28	17	User Alarm 7	16 character text string
This setting works in the same way as user alarm 1				
User Alarm 8	28	18	User Alarm 8	16 character text string
This setting works in the same way as user alarm 1				
User Alarm 9	28	19	User Alarm 9	16 character text string
This setting works in the same way as user alarm 1				
User Alarm 10	28	1A	User Alarm 10	16 character text string
This setting works in the same way as user alarm 1				
User Alarm 11	28	1B	User Alarm 11	16 character text string
This setting works in the same way as user alarm 1				
User Alarm 12	28	1C	User Alarm 12	16 character text string
This setting works in the same way as user alarm 1				
User Alarm 13	28	1D	User Alarm 13	16 character text string
This setting works in the same way as user alarm 1				
User Alarm 14	28	1E	User Alarm 14	16 character text string
This setting works in the same way as user alarm 1				
User Alarm 15	28	1F	User Alarm 15	16 character text string
This setting works in the same way as user alarm 1				
User Alarm 16	28	20	User Alarm 16	16 character text string
This setting works in the same way as user alarm 1				
User Alarm 17	28	21	User Alarm 17	16 character text string
This setting works in the same way as user alarm 1				
User Alarm 18	28	22	User Alarm 18	16 character text string
This setting works in the same way as user alarm 1				
User Alarm 19	28	23	User Alarm 19	16 character text string
This setting works in the same way as user alarm 1				
User Alarm 20	28	24	User Alarm 20	16 character text string
This setting works in the same way as user alarm 1				
User Alarm 21	28	25	User Alarm 21	16 character text string
This setting works in the same way as user alarm 1				
User Alarm 22	28	26	User Alarm 22	16 character text string

Menu Text	Col	Row	Default Setting	Available Setting
Description				
This setting works in the same way as user alarm 1				
User Alarm 23	28	27	User Alarm 23	16 character text string
This setting works in the same way as user alarm 1				
User Alarm 24	28	28	User Alarm 24	16 character text string
This setting works in the same way as user alarm 1				
User Alarm 25	28	29	User Alarm 25	16 character text string
This setting works in the same way as user alarm 1				
User Alarm 26	28	2A	User Alarm 26	16 character text string
This setting works in the same way as user alarm 1				
User Alarm 27	28	2B	User Alarm 27	16 character text string
This setting works in the same way as user alarm 1				
User Alarm 28	28	2C	User Alarm 28	16 character text string
This setting works in the same way as user alarm 1				
User Alarm 29	28	2D	User Alarm 29	16 character text string
This setting works in the same way as user alarm 1				
User Alarm 30	28	2E	User Alarm 30	16 character text string
This setting works in the same way as user alarm 1				
User Alarm 31	28	2F	User Alarm 31	16 character text string
This setting works in the same way as user alarm 1				
User Alarm 32	28	30	User Alarm 32	16 character text string
This setting works in the same way as user alarm 1				

Table 42 - User Alarms

5.22 Ctrl I/P Labels

There are many of these labels. These are all recorded in a block of settings within the MiCOM relay. They all have the same Default and Available Settings and the same Description applies to all of them. The following table shows the labels in the sequence.

Menu Text	Col	Row	Default Setting	Available Setting
Description				
CTRL I/P LABELS	29	00		
This column contains CTRL I/P LABELS parameters				
Control Input 1	29	01	Control Input 1	16 character text string
Text label to describe each individual control input. This text is displayed when a control input is accessed by the hotkey menu. It is displayed in the programmable scheme logic description of the control input				
Control Input 2	29	02	Control Input 2	16 character text string
This setting works in the same way as Control Input 1				
Control Input 3	29	03	Control Input 3	16 character text string
This setting works in the same way as Control Input 1				
Control Input 4	29	04	Control Input 4	16 character text string
This setting works in the same way as Control Input 1				
Control Input 5	29	05	Control Input 5	16 character text string
This setting works in the same way as Control Input 1				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
Control Input 6	29	06	Control Input 6	16 character text string
This setting works in the same way as Control Input 1				
Control Input 7	29	07	Control Input 7	16 character text string
This setting works in the same way as Control Input 1				
Control Input 8	29	08	Control Input 8	16 character text string
This setting works in the same way as Control Input 1				
Control Input 9	29	09	Control Input 9	16 character text string
This setting works in the same way as Control Input 1				
Control Input 10	29	0A	Control Input 10	16 character text string
This setting works in the same way as Control Input 1				
Control Input 11	29	0B	Control Input 11	16 character text string
This setting works in the same way as Control Input 1				
Control Input 12	29	0C	Control Input 12	16 character text string
This setting works in the same way as Control Input 1				
Control Input 13	29	0D	Control Input 13	16 character text string
This setting works in the same way as Control Input 1				
Control Input 14	29	0E	Control Input 14	16 character text string
This setting works in the same way as Control Input 1				
Control Input 15	29	0F	Control Input 15	16 character text string
This setting works in the same way as Control Input 1				
Control Input 16	29	10	Control Input 16	16 character text string
This setting works in the same way as Control Input 1				
Control Input 17	29	11	Control Input 17	16 character text string
This setting works in the same way as Control Input 1				
Control Input 18	29	12	Control Input 18	16 character text string
This setting works in the same way as Control Input 1				
Control Input 19	29	13	Control Input 19	16 character text string
This setting works in the same way as Control Input 1				
Control Input 20	29	14	Control Input 20	16 character text string
This setting works in the same way as Control Input 1				
Control Input 21	29	15	Control Input 21	16 character text string
This setting works in the same way as Control Input 1				
Control Input 22	29	16	Control Input 22	16 character text string
This setting works in the same way as Control Input 1				
Control Input 23	29	17	Control Input 23	16 character text string
This setting works in the same way as Control Input 1				
Control Input 24	29	18	Control Input 24	16 character text string
This setting works in the same way as Control Input 1				
Control Input 25	29	19	Control Input 25	16 character text string
This setting works in the same way as Control Input 1				
Control Input 26	29	1A	Control Input 26	16 character text string
This setting works in the same way as Control Input 1				
Control Input 27	29	1B	Control Input 27	16 character text string

Menu Text	Col	Row	Default Setting	Available Setting
Description				
This setting works in the same way as Control Input 1				
Control Input 28	29	1C	Control Input 28	16 character text string
This setting works in the same way as Control Input 1				
Control Input 29	29	1D	Control Input 29	16 character text string
This setting works in the same way as Control Input 1				
Control Input 30	29	1E	Control Input 30	16 character text string
This setting works in the same way as Control Input 1				
Control Input 31	29	1F	Control Input 31	16 character text string
This setting works in the same way as Control Input 1				
Control Input 32	29	20	Control Input 32	16 character text string
This setting works in the same way as Control Input 1				

Table 43 - Ctrl I/P Labels

5.23 Recorder Extraction

Menu Text	Col	Row	Default Setting	Available Setting
Description				
RECORDER EXTRACTION COLUMN (No Header)	B4	00		
RECORDER EXTRACTION COLUMN (No Header)				
Select Record	B4	01	0	-199 to 199 step 1
Select Record				
Trigger Time	B4	02		Not settable
Trigger Time				
Active Channels	B4	03		Not settable
Active Channels				
Channel Types	B4	04		Not settable
Channel Types				
Channel Offsets	B4	05		Not settable
Channel Offsets				
Channel Scaling	B4	06		Not settable
Channel Scaling				
Channel SkewVal	B4	07		Not settable
Channel SkewVal				
Channel MinVal	B4	08		Not settable
Channel MinVal				
Channel MaxVal	B4	09		Not settable
Channel MaxVal				
Format	B4	0A		Not settable
Format				
Upload	B4	0B		Not settable
Upload				
No. Of Samples	B4	10		Not settable

Menu Text	Col	Row	Default Setting	Available Setting
Description				
No. Of Samples				
Trig Position	B4	11		Not settable
Trig Position				
Time Base	B4	12		Not settable
Time Base				
Sample Timer	B4	14		Not settable
Sample Timer				
Dist. Channel 1	B4	20		Not settable
Dist. Channel 1				
Dist. Channel 2	B4	21		Not settable
Dist. Channel 2				
Dist. Channel 3	B4	22		Not settable
Dist. Channel 3				
Dist. Channel 4	B4	23		Not settable
Dist. Channel 4				
Dist. Channel 5	B4	24		Not settable
Dist. Channel 5				
Dist. Channel 6	B4	25		Not settable
Dist. Channel 6				
Dist. Channel 7	B4	26		Not settable
Dist. Channel 7				
Dist. Channel 8	B4	27		Not settable
Dist. Channel 8				
Dist. Channel 9	B4	28		Not settable
Dist. Channel 9				
Dist. Channel 10	B4	29		Not settable
Dist. Channel 10				
Dist. Channel 11	B4	2A		Not settable
Dist. Channel 11				
Dist. Channel 12	B4	2B		Not settable
Dist. Channel 12				
Dist. Channel 13	B4	2C		Not settable
Dist. Channel 13				
Dist. Channel 31	B4	3E		Not settable
Dist. Channel 31				
Dist. Channel 32	B4	3F		Not settable
Dist. Channel 32				

Table 44 - Recorder Extraction

5.24 Comms System Data

Menu Text	Col	Row	Default Setting	Available Setting
Description				
COMMS SYS DATA	BF	00		
This column contains COMMS SYS DATA parameters				
Dist Record Cntrl Ref	BF	01	B300	Not settable
Dist Record Cntrl Ref				
Dist Record Extract Ref	BF	02	B400	Not settable
Dist Record Extract Ref				
Setting Transfer	BF	03		
This records the Setting Transfer parameter				
Reset Demand	BF	04		Not settable
Reset Demand - this is data but it supports the Reset Menu cell.				
Block Xfer Ref	BF	06	B200	Not settable
Block Xfer Ref				
Read Only Mode	BF	07		
Read only mode				
Connected i/face	BF	11		
Security Column	BF	12	25 00	
Port Disable	BF	13	25 05	
Port Disable end	BF	14	25 0B	
PW Entry Needed	BF	15	0	
PW Entry Needed	BF	16	0	
Password Reset	BF	F0		

Table 45 - Comms System Data

5.25 Ethernet Status

Menu Text	Col	Row	Default Setting	Available Setting
Description				
ETHERNET STATUS	F0	00		
This column contains ETHERNET STATUS parameters				
Ethernet Status Selector	F0	01		0 to 239 step 1
Ethernet Status Selector				
Ethernet Status Number	F0	03		Not settable
Ethernet Status Number				
Ethernet Fatal Error	F0	04		Not settable
Ethernet Fatal Error				

Table 46 - Ethernet Status

OPERATION

CHAPTER 5

Date:	07/2018
Products covered by this chapter:	This chapter covers the specific versions of the MiCOM products listed below. This includes ***only*** the following combinations of Software Version and Hardware Suffix.
Hardware Suffix:	L (P642) M (P643/P645)
Software Version:	B4 - P64x (P642, P643 & P645)
Connection Diagrams:	10P642xx (xx = 01 to 10) 10P643xx (xx = 01 to 06) 10P645xx (xx = 01 to 09)

CONTENTS

FIGURES

Page (OP) 5-

TABLES

Notes:

1 SIGNAL PROCESSING

The sampling rate of the P64x is 24 samples per cycle. The raw samples of each channel are buffered in a 2-cycle rotating buffer.

One-cycle Fourier filter is used to extract the fundamental sine and cosine components of each signal channel, and the second and fifth harmonic sine and cosine components of every phase differential current.

Magnitude and phase angle for each channel is calculated, as well as other derived quantities.

The protection functions require a combination of raw samples, Fourier components, magnitudes, phase, and other derived quantities as appropriate. These are specified in the analogue input section of each function.

Data acquisition is performed at a rate of 24 samples per cycle. The frequency tracking runs from the protection scheduler every 3rd sample. The differential protection task runs every 3 samples. The programmable scheme logic and the current differential run at a rate of 8 times per cycle. The following ***Execution rates*** table shows the execution rate of other functions:

Function	Execution rate (times/cycle)
CTS, zero crossing detection algorithm used by the CBF function, CT saturation detection, no gap detection, internal/external fault detector.	8
High impedance REF, Low impedance REF, VTS, poledead, circuit breaker failure.	4
Phase overcurrent, negative phase overcurrent, standby overcurrent, under/overvoltage, residual overvoltage, voltage controlled overcurrent, negative sequence overvoltage.	2
CLIO, RTD, overflux, through fault monitoring, thermal overload.	1

Table 1 - Execution rates

The frequency tracking algorithm is used to determine the power system frequency and to adjust the sampling clock so that it will be in exact multiples of the power system frequency. The P64x frequency tracking range is 45 to 66 Hz. The relay will track fundamental frequency down to the following levels of voltage (10V ±5%) and current (50 mA). The frequency tracking channel order is VA, VB, VC, VX, IA1, IB1, IC1, IA2, IB2, IC2, IA3, IB3, IC3, IA4, IB4, IC4, IA5, IB5, IC5. VA, VB, VC are only available in P643/P645 when the three-phase VT option is selected. The voltage channels have the priority. Only if a voltage channel is not available, a current channel would be used. If a current channel is being used and a voltage channel becomes available, the frequency tracking will automatically switch to the voltage channel. However, if neither a voltage channel nor IA1 are on hand, IB1 would be used. If IA1 becomes available and not voltage channel is available, the frequency tracking algorithm will continue using IB1.

2 OPERATION OF INDIVIDUAL PROTECTION FUNCTIONS

2.1 Differential Protection (DIFF)

The P64x is designed for the protection of transformers as well as for the protection of motors and reactors and of other two-winding (P642, P643, P645), three-winding (P643, P645) or five biased inputs (P645) arrangements.
For application of the device as transformer differential protection, ratio correction is required. This is achieved simply by setting of the reference power generally to the nominal power of the transformer and of the primary nominal voltages for all windings of the transformer. To minimize unbalance due to tap changer operation, current inputs to the differential element should be matched for the mid-tap position and not the nominal voltage.
Vector group matching is achieved by input of the relevant vector group identification number. Zero-sequence current filtering is also available. For conditions where it is possible to temporarily load the transformer with a voltage in excess of the nominal voltage, the overfluxing blocking prevents unwanted tripping. The 5th harmonic blocking feature does not require a voltage signal. A 5th harmonic signal is derived from the differential current waveform on each phase and blocking is on a per phase basis. The overfluxing protection should be used in such applications to protect the transformer accordingly.
For applications as a differential protection device for motors, the second harmonic blocking (inrush compensation) can be set to maximum. The start-up of directly switched asynchronous motors represents a problem in differential protection due to transient transformer saturation caused by a displacement of the start-up current for relatively high primary time constants. The P64x uses transient bias to reduce the effects of CT saturation.

2.1.1 Enabling or Disabling Differential Protection

Differential protection can be disabled or enabled from the local control panel. Moreover, enabling can be done separately for each setting group.

To enable the differential protection, set the cell [090C: Diff Protection] to **enabled** under the **CONFIGURATION** menu heading. Also the differential function must be enabled in the required setting group, for example, set the cell [3101: Trans Diff] to **enabled** under **GROUP 1 DIFF PROTECTION** menu heading. This enables setting group1 differential protection.

2.1.2 Current Inputs Selection

The current inputs associated to each transformer winding are set in HV CT Terminals, LV CT Terminals and TV CT Terminals.
The current inputs may be assigned as follows:

	P642	P643	P645
HV CT Terminals	01	001 011	00001 00011 00111 01011 01111
LV CT Terminals	10	100 110	10000 11000 11100 11010 11110
TV CT Terminals		010	00100 01100 00110 01110

Table 2 - Current inputs

The CT inputs are as follows:

- 1 means that the CT input is being used by the xx CT Terminals
- 0 means that the CT input is not being used by the xx CT Terminals

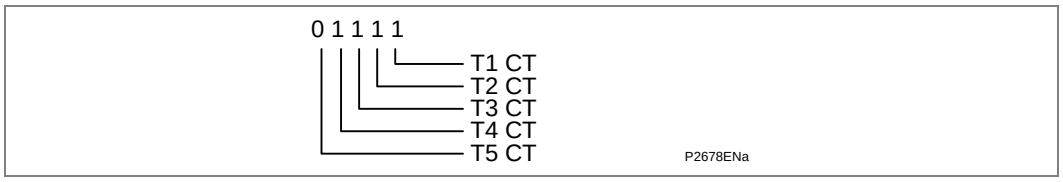


Figure 1 - CT inputs

If any CT is assigned to more than one winding, then a CT selection alarm is issued (DDB 483). When DDB 483 is asserted, the protection is also blocked (see the CT selection diagram).

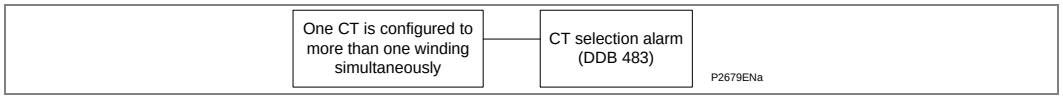


Figure 2 - CT selection diagram

2.1.3 Ratio Correction

The relay automatically calculates the ratio correction factor for each of the current inputs. The matching factors are displayed under **GROUP x SYSTEM CONFIG** menu heading as **Match Factor CT1**, **Match Factor CT2**, **Match Factor CT3**, **Match Factor CT4** and **Match Factor CT5**. The reference power for the protected object, identical for all windings, needs to be defined. For two-winding arrangements, the nominal power will usually be the reference power. For three transformers, the nominal power of the highest-power winding should be set as the reference power. The reference power is set in the cell [3007: Sref] under the **GROUP x SYSTEM CONFIG** menu heading.
The calculates the ratio correction factors on the basis of the reference power, winding nominal voltage, and primary nominal currents of the current transformers.

$$I_{ref,n} = \frac{S_{ref}}{\sqrt{3}\, V_{nom,n}} \qquad K_{amp,n} = \frac{I_{nom,n}}{\sqrt{\frac{S_{ref}}{3V_{nom,n}}}}$$

Sref: common reference power for all ends
n: is CT1 and CT2 (etc) for each of the available CT inputs
Iref, n: reference current for the respective CT input
Kamp, n: amplitude-matching factor for the respective CT input
Inom, n: primary nominal currents for the respective CT input
Vnom, n: primary nominal voltage for the respective CT input

The relay checks that the matching factors are within their permissible ranges. The matching factors must satisfy the following condition:

- The matching factors must always be $0.05 \leq Kamp,n \leq 20$

The *CT parameter mismatch logic diagram* is shown below.

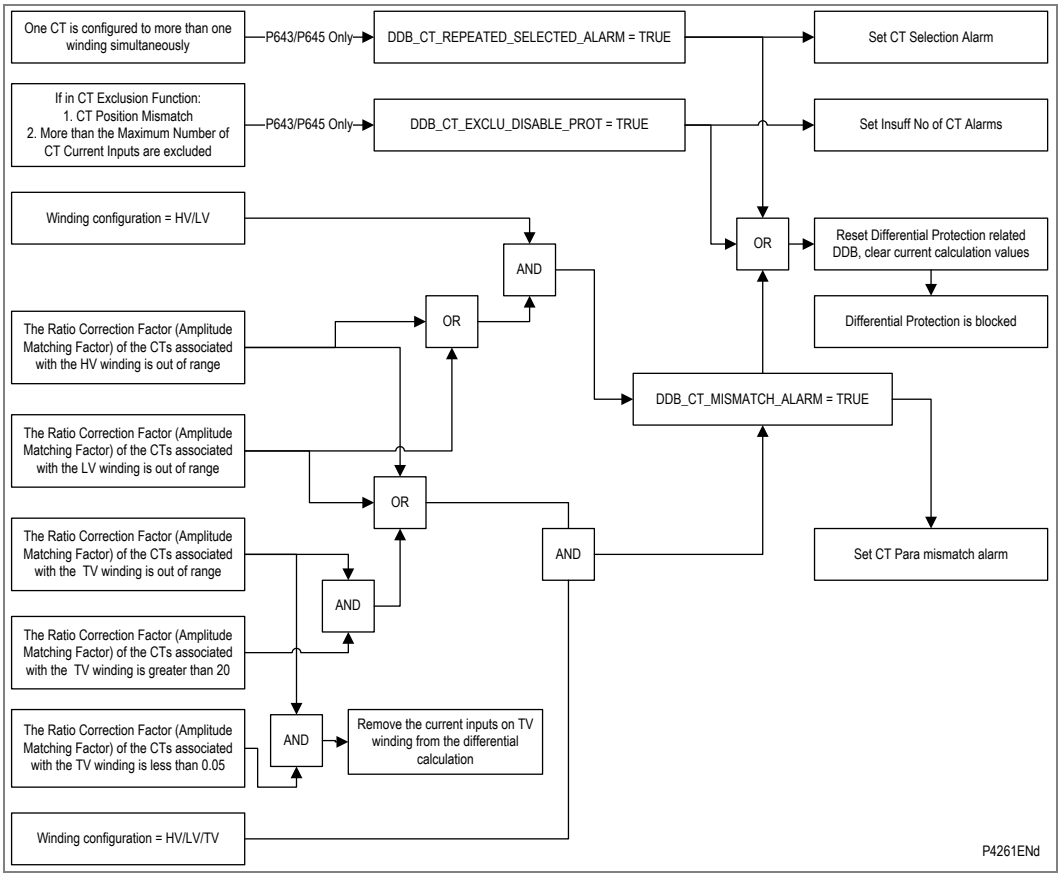


Figure 3 - CT para mismatch logic diagram

If any of the ratio correction factors in two winding applications is out of range, the CT para mismatch alarm is asserted. In three winding applications, if the ratio correction factor of the CTs associated to HV or LV windings are out of range or if the ratio correction factor of the CTs associated to TV winding is greater than 20, then the CT para mismatch alarm is asserted. **In some applications, if the ratio correction factor of the CT associated to TV winding is lower than 0.05, it may be preferred to automatically remove this current from the differential calculation. The logic shown in the diagram allows the relay to do so.**

If the CT para mismatch alarm is asserted the protection is also blocked.

The measured values of the phase currents of the windings of the protected object are multiplied by the relevant matching factors and are then available for further processing. Consequently, all threshold values and measured values always refer to the relevant reference currents rather than to the transformer nominal currents or the nominal currents of the device.

Caution	***If the CT para mismatch alarm is asserted, the differential protection will be blocked. Other protection functions will still be working.***

2.1.4 Vector Group Matching

The transformer HV windings are indicated by capital letters and the LV winding by lower case letters. The numbers refer to positions on a clock face and indicate the phase displacement of balanced 3-phase LV line currents with respect to balanced 3-phase HV line currents. The HV side is taken as reference and it is the 12 o'clock position. Therefore, each hour represents a 30° shift; i.e. 1 represents a 30° lag and 11 represents a 30° lead (LV with respect to HV). An additional N, YNd1, (lower case for LV, d) indicates a neutral to earth connection on the high voltage winding of the power transformer.

By studying the relative phase shifts that can be obtained, it can be seen that star-star windings allow even vector group configurations and star-delta/delta-star windings allow odd group configurations.

Examples

A YNd1 connection indicates a two winding transformer with an earthed, Star-connected, high voltage winding and a Delta-connected low voltage winding. The low voltage balanced line currents lag the high voltage balanced line currents by 30° (−30° phase shift).

A Dyn1yn11 connection indicates a three winding transformer with a Delta-connected high voltage winding and two earthed Star-connected low voltage windings. The phase displacement of the first LV winding with respect to the HV winding is 30° lag (−30° phase shift), the phase displacement of the second LV winding with respect to the HV winding is 30° lead (+30° phase shift).

Vector group matching is performed on the amplitude-matched phase currents of the *low-voltage* and *tertiary voltage* side in accordance with the characteristic vector group number.

When the relay is configured to protect a YNd1 transformer, the software interposing CTs used by the relay to achieve vector correction are as shown in the *Software interposing CTs for a Yd1 transformer* diagram. No vector correction is performed on the HV amplitude matched phase currents. If the relay is in simple mode, zero sequence filtering is applied when the cell **[HV Grounding]** under the **GROUP 1 SYSTEM CONFIG** menu heading is set to grounded. If the relay is in advanced mode, the zero sequence filtering is enabled or disabled in the cell [Zero seq filt HV] under the **GROUP 1 DIFF PROTECTION** menu heading. Therefore, on the Y high voltage side of the transformer the software interposing CT is either Yy0 (no zero sequence filtering is required) or Ydy0 (zero sequence filtering is required). The currents on the low voltage side lag by 30° the currents on the high voltage side due to the vector group (1). The relay brings the low voltage current in phase with the high voltage current by using a Yd11 software interposing CT on the low voltage side.

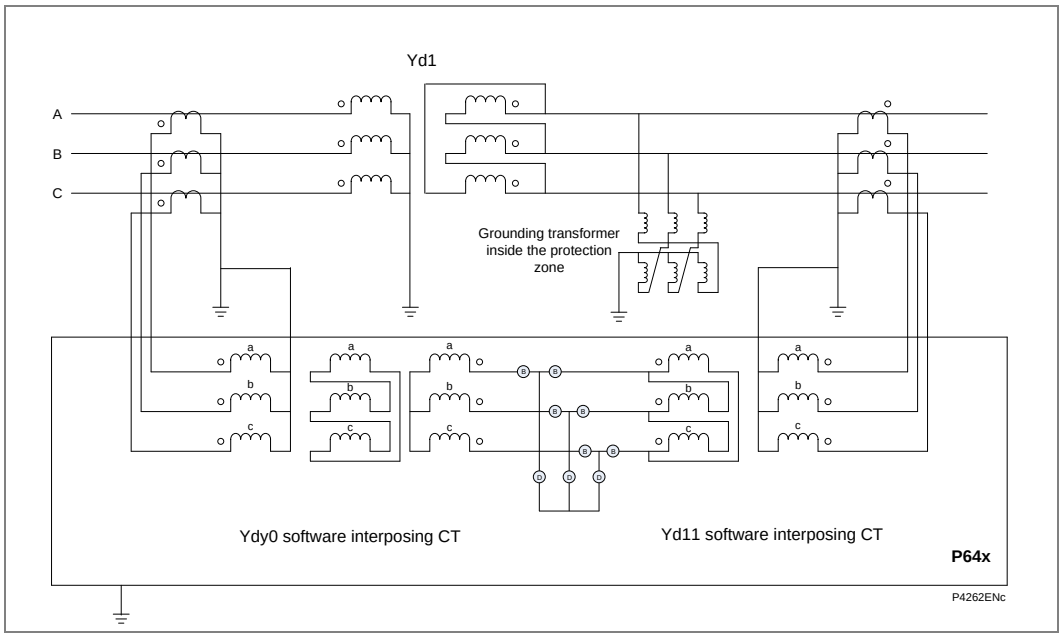


Figure 4 - Software interposing CTs for a Yd1 transformer

Consider the Y grounded winding of the Yd1 transformer during external ground faults on the high voltage side. Also consider that a source is connected to the delta side. The zero sequence component of the fault current flows through the grounded neutral that lies inside the transformer differential protection zone. The zero sequence component of the fault current is only seen by the CTs in the HV side. Therefore, zero sequence filtering for a Y grounded winding must be enabled to avoid undesirable tripping when an external ground fault occurs.

The Ydy0 software interposing CT is the equivalent of subtracting the zero sequence component from the phase currents on the high voltage side. The zero-sequence current is determined as follows from the amplitude-matched phase currents:

$$I_{amp,zero,n} = \frac{1}{3}\left(I_{amp,A,n} + I_{amp,B,n} + I_{amp,C,nC}\right)$$

$$I_{amp,A,n,filtered} = I_{amp,A,n} - I_{amp,zero,n}$$

n:	T1 CT, T2 CT, T3 CT, T4 CT, T5 CT for each of the CT inputs
Iamp, zero, n:	zero sequence amplitude matched current for the respective CT input
Iamp, A, n:	phase A amplitude matched current of the respective CT input

The grounding transformer connected to the LV side of the power transformer provides a path for LV ground faults. To avoid misoperation during external ground faults the zero sequence component needs to be filtered. In addition, the LV currents need to be in phase with the HV currents. The relay achieves zero sequence filtering and vector correction by using a Yd11 software interposing CT.

As previously discussed, star-star windings allow even vector group configurations and star-delta/delta-star windings allow odd group configurations. The following tables show that for all odd-numbered vector group characteristics the zero-sequence current on the low-voltage side is basically always filtered out, whereas for even-numbered vector group characteristics the zero-sequence current on the low-voltage side is never filtered out automatically. The latter is also true for the high-voltage side since in that case, as explained above, no vector correction is performed.

Vector group matching and zero-sequence current filtering must always be viewed in combination. The following tables list the mathematical phasor operations executed by the relay during vector correction.

- Table 3 - Mathematical phasor operations on the HV side
- Table 4 - Phasor operations on LV side of an even-numbered vector group

- Table 5 - Phasor operations on LV side of an odd-numbered vector group

The indices in the formulae have the following meaning:

am: amplitude-matched
s: amplitude- and vector group-matched
x: phase A, B or C
y: differential measuring system that corresponds to phases A, B or C.
n: T1 CT, T2 CT, T3 CT, T4 CT, T5 CT for each of the CT inputs
x+1: cyclically lagging phase
x-1: cyclically leading phase

No vector correction is done on the HV side of the transformer. Only zero sequence filtering is carried on if in the simple mode the winding is set as grounded or if in the advanced mode the high voltage zero sequence filter is enabled. As a result, the relay may perform the following mathematical operations on the HV side:

	With I_{zero} filtering	Without I_{zero} filtering
0	$I_{vec,y,n} = I_{amp,x,n} - I_{amp,zero,n}$	$I_{vec,y,n} = I_{amp,x,n}$

Table 3 - Mathematical phasor operations on the HV side

The following *Yy transformer connections* diagram shows the various even-numbered vector group configurations:

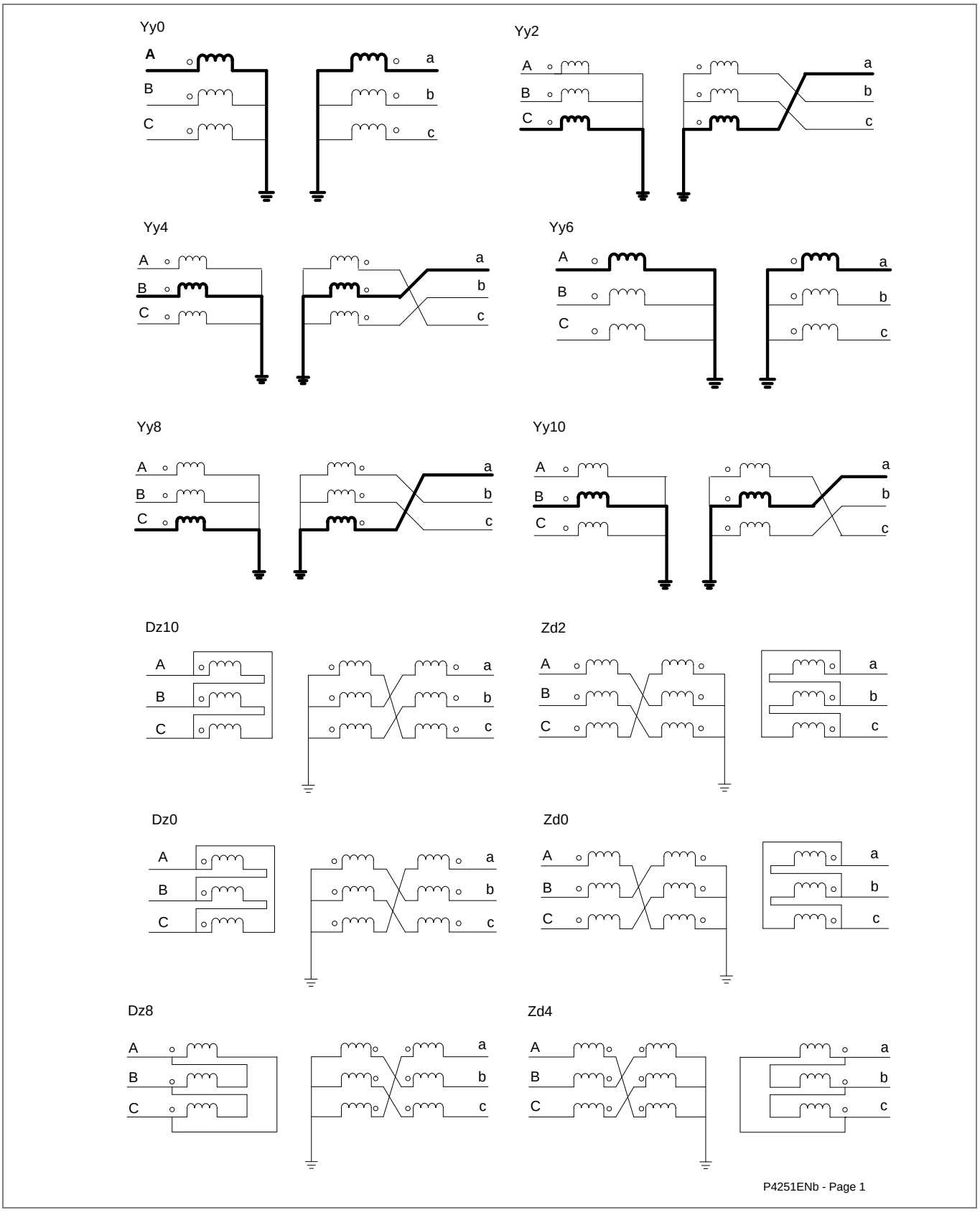


Figure 5 - Even-numbered vector groups - Page 1

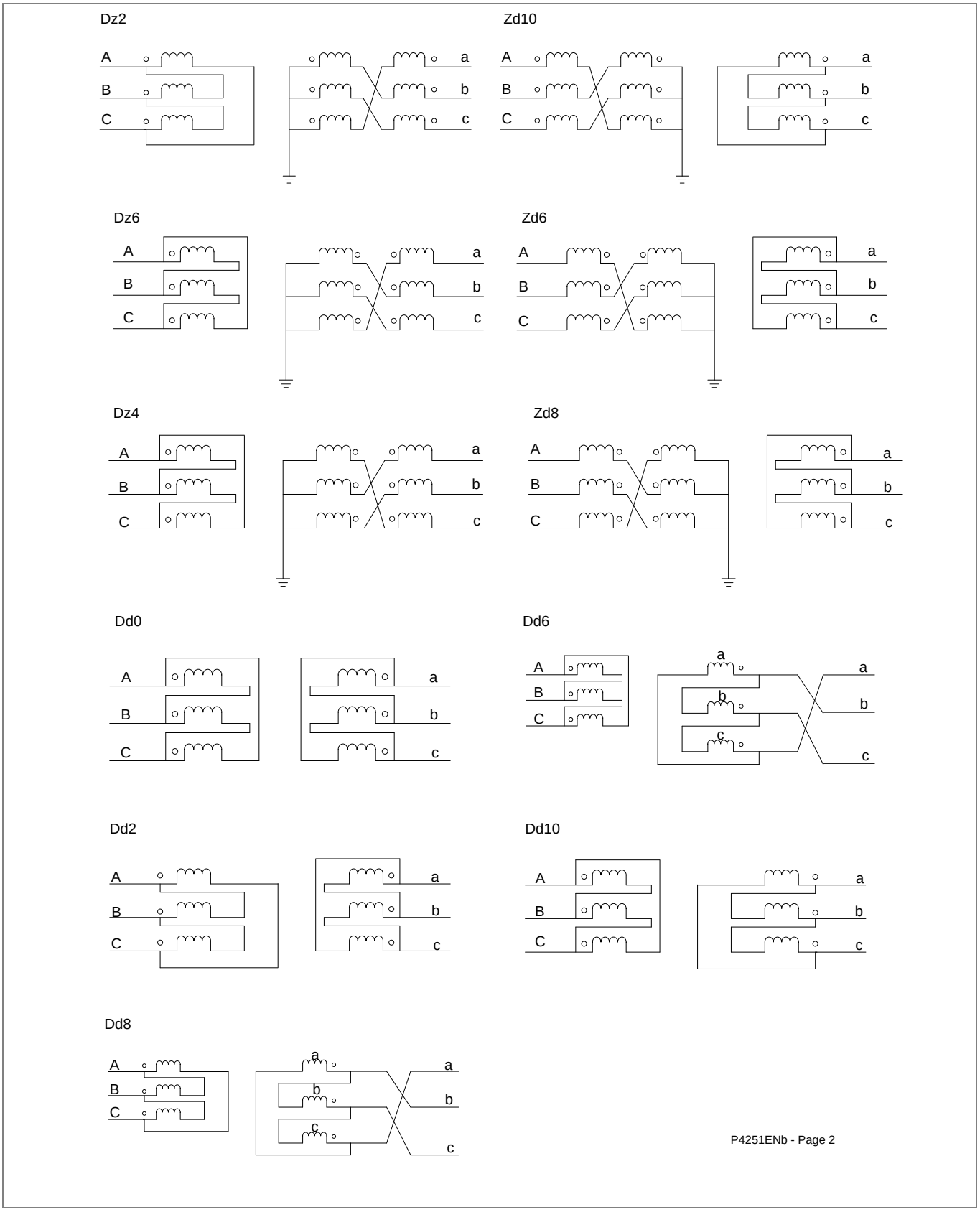


Figure 6 - Even-numbered vector groups - Page 2

Consider the configurations as shown in the above *Yy transformer connections* diagram.

- In a Yy0, Dd0, Dz0 or Zd0 power transformer configuration, the LV currents are already in phase with the HV currents. Therefore, the relay only filters the zero sequence current as required.
- In a Yy2, Dd2, Dz2 or Zd2 power transformer configuration, the LV currents lag the HV currents by 60°. To bring the LV currents in phase with the HV currents, the P64x uses a Yy10 software interposing CT.
- In a Yy4, Zd4 or Dz4 power transformer configuration, the LV currents lag the HV currents by 120°. To bring the LV currents in phase with the HV currents, the P64x uses a Yy8 software interposing CT.
- In a Yy6, Dz6, Zd6 or Dd6 power transformer configuration, the LV currents lag the HV currents by 180°. To bring the LV currents in phase with the HV currents, the P64x uses a Yy6 software interposing CT.
- In a Yy8, Dz8, Zd8 or Dd8 power transformer configuration, the LV currents lead the HV currents by 120°. To bring the LV currents in phase with the HV currents, the P64x uses a Yy4 software interposing CT.
- In a Yy10, Dz10, Zd10 or Dd10 power transformer configuration, the LV currents lead the HV currents by 60°. To bring the LV currents in phase with the HV currents, the P64x uses a Yy2 software interposing CT.

The following *Phasor operations on the LV side of Yy power transformers* table shows the mathematical operations, equivalent to the corresponding software interposing CT, on the low-voltage side for an even-numbered vector group characteristic.

VG	With $\underline{I}_{zero}$ filtering	Without $\underline{I}_{zero}$ filtering
0	$I_{vec,y,n} = I_{amp,x,n} - I_{amp,zero,n}$	$I_{vec,y,n} = I_{amp,x,n}$
2	$I_{vec,y,n} = -\left(I_{amp,x+1,n} - I_{amp,zero,n}\right)$	$I_{vec,y,n} = -I_{amp,x+1,n}$
4	$I_{vec,y,n} = I_{amp,x-1,n} - I_{amp,zero,n}$	$I_{vec,y,n} = I_{amp,x-1,n}$
6	$I_{vec,y,n} = -\left(I_{amp,x,n} - I_{amp,zero,n}\right)$	$I_{vec,y,n} = -I_{amp,x,n}$
8	$I_{vec,y,n} = I_{amp,x+1,n} - I_{amp,zero,n}$	$I_{vec,y,n} = I_{amp,x+1,n}$
10	$I_{vec,y,n} = -\left(I_{amp,x-1,n} - I_{amp,zero,n}\right)$	$I_{vec,y,n} = -I_{amp,x-1,n}$

Table 4 - Phasor operations on LV side of an even-numbered vector group

The following *Software interposing CTs for a Yy0 transformer* diagram shows the software interposing CTs used by the relay when a Yy0 power transformer is being protected. Notice that zero sequence filter is enabled on the HV and LV sides since Ydy0 interposing CTs are being used.

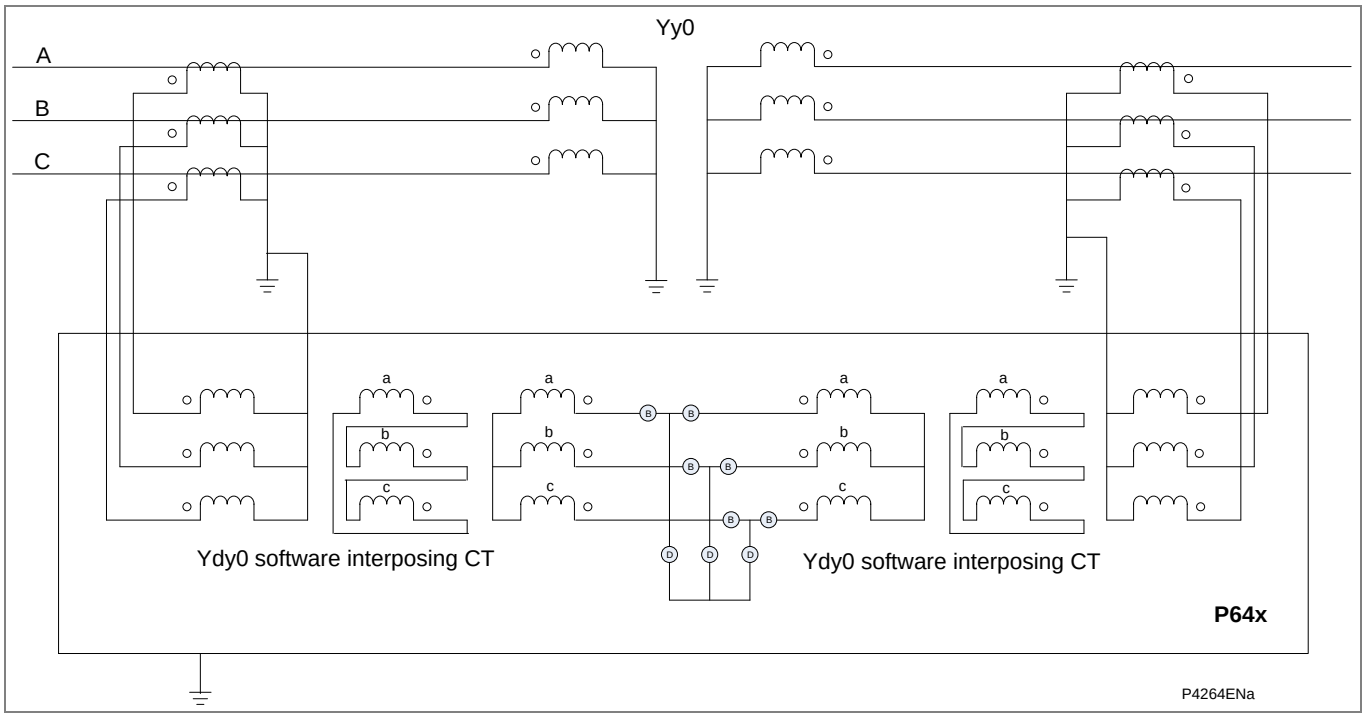


Figure 7 - Software interposing CTs for a YNyn0 transformer

The following *Yd or Dy transformer connections* diagram shows the various odd-numbered vector group configurations:

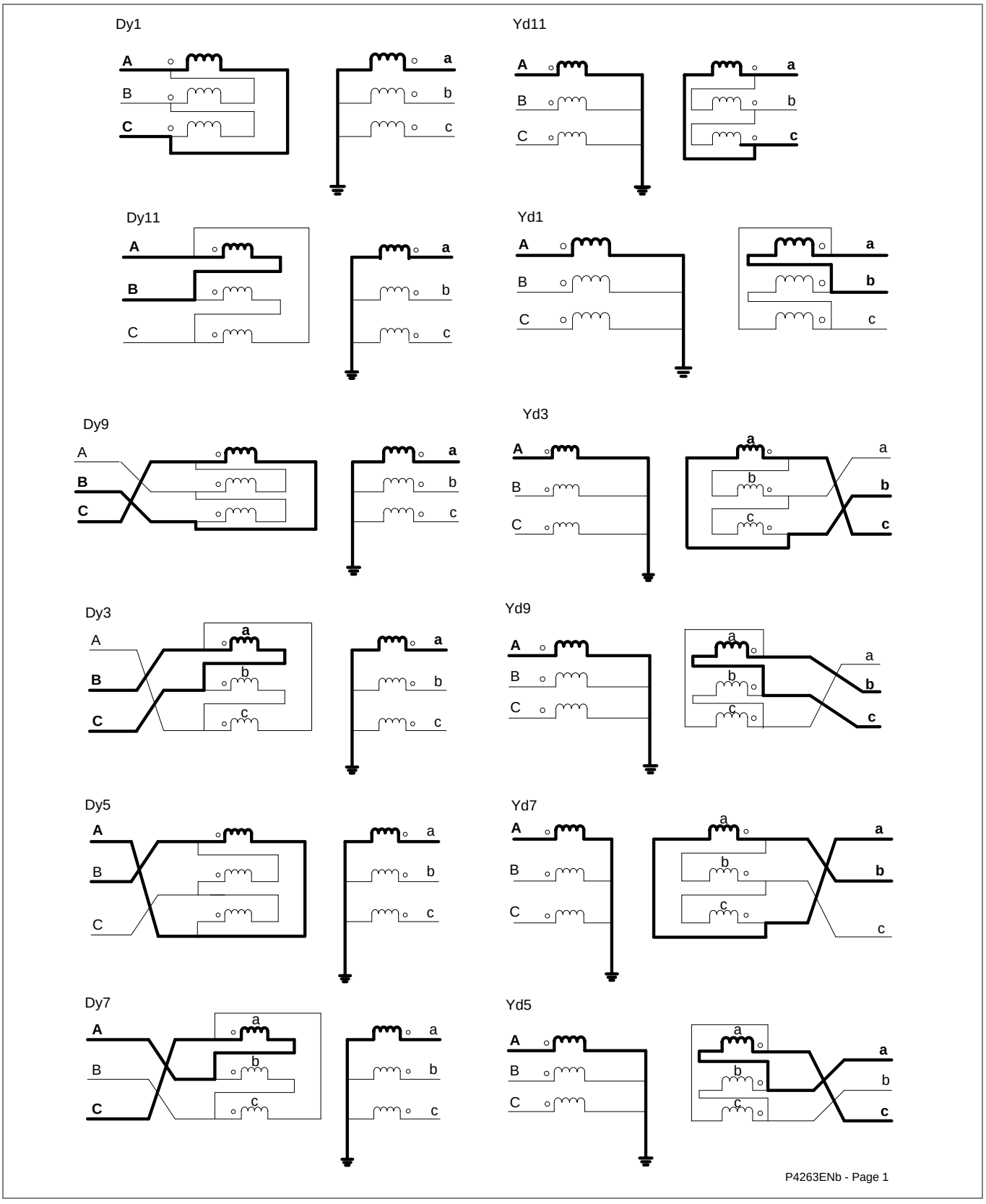


Figure 8 - Odd-numbered vector group connections - Page 1

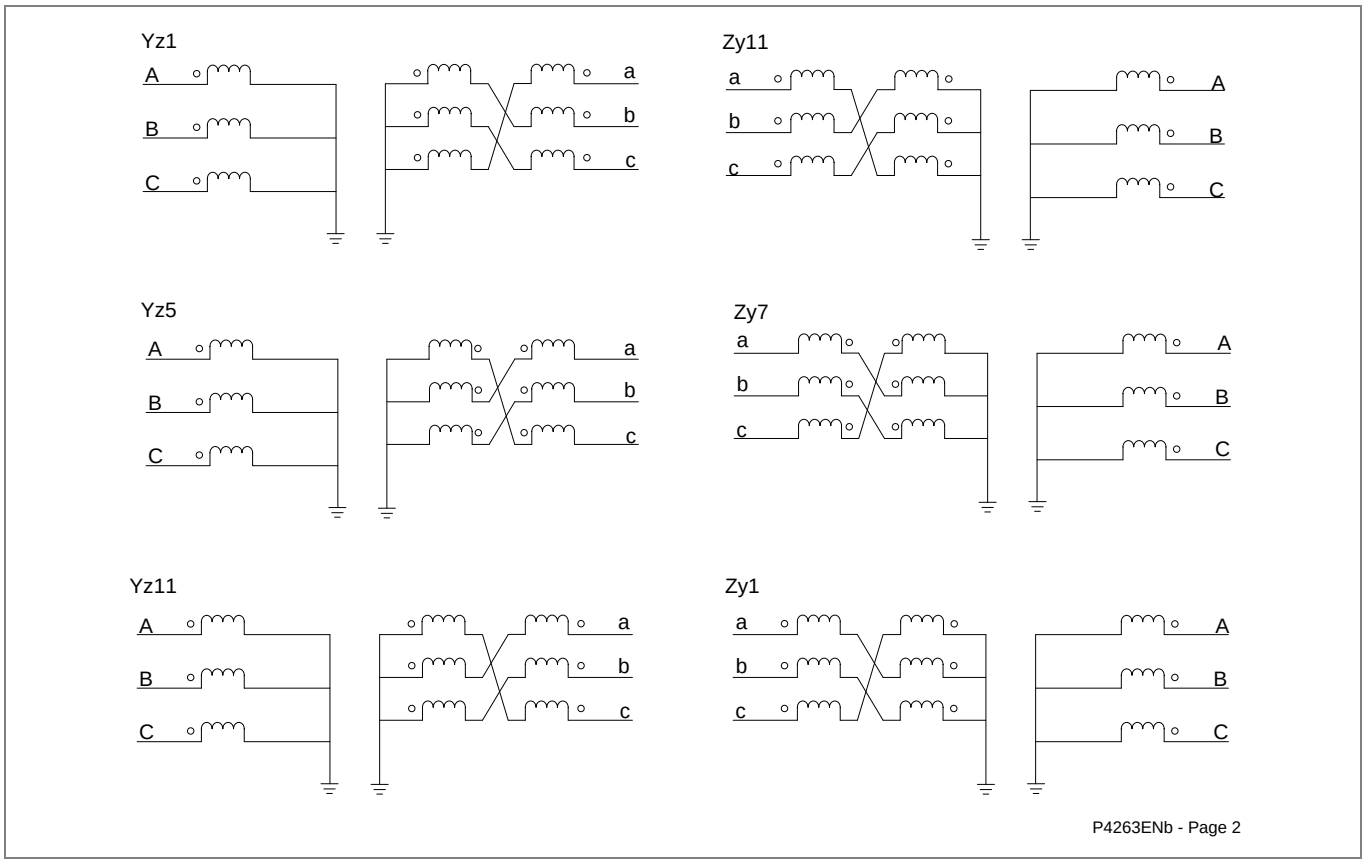


Figure 9 - Odd-numbered vector group connections - Page 2

Consider the configurations shown in the above *Yd or Dy transformer connections* diagram.

- In a Dy1, Yd1, Yz1 or Zy1 power transformer configuration, the LV currents lag the HV currents by 30°. The P64x uses a Yd11 software interposing CT to bring the LV currents in phase with the HV currents.
- In a Dy3 or Yd3 power transformer configuration, the LV currents lag the HV currents by 90°. The P64x uses a Yd9 software interposing CT to bring the LV currents in phase with the HV currents.
- In a Dy5, Yd5 or Yz5 power transformer configuration, the LV currents lag the HV currents by 150°. The P64x uses a Yd7 software interposing CT to bring the LV currents in phase with the HV currents.
- In a Dy7, Yd7 or Zy7 power transformer configuration, the LV currents lead the HV currents by 150°. The P64x uses a Yd5 software interposing CT to bring the LV currents in phase with the HV currents.
- In a Dy9 or Yd9 power transformer configuration, the LV currents lead the HV currents by 90°. The P64x uses a Yd3 software interposing CT to bring the LV currents in phase with the HV currents.
- In a Dy11, Yd11, Yz11 or Zy11 power transformer configuration, the LV currents lead the HV currents by 30°. The P64x uses a Yd1 software interposing CT to bring the LV currents in phase with the HV currents.

The following *Phasor operations on the LV side of Yd or Dy power transformers* table shows the mathematical operations, equivalent to the corresponding software interposing CT, on the low-voltage side for an odd-numbered vector group characteristic:

VG	With or without I_{zero} filtering
1	$I_{vec,y,n} = \frac{1}{\sqrt{3}} \cdot \left(I_{amp,x,n} - I_{amp,x+1,n} \right)$
3	$I_{vec,y,n} = \frac{1}{\sqrt{3}} \cdot \left(I_{amp,x-1,n} - I_{amp,x+1,n} \right)$
5	$I_{vec,y,n} = \frac{1}{\sqrt{3}} \cdot \left(I_{amp,x-1,n} - I_{amp,x,n} \right)$
7	$I_{vec,y,n} = \frac{1}{\sqrt{3}} \cdot \left(I_{amp,x+1,n} - I_{amp,x,n} \right)$
9	$I_{vec,y,n} = \frac{1}{\sqrt{3}} \cdot \left(I_{amp,x+1,n} - I_{amp,x-1,n} \right)$
11	$I_{vec,y,n} = \frac{1}{\sqrt{3}} \cdot \left(I_{amp,x,n} - I_{amp,x-1,n} \right)$

Table 5 - Phasor operations on LV side of an odd-numbered vector group

Vector group matching is by input of the vector group identification number provided that the phase currents of the high and low voltage side(s) are connected in standard configuration. For other configurations, special considerations may apply. A reverse phase rotation (phase sequence A-C-B) needs to be taken into account by making the appropriate setting at the relay. The relay will then automatically form the complementary value of the set vector group ID to the number 12 (vector group ID = 12 - set ID).

2.1.5 Tripping Characteristics

The differential and bias currents for each phase are calculated from the current variables after amplitude and vector group matching.

Calculation of differential and biased currents is as follows:

$$I_{diff,y} = \left| \vec{I}_{s,y,CT1} + \vec{I}_{s,y,CT2} I + \vec{I}_{s,y,CT3} + \vec{I}_{s,y,CT4} + \vec{I}_{s,y,CT5} \right|$$

$$I_{bias,y} = 0.5 \left[\left| \vec{I}_{S,y,CT1} \right| + \left| \vec{I}_{S,y,CT2} \right| + \left| \vec{I}_{S,y,CT3} \right| + \left| \vec{I}_{S,y,CT4} \right| + \left| \vec{I}_{S,y,CT5} \right| \right]$$

y is the measuring system that corresponds to phases A, B or C.
s is the current after the amplitude and vector group are matched.
To provide further stability for external faults, additional measures are considered on the calculation of the bias current:

2.1.5.1 Delayed Bias

The bias quantity is the maximum of the mean bias quantities calculated within the last cycle. The mean bias is the fundamental bias current. This is to maintain the bias level, therefore stability is provided when an external fault is cleared. This feature is implemented on a per-phase basis. The algorithm is expressed as follows; the function is executed 8 times per cycle:

$I_{Bias\ A\_delayed}$ = Maximum [$I_{bias,\ A}(n)$, $I_{bias,\ A}(n-1)$, ..., $I_{bias,\ A}(n-7)$]

$I_{Bias\ B\_delayed}$ = Maximum [$I_{bias,\ B}(n)$, $I_{bias,\ B}(n-1)$, ..., $I_{bias,\ B}(n-7)$]

$I_{Bias\ C\_delayed}$ = Maximum [$I_{bias,\ C}(n)$, $I_{bias,\ C}(n-1)$, ..., $I_{bias,\ C}(n-7)$]

2.1.5.2 Maximum Bias

The maximum delayed bias current calculated from all three phases is the maximum bias:

$I_{bias,max}$ = Maximum [$I_{biasA\_delayed}$, $I_{biasB\_delayed}$, $I_{biasC\_delayed}$]

The maximum bias is used to calculate the differential operating current. The differential operating current is calculated using the following characteristic equations:

Characteristic equation for the range $0 \leq I_{biasmax} \leq \frac{I_{s1}}{K_1}$

$I_{op} = I_{s1}$

Characteristic equation for the range $\frac{I_{s1}}{K_1} \leq I_{biasmax} \leq I_{s2}$

$I_{op} = K_1\ I_{biasmax}$

Characteristic equation for the range $I_{biasmax} \geq I_{s2}$

$I_{op} = K_1\ I_{s2} + K_2\ (I_{biasmax} - I_{s2})$

K_1 gradient of characteristic in range $\frac{I_{s1}}{K_1} \leq I_{biasmax} \leq I_{s2}$

K_2 gradient of characteristic in range $I_{biasmax} \geq I_{s2}$

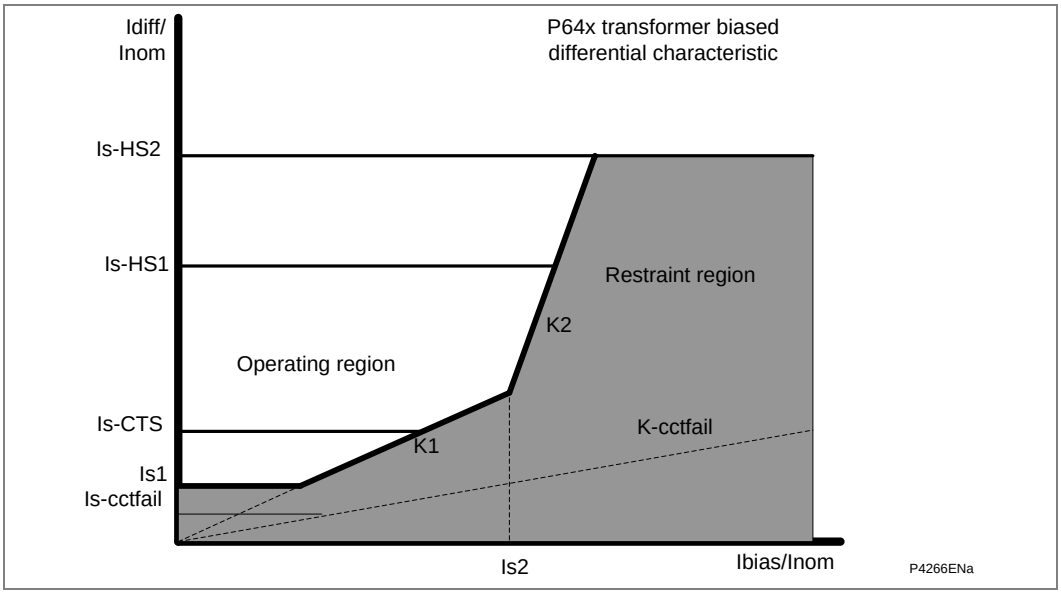


Figure 10 - Tripping characteristic of differential protection

The tripping characteristic of the differential protection device P64x has two knees. The first knee is dependent on the settings of I_{s1} and K1. The second knee of the tripping characteristic is defined by the setting I_{s2}. The lower slope provides sensitivity for internal faults. The higher slope provides stability under through fault conditions, since transient differential currents may be present due to current transformer saturation.

2.1.5.3 Transient Bias

If there is a sudden increase in the mean-bias measurement, an additional bias quantity is introduced in the bias calculation, on a per-phase basis. This quantity, named transient bias, decays exponentially. The transient bias resets to zero once the relay trips, or if the mean bias quantity is below the Is1 setting. The mean bias is the fundamental of the bias current. As explained in the *Maximum Bias* section the relay calculates the operating current at the maximum bias current. The transient bias is calculated on a per phase basis and it is added to the operating current calculated at the maximum bias. Therefore, these differential current thresholds are available:

Differential threshold phase A = Iop at max bias + transient bias_phase A

Differential threshold phase B = Iop at max bias + transient bias_phase B

Differential threshold phase C = Iop at max bias + transient bias_phase C

The fundamental of the differential current is compared against the differential current threshold given above on a per phase basis. The relay calculates the differential current on a sample basis using the following equation:

$$I_{diff,y} = \left| \overrightarrow{I_{s,y,T1\ CT}} + \overrightarrow{I_{s,y,T2\ CT}} + \overrightarrow{I_{s,y,T3\ CT}} + \overrightarrow{I_{s,y,T4\ CT}} + \overrightarrow{I_{s,y,T5\ CT}} \right|$$

The relay calculates the fundamental of the differential current using a Fourier filter.

If the fundamental of the differential current is above the threshold, then the low set differential element might trip as long as there is no second harmonic or fifth harmonic blocking.

The transient bias technique considers a time decay constant, stability coefficients and the differential function settings to provide a dynamic bias characteristic. The following diagram shows the relay behavior during an external fault. The transient bias enhances relay stability. For the relay to trip, the fundamental of the differential current should be above the operating current at max bias + transient bias.

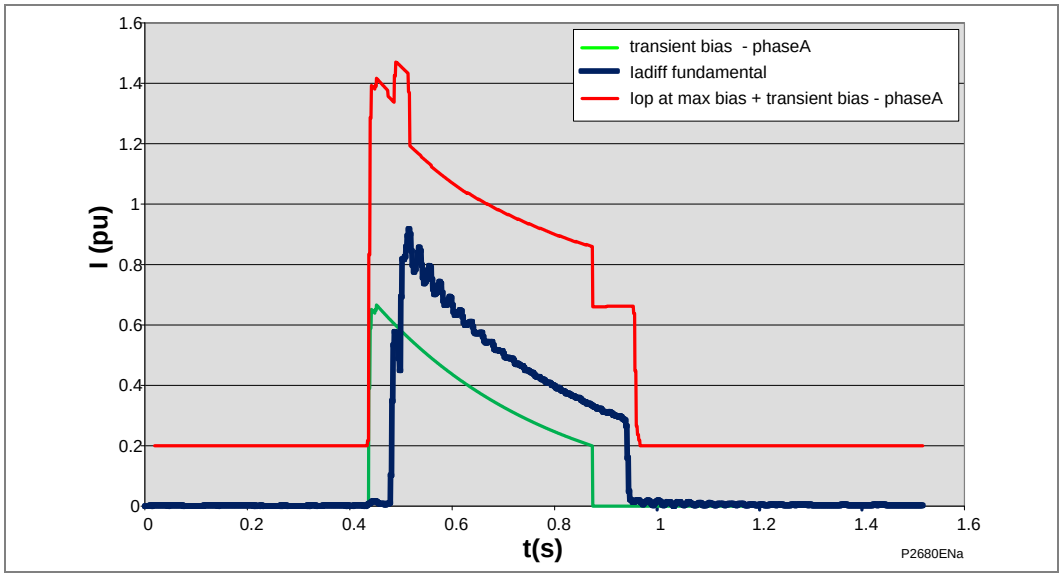


Figure 11 - Transient bias characteristic

The transient bias enhances the stability of the differential element during external faults and allows for the time delay in CT saturation caused by small external fault currents and high X/R ratios. For internal single-end or double-end fed faults the differential current is dominant and the transient bias has no effect.

The transient bias is removed after the relay has tripped to avoid the possibility of chattering. It is also removed when Ibias is less than Is1 to avoid the possibility of residual values due to the numerical effects.

No transient bias is produced under load switching conditions. Also, no transient bias is generated when the CT comes out of saturation.

2.1.6 High-Set Differential Protection Function

The high set 1 algorithm uses a peak detection method to achieve fast operating times. The peak value is the largest absolute value in the latest 24 samples (latest cycle). Since the high set 1 algorithm uses a peak detection method, **Is-HS1** is set above the expected highest magnetizing inrush peak to maintain immunity to magnetizing inrush conditions.

To declare high set 1 trip, two conditions must be fulfilled:

- The peak value of the differential current is greater than **Is-HS1** setting
- The bias characteristic is in the operating region

Above the adjustable threshold **Is-HS1** of the differential current, the relay will trip without taking into account either the second harmonic blocking or the overfluxing blocking, but the bias current is considered. The high set 1 resets when the differential and bias currents are in the restraint area (i.e. the gray area in the *Tripping characteristic of differential protection* diagram).

The high set 2 algorithm uses Fourier quantities. If the differential current exceeds the adjustable threshold **Is-HS2**, the bias current, the second harmonic and overfluxing restraints are no longer taken into account. As a result, the relay issues a high set 2 trip regardless of the harmonic blocking or biased current. The high set 2 element resets when the differential current drops below 0.95*Is-HS2.

2.1.7 Low-Set Differential Protection Function

Transient bias is added for through fault stability. The transient bias is on a per-phase basis and is not affected by K1 or K2 settings.

Once the differential and bias currents are calculated, the following comparisons are made and an operate/restrained signal is obtained:

Flat slope:

$I_{diff} \geq I_{s1}$ + Transient Bias

K1 slope:

$I_{diff} \geq K_1 I_{biasmax}$ + Transient Bias

K2 slope: $I_{bias} \geq I_{s2}$

$I_{diff} \geq K_1 I_{s2} + K_2 (I_{biasmax} – I_{s2})$ + Transient Bias

A count strategy is used so that the protection operates slower near the boundary of operation. This approach is used to stabilize the relay under some marginal transient conditions. The protection trips on a count of 2, which is approximately 5 ms after fault detection. The count is increased to 4 if the differential current is within 0.5*Is1 of the threshold.

2.1.8 Magnetizing Inrush Current Blocking

The phenomenon of magnetizing inrush is a transient condition which occurs primarily when a transformer is energized. It is not a fault condition, and therefore does not require the operation of the protection, which, on the contrary must remain stable during the inrush transient.

Magnetizing inrush can occur under three conditions:

- Initial
- Recover
- Sympathetic

Initial Magnetization Inrush:

The initial magnetizing inrush may occur when energizing the transformer after a prior period of de-energization. This has the potential of producing the maximum magnetizing inrush.

The following diagram shows a transformer magnetizing characteristic. To minimize material costs, weight and size, transformers are generally operated near to the knee point of the magnetizing characteristic. Consequently, only a small increase in core flux above normal operating levels will result in a high magnetizing current.

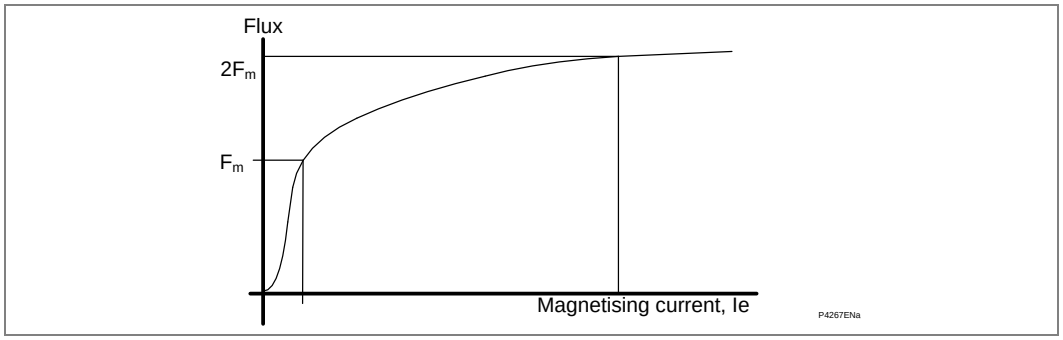


Figure 12 - Transformer magnetizing characteristic

Under normal steady state conditions, the magnetizing current associated with the operating flux level is relatively small (2-5% of full load current). However, if a transformer winding is energized at a voltage zero, with no remnant flux, the flux level during the first voltage cycle (2 x normal max flux) will result in core saturation and in a high, non-sinusoidal magnetizing current waveform. This current is commonly referred to as magnetizing inrush current and may persist for several cycles. The maximum initial-magnetizing current may be as high as 8-30 times the full-load current. Resistance in the supply circuit and transformer and the stray losses in the transformer reduce the peaks of the inrush current such that it decays to the normal exciting current value. The time constant varies from 10 cycles to as long as 1 minute in very high inductive circuits. The following diagram shows the magnetizing inrush phenomenon.

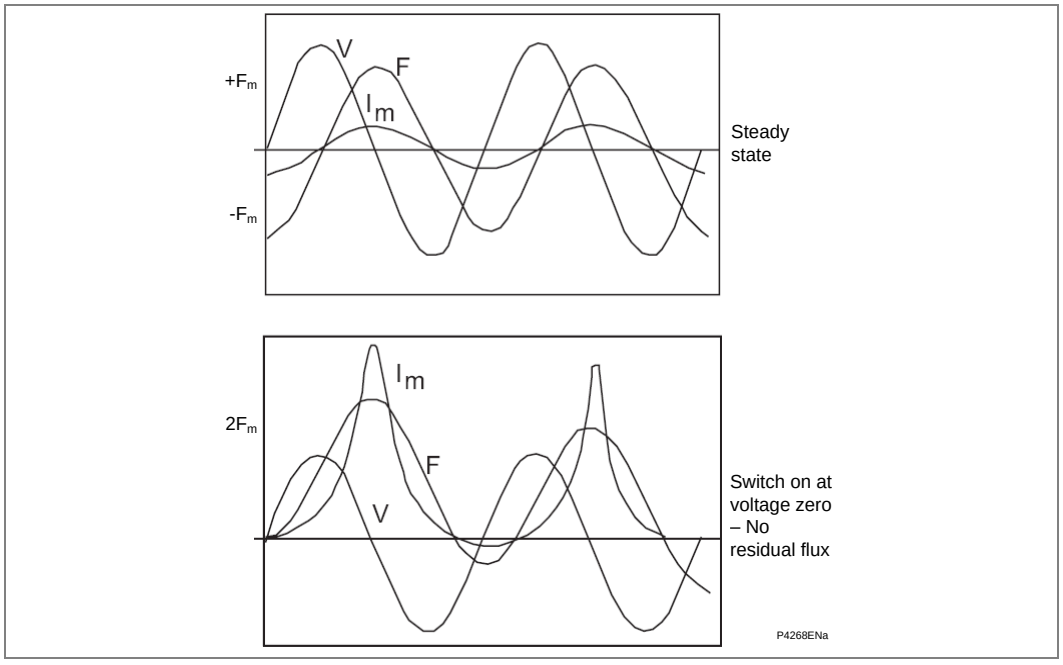


Figure 13 - Magnetizing inrush phenomenon

The magnitude and duration of magnetizing inrush current waveforms are dependant on a number of factors such as transformer design, size, system fault level, point on wave of switching, number of banked transformers etc.

Some inrush will always occur in one or two phases and generally all three phases in a three phase circuit. The following diagram indicates typical magnetizing inrush wave forms as seen by the differential protection.

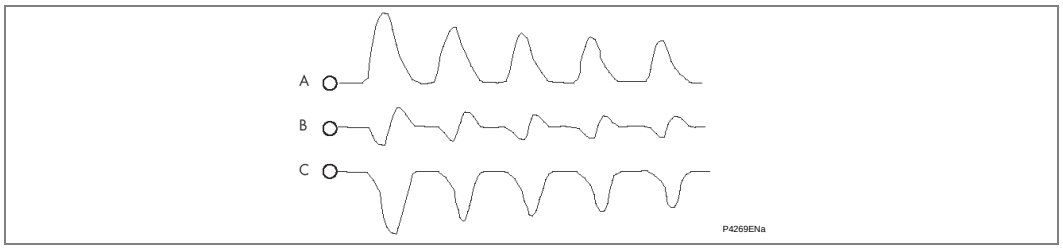


Figure 14 - Magnetizing inrush current waveforms

Recovery magnetizing inrush:

As stated in IEEE Std. C37.91-2000, magnetizing inrush can be caused by any abrupt change of magnetizing voltage. These include the occurrence of a fault, the removal of the fault, change of character of a fault (a single phase fault evolving to two phase fault). The recovery inrush is when the voltage returns back to normal. The worst case of recovery inrush occurs after a solid three phase external fault near a transformer bank is removed and the voltage gets back to normal.

Sympathetic magnetizing inrush:

According to IEEE Std. C37.91-2000, a severe magnetizing inrush may occur when energizing a transformer at a station at which at least one other transformer is already energized. This inrush will involve transformers that are already energized as well as transformers being energized. This inrush transient may be particularly long in duration. The inrush into the transformer being energized occurs during the opposite half-cycle to that of the already energized transformer. Therefore, the net inrush into all transformers may approximate a sine wave of fundamental frequency, and therefore not operate the second harmonic blocking unit of the differential relay if it is protecting both parallel transformers.

As described above, when an unloaded transformer is energized, the inrush current at unfavorable points on wave such as for voltage zero may have values that exceed the transformer nominal current several times over. Since the high inrush current flows on the connected side only, the tripping characteristic of differential protection may give rise to a trip unless stabilizing action is taken. The fact that the inrush current has a high proportion of second harmonics offers a possibility of stabilization against tripping by the inrush current.

The MiCOM relay filters the differential current. The fundamental $I_{diff}(fn)$ and second harmonic components $I_{diff}(2*fn)$ of the differential current are determined. Second harmonic blocking is phase segregated. If the ratio $I_{diff}(2*fn)/I_{diff}(fn)$ exceeds a specific adjustable value in at least one phase in two consecutive calculations, and if the differential current is larger than 0.1 pu (minimum setting of Is1), tripping is blocked optionally in one of the following modes:

- Across all three phases
- Selectively for one phase

There will be no blocking if the differential current exceeds the set thresholds **Is-HS1** or **Is-HS2**.

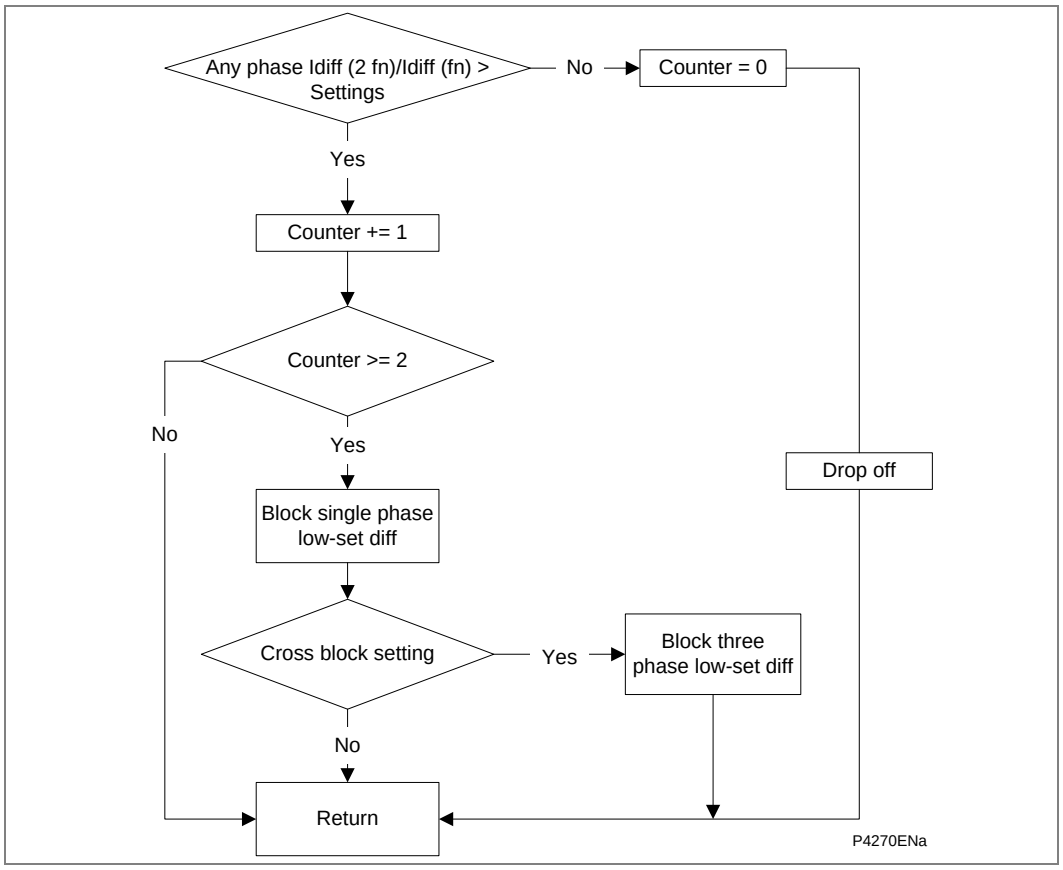


Figure 15 - Inrush stabilization (second harmonic blocking)

2.1.9 CT Saturation Detection

A CT saturation detection technique has been implemented in the P64x relay. This technique unblocks the low set differential element during internal faults with heavy CT saturation. During CT saturation the content of second harmonic may be high enough so that the second harmonic blocking element would be asserted thus blocking the low set differential element. As a result, the operation of the low set differential element is delayed. The CT saturation detection logic unblocks the low set differential element during CT saturation. During magnetizing inrush conditions, the ratio of second harmonic to fundamental is used to stabilize the relay. The CT saturation detection technique distinguishes between magnetizing inrush and saturation; therefore, the relay stability is maintained during inrush conditions.

To detect a CT saturation condition the differential current samples on a per phase basis are considered. The relay analyzes the differential current waveforms considering their derivatives, dynamic and fixed thresholds that were determined by Real Time Digital Simulator (RTDS) tests.

2.1.10 No Gap Detection Technique

The no gap detection technique detects light CT saturation on a per phase basis. During CT saturation the content of second harmonic may be high enough so that the second harmonic blocking element is asserted thus blocking the low set differential element. As a result, the operation of the low set differential element is delayed. The no gap detection technique unblocks the low set differential element during light CT saturation allowing the low set differential element to trip faster. Stability during inrush conditions is maintained, as this technique distinguishes between an inrush and a saturated waveform.

The no gap detection technique considers two dynamic thresholds. One is related to the gap region and the other to the wave width region of the differential current waveform. The derivatives of the differential current on a per phase basis are considered as well. To assert the no gap detection algorithm the following two conditions must be fulfilled:

- The number of continuous samples within a cycle above the dynamic gap threshold is below a fixed threshold.
- The number of continuous samples within a cycle above the dynamic wave width threshold is above a fixed threshold.

2.1.11 External Fault Detection Technique

An external fault detection technique has been implemented so that the CT saturation and No gap detection techniques do not affect the second harmonic blocking during an external fault.

The external fault detection technique considers the time to saturation, a delta bias start signal, a delta differential start signal and the ratio of delta differential to delta bias at the time of start. As soon as an external fault occurs, the bias current changes, but the differential current only increases after the time to saturation as shown in the following *Time to saturation - External AN fault* diagram. The external fault detection algorithm is asserted if the following conditions are fulfilled:

- The delta bias start signal is asserted first. The delta bias start signal and the delta differential start signal are asserted if the delta bias and delta differential currents are greater than 0.65Is1 respectively.
- The time difference between the assertion of the delta bias start signal and the assertion of the delta differential signal is greater than the time to saturation. The time to saturation in a 50Hz system is 2.5ms and it is 2.08ms in a 60Hz system.
- The ratio of delta differential to delta bias is smaller than a fixed threshold when the delta bias start signal is asserted.

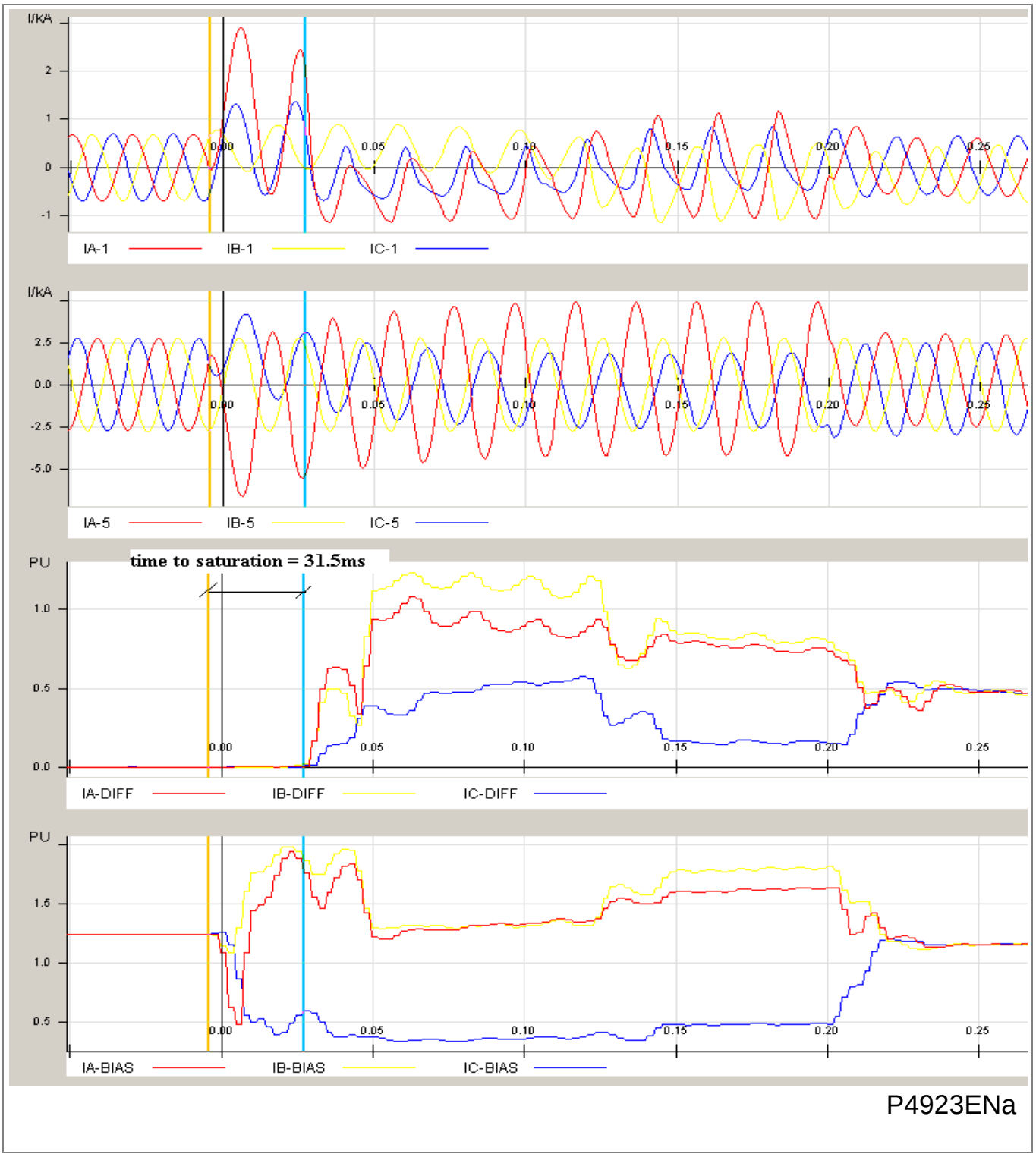


Figure 16 - Time to saturation - External AN fault

The external fault detection algorithm is on a per phase basis. If an external fault is detected on phase A, B or C, signals Ext Flt Phase A (DDB 839), Ext Flt Phase B (DDB 840) or Ext Flt Phase C (DDB 841) are asserted.

2.1.12 Differential Biased Trip Logic

The differential biased trip is affected by the CT saturation technique and by the no gap detection technique. If the second harmonic blocking is asserted and either the CT saturation detection or no gap detection technique is asserted, then the biased differential trip is unblocked. A biased differential trip will occur if the fifth harmonic blocking is not asserted and the bias differential start signal is asserted. The differential biased trip logic is described in this diagram:

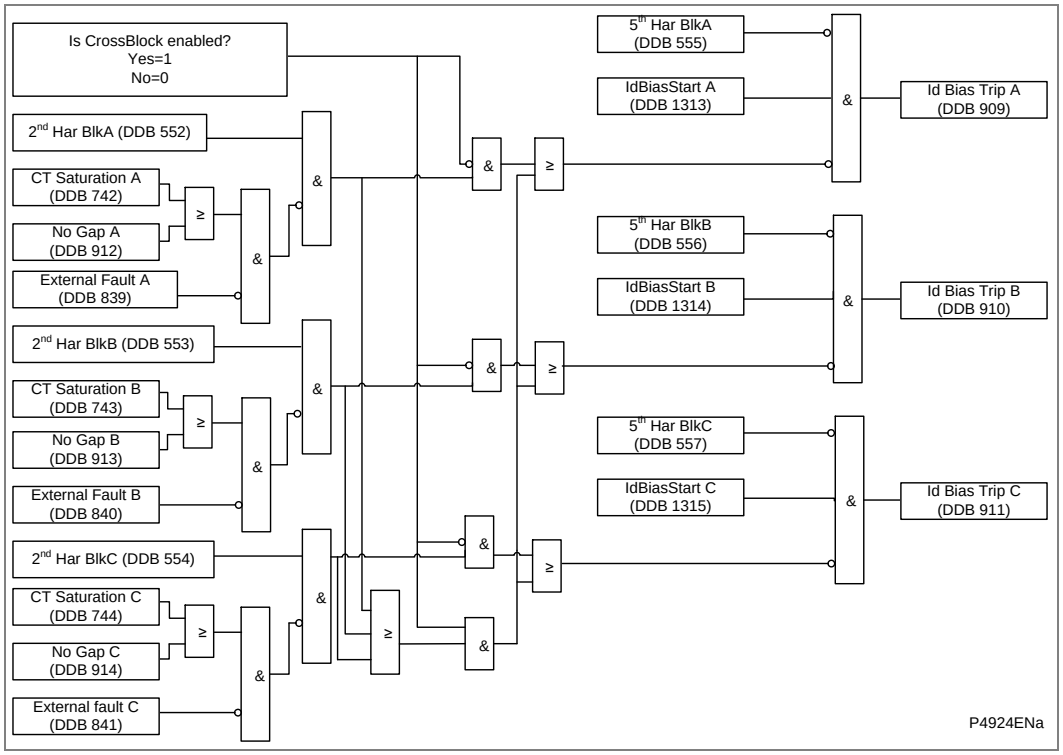


Figure 17 - Differential biased trip logic

2.1.13 Overfluxing Restraint

If the transformer is loaded with a voltage in excess of the nominal voltage, saturation effects occur. Without stabilization, these could lead to differential protection tripping. The fact that the current of the protected object under saturation conditions has a high proportion of fifth harmonic serves as the basis of stabilization.
The MiCOM relay filters the differential current and determines the fundamental component $I_{diff}(fn)$ and the fifth harmonic component $I_{diff}(5 \cdot fn)$. If the ratio $I_{diff}(5 \cdot fn)/I_{diff}(fn)$ exceeds the set value Ih(5)%> in at least one phase in two consecutive calculations, and if the differential current is larger than 0.1 pu (minimum setting of Is1), tripping is blocked selectively for one phase.
There will be no blocking if the differential current exceeds the set thresholds **Is-HS1** or **Is-HS2**.

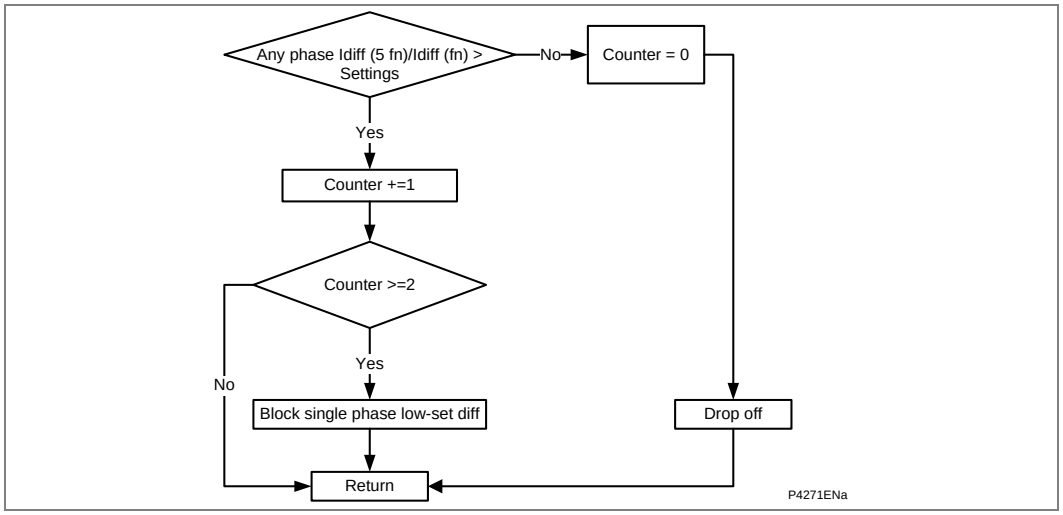


Figure 18 - Overfluxing restraint

The following logic diagram shows the inhibiting of the differential algorithm by magnetizing inrush or overfluxing conditions:

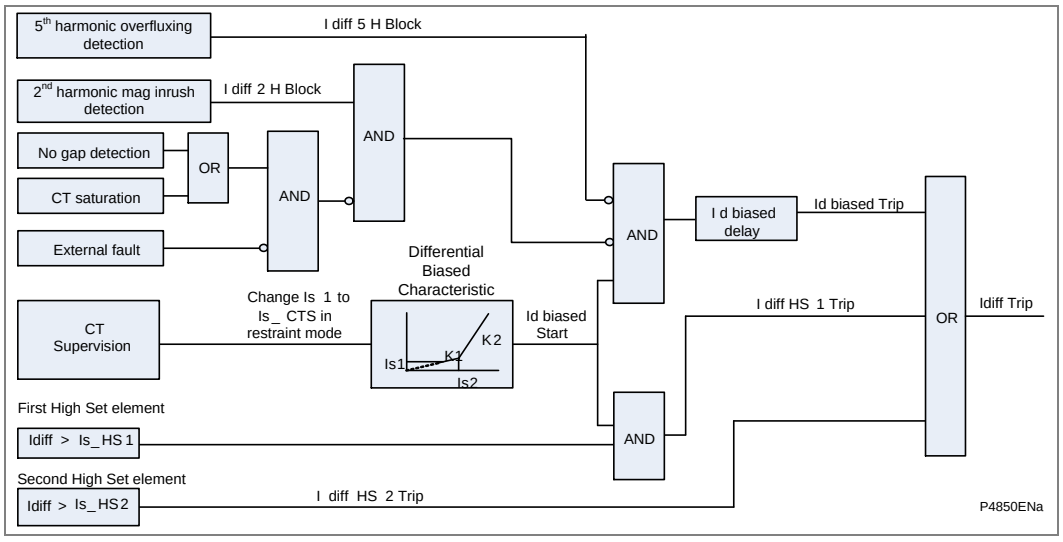


Figure 19 - Differential protection

2.2 Restricted Earth Fault (REF) Protection

The settings REF HV status, REF LV status, REF TV status and REF Auto can be set to disabled, low impedance REF or high impedance REF.

2.2.1 Low Impedance Restricted Earth Fault (REF)

A low impedance REF protection function per transformer winding is available for up to three ends. The low impedance REF uses a triple slope biased characteristic, the same as the differential current function. Low impedance REF is based on comparing the vector sum of the phase currents of the transformer winding to the neutral point current. The differential and bias currents are calculated from the current variables after scaling the phase currents.

If current transformer supervision operates, the low impedance REF is blocked. The activation of HV StubBus Act, LV StubBus Act or TV StubBus Act signals also blocks the low impedance REF on a per-winding basis.

In a biased differential relay, the through current is measured and used to increase the setting of the differential element. For heavy through faults, one CT in the scheme can be expected to become more saturated than the other and hence differential current can be produced. However, biasing increases the relay setting so the resulting differential current is insufficient to cause operation of the relay.

To provide further stability for external faults and CT saturation, a transient bias current is considered on the calculation of the operating current.

2.2.1.1 Single Breaker Applications

The calculation of differential and mean bias currents in single breaker applications is:

$$I_{bias} = \frac{1}{2}\left\{\max\left[\left|I_{A\,CT_n}\right|, \left|I_{B\,CT_n}\right|, \left|I_{C\,CT_n}\right|\right] + I_N \times K\right\}$$

$$I_{diff} = \left[\left(\vec{I}_{A\,CT_n} + \vec{I}_{B\,CT_n} + \vec{I}_{C\,CT_n}\right) + \vec{I}_N \times K\right]$$

Where:

CTn is the reference current.
For HV REF CTn = T1 CT.
For LV REF CTn = T2 CT for P642, T3 CT for P643 and T5 CT for P645.
For TV REF CTn = T2 CT for P643 and T3 CT for P645.
If the CTn setting changes, Is1 and Is2 settings are affected accordingly.

Up to three neutral CT inputs are available depending on the relay model:
TN1 CT is related to the HV REF function;
TN2 CT to the LV REF function and
TN3 CT to the TV REF function.

scaling factor K = Neutral CT ratio/CTn ratio

The scaling factor is required to match the summation of the line currents with the current measured in the star point.

I_N = current measured by the neutral CT

Note	*In some previous firmware versions, the reference CT is not the phase CT. Please check the relevant P64x Technical Manual.*

2.2.1.2 One and a Half Breaker Applications

The low impedance REF function in the P64x can also be used in one and a half breaker applications. Also the line CT ratios can be different. The relay uses these equations to calculate the mean bias and differential currents:

$$I_{bias} = \frac{1}{2}\left\{\max\left[\left|\vec{I}_{A\,CT_n}\right|, \left|\vec{I}_{A\,CT_m}\right| x\,K_1, \left|\vec{I}_{B\,CT_n}\right|, \left|\vec{I}_{B\,CT_m}\right| x\,K_1, \left|\vec{I}_{C\,CT_n}\right|, \left|\vec{I}_{C\,CT_m}\right| x\,K_1\right] + I_N\,x\,K_2\right\}$$

$$I_{diff} = \left|\left(\vec{I}_{A\,CT_n} + \vec{I}_{B\,CT_n} + \vec{I}_{C\,CT_n} + \left(\vec{I}_{A\,CT_m} + \vec{I}_{B\,CT_m} + \vec{I}_{C\,CT_m}\right) x\,K_1\right) + \vec{I}_N\,x\,K_2\right|$$

Where:

CT_n and CT_m = T1 CT, T2 CT, T3 CT, T4 CT or T5 CT. CT_n and CT_m are the current inputs assigned to each transformer winding, and they are given in the settings HV CT Terminals, LV CT Terminals and TV CT Terminals. CT_n is always the reference current, so Is1 and Is2 settings are relative to this CT.
For HV REF CT_n = T1 CT.
For LV REF CT_n = T3 CT for P643 and T5 CT for P645.
For TV REF CT_n= T3 CT for P645.
If the CT_n setting changes, Is1 and Is2 settings are affected accordingly.

Up to three neutral CT inputs are available depending on the relay model. TN1 CT is related to the HV REF function; TN2 CT to the LV REF function and TN3 CT to the TV REF function.

K1 = CT_m ratio / CT_n ratio

K2 = Neutral CT ratio/CT_n ratio

IN = current measured by the neutral CT

From the differential and bias equations, it can be observed that first the current flowing through CT_m is referred to CT_n. Second, the neutral CT is also referred to CT_n.

Consider the HV REF function in a P645. If the HV CT Terminals setting is 00011, then CT_n = T1 CT and CT_m = T2 CT. Therefore, K1 = T2 CT ratio / T1 CT ratio and K2 = Neutral CT ratio/T1 CT ratio.

Now, consider the LV REF function. If the LV CT Terminals setting is 11000, then CT_n = 5 and CT_m = 4. Therefore, K1 = T4 CT ratio / T5 CT ratio and K2 = Neutral CT/T5 CT ratio.

Finally, consider the TV REF function. In this example, only current input three is available; so the LV CT Terminals setting is 00100. In this case, the relay uses the differential and bias equations for single breaker applications, and K = Neutral CT ratio/T3 CT ratio.

If more than two line current transformers are assigned to the HV/LV/TV CT Terminals, the low impedance REF can also be applied. The number of scaling factors is increased accordingly.

2.2.1.3 Autotransformer Applications

The low impedance REF function in the P64x can also be used to protect an autotransformer as shown in the Low impedance REF diagram. The line CT ratios can be different and Kn is the scaling factor of each of the current transformers involved in the application. The setting cell REF Auto Status is only available when the Winding Type setting cell is set to Auto.

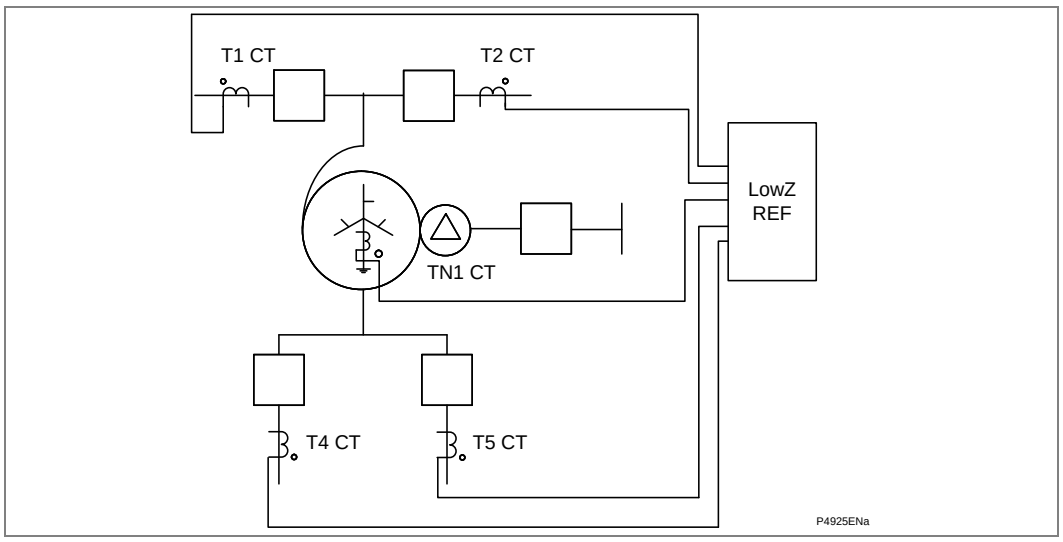


Figure 20 - Low impedance REF

The relay uses these equations to calculate the mean bias and differential currents:

$$I_{bias} = \frac{1}{2}\left\{\max\left[\left|\vec{IA}_{T_mCT}\right| x\, K_m, \left|\vec{IB}_{T_mCT}\right| x\, K_m, \left|\vec{IC}_{T_mCT}\right| x\, K_m\right] + \vec{I}_{TN1CT} x\, K\right\}$$

$$I_{diff} = \left|\sum_{n=1}^{m}\left[\left(\vec{IA}_{TnCT} + \vec{IB}_{TnCT} + \vec{IC}_{T_nCT}\right) * K_n\right] + \vec{I}_{TN1CT} x\, K\right|$$

Where:
m = HV CT and LV CT terminals
K_m = TmCT ratio/T1CT ratio
K_n = TnCT ratio/T1CT ratio
K = TN1CT ratio/T1CT ratio
For example, the bias and differential calculations for the application shown in the *Low impedance REF* diagram are as follows:

$$I_{bias} = \frac{1}{2} x \left\{\max\left[\begin{array}{l}\left|\vec{IA}_{T1CT}\right|, \left|\vec{IA}_{T2CT}\right| x K_2, \left|\vec{IA}_{T4CT}\right| x K_4, \left|\vec{IA}_{T5CT}\right| x K_5, \\ \left|\vec{IB}_{T1CT}\right|, \left|\vec{IB}_{T2CT}\right| x K_2, \left|\vec{IB}_{T4CT}\right| x K_4, \left|\vec{IB}_{T5CT}\right| x K_5, \\ \left|\vec{IC}_{T1CT}\right|, \left|\vec{IC}_{T2CT}\right| x K_2, \left|\vec{IC}_{T4CT}\right| x K_4, \left|\vec{IC}_{T5CT}\right| x K_5,\end{array}\right] + \left|I_{T1CT}\right| x K\right\}$$

$$I_{diff} = \left(\vec{IA}_{T1CT} + \vec{IB}_{T1CT} + \vec{IC}_{T1CT}\right) + \left(\vec{IA}_{T2CT} + \vec{IB}_{T2CT} + \vec{IC}_{T2CT}\right) * K_2 +$$
$$\left(\vec{IA}_{T4CT} + \vec{IB}_{T4CT} + \vec{IC}_{T4CT}\right) * K_4 + \left(\vec{IA}_{T5CT} + \vec{IB}_{T5CT} + \vec{IC}_{T5CT}\right) * K_5 + \left(\vec{I}_{TN1CT} x K\right)$$

Where:
K2 = T2 CT_ratio / T1 CT_ratio
K4 = T4 CT_ratio / T1 CT_ratio
K5 = T5 CT_ratio / T1 CT_ratio
K = Neutral CT_ratio / T1 CT_ratio
T1 CT is always the reference CT in an autotransformer application.
If T1 CT setting changes, Is1 and Is2 settings are affected accordingly.

2.2.2 Scaling Factor(s)

The scaling factor(s) are described in these sections:

- 2.2.1.1 - Single Breaker Applications
- 2.2.1.2 - One and a Half Breaker Applications
- 2.2.1.3 - Autotransformer Applications

Autotransformer applications must satisfy the following condition:

- The scaling factor(s) must always be $0.05 \leq K \leq 20$
  (except for TV applications where scaling factors less than 0.05 will be excluded from the differential calculations)

If this condition is not satisfied, then an alarm is issued and the low impedance REF protection is blocked. The alarm of scaling factor will be raised when the scaling factor is out-of-range whether the REF HV (LV or TV or Auto) Status is enabled or disabled.

2.2.2.1 Transient Bias

An additional bias quantity is introduced on a per-winding basis, if there is a sudden increase in the mean bias calculation. Transient bias is added for through fault stability and it decays exponentially. The transient bias is reset to zero once the relay trip or if the mean bias quantity is below 0.5*Is1.

The transient bias is removed after the relay has tripped to avoid the possibility of chattering. It is also removed when Ibias is less than 0.5*Is1 to avoid the possibility of residual values due to the numerical effects.

No transient bias is produced under load switching conditions or when the CT comes out of saturation, which will also cause an increase of bias.

The mean bias current is available as a measurement display and in the fault records.

2.2.2.2 Tripping Characteristic

The tripping characteristic of the low impedance REF has two knees. The first knee is dependent on the settings of I_{s1} and K1. The second knee of the tripping characteristic is defined by the setting I_{s2}. The lower slope provides sensitivity for internal faults. The higher slope provides stability under through fault conditions, since transient differential currents may be present due to current transformer saturation.

Once the differential and bias currents are calculated, the following comparisons are made and an operate/restrained signal is obtained:

Flat slope:

$$I_{bias} \leq \frac{I_{s1}}{K_1}$$

$$I_{diff} \geq I_{s1} + \text{Transient Bias}$$

K1 slope:

$$\frac{I_{s1}}{K_1} \leq I_{bias} \leq I_{s2}$$

$$I_{diff} \geq K_1 I_{bias} + \text{Transient Bias}$$

K2 slope:

$$I_{bias} \geq I_{s2}$$

$$I_{diff} \geq K_1 I_{s2} + K_2 (I_{bias} - I_{s2}) + \text{Transient Bias}$$

In the equations above, $I_{bias,y}$ is the delayed bias and as explained previously it is the highest bias current in the last cycle.

The protection trips on a count of 5, which is approximately 25 ms after fault detection.

The *Low impedance REF characteristic* diagram shows the operating characteristic for the low impedance REF.

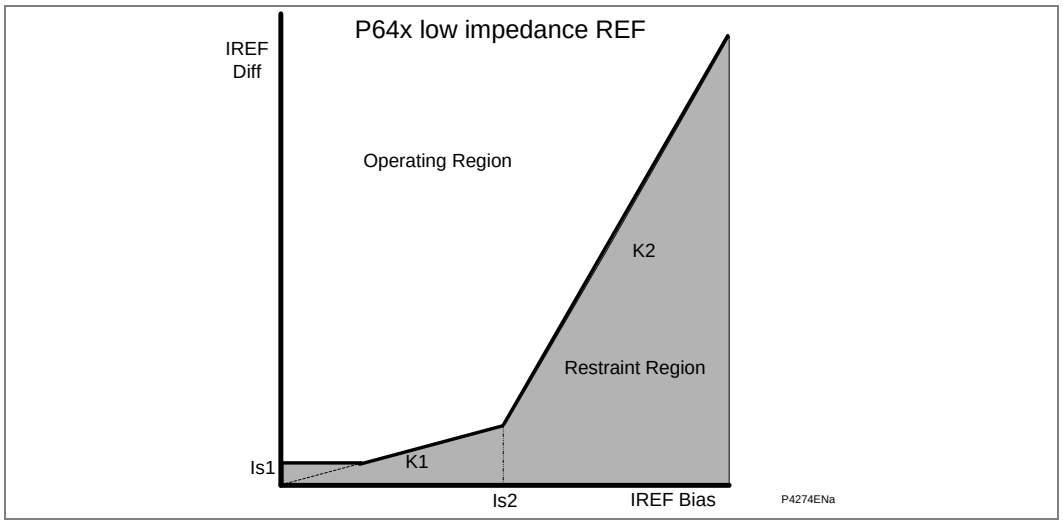


Figure 21 - Low impedance REF characteristic

2.2.3 High Impedance Restricted Earth Fault (REF)

A high impedance Restricted Earth Fault (REF) protection function per transformer winding is available for up to three ends. An external resistor is required to provide stability in the presence of saturated line current transformers.

The high impedance REF protection works on the high impedance circulating current principle shown in this diagram.

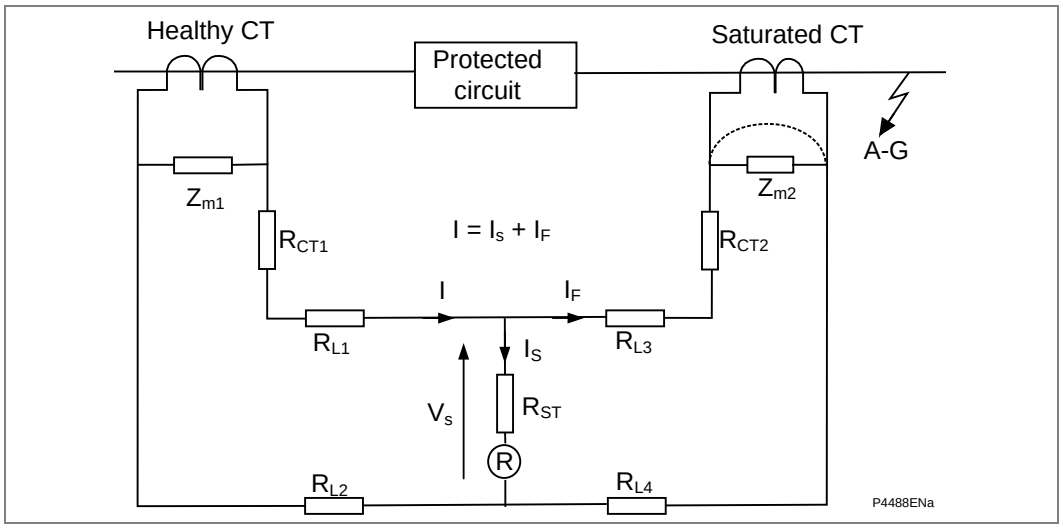


Figure 22 - High impedance differential principle

When subjected to heavy through faults the line current transformer may enter saturation unevenly, resulting in unbalance. To ensure stability under these conditions a series connected external resistor is required, so that most of the unbalanced current will flow through the saturated CT. As a result, the current flowing through the relay will be less than the setting, thus maintaining stability during external faults. Harmonics are rejected by basing the measurement on the fundamental frequency Fourier magnitude.

TN1 CT is associated to the HV winding high impedance REF, or to the autotransformer high impedance .
TN2 CT is associated to the LV winding high impedance REF.
TN3 CT is associated to the TV winding high impedance REF.

Current transformer supervision, HV StubBus Act, LV StubBus Act or TV StubBus Act signals do not block the high impedance REF. The appropriate logic must be configured in PSL to block the high impedance REF when any of the above signals is asserted.

2.3 Overcurrent Protection (50/51)

Three four-stage overcurrent elements are included in the P64x relays.

The overcurrent protection included in the relay provides four-stage non-directional/ directional three-phase overcurrent protection with independent time delay characteristics. All overcurrent and directional settings apply to all three phases but are independent for each of the four stages.

The overcurrent element operating quantity may be selected in the setting cell **Overcurrent x**. It can be set as T1, T2, T3, T4, T5, HV winding, LV winding and TV winding. HV, LV and TV winding consider the vectorial sum of the CT inputs associated to a particular winding.

- In a P642 relay, the HV Winding **I>x Current Set** settings are relative to T1 CT, and the LV Winding **I>x Current Set** settings are relative to T2 CT.
- In a P643 relay, the HV Winding **I>x Current Set** settings are relative to T1 CT. If the HV CT Terminals setting is 011, then T1 CT and T2 CT are assigned to the HV winding. If the T1 CT setting changes, **I>x Current Set** is affected accordingly. However, if the T2 CT setting changes, **I>x Current Set** settings are not affected. LV Winding **I>x Current Set** settings are relative to T3 CT. TV Winding **I>x Current Set** settings are relative to T2 CT.
- In a P645 relay, the HV Winding **I>x Current Set** settings are relative to T1 CT. The LV Winding **I>x Current Set** settings are relative to T5 CT. The TV Winding **I>x Current Set** settings are relative to T3 CT. If the TV CT Terminals setting is 00110, then T2 CT and T3 CT are assigned to the TV winding. If T3 CT setting changes, **I>x Current Set** settings are affected accordingly. However, if the T2 CT setting changes, **I>x Current Set** settings are not affected.

The overcurrent element may be set as directional only if the three phase VT input is available in the P643/P645 and if the two single phase VT inputs are available in the P642. The VT may be assigned to the HV, LV or TV winding. Therefore, overcurrent directional elements are available to the current inputs associated to the winding which has the VT input assigned.

The first two stages of overcurrent protection have time-delayed characteristics which are selectable between Inverse Definite Minimum Time (IDMT), or Definite Time (DT). The third and fourth stages have definite time characteristics only.

Various methods are available to achieve correct relay co-ordination on a system; by means of time alone, current alone or a combination of both time and current. Grading by means of current is only possible where there is an appreciable difference in fault level between the two relay locations. Grading by time is used by some utilities but can often lead to excessive fault clearance times at or near source substations where the fault level is highest. For these reasons the most commonly applied characteristic in co-ordinating overcurrent relays is the IDMT type.

The inverse time delayed characteristics indicated above, comply with the following formula:

IEC curves **or** **IEEE curves**

$$t = Tx\left(\frac{\beta}{(M^{\alpha} - 1)} + L\right) + C \qquad t = TD \times \left(\frac{\beta}{M^{\alpha} - 1} + L\right) + C$$

Where:

t = Operation time
β = Constant
M = I/Is
I = Measured current
Is = Current threshold setting
α = Constant
L = ANSI/IEEE constant (zero for IEC curves)
T = Time multiplier setting for IEC curves
TD = Time dial setting for IEEE curves
C = Definite time adder (zero for standard curves)

IDMT Curve description	Standard	β constant	α constant	L constant
Standard Inverse	IEC	0.14	0.02	0
Very Inverse	IEC	13.5	1	0
Extremely Inverse	IEC	80	2	0
Long Time Inverse	UK	120	1	0
Rectifier	UK	45900	5.6	0
Moderately Inverse	IEEE	0.0515	0.02	0.114
Very Inverse	IEEE	19.61	2	0.491
Extremely Inverse	IEEE	28.2	2	0.1217
Inverse	US	5.95	2	0.18
Short Time Inverse	US	0.16758	0.02	0.11858

Table 6 - Curve descriptions, standards and constants

Note	*The IEEE and US curves are set differently to the IEC/UK curves, with regard to the time setting. A Time Multiplier Setting (TMS) is used to adjust the operating time of the IEC curves, whereas a time dial setting is employed for the IEEE/US curves. The menu is arranged so that if an IEC/UK curve is selected, the **I>1 Time Dial** cell is not visible and if the IEEE/US curve is selected the **I>1 TMS** cell is not visible.*

The IEC/UK inverse characteristics can be used with a definite time reset characteristic, however, the IEEE/US curves may have an inverse or definite time reset characteristic. The following equation can used to calculate the inverse reset time for IEEE/US curves:

$$tRESET = \frac{TD \times S}{(1 - M^2)} \text{ in seconds}$$

Where:
TD = Time dial setting for IEEE curves
S = Constant
M = I/Is

Curve Description	Standard	S Constant
Moderately Inverse	IEEE	4.85
Very Inverse	IEEE	21.6
Extremely Inverse	IEEE	29.1
Inverse	US	5.95
Short Time Inverse	US	2.261

Table 7 - Curve description standards

Note	*The rectifier curve is only provided in the first and second stage characteristic setting options for phase overcurrent protection.*

2.3.1 RI Curve

The RI curve (electromechanical) has been included in the first and second stage characteristic setting options for phase overcurrent and earth protections. The curve is represented by the following equation.

Where K is adjustable from 0.1 to 10 in steps of 0.05, and M = I / Is

$$t = K \times \left(\frac{1}{0.339 - \left({}^{0.236}/_{M} \right)} \right) \text{ in seconds}$$

2.3.2 Timer Hold Facility

The first two stages of overcurrent protection in the relays are provided with a timer hold facility, which may either be set to zero or to a definite time value. Setting of the timer to zero means that the overcurrent timer for that stage will reset instantaneously once the current falls below 95% of the current setting. Setting of the hold timer to a value other than zero, delays the resetting of the protection element timers for this period.

When the reset time of the overcurrent relay is instantaneous, the relay will be repeatedly reset and not be able to trip until the fault becomes permanent. By using the Timer Hold facility the relay will integrate the fault current pulses, thereby reducing fault clearance time.

The timer hold facility can be found for the first and second overcurrent stages as settings **I>1 tRESET** and **I>2 tRESET**, respectively.

If an IEC inverse or DT operating characteristic is chosen, this time delay is set using the **I>1/2 tRESET** setting. If an IEEE/US operate curve is selected, the reset characteristic may be set to either definite time or inverse time as selected in cell **I>1/2 Reset Char**. If definite time ('DT') is selected the **I>1/2 tRESET** cell may be used to set the time delay. If inverse time reset (**Inverse**) is selected the reset time will follow the inverse time operating characteristic, modified by the time dial setting, selected for **I>1/2 Function**.

The functional logic diagram for non-directional overcurrent is shown in the *Non-directional overcurrent logic* diagram.

A timer block input is available for each stage which will reset the overcurrent timers of all three phases if energized, taking account of the reset time delay if selected for the **I>1** and **I>2** stages.

A DDB (Digital Data Bus) signal is available to indicate the start and trip of each phase of the short circuit protection stages (Start I>1/2/3/4 A,B,C: DDB 242,243,244/DDB 253,254,255/DDB 343,344,345/DDB 354,355,356 Trip I>1/2/3/4 A,B,C: DDB 245,246,247/ DDB 256,257,258/DDB 346,347,348/DDB 357,358,359). In addition a three phase start and trip DDB signal is provided (Start I>1/2/3/4: DDB 241/252/342/353 Trip I>1/2/3/4: DDB237/ 248/338/349). These signals are used to operate the output relays and trigger the disturbance recorder as programmed into the programmable Scheme Logic (PSL). The state of the DDB signals can also be programmed to be viewed in the **Monitor Bit x** cells of the **COMMISSION TESTS** column in the relay.

DDB signals are also available to indicate the start and trip of each phase of each stage of protection. The state of the DDB signals can be programmed to be viewed in the **Monitor Bit x** cells of the **COMMISSION TESTS** column in the relay.

Overcurrent protection starts 1/2/3/4 are mapped internally to the ANY START DDB signal - DDB 1312.

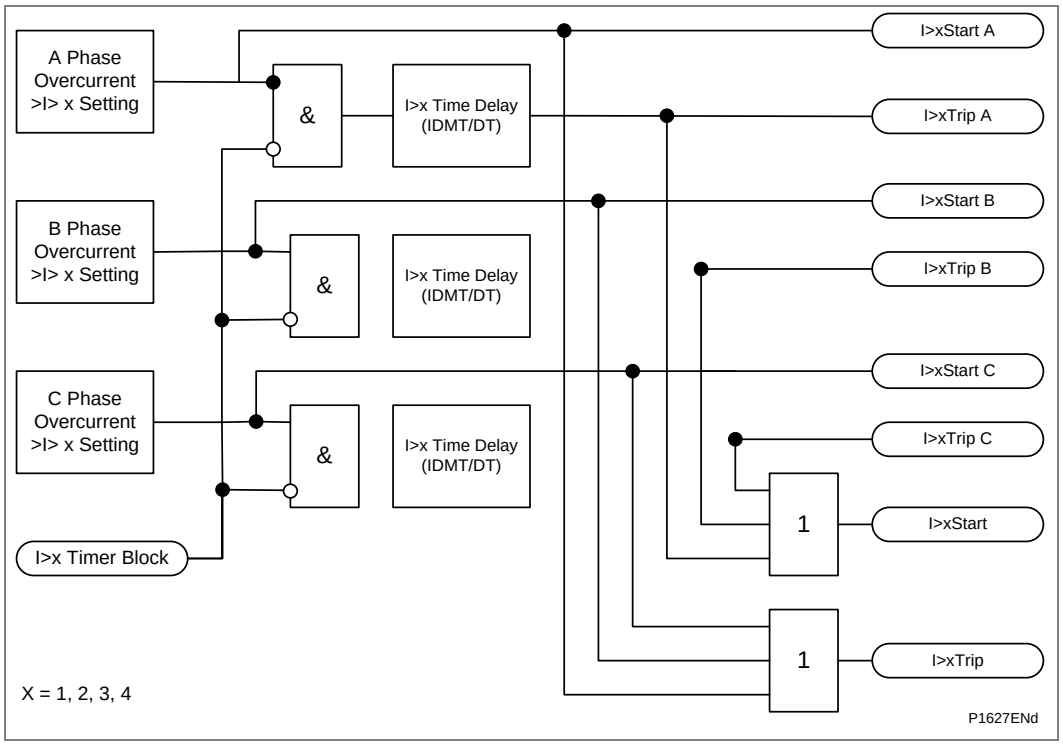


Figure 23 - Non-directional overcurrent logic diagram

2.4 Directional Overcurrent Protection (67)

The P643 and P645 can be provided with an additional three-phase VT input. Therefore it will only be possible to set the directionality of the overcurrent phase fault protection when this optional VT input is provided in the P643/P645. It is possible to set the directionality of the overcurrent phase fault protection in the P642 when two single phase VT inputs are available.

In a P643 relay, the HV Winding **I>x Current Set** settings are relative to T1 CT. If the HV CT Terminals setting is 011, then T1 CT and T2 CT are assigned to the HV winding. If the T1 CT setting changes, **I>x Current Set** is affected accordingly. However, if the T2 CT setting changes, **I>x Current Set** settings are not affected. LV Winding **I>x Current Set** settings are relative to T3 CT. TV Winding **I>x Current Set** settings are relative to T2 CT.

In a P645 relay, the HV Winding **I>x Current Set** settings are relative to T1 CT. The LV Winding **I>x Current Set** settings are relative to T5 CT. The TV Winding **I>x Current Set** settings are relative to T3 CT. If the TV CT Terminals setting is 00110, then T2 CT and T3 CT are assigned to the TV winding. If the T3 CT setting changes, **I>x Current Set** settings are affected accordingly. However, if the T2 CT setting changes, **I>x Current Set** settings are not affected.

The phase fault elements of the P64x relays are internally polarized by the quadrature phase-phase voltages, as shown in the table below:

Phase of Protection	Operate Current	Polarizing Voltage
A Phase	IA	VBC
B Phase	IB	VCA
C Phase	IC	VAB

Table 8 - Phase, Operating Current and Polarizing Voltages

Under system fault conditions, the fault current vector will lag its nominal phase voltage by an angle dependent upon the system X/R ratio. It is therefore a requirement that the relay operates with maximum sensitivity for currents lying in this region. This is achieved by means of the relay characteristic angle (RCA) setting; this defines the angle by which the current applied to the relay must be displaced from the voltage applied to the relay to obtain maximum relay sensitivity. This is set in cell "**I>Char Angle**" in the overcurrent menu. On the relays, it is possible to set characteristic angles anywhere in the range –95° to +95°.

The functional logic block diagram for directional overcurrent is shown in the following *Directional overcurrent logic* diagram.

The overcurrent block is a level detector that detects that the current magnitude is above the threshold and together with the respective polarizing voltage, a directional check is performed based on the following criteria:

Directional forward -90° < (angle(I) - angle(V) - RCA) < 90°

Directional reverse -90° > (angle(I) - angle(V) - RCA) > 90°

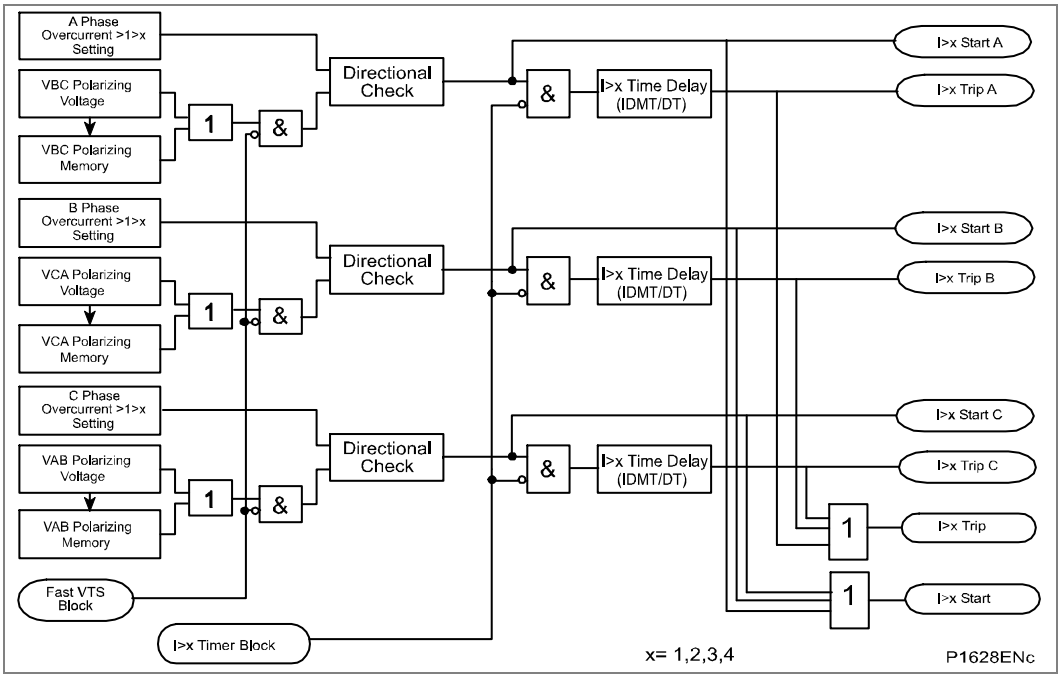


Figure 24 - Directional overcurrent logic

Any of the four overcurrent stages may be configured to be directional noting that IDMT characteristics are only selectable on the first two stages. When the element is selected as directional, a VTS Block option is available in the **I> Function Link** setting. When the relevant bit is set to 1, operation of the Voltage Transformer Supervision (VTS), will block the stage if directionalized. When set to 0, the stage will revert to non-directional upon operation of the VTS.

2.4.1 Synchronous Polarization

For a close-up 3-phase fault, all three voltages will collapse to zero and no healthy phase voltages will be present. For this reason, the MiCOM relays include a synchronous polarization feature that stores the pre-fault voltage information and continues to apply it to the Directional Overcurrent (DOC) elements for a period of 3.2 seconds. This ensures that either instantaneous or time-delayed directional overcurrent elements will be allowed to operate, even with a 3-phase voltage collapse.

2.5 Voltage Controlled Overcurrent (VCO)

A two-stage 3-phase Voltage Controlled Overcurrent (VCO) element is available in P643/P645 when the 3-phase VT has been fitted and in P642 when the two single-phase VTs have been fitted. Phase-to-phase voltages are used by the VCO function. In P643/P645, the phase-to-phase voltages are derived from the measured phase-to-neutral voltages. In the P642, two phase-to-phase voltages are measured and the third one is calculated. In the P642 Vab and Vbc are measured, then Vca is calculated as:

$V_{ca} = -(\vec{V}_{bc} + \vec{V}_{ab})$

If the current seen by a local relay for a remote fault condition is below it's overcurrent setting, a VCO element may be used to increase the relay sensitivity to such faults. In this case, a reduction in system voltage will occur; this is used to reduce the pick-up level of the overcurrent protection. The current setting is modified by a multiplier K when the voltage falls below a threshold as shown in the following table:

Element	Phase to Phase control voltage	Element pickup when control voltage > setting	Element pickup when control voltage < setting
Ia>	Vab	VCO>1 I>Set, VCO>2 I>Set	VCO>1 K(RI) * VCO>1 I>Set, VCO>1 K Set * VCO>1 I>Set, VCO>2 K(RI) * VCO>2 I>Set, VCO>2 K Set * VCO>2 I>Set,
Ib>	Vbc	VCO>1 I>Set, VCO>2 I>Set	VCO>1 K(RI) * VCO>1 I>Set, VCO>1 K Set * VCO>1 I>Set, VCO>2 K(RI) * VCO>2 I>Set, VCO>2 K Set * VCO>2 I>Set,
Ic>	Vca	VCO>1 I>Set, VCO>2 I>Set	VCO>1 K(RI) * VCO>1 I>Set, VCO>1 K Set * VCO>1 I>Set, VCO>2 K(RI) * VCO>2 I>Set, VCO>2 K Set * VCO>2 I>Set,

Table 9 - Current setting modification multipliers

The voltage threshold is set in **VCO>1 V< Set, VCO>2 V< Set** setting cells. The current setting is set in **VCO>1 I>Set** and **VCO>2 I>Set** setting cells. The K multiplier is set in **VCO>1 K(RI), VCO>2 K(RI), VCO>1 K Set,** or **VCO>2 K Set** settings cells.

Two VCO stages are available and each one can be set to HV winding, LV winding, TV winding, T1 CT, T2 CT, T3 CT, T4 CT, T5 CT or disabled. If the current signal chosen for a VCO stage does not belong to the winding where the VT is located, then the VCO element is blocked and a configuration error alarm is asserted. VCO1 Config err (DDB 472) or VCO2 Config err (DDB 473) alarms might be asserted.

Note	*Voltage-dependent overcurrent relays are more often applied in generator protection applications to give adequate overcurrent relay sensitivity for close-up fault conditions. The fault characteristic of this protection must then co-ordinate with any of the downstream overcurrent relays that are responsive to the current decrement condition.*

2.6 Voltage Restrained Overcurrent Protection

In voltage restrained mode the effective operating current of the protection element is continuously variable as the applied voltage varies between two voltage thresholds, “V OC V<1 Set” and “V OC V<2 Set”, as shown in the figure below. In this mode, it is quite difficult to determine the behaviour of the protection function during a fault. This protection mode is, however, considered to be better suited to applications where the generator is connected to the system via a generator transformer.

With indirect connection of the generator, a solid phase-phase fault on the local busbar will result in only a partial phase-phase voltage collapse at the generator terminals.

The voltage-restrained current setting is related to measured voltage as follows:

For V > V<1: Current setting (I_s) = I>
For V<2 < V < V<1: Current setting (I_s) = K.I> + (I > - K. I>) {V – V<2 / V<1 – V<2}
For V < V<2: Current setting (I_s) = K.I>

Where:
I> = Over current stage setting
I_s = Current setting at voltage V
V = Voltage applied to relay element
V<1 = “V OC V<1 Set”
V<2 = “V OC V<2 Set”

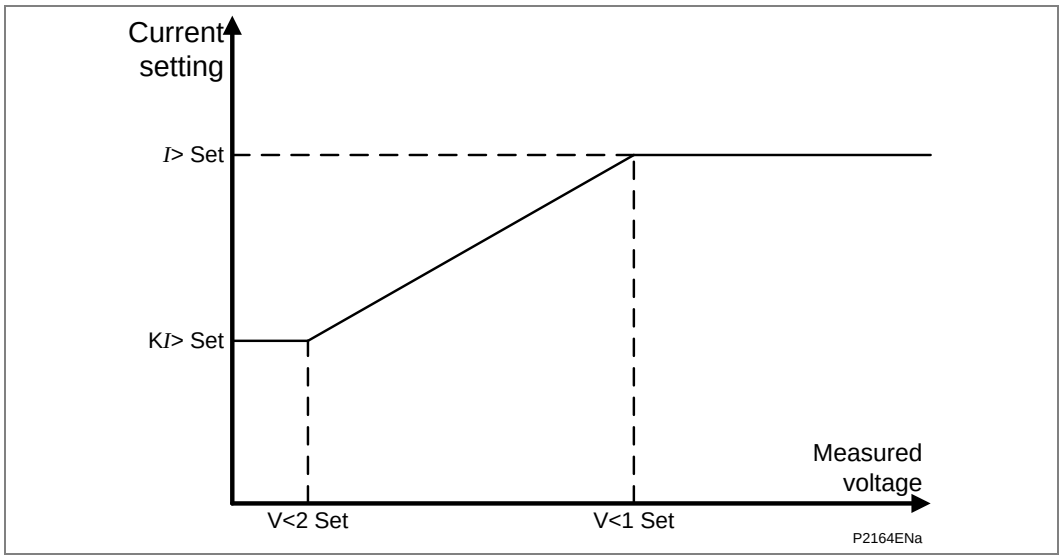


Figure 25 - Modification of current pickup level for voltage restrained overcurrent protection

2.7 Earth Fault (EF)

The earth fault element is based on the neutral current of any of the transformer windings or any of the current transformer inputs. The user can select between measured neutral current or derived neutral current in the **EF x Input** setting. The earth fault derived current signal may be selected in the **EF x Derived** setting and the options are HV winding, LV winding, TV winding, T1, T2, T3, T4 and T5. If HV winding, LV winding or TV winding is chosen, then the derived zero sequence current considers the CTs assigned in **HV CT Terminals, LV CT Terminals or TV CT Terminals** respectively. If the **EF x Input** is set to measured, then the **EF x Measured** setting options are TN1, TN2 and TN3.

Three four-stage earth fault elements are available. The first and second stages have selectable IDMT or DT characteristics, while the third and fourth stages are DT only. Each stage is selectable to be either non-directional, directional forward or directional reverse. The Timer Hold facility, previously described for the overcurrent element, is available on each of the first two stages.

The description in these paragraphs is valid when the **EF x Input** setting is **Derived**.

- In a P642 relay, the HV Winding **IN>x Current** settings are relative to T1 CT, and the LV Winding **IN>x Current** settings are relative to T2 CT.
- In a P643 relay, the HV Winding **IN>x Current** settings are relative to T1 CT. If the **HV CT Terminals** setting is 011, then T1 CT and T2 CT are assigned to the HV winding. If the T1 CT setting changes, **IN>x Current** is affected accordingly. However, if the T2 CT setting changes, the **IN>x Current** settings are not affected. The LV Winding **IN>x Current** settings are relative to T3 CT. The TV Winding **IN>x Current** settings are relative to T2 CT.
- In a P645 relay, the HV Winding **IN>x Current** settings are relative to T1 CT. The LV Winding **IN>x Current** settings are relative to T5 CT. The TV Winding **IN>x Current** settings are relative to T3 CT. If the TV CT Terminals setting is 00110, then T2 CT and T3 CT are assigned to the TV winding. If the T3 CT setting changes, the **IN>x Current** settings are affected accordingly. However, if the T2 CT setting changes, the **IN>x Current** settings are not affected.

The logic diagram for non-directional earth fault overcurrent is shown below:

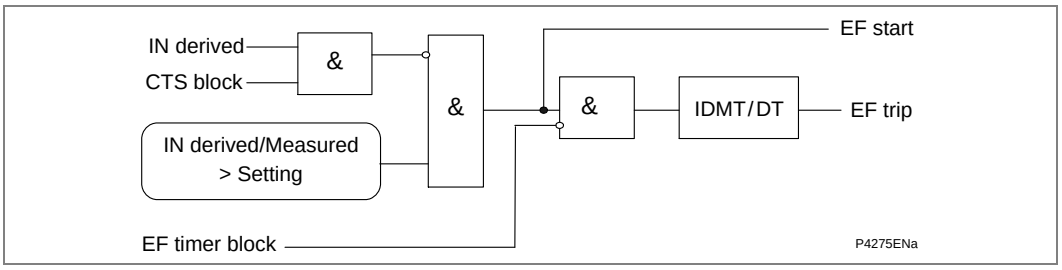


Figure 26 - Non-directional EF logic (single stage)

The earth fault protection can be set IN/OUT of service using the appropriate DDB inhibit signal that can be operated from an opto input or control command.

For inverse time delayed characteristics refer to the phase overcurrent elements, see the *Overcurrent Protection (50/51)* section.

2.7.1 IDG Curve

The IDG curve is commonly used for time delayed earth fault protection in the Swedish market. This curve is available in stages 1 and 2 of Earth Fault protection.
The IDG curve is represented by the following equation:

$$t = 5.8 - 1.35 \log_e \left(\frac{I}{IN > Setting} \right) \text{ in seconds}$$

Where:

I	=	Measured current
IN>Setting	=	An adjustable setting which defines the start point of the characteristic

Although the start point of the characteristic is defined by the "**IN>**" setting, the actual relay current threshold is a different setting called "**IDG Is**". The "**IDG Is**" setting is set as a multiple of "**IN>**".

An additional setting "**IDG Time**" is also used to set the minimum operating time at high levels of fault current.

The following *IDG characteristic* diagram shows how the IDG characteristic is implemented.

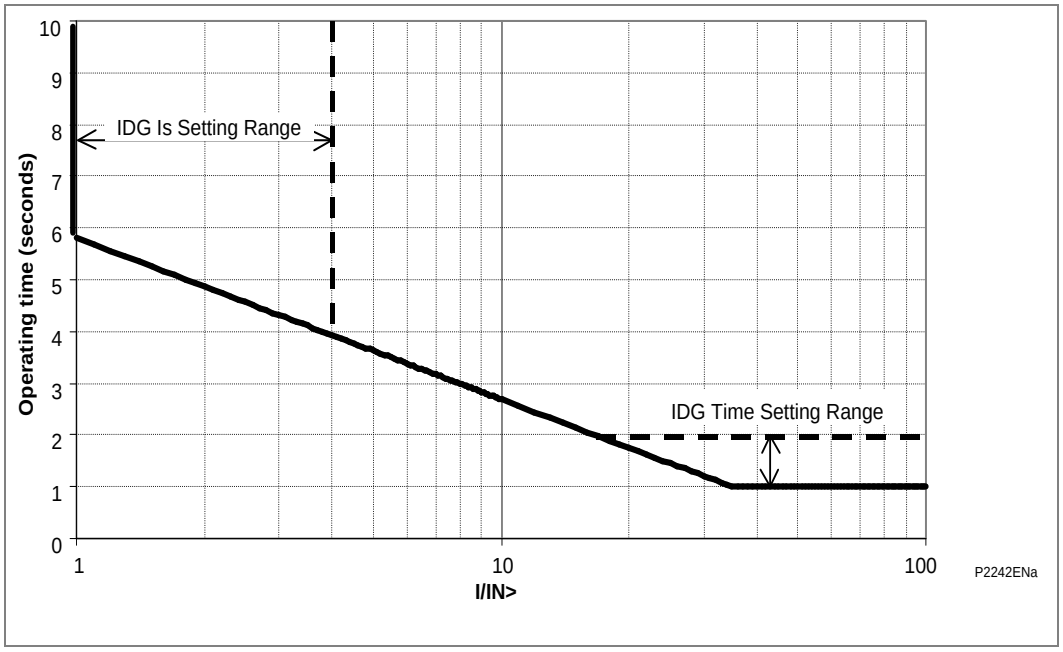


Figure 27 - IDG characteristic

2.8 Directional Earth Fault (DEF) Protection

If the earth fault element is set as directional and the **EF x Input** is set to measured, then only TN1 might be chosen to measure the zero current on the HV winding or the zero sequence current of any of the CTs assigned to the HV winding. Only TN2 might be chosen to measure the zero current on the LV winding or the zero sequence current of any of the CTs assigned to the LV winding. Only TN3 might be chosen to measure the zero current on the TV winding or the zero sequence current of any of the CTs assigned to the TV winding.

The following description is valid when the **EF x Input** setting is set to **Derived**.

- In a P642 relay, if **EF x Derived** is set to HV Winding, then **IN>x Current** settings are relative to T1 CT. If **EF x Derived** is set to LV Winding, then **IN>x Current** settings are relative to T2 CT.
- In a P643 relay, if **EF x Derived** is set to HV Winding, then **IN>x Current** settings are relative to T1 CT. Consider that HV CT Terminals is set to 011, therefore T1 CT and T2 CT are assigned to the HV winding. If T1 CT setting changes, **IN>x Current** is affected accordingly. However, if T2 CT setting changes, **IN>x Current** settings are not affected. If **EF x Derived** is set to LV Winding, then **IN>x Current** settings are relative to T3 CT. If **EF x Derived** is set to TV Winding, then IN**>x Current** settings are relative to T2 CT.
- In a P645 relay, if **EF x Derived** is set to the HV Winding, then **IN>x Current** settings are relative to T1 CT. If **EF x Derived** is set to The LV Winding, then **IN>x Current** settings are relative to T5 CT. If **EF x Derived** is set to The TV Winding, then **IN>x Current** settings are relative to T3 CT. Consider that **TV CT Terminals** is 00110; therefore, T2 CT and T3 CT are assigned to the TV winding. If the T3 CT setting changes, **IN>x Current** settings are affected accordingly. However, if the T2 CT setting changes, **IN>x Current** settings are not affected.

Each of the four stages may be set to be directional if required. Consequently, a suitable voltage supply is required by the relay to provide the necessary polarization. The P643 and P645 may be provided with an additional three-phase VT input. Therefore, only when this optional VT input is provided in the P643 or P645, it is possible to set the directionality of the overcurrent earth fault protection. In P643/P645 two options are available for polarization; Residual Voltage or Negative Sequence. In P642, it may also be possible to directionalize the earth fault element when two single phase VTs are available. In the P642, only negative sequence can be used for polarization.

2.8.1.1 Residual Voltage Polarization

With earth fault protection, the polarizing signal must be representative of the earth fault condition. As residual voltage is generated during earth fault conditions, this quantity is commonly used to polarize DEF elements. The P64x relay internally derives this voltage from the 3-phase voltage input that must be supplied from either a 5-limb or three single-phase VTs. A three-limb VT has no path for residual flux and is therefore unsuitable to supply the relay.

It is possible that small levels of residual voltage will be present under normal system conditions due to system imbalances, VT inaccuracies, relay tolerances etc. Hence, the relay includes a user settable threshold (***IN>VNPol set***) which must be exceeded for the DEF function to be operational. The residual voltage measurement provided in the **Measurements 1** column of the menu may assist in determining the required threshold setting during the commissioning stage, as this will indicate the level of standing residual voltage present.

Note	*Residual voltage is nominally 180° out of phase with residual current. Consequently, the DEF elements are polarized from the "**-Vres**" quantity. This 180° phase shift is automatically introduced within the relay.*

The *Directional EF with neutral voltage polarization logic diagram* is shown below:

VT Supervision (VTS) selectively blocks the directional protection or causes it to revert to non-directional operation. When selected to block the directional protection, VTS blocking is applied to the directional checking which effectively blocks the start outputs as well.

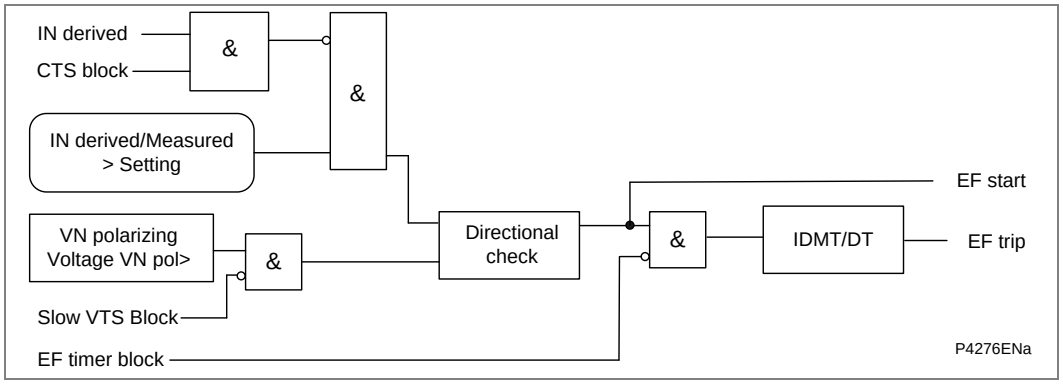


Figure 28 - Directional EF with neutral voltage polarization (single state)

2.8.2 Negative Sequence Polarization

In certain applications, the use of residual voltage polarization of DEF may either be not possible to achieve, or problematic. An example of the former case would be where a suitable type of VT was unavailable, for example if only a three limb VT was fitted. An example of the latter case would be an HV/EHV parallel line application where problems with zero sequence mutual coupling may exist.

In either of these situations, the problem may be solved by using Negative Phase Sequence (NPS) quantities for polarization. This method determines the fault direction by comparison of NPS voltage with NPS current. The operate quantity, however, is still residual current.

This is available for selection on both the derived and measured standard earth fault elements (EF1 and EF2) but not on the SEF protection. It requires a suitable voltage and current threshold to be set in cells "**IN>V2pol set**" and "**IN>I2pol set**", respectively.

Negative sequence polarizing is not recommended for impedance earthed systems regardless of the type of VT feeding the relay. This is due to the reduced earth fault current limiting the voltage drop across the negative phase sequence source impedance (V2pol) to negligible levels. If this voltage is less than 0.5 volts the relay will cease to provide DEF.

The logic diagram for Directional Earth Fault (DEF) overcurrent with negative sequence polarization is shown in this diagram.

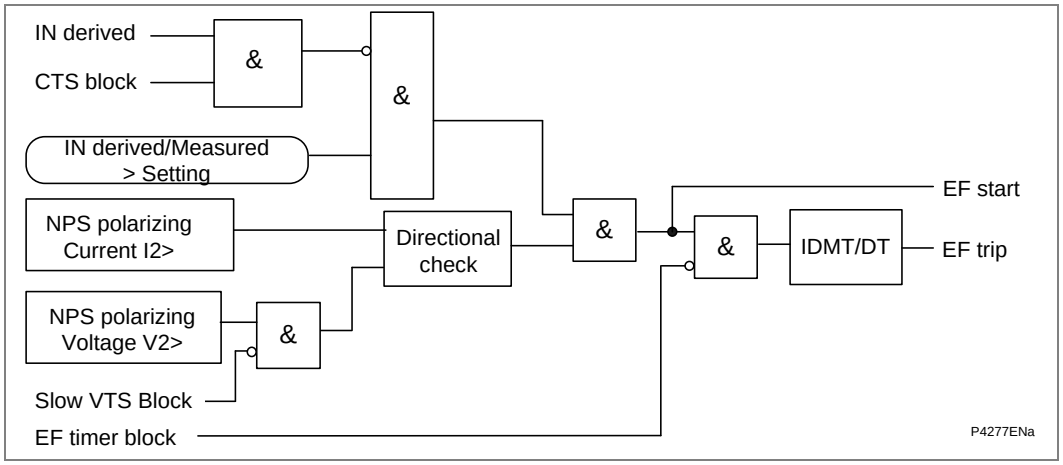


Figure 29 - Directional EF with negative sequence polarization (single stage)

The directional criteria with negative sequence polarization is given below:

Directional forward	-90° < (angle(I2) - angle(V2 + 180°) - RCA) < 90°
Directional reverse	-90° > (angle(I2) - angle(V2 + 180°) - RCA) > 90°

2.9 Negative Phase Sequence (NPS) Overcurrent Protection (46 OC)

Three four-stage Negative Phase Sequence (NPS) overcurrent elements are available. The negative sequence overcurrent element operating quantity is either the vectorial sum of the negative sequence currents of the CT inputs associated to a particular winding or the negative sequence current flowing through any of the current inputs. The operating quantity may be selected in the setting cell **NPS O/C x**.

- In a P642 relay, if **NPS O/C x** is set to HV Winding, then **I2>x Current Set** settings are relative to T1 CT. I, and f **NPS O/C x** is set to LV Winding, then **I2>x Current Set** settings are relative to T2 CT.
- In a P643 relay, if **NPS O/C x** is set to HV Winding, then **I2>x Current Set** settings are relative to T1 CT. If the HV CT Terminals setting is 011, then T1 CT and T2 CT are assigned to the HV winding. If the T1 CT setting changes, **I2>x Current Set** is affected accordingly. However, if the T2 CT setting changes, **I2>x Current Set** settings are not affected. If **NPS O/C x** is set to LV Winding, then **I2>x Current Set** settings are relative to T3 CT. If **NPS O/C x** is set to TV Winding, then **I2>x Current Set** settings are relative to T2 CT.
- In a P645 relay, if **NPS O/C x** is set to HV Winding, then **I2>x Current Set** settings are relative to T1 CT. If **NPS O/C x** is set to LV Winding, then **I2>x Current Set** settings are relative to T5 CT. If **NPS O/C x** is set to TV Winding, then **I2>x Current Set** settings are relative to T3 CT. If the TV CT Terminals setting is 00110, then T2 CT and T3 CT are assigned to the TV winding. If the T3 CT setting changes, **I2>x Current Set** settings are affected accordingly. However, if the T2 CT setting changes, **I2>x Current Set** settings are not affected.

The relay provides four independent stages of Negative Phase Sequence (NPS) overcurrent protection.

The first two stages have time-delayed characteristics which are selectable between Inverse Definite Minimum Time (IDMT) and Definite Time (DT). The third and fourth stages have definite time characteristics only. The user may choose to directionalize operation of the elements, for either forward or reverse fault protection for which a suitable relay characteristic angle may be set. Alternatively, the elements may be set as non-directional.

For the NPS directional elements to operate, the relay must detect a polarizing voltage above a minimum threshold, "**I2> V2pol Set**".

When the element is selected as directional, a VTS Block option is available. When the relevant bit is set to 1, operation of the Voltage Transformer Supervision (VTS), will block the stage if directionalized. When set to 0, the stage will revert to non-directional upon operation of the VTS.

A timer block input is available for each stage which will reset the NPS overcurrent timers of the relevant stage if energized, (DDB 664-667, 669-672, 674-677). All 4 stages can be blocked by energizing the inhibit DDB signal via the PSL (I2> Inhibit: DDB 663, 668, 673). DDB signals are also available to indicate the start and trip of each stage of protection, (Starts: DDB 1532-1543, Trips: DDB 1154-1165).

The state of the DDB signals can be programmed to be viewed in the **Monitor Bit x** cells of the **COMMISSION TESTS** column in the relay.

NPS overcurrent protection starts 1/2/3/4 are mapped internally to the ANY START DDB signal - DDB 1312.

The non-directional and directional operation is shown in these diagrams:

- Negative sequence overcurrent non-directional operation
- Directionalizing the negative phase sequence overcurrent element

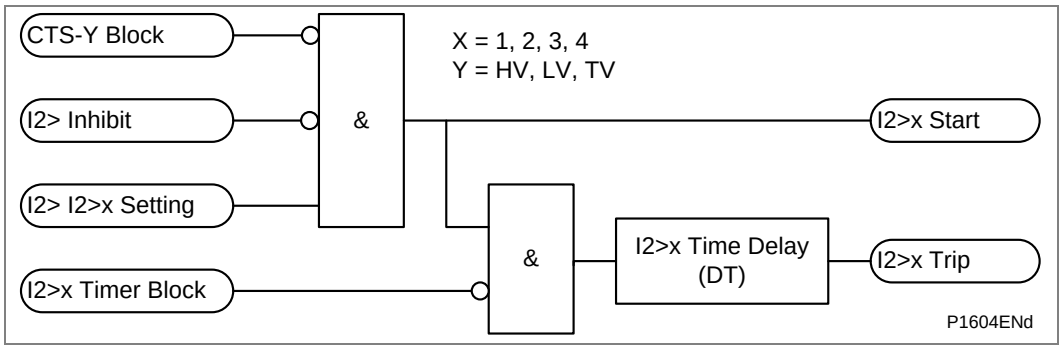


Figure 30 - Negative sequence overcurrent non-directional operation

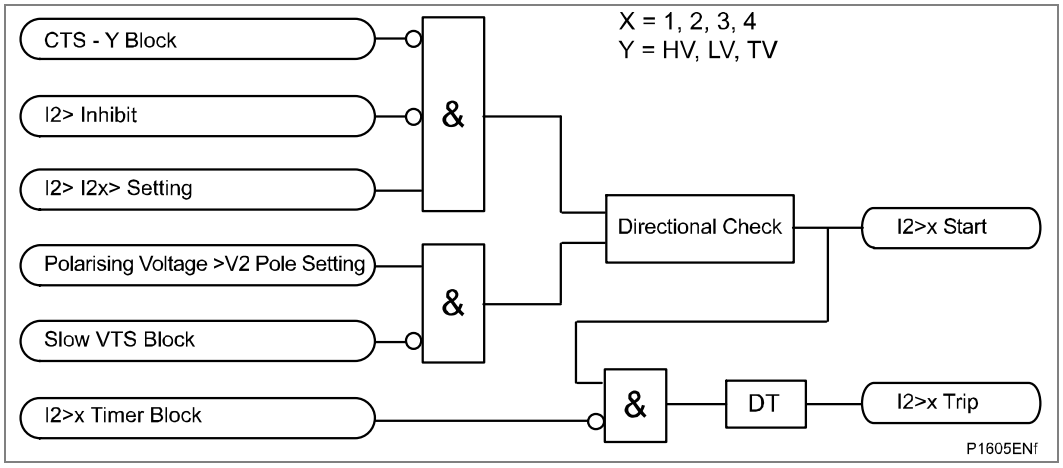


Figure 31 - Directionalizing the negative phase sequence overcurrent element

Directionality is achieved by comparison of the angle between NPS voltage and the NPS current and the element may be selected to operate in either the forward or reverse direction. A suitable relay characteristic angle setting (I2> Char Angle) is chosen to provide optimum performance. This setting should be set equal to the phase angle of the negative sequence current with respect to the inverted negative sequence voltage (–V2), in order to be at the center of the directional characteristic.

For the NPS directional elements to operate, the relay must detect a polarizing voltage above a minimum threshold, "**I2> V2pol Set**". This must be set in excess of any steady state NPS voltage. This may be determined during the commissioning stage by viewing the NPS measurements in the relay.

2.10 Stub Bus Protection

The stub bus protection is only available in the P643 and P645.

When the protection is used in one-and-half breaker busbar topology and the disconnector of any of the three windings of the transformer is open, the differential, REF, breaker failure, and differential CTS elements related to this winding are affected.

The differential and REF protections should not trip for a stub bus fault. Therefore, the differential trip may be blocked on a per winding basis if the PSL given in the *Differential trip blocked due to stub bus activation* diagram is used. The signals HV StubBus Act (DDB 647), LV StubBus Act (DDB 648) and TV StubBus Act (DDB 649) are asserted when the appropriate conditions are met as shown in the *Stub bus trip* diagram. The REF is blocked internally on a per winding basis by the fixed logic. For example, if HV StubBus Act (DDB 647) is activated, then HV REF is blocked.

The differential and REF protection trips are blocked when the signals HV StubBus Act (DDB 647), LV StubBus Act (DDB 648) and TV StubBus Act (DDB 649) are on.

The stub bus can be protected by a non-directional DT phase overcurrent element with a delay time set to zero seconds. To issue a stub bus trip, the overcurrent element and the StubBus Act DDB signal must assert. This can be configured in the PSL, and it is shown in the *Stub bus trip* diagram.

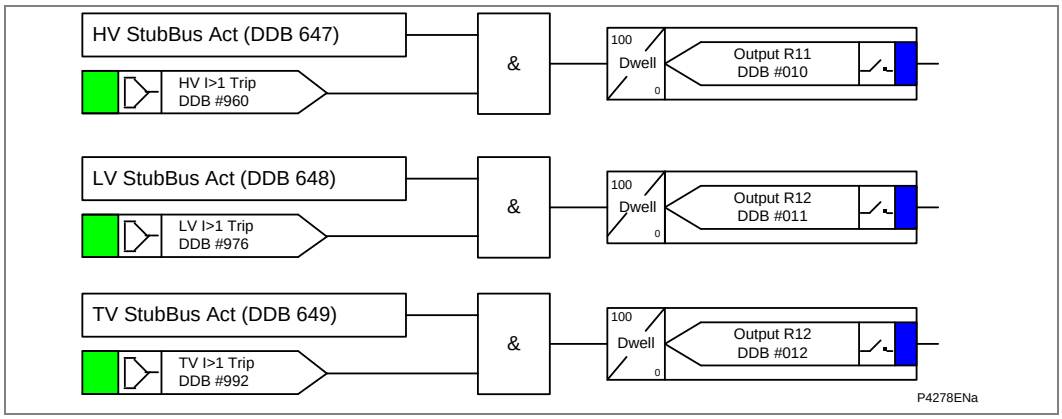


Figure 32 - Stub bus trip

2.10.1 Inputs

Signal name	Description
IA-1, IB-1, IC-1, IA-2, IB-2, IC-2, IA-3, IB-3, IC-3, IA-4, IB-4, IC-4, IA-5, IB-5, IC-5	Phase current levels (Fourier magnitudes)
HV StubBus En	High voltage stub bus enabled
LV StubBus En	Low voltage stub bus enabled
TV StubBus En	Tertiary voltage stub bus enabled

Table 10 - Inputs

2.10.2 Outputs

Signal name	Description
HV StubBus Act	High voltage stub bus activated
LV StubBus Act	Low voltage stub bus activated
TV StubBus Act	Tertiary voltage stub bus activated
HV UndCurrent	HV undercurrent detection
LV UndCurrent	LV undercurrent detection
TV UndCurrent	TV undercurrent detection

Table 11 - Outputs

2.10.3 Operation

The stub bus activation logic is shown in the *Stub bus activation logic* diagram. The inputs HV StubBus En, LV StubBus En and TV StubBus En may be assigned to opto inputs in the PSL. Each opto input is connected to a normally closed auxiliary contact from the HV, LV and TV disconnector respectively. When the opto input is energized and the undercurrent element is asserted, the StubBus Act signal will also be asserted. The outputs of this logic (HV StubBus Act, LV StubBus Act and TV StubBus Act) can be used to change the trip logic and to initiate an indication if necessary.

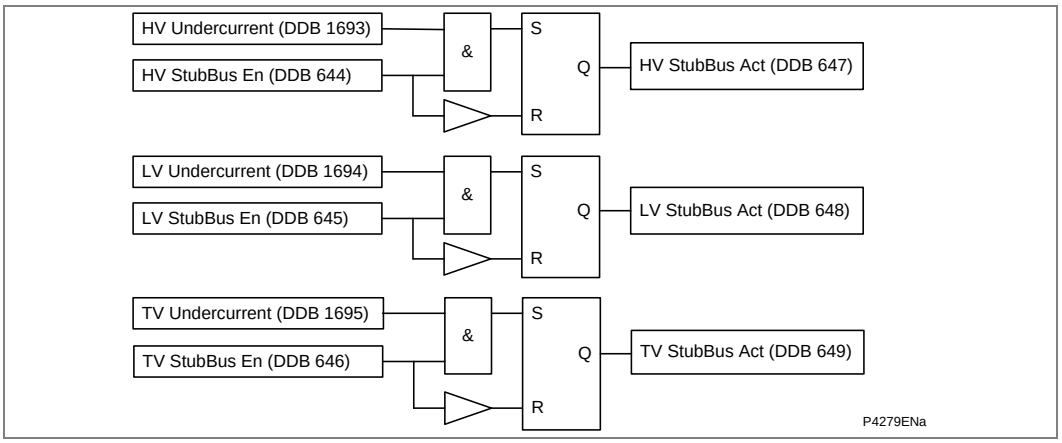


Figure 33 - Stub bus activation logic

Whenever stub bus is activated, the current signals from the winding whose isolator is open are not taken into consideration in the calculation of the differential and bias currents. For example, if a fault occurs within the protected zone and the low voltage stub bus is activated, the differential element would only trip the breakers connected to the high and tertiary sides of the transformer if the configuration shown in the *Differential trip blocked due to stub bus activation* diagram is used. Considering a lockout relay (86) per circuit breaker, the trip output contacts may be configured as shown in the *Differential trip blocked due to stub bus activation* diagram.

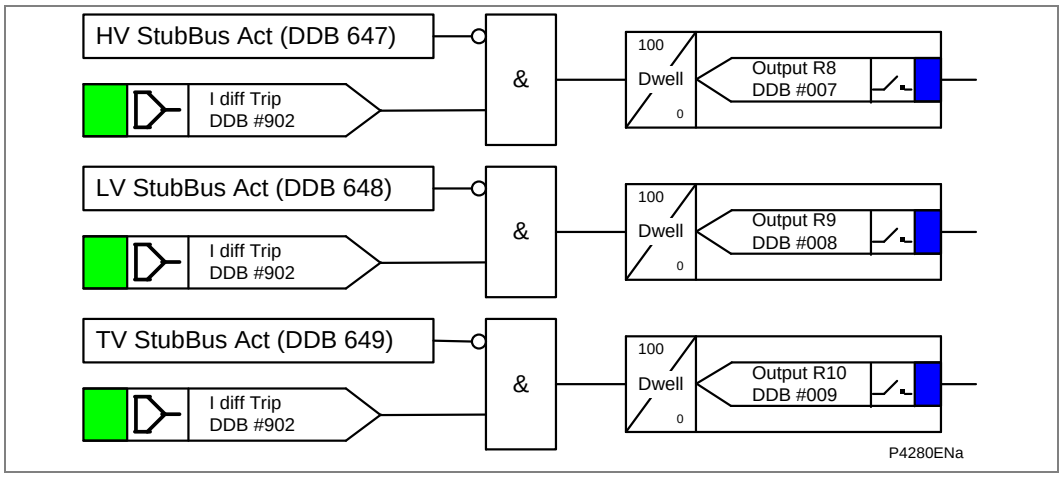


Figure 34 - Differential trip blocked due to stub bus activation

In applications where the 86 is per differential scheme, it is not possible to apply the logic in the *Differential trip blocked due to stub bus activation* diagram since the differential protection trip will be blocked each time any stub bus is activated. Hence, for this application, the stub bus protection can not be used.

The REF protection is internally blocked by the stub bus activation logic on a per winding basis. The CTS is also internally blocked by the stub bus activation logic on a per CT input basis. The breaker failure is not initiated by any general overall trip if the stub bus protection is activated (see the *Circuit Breaker Fail (CBF) Protection* section).

2.11 Circuit Breaker Fail (CBF) Protection

Up to five independent sets of Circuit Breaker Failure (CBF) settings are available. It is possible to set five breaker failure functions in the P645, three in the P643 and two in the P642. One phase and one earth undercurrent element are available per CBF function. The earth undercurrent element can be set as enabled or disabled. When enabled, it can be set as measured or derived. In the P645 and P643, TN1, TN2 and TN3 are single phase CTs that might be used by the CBF function. In the P642, single phase CTs TN1 and TN2 are available. Whenever TN1, TN2 or TN3 is wired to measure the neutral current associated to a particular breaker and **In< Input** is set as measured then TN1, TN2 or TN3 can be set in **In< Terminal**.

When there is a fault and the circuit breaker interrupts the CT primary current, the flux in the CT core decays to a residual level. This decaying flux introduces a decaying DC current in the CT secondary circuit known as subsidence current. The closer the CT is driven to its saturation point, the higher the subsidence current. The time constant of this subsidence current depends on the CT secondary circuit time constant and it is generally long. If the primary/secondary protection clears the fault, then the CBF function should reset fast to avoid operation of the CBF due to the subsidence current. A zero crossing detection algorithm has been implemented so that the CBF re-trip and back-trip signals are not asserted while subsidence current is flowing preventing the undercurrent elements to assert. The zero crossing detection algorithm considers the current inputs T1, T2, T3, T4 and T5 on a per phase basis. If **In< Input** is set as measured, current inputs TN1, TN2 and TN3 are considered by the zero crossing detection algorithm. If **In< Input** is set as derived, the neutral currents derived from T1, T2, T3, T4 and T5 current inputs are considered. If more than 12 consecutive samples are greater than 0A or more than 12 consecutive samples are smaller than 0A, then zero crossing detection is asserted; thus blocking the operation of the CBF. The zero crossing detection is asserted once the breaker in the primary system has opened so that the current flowing in the AC secondary circuit is the subsidence current.

The CBF protection incorporates two timers, CB Fail 1 Timer and CB Fail 2 Timer, allowing configuration for these situations:

- Simple CBF, where only **CB Fail 1 Timer** is enabled. Where Internal CB Fail is initiated, the **CB Fail 1 Timer** is started, and normally reset when the Circuit Breaker (CB) opens to isolate the fault.
- Internal Trip using the Programmable Scheme Logic (PSL):
- If CB opening is not detected, **CB Fail 1 Timer** times out and closes an output contact assigned to CB failure (using the PSL). This contact is used to backtrip upstream switchgear, generally tripping all infeeds connected to the same busbar section. DDB's 1528, 1530, 1532, 1534 and 1536 are associated to CBF timer1.
- A re-tripping scheme, plus delayed backtripping. Here, **CB Fail 1 Timer** is used to route a trip to a second trip circuit of the same CB. This requires duplicated CB trip coils, and is known as re-tripping. Should re-tripping fail to open the CB, a backtrip may be issued following an additional time delay. The backtrip uses **CB Fail 2 Timer**, which is also started at the instant of the initial protection element trip. DDBs 1528, 1530, 1532, 1534 and 1536 are re-trip signals and they are associated to CBF timer1. DDB's 1529, 1531, 1533, 1535 and 1537 are back-trip signals and they are associated to CBF timer2.
- CBF elements **CB Fail 1 Timer** and **CB Fail 2 Timer** can be configured to operate for trips triggered by protection elements in the relay or using an external protection trip. The latter is achieved by allocating one of the relay opto-isolated inputs to **External Trip** using the PSL.

Resetting of the CBF is possible from a breaker open indication (from the relay's pole dead logic) or from a protection reset. In these cases, resetting is only allowed provided the undercurrent elements have also reset. The resetting options are summarized in this table:

Initiation (menu selectable)	CB fail timer reset mechanism
Current based protection (e.g. 50/51/46/87.)	The resetting mechanism is fixed. [IA< operates] & [IB< operates] & [IC< operates]
Non-current based protection CBF Non I Reset setting (e.g. 27/59/81)	Three options are available. The user can select from these options. [All I< elements operate] AND [Protection element reset] [All I< elements operate] AND CB open (all 3 poles) [All I< elements operate]
External protection CBF Ext Reset	Three options are available. The user can select any or all of the options. [All I< elements operate] AND [External trip reset] [All I< elements operate] AND CB open (all 3 poles) [All I< elements operate]

Table 12 -Resetting options

If the reset option is set to I<Only, then the INTSIG Latch ResetState signal as shown in the *CB fail logic* diagram is always zero. In this case the zero-crossing detection algorithm prevents the re-trip and back-trip signals from asserting.

The CB failure logic for CB 1 is shown in the *CB fail logic* diagram. The current signals come from T1 CT. Five CBF logics are available in the P645, three in the P643 and two in the P642.

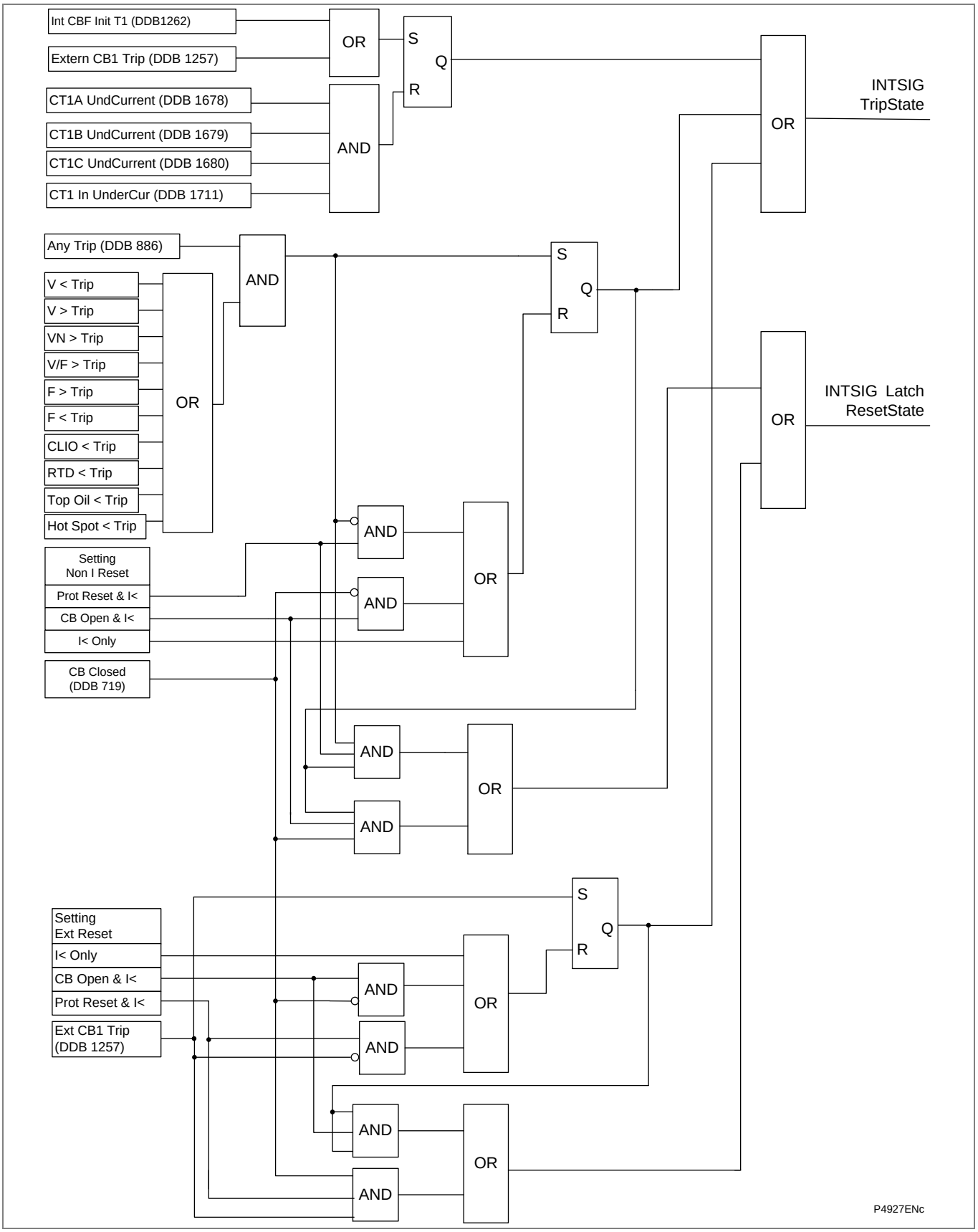


Figure 35 - CB fail logic

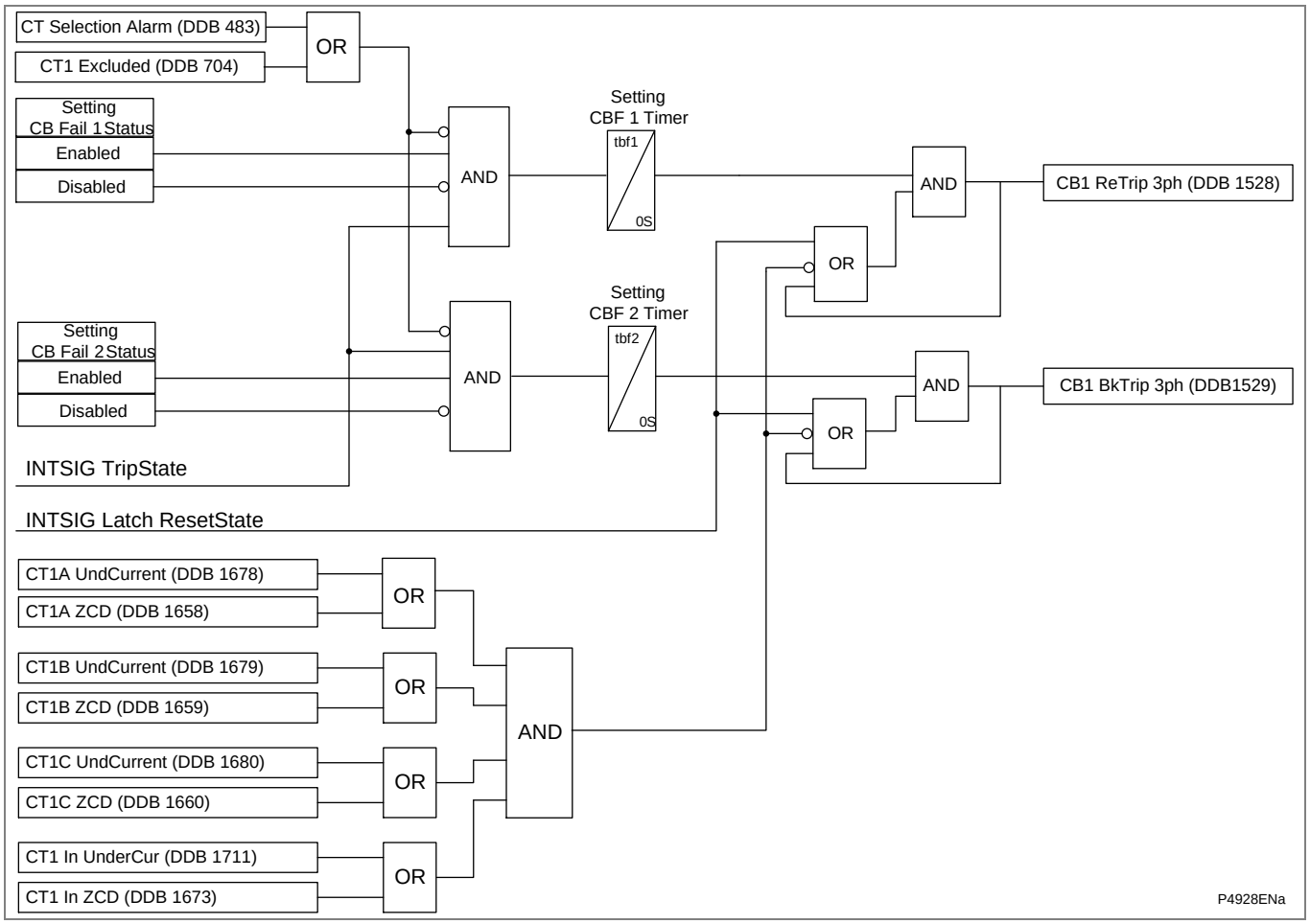


Figure 36 - CB fail logic

The waveforms shown in previous diagrams were injected to the relay. A differential trip is expected and no retrip or backtrip signals should be asserted. Note that a current waveform with maximum offset has been injected; therefore, a high flux level is expected in the CT core.

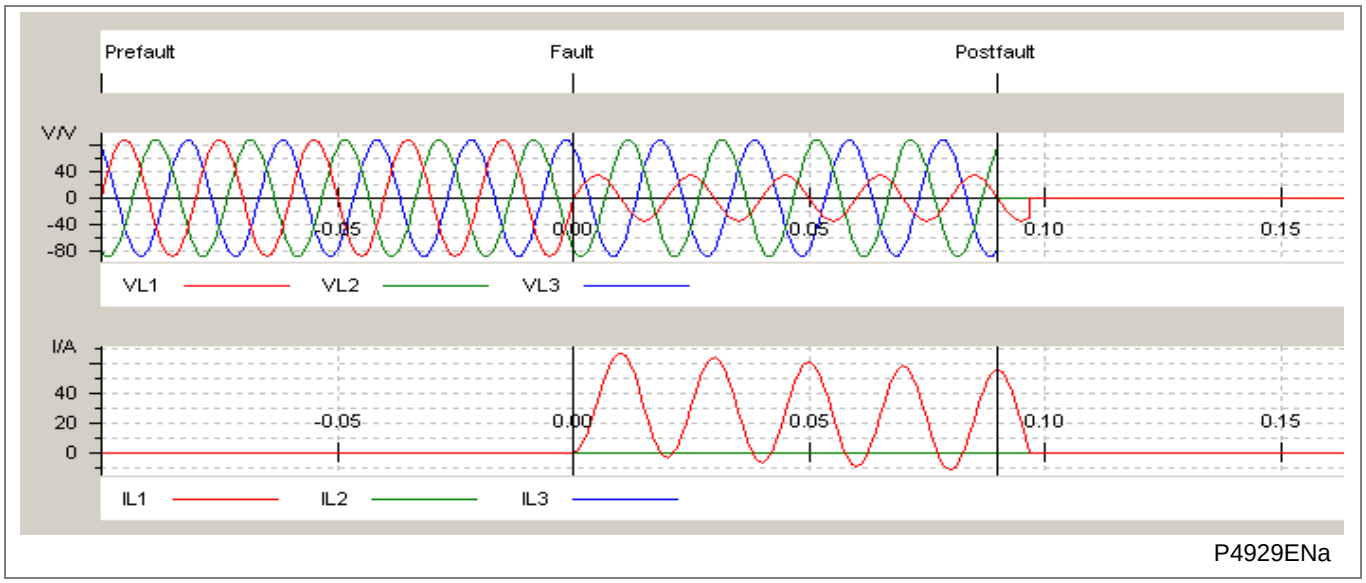


Figure 37 - CBF test - injected waveforms

The following diagram shows the disturbance record extracted from the relay. The subsidence current in phase A due to the internal CT within the relay can be observed. It takes 15ms approximately for CT1A ZCD to assert once the current is interrupted. Even if CT1A UndCurrent is not asserted, the activation of CB1 BkTrip 3ph is prevented, because CT1A ZCD asserts.

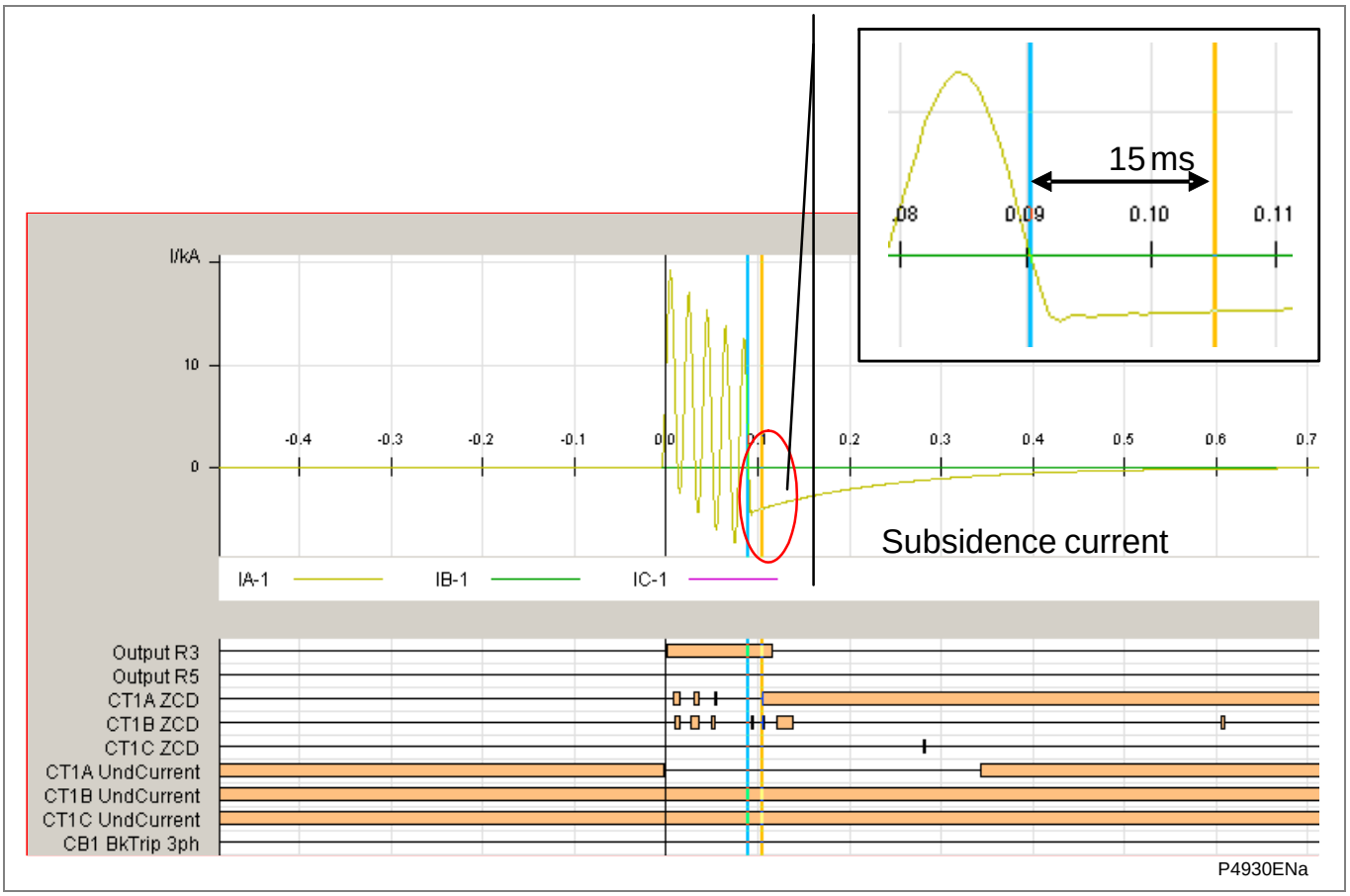


Figure 38 - CBF test - relay disturbance record

2.12 Overvoltage Protection

The overvoltage protection function is in the relay menu **Volt Protection** and it is only included in the P643 and P645 when the 3-phase VT input is available. It consists of two independent stages. These are configurable as either phase to phase or phase to neutral measuring in the **V>Measur't mode** cell.

Stage 1 may be selected as **IDMT**, **DT** or **Disabled**, in the **V>1 Function** cell. Stage 2 is **DT** only and in the **V>2 status** cell can be set as **enabled** or **disabled**.

The IDMT characteristic available on the first stage is defined by the formula:

$t = K/(M - 1)$

Where:

K = Time Multiplier Setting (TMS)
t = Operating Time in seconds
M = Measured voltage / relay setting voltage (V> Voltage Set)

The logic diagram of the first stage overvoltage function is shown in this diagram.

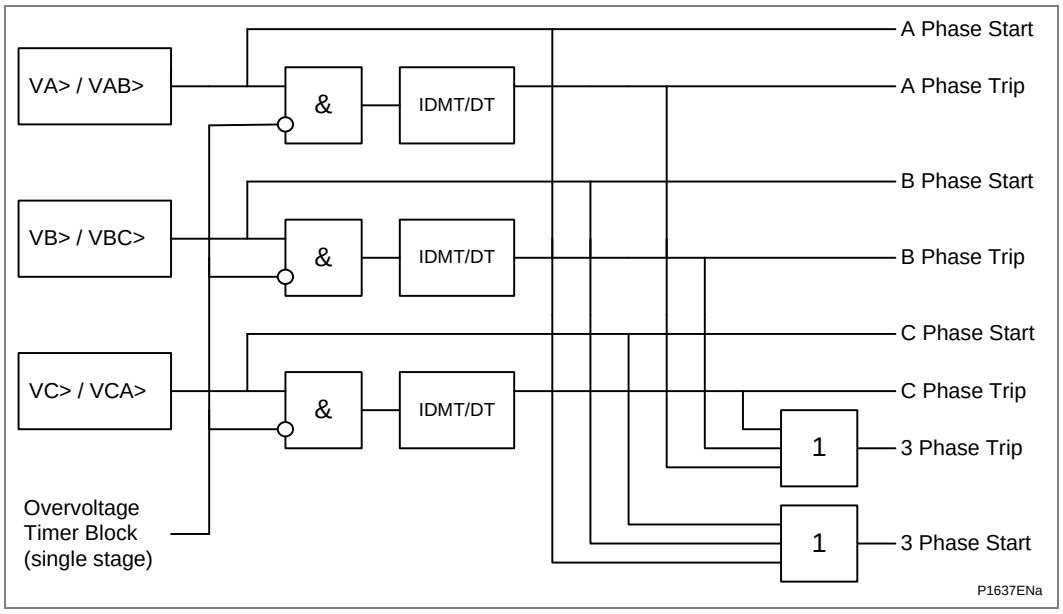


Figure 39 - Overvoltage logic diagram (single stage)

2.13 Negative Sequence Overvoltage

One definite time stage of negative sequence overvoltage is available in the P643 and P645 when the three phase VT option is fitted. This function is also available in the P642 when two single phase VTs are fitted. The negative sequence overvoltage element may be enabled/disabled within the **V2>status** cell.

In the P642, phase-to-phase voltages V_{ab} and V_{bc} are required, and the relay calculates the negative sequence voltage as:

$$\frac{\vec{V}_{ab} - a\vec{V}_{bc}}{3}$$

Where:

$$a = 1\angle 120^\circ = -0.5 + j0.866$$

The logic diagram for the negative sequence overvoltage protection is shown here:

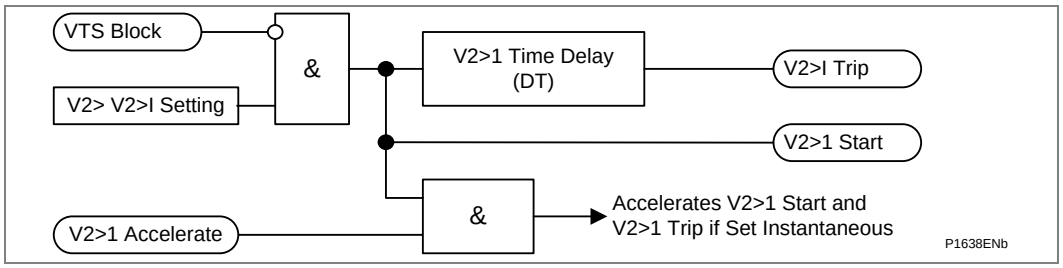


Figure 40 - Negative sequence overvoltage logic diagram

DDB signals are available to indicate a start and a trip, (Start: DDB 1622, Trip: DDB 1215). There is also a signal to accelerate the NPS overvoltage protection start (V2>1 Accelerate: DDB 663) which accelerates the operating time of the function from typically 80 ms to 40 ms when set to instantaneous.

The state of the DDB signals can be programmed to be viewed in the **Monitor Bit x** cells of the COMMISSION TESTS column in the relay.

2.14 Undervoltage Protection

The undervoltage protection function is in the relay menu **Volt Protection**, and it is only included in the P643 and P645 when the 3-phase VT input is available It consists of two independent stages. These are configurable as either **phase-to-phase** or **phase-to - neutral** measuring in the **V<Measur't mode** cell.

Stage 1 may be selected as **IDMT**, **DT** or **Disabled**, in the **V<1 Function** cell. Stage 2 is **DT** only and in the **V<2 status** cell it can be is **enabled** or **disabled**.

The IDMT characteristic available on the first stage is defined by the following formula:

$t = K/(1 - M)$

Where:

K = Time multiplier setting
t = Operating time in seconds
M = Measured voltage/relay setting voltage (V< Voltage Set)

Two stages are included to provide both alarm and trip stages, where required. Alternatively, different time settings may be required depending upon the severity of the voltage dip, i.e. motor loads will be able to withstand a small voltage depression for a longer time than if a major voltage excursion were to occur.

Outputs are available for single or three-phase conditions via the "**V<Operate Mode**" cell.

The logic diagram of the first stage undervoltage function is shown in the *Undervoltage - single and three phase tripping mode (single stage)* diagram below:

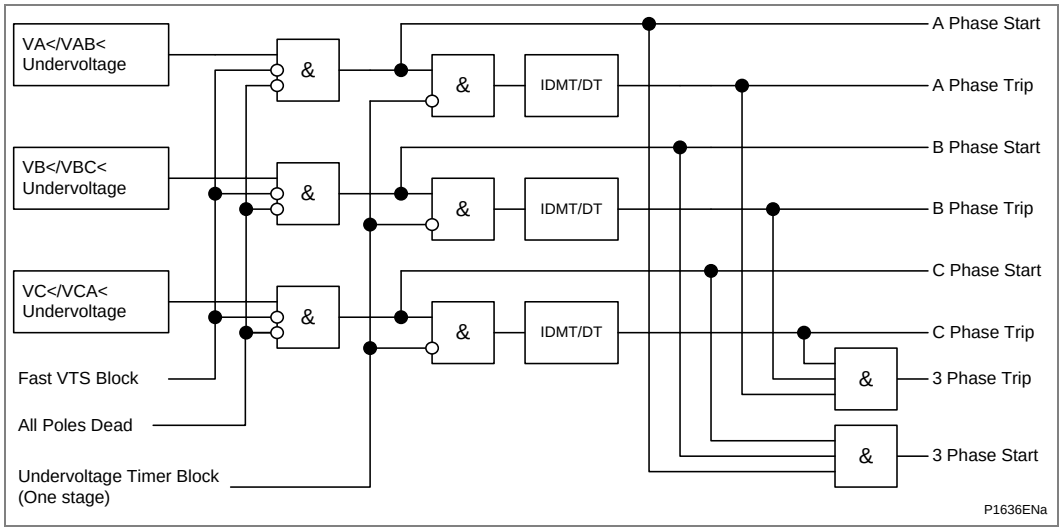


Figure 41 - Undervoltage logic diagram (single stage)

When the protected feeder is de-energized, or the circuit breaker is opened, an undervoltage condition would be detected. Therefore, the "**V<Poledead Inh**" cell is included for each of the two stages to block the undervoltage protection from operating for this condition. If the cell is enabled, the relevant stage will become inhibited by the in-built pole dead logic within the relay. This logic produces an output when it detects either an open circuit breaker via auxiliary contacts feeding the relay opto inputs or it detects a combination of both undercurrent and undervoltage on any one phase.

Note	*When the setting "**oper mode**" set to '**Any Phase**', the stage DDB will be from an OR gate output of the three individual phases start/trip and when it is set to '**Three Phase**', the stage DDB will be from an AND gate output of the three individual phases signal. This is applicable for over voltage and rate of change of voltage protection.*

2.15 Residual Overvoltage (Neutral Displacement) Protection

The residual overvoltage protection is included in the P643 and P645 when the 3-phase VT input is available.

On a healthy 3-phase power system, the addition of each of the 3-phase to earth voltages is nominally zero, as it is the vector addition of three balanced vectors at 120° to one another. However, when an earth fault occurs on the primary system this balance is upset and a 'residual' voltage is produced. This could be measured, for example, at the secondary terminals of a voltage transformer having a "broken delta" secondary connection. Hence, a residual voltage-measuring relay can be used to offer earth fault protection on such a system.

Note	*This condition causes a rise in the neutral voltage with respect to earth that is commonly referred to as "neutral voltage displacement" or NVD.*

The detection of a residual overvoltage condition is an alternative means of earth fault detection, which does not require any measurement of current. This may be particularly advantageous in high impedance earthed or insulated systems, where the provision of core balance CTs on each feeder may be either impractical, or uneconomic.

The relay internally derives the NVD voltage from the 3-phase voltage input that must be supplied from either a 5-limb or three single-phase VTs. The NVD element in the P64x relays is a two-stage design, each stage having separate voltage and time delay settings. Stage 1 may be set to operate on either an IDMT or DT characteristic, while stage 2 may be set to DT only.

The IDMT characteristic available on the first stage is defined by the formula:

$t = K/(M-1)$

Where:

K = Time multiplier setting
t = Operating time in seconds
M = Derived residual voltage/relay setting voltage (VN> Voltage Set)

Two stages are included for the NVD protection to account for applications that require both alarm and trip stages, for example, an insulated system. It is common in such a case for the system to have been designed to withstand the associated healthy phase overvoltages for a number of hours following an earth fault. In such applications, an alarm is generated soon after the condition is detected, which serves to indicate the presence of an earth fault on the system. This gives time for system operators to locate and isolate the fault. The second stage of the protection can issue a trip signal if the fault condition persists.

The functional block diagram of the first stage residual overvoltage is shown in the following *Residual overvoltage logic (single stage)* diagram:

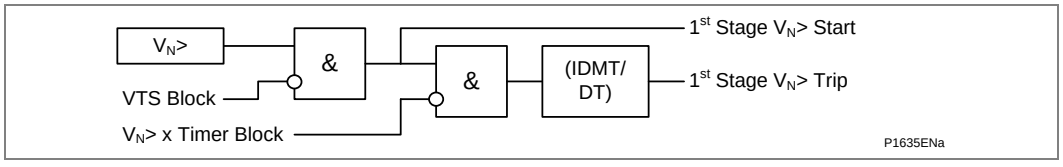


Figure 42 - Residual overvoltage logic (single stage)

VTS blocking when asserted, effectively blocks the start outputs.

When enabled, these signals are set by the residual overvoltage logic according to the status of the monitored function:

VN>1 Start	(DDB 1596)	1st Stage Residual Overvoltage Start
VN>2 Start	(DDB 1597)	2nd Stage Residual Overvoltage Start
VN>1 Timer Blk	(DDB 566)	Block Residual Overvoltage Stage 1 Time Delay
VN>2 Timer Blk	(DDB 567)	Block Residual Overvoltage Stage 2 Time Delay
VN>1 Trip	(DDB 1238)	1st Stage Residual Overvoltage Trip
VN>2 Trip	(DDB 1239)	2nd Stage Residual Overvoltage Trip

2.16 Frequency Protection

The P14x/P341/P34x/P391/P445/P44y/P54x/P64x/P841 feeder relay includes 4 stages of underfrequency and 2 stages of overfrequency protection to facilitate load shedding and subsequent restoration. The underfrequency stages may be optionally blocked by a pole dead (CB Open) condition. All the stages may be enabled/disabled in the "**F<n Status**" or "**F>n Status**" cell depending on which element is selected.

The logic diagram for the underfrequency logic is as shown in the following *Underfrequency logic (single stage)* diagram. Only a single stage is shown. The other three stages are identical in functionality.

If the frequency is below the setting and not blocked the DT timer is started. Blocking may come from the All_Poledead signal (selectively enabled for each stage) or the underfrequency timer block.

If the frequency cannot be determined, the function is also blocked.

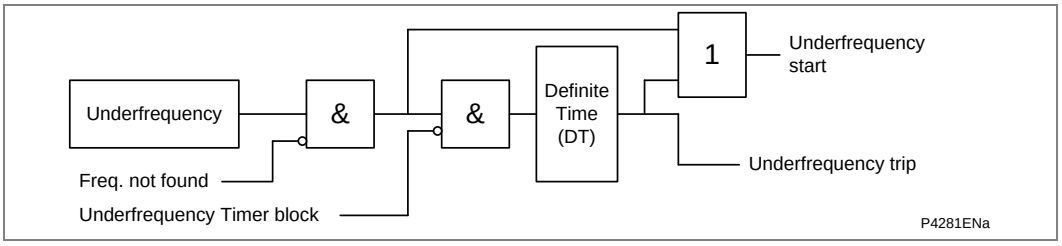


Figure 43 - Underfrequency logic (single stage)

The functional logic for the overfrequency function as shown in the *Overfrequency logic (single stage)* diagram. Only a single stage is shown as the other stages are functionally identical. If the frequency is above the setting and not blocked the DT timer is started and after this has timed out the trip is produced. Blocking may come from the All_Poledead signal (selectively enabled for each stage) or the overfrequency timer block.

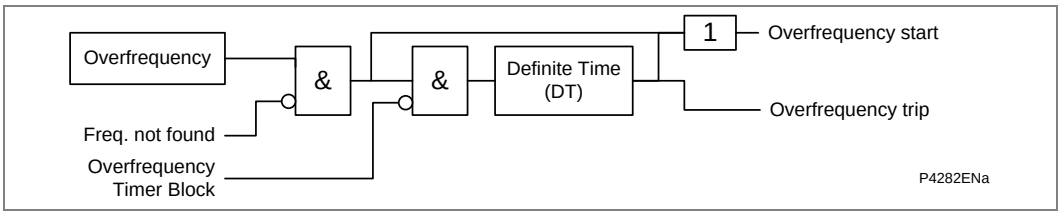


Figure 44 - Overfrequency logic (single stage)

When enabled, the following signals are set by the under/overfrequency logic according to the status of the monitored functions.

Function	DDb	Description
F<1 Timer Block	(DDB 638)	Block Underfrequency Stage 1 Timer
F<2 Timer Block	(DDB 639)	Block Underfrequency Stage 2 Timer
F<3 Timer Block	(DDB 640)	Block Underfrequency Stage 3 Timer
F<4 Timer Block	(DDB 641)	Block Underfrequency Stage 4 Timer
F>1 Timer Block	(DDB 642)	Block Overfrequency Stage 1 Timer
F>2 Timer Block	(DDB 643)	Block Overfrequency Stage 2 Timer
F<1 Start	(DDB 1608)	Underfrequency Stage 1 Start
F<2 Start	(DDB 1609)	Underfrequency Stage 2 Start
F<3 Start	(DDB 1610)	Underfrequency Stage 3 Start
F<4 Start	(DDB 1611)	Underfrequency Stage 4 Start
F>1 Start	(DDB 1612)	Overfrequency Stage 1 Start
F>2 Start	(DDB 1613)	Overfrequency Stage 2 Start
F<1 Trip	(DDB 1230)	Underfrequency Stage 1 Trip
F<2 Trip	(DDB 1231)	Underfrequency Stage 2 Trip
F<3 Trip	(DDB 1232)	Underfrequency Stage 3 Trip
F<4 Trip	(DDB 1233)	Underfrequency Stage 4 Trip
F>1 Trip	(DDB 1228)	Overfrequency Stage 1 Trip
F>2 Trip	(DDB 1229)	Overfrequency Stage 2 Trip

Table 13 - Signals logic

2.17 Thermal Overload Protection (49)

Transformer thermal overload protection is designed to protect the equipment from sustained overload that results in the machine's thermal rating being exceeded. Thermal overload protection compliments the transformer overcurrent protection by allowing modest but transient overload conditions to occur, while tripping for sustained overloads that the overcurrent protection will not detect.

The thermal overload function is based on the IEEE Standard C57.91-1995. This function can be enabled or disabled in the setting or it can be blocked in the PSL. Two three-stage definite time-delayed trip elements based on hot spot or top oil temperature are available. A pre-trip alarm is offered in the tPre-trip Set setting. This alarm indicates that thermal overload will trip after the settable time if load level remains unchanged.

Four cooling modes are available, and the oil exponent and winding exponent can be set independently for each mode. The cooling mode selection can be done automatically via PSL or manually in the setting file. Two opto inputs must be configured as CM Select 1X (DDB 709) and CM Select X1 (DDB 710) in PSL and the appropriate contacts must be wired to energize/de-energize these inputs. The selected cooling mode would vary as indicated below:

CM Select 1X (DDB 709)	CM Select X1 (DDB 710)	Selected Cooling Mode
0	0	1
0	1	2
1	0	3
1	1	4

Table 14 - Selected cooling modes

The monitor winding can be set to HV, LV, TV or biased current. If the monitor winding is set to HV and the HV breaker is open, then the current flows from LV to TV. Likewise, if the monitor winding is set to LV and the LV breaker is open, then the current flows from HV to TV. If the monitor winding is set to biased current an overall through loading picture of the transformer is provided.

To calculate the top oil and hot spot winding temperature, the relay takes into consideration the ratio of the ultimate load to the rated load. The rated load is determined by the IB and the rating settings. When the monitored winding is set as the HV winding, the rated load is calculated using the HV Rating and the IB settings. When the monitored winding is set as the LV winding, the rated load is calculated using the LV Rating and the IB settings. When the monitored winding is set as the TV winding, the rated load is calculated using the TV Rating and the IB settings. When the monitored winding is set as the biased current, the rated load is calculated using the REF Power S and the IB settings. The ultimate load is the load that is actually being fed by the transformer.

The biased current used by the thermal protection is not the same as the biased current used by the differential protection. No vector correction or zero sequence filtering is taken into account. To calculate the bias current, the thermal element considers the maximum rms current on a per winding basis. Note that the bias current calculation performed by the thermal element is not on a per-phase basis. The thermal bias current calculation is as follows:

$$I_{bias} = \frac{\frac{\text{Max}\,[I_{HVArms}, I_{HVBrms}, I_{HVCrms},]}{HV\_FLC_{Sref}} + \frac{\text{Max}\,[I_{LVArms}, I_{LVBrms}, I_{LVCrms},]}{LV\_FLC_{Sref}} + \frac{\text{Max}\,[I_{TVArms}, I_{TVBrms}, I_{TVCrms},]}{TV\_FLC_{Sref}}}{2}$$

Where:
HV_FLC_{Sref} = HV full load current at the reference power
LV_FLC_{Sref} = LV full load current at the reference power
TV_FLC_{Sref} = TV full load current at the reference power

The thermal overload model is executed once every power cycle. The thermal overload trip can be based on either hot spot temperature or top oil temperature, or both.

2.17.1 Inputs

Signal name	Description
IA-HV, IB-HV, IC-HV, IA-LV, IB-LV, IC-LV, IA-TV, IB-TV, IC-TV	Phase current levels (raw samples). The currents required by the thermal overload element are the currents of the winding being monitored.
IA-bias, IB-bias, IC-bias	Bias currents
Θ_{TO}	Measured top oil temperature
Θ_A	Measured ambient temperature
Reset thermal (DDB 888)	Reset thermal overload
TRF De-energized (DDB 878)	Transformer de-energized. If it is asserted, the transformer no-load losses are not considered.
CM Select 1X (DDB 709)	CM Select 1X is used together with CM Select X1 to configure the cooling mode selector in PSL. This selector allows choosing one of four cooling modes.
CM Select X1 (DDB 710)	CM Select 1X is used together with CM Select X1 to configure the cooling mode selector in PSL. This selector allows choosing one of four cooling modes.

Table 15 - Inputs

2.17.2 Outputs

Signal name	Description
Top oil >1 start (DDB 1337)	Top oil first stage start
Top oil >2 start (DDB 1338)	Top oil second stage start
Top oil >3 start (DDB 1339)	Top oil third stage start
Top oil >1 trip (DDB 957)	Top oil first stage trip
Top oil >2 trip (DDB 958)	Top oil second stage trip
Top oil >3 trip (DDB 959)	Top oil third stage trip
Hot spot >1 start (DDB 1334)	Hot spot first stage start
Hot spot >2 start (DDB 1335)	Hot spot second stage start
Hot spot >3 start (DDB 1336)	Hot spot third stage start
Hot spot >1 trip (DDB 954)	Hot spot first stage trip
Hot spot >2 trip (DDB 955)	Hot spot second stage trip
Hot spot >3 trip (DDB 956)	Hot spot third stage trip
Pre-trip alarm (DDB 478)	Thermal pre-trip alarm
Ambient T	Ambient temperature measurement
Top oil T	Top oil temperature measurement
Hot spot T	Hot spot temperature measurement
TOL Pre-trip left	Pre-trip time left measurement

Table 16 - Outputs

2.17.3 Operation

The thermal overload protection in the relay uses the thermal model given by the equations for hot spot and top oil temperatures. A discrete time thermal replica model is implemented and it is described by the equations for $\Delta\Theta_{TOn}$ and $\Delta\Theta_{Hn}$.

If the top oil temperature is not available as a measured input quantity, it is calculated every cycle by the following equation:

$$\Theta_{TO} = \Theta_A + \Delta\Theta_{TO}$$

Where:
Θ_{TO} = Top oil temperature
Θ_A = Ambient temperature
$\Delta\Theta_{TO}$ = Top oil rise over ambient temperature due to a step load change

The ambient temperature can be measured directly or it can be set in the Average Amb T setting. $\Delta\Theta_{TO}$ is given by the following exponential expression containing an oil time constant:

$$\Delta\Theta_{TOn} = (\Delta\Theta_{TO,U} - \Delta\Theta_{TO,n-1}) \left(1-e^{-\left(\frac{\Delta t}{\tau_{TO}}\right)}\right) + \Delta\Theta_{TO,n-1}$$

Where:
$\Delta\Theta_{TO,U}$ = ultimate top oil rise over ambient temperature for load L
$\Delta\Theta_{TO,n-1}$ = the previous top oil rise over ambient temperature
Δ_t = elapsed time between the ultimate top oil rise and the initial top oil rise
τ_{TO} = oil time constant of the transformer for any load L between the ultimate top oil rise and the initial top oil rise. This parameter is set by the user.

By using power series, top oil rise, $\Delta\Theta_{TOn}$, can be approximated as shown below:

$$\Delta\Theta_{TOn} = (\Delta\Theta_{TO,U} - \Delta\Theta_{TO,n-1}) \left(\frac{\Delta t}{\tau_{TO}}\right) + \Delta\Theta_{TO,n-1}$$

$$\tau_{TOcorrected} = t_{TO} \times \frac{\left(\frac{\Delta\Theta_{TO,U}}{\Delta\Theta_{TO,R}}\right) - \left(\frac{\Delta\Theta_{TO,n-1}}{\Delta\Theta_{TO,R}}\right)}{\left(\frac{\Delta\Theta_{TO,U}}{\Delta\Theta_{TO,R}}\right)^{\frac{1}{n}} - \left(\frac{\Delta\Theta_{TO,n-1}}{\Delta\Theta_{TO,R}}\right)^{\frac{1}{n}}}$$

Where:
τ_{TO} = oil time constant of the transformer for any load L between the ultimate top oil rise and the initial top oil rise. This parameter is set by the user.
$\Delta\Theta_{TO,U}$ = ultimate top oil rise over ambient temperature for load L.
$\Delta\Theta_{TO,n-1}$ = the previous top oil rise over ambient temperature.
n = Oil exponent. This parameter is set by the user.

The ultimate top oil rise is given by the following equation:

$$\Delta\Theta_{TO,U} = \Delta\Theta_{TO,R} \left[\frac{K_U^2 R+1}{R+1}\right]^n$$

Where:
K^u= the ratio of ultimate load L to rated load
R = the ratio of the load loss at rated load to no load loss. This parameter is set by the user.
n = Oil exponent. This parameter is set by the user.
$\Delta\Theta_{TO,R}$ = top oil rise over ambient temperature at rated load. This parameter is set by the user.

The hot spot temperature can only be obtained by calculation. This equation is used to calculate the hot spot temperature every cycle:

$$\Theta_H = \Theta_{TO} + \Delta\Theta_H$$

Where:
Θ_H = Hot spot (winding) temperature
Θ_{TO} = Top oil temperature
$\Delta\Theta_H$ = Hot spot rise above top oil temperature

The hot spot temperature rise over top oil temperature, $\Delta\Theta_H$, is given by:

$$\Delta\Theta_{Hn} = (\Delta\Theta_{H,U} - \Delta\Theta_{H,n-1})\left(1\text{-}e^{-\left(\frac{\Delta t}{\tau_w}\right)}\right) + \Delta\Theta_{H,n-1}$$

Where:
$\Delta\Theta_{H,U}$ = ultimate hot spot rise over top oil temperature for load L
$\Delta\Theta_{H,n-1}$ = previous hot spot rise over top oil temperature
Δt = elapsed time between the ultimate hot spot rise and the initial hot spot rise. Δt is one cycle.
τ_W = winding time constant at hot spot location. This parameter is set by the user.

By using power series, hot spot temperature rise, $\Delta\Theta_{Hn}$, can be approximated as below:

$$\Delta\Theta_{Hn} = (\Delta\Theta_{H,U} - \Delta\Theta_{H,n-1})\left(\frac{\Delta t}{\tau_w}\right) + \Delta\Theta_{H,n-1}$$

The ultimate hot spot rise over top oil is given by:

$$\Delta\Theta_{H,U} = \Delta\Theta_{H,R}\, K_U^{2m}$$

Where:
$\Delta\Theta_{H,R}$ = winding hottest spot rise over top oil temperature at rated load. This parameter is set by the user.
K_U = the ratio of ultimate load L to rated load
m = winding exponent. This parameter is set by the user.

The load current used in the calculations is the rms value. The rms current is calculated according to the following equation:

$$L_{rms} = \sqrt{\frac{L_1^2 + L_2^2 + \ldots + L_{24}^2}{24}}$$

Where L_n is the sample, there are 24 sample per cycle.

Hot spot temperature, Top oil temperature and ambient temperature are stored in non-volatile memory. These measurements are updated every power cycle. The thermal state can be reset to zero by any of the following:

- The **Reset X Thermal** cell under the **MEASUREMENT 4** heading on the front panel
- A remote communications interface command
- A status input state change.

The top oil temperature, hot spot temperature, ambient temperature and pre-trip time left are available as a measured value in the **Measurement 4** column.

If a more accurate representation of the thermal state of the transformer is required, the use of temperature monitoring devices (RTDs or CLIO) which target specific areas is recommended. Also, for short time overloads the application of RTDs/CLIO and overcurrent protection can provide better protection.

The transformer de-energized signal (DDB 878) has been configured in the default PSL logic. It is asserted when all the breakers are open. If this signal is asserted, the transformer no-load losses are not considered. As a result, the top oil and hottest spot temperatures are equal to the ambient temperature when the monitored current is zero. If this signal is de-asserted, the top oil and hottest spot temperatures are not equal to the ambient temperature even when the monitored current is zero. In this case the top oil and hottest spot temperatures will increase according to the equations described above.

2.18 Loss Of Life (LOL) Statistics

Deterioration of insulation is a time function of temperature. Since the temperature distribution is not uniform, the part that is operating at the highest temperature undergoes the greatest deterioration. Therefore the hot spot temperature is considered in loss of life statistics. The loss of life model is executed every cycle.

Two one-stage definite time delay alarm based on aging acceleration factor (F_{AA}) or loss of life (LOL) are available.

A reset command is provided to allow the user to reset the calculated parameters: LOL status, LOL aging factor (F_{AA}), mean aging factor ($F_{AA.m}$), rate of loss of life (Rate of LOL), residual life at F_{AAm} (Lres at $F_{AA,m}$), residual life at designed (Lres at designed).

2.18.1 Inputs

Signal name	Description
IA-HV, IB-HV, IC-HV, IA-LV, IB-LV, IC-LV, IA-TV, IB-TV, IC-TV	Phase current levels (raw samples). The currents required by the thermal overload element are the currents of the winding being monitored.
IA-bias, IB-bias, IC-bias	Bias currents
Θ_H	Calculated hot spot temperature
Reset LOL	Reset loss of life

Table 17 - Inputs

2.18.2 Outputs

Signal name	Description
FAA Alarm	Aging acceleration factor alarm
Loss of Life Alm	Loss of life alarm
LOL status	Accumulated loss of life (LOL) measurement in hrs
Lres at designed	Residual life at reference hottest spot temperature
Rate of LOL	Rate of loss of life (ROLOL) measurement in %
LOL aging factor	Aging acceleration factor (F_{AA}) measurement
FAA,m	Mean aging acceleration factor ($F_{AA,m}$) measurement
Lres at FAA,m	Residual life hours at $F_{AA,m}$ ($L_{res}(F_{AA,m})$) measurement

Table 18 - Outputs

2.18.3 Operation

As indicated in IEEE Std. C57.91-1995 the aging acceleration factor is the rate at which transformer insulation aging for a given hottest spot temperature is accelerated compared with the aging rate at a reference hottest spot temperature. For 65°C average winding rise transformers, the reference hottest spot temperature is 110°C. For 55°C average winding rise transformers, the reference hottest spot temperature is 95°C. For hottest spot temperatures in excess of the reference hottest spot temperature the aging acceleration factor is greater than 1. For hottest spot temperatures lower than the reference hottest spot temperature, the aging acceleration factor is less than 1.

The model used for loss of life statistics is given by the equations for LOL and F_{AA}. LOL is calculated every hour according to this formula:

$$LOL = L(\Theta_{H,r}) - L_{res}(\Theta_{H,r})$$

Where:

$L(\Theta_{H,r})$ = life hours at reference winding hottest-spot temperature. This parameter is set by the user.

$L_{res}(\Theta_{H,r})$ = residual life hours at reference winding hottest-spot temperature

The aging acceleration factor F_{AA} is calculated every cycle as follows:

$$F_{AA} = \frac{L(\Theta_{H,r})}{L(\Theta_H)} = \frac{e^{\left[A + \frac{B}{\Theta_{H,r} + 273}\right]}}{e^{\left[A + \frac{B}{\Theta_H + 273}\right]}} = e^{\left[\frac{B}{\Theta_{H,r} + 273} - \frac{B}{\Theta_H + 273}\right]}$$

If a 65°C average winding rise transformer is considered, the equation for F_{AA} is:

$$FAA = e^{\left[\frac{B}{383} - \frac{B}{\Theta_H + 273}\right]}$$

If a 55°C average winding rise transformer is considered, the equation for F_{AA} is:

$$FAA = e^{\left[\frac{B}{368} - \frac{B}{\Theta_H + 273}\right]}$$

Where:

$L(\Theta_H)$ = life hours at winding hottest-spot temperature

Θ_H = hottest-spot temperature as calculated in thermal overload protection

$\Theta_{H,r}$ = hottest-spot temperature at rated load.

B = constant B from life expectancy curve. This parameter is set by the user. IEEE Std. C57.91-1995 recommends a B value of 15000.

The residual life hours at reference hottest-spot temperature is updated every hour as follows:

$$L_{res}(\Theta_{H,r}) = L_{res,p}(\Theta_{H,r}) - \frac{\sum_{i=1}^{3600} F_{AA,i}(\Theta_H)}{3600}$$

Where:

$L_{res,p}(\Theta H,r)$ = residual life hours at reference temperature one hour ago

$F_{AA,i}(\Theta H)$ = Mean aging acceleration factor, as calculated above. It is calculated every second.

The accumulated Loss Of Life (LOL) will be updated in non-volatile memory once per hour. It will be possible to reset and set a new loss of life figure, in the event that a relay is applied in a new location with a pre-aged resident transformer.

The Rate Of Loss Of Life (ROLOL) in percent per day is given as follows, and it is updated every day:

$$ROLOL = \frac{24}{L_{res}(\Theta_{H,r})} F_{AA,m}(\Theta_H)\ 100\%$$

The mean aging acceleration factor, $F_{AA,m}$, is updated per day, and it is given by:

$$F_{AA,m} = \frac{\sum_{n=1}^{N} F_{AAn}\,\Delta t_n}{\sum_{n=1}^{N} \Delta t_n} = \frac{\sum_{n=1}^{N} F_{AAn}}{N}$$

Where:

F_{AAn} is calculated every cycle

Δtn = 1cycle

$F_{AA,\,m}$ states the latest one-day statistics of F_{AA}. When the relay is energized for the first time, $F_{AA,\,m}$ default value is 1.

The residual life in hours at $F_{AA,m}$ is updated per day, and it is given by:

$$L_{res}(F_{AA,m}) = \frac{L_{res}(\Theta_{H,r})}{F_{AA,m}}$$

2.19 Through Fault Monitoring

Through faults are a major cause of transformer damage and failure. Both the insulation and the mechanical effects of fault currents are considered. The through fault current monitoring function in the relay gives the fault current level, the duration of the faulty condition, the date and time for each through fault. An I^2t calculation based on the recorded time duration and maximum current is performed for each phase. This calculation is only performed when the current is above the **TF I> Trigger** setting and if **Any Differential Start** is not asserted. Cumulative stored calculations for each phase are monitored so that the user may schedule the transformer maintenance based on this data. This may also justify possible system enhancement to reduce through fault level.

One stage alarm is available for through-fault monitoring. The alarm is issued if the maximum cumulative I^2t in the three phases exceeds **the TF I2t> Alarm** setting. A through fault event is recorded if any of the phase currents is bigger than the TF I> Trigger setting. Set **TF I> Trigge**r greater than the overload capability of the transformer. According to IEEE Std. C57.109-1993, values of 3.5 or less times normal base current may result from overloads rather than faults. IEEE Std. C57.91-1995, states that the suggested limit of load for loading above the nameplate of a distribution transformer with 65°C rise is 300% of rated load during short-time loading (0.5 hours or less). On the other hand, the suggested limit of load for loading above the nameplate of a power transformer with 65°C rise (55°C in the P64x) is 200% maximum.

To set **TF I2t> Alarm** consider the recommendations given in IEEE Std. C57.109-1993 for transformers built beginning in the early 1970s. Consult the transformer manufacturer regarding the short circuit withstand capabilities for transformers built prior the early 1970s.

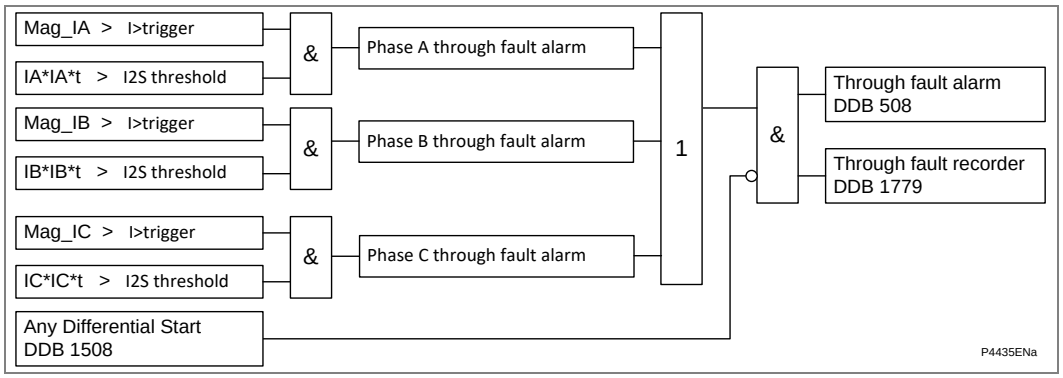


Figure 45 - Through fault alarm logic

2.19.1 Inputs

Signal name	Description
IA-HV, IB-HV, IC-HV or IA-LV, IB-LV, IC-LV or IA-TV, IB-TV, IC-TV	Phase current levels (Fourier magnitudes) of the selected winding
Any Diff start (DDB1508)	Any 87 or 64 start used by the through fault monitoring logic to avoid:calculating I^2t if either the 87 or 64 element has started. Asserting a through fault alarm when either the 87 or 64 element has started.

Table 19 - Inputs

2.19.2 Outputs

Signal name	Description
IA peak, IB peak, IC peak	Peak current in the monitor winding in a per phase basis
I^2t phase A, I^2t phase B, I^2t phase C	I^2t magnitude in the monitor winding in a per phase basis
Through fault alarm (DDB508)	Through fault monitoring alarm
Through fault recorder (DDB1779)	Output signal from the through fault monitoring logic used to trigger the fault recorder

Table 20 - Outputs

IA peak, IB peak, IC peak, I2t phase A, I2t phase B and I2t phase C are given in the VIEW RECORDS menu in the setting file.

2.20 Resistive Temperature Device (RTD) Thermal Protection

To protect against any general or localized overheating, the relay can accept inputs from up to 10 - 3-wire Type A PT100, Ni100 or Ni120 Resistive Temperature Sensing Devices (RTD). These are connected as shown in the *Connection for RTD thermal probes* diagram below.

Such probes can be strategically placed in areas of the machine that are susceptible to overheating or heat damage.

The probes can also be used to measure the external ambient temperature. The ambient temperature can be used to adapt the thermal overload protection operating time. A main and back-up RTD can be selected in the settings for the external ambient temperature.

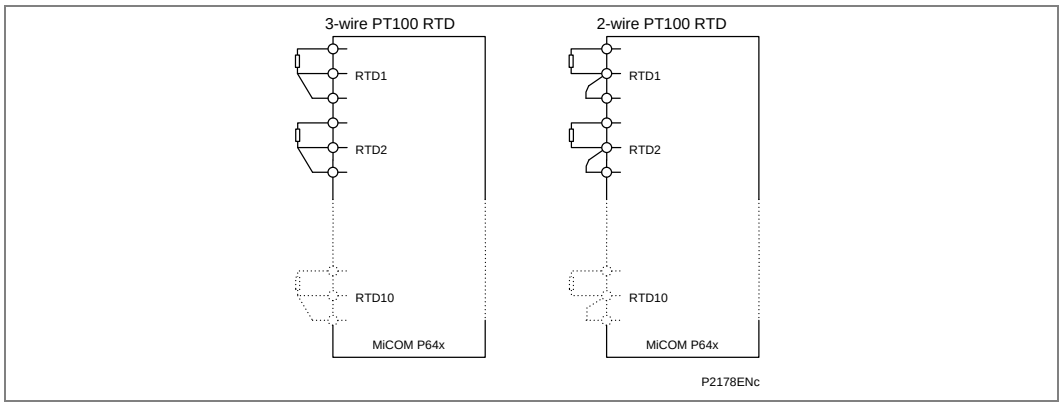


Figure 46 - Connection for RTD thermal probes

The units of temperature measurement Celsius or Fahrenheit can also be selected.

Typically, a PT100 RTD probe can measure temperature within the range -40° to +300°C. The resistance of these devices changes with temperature, at 0°C they have a resistance of 100Ω.

If the measured resistance is outside the permitted range, an RTD failure alarm will be raised, indicating an open or short circuit RTD input.

These conditions are signaled using DDB signals available in the PSL (DDB 453-456) and are also shown in the **Measurements 3** menu.

DDB signals are also available to indicate the alarm and trip of the each and any RTD, (Alarm: DDB 1728-1737, 452 Trip: DDB 1188-1197, 1198). The state of the DDB signals can be programmed to be viewed in the **Monitor Bit x** cells of the **COMMISSION TESTS** column in the relay.

See the *Installation* chapter, for recommendations on RTD connections and cables.

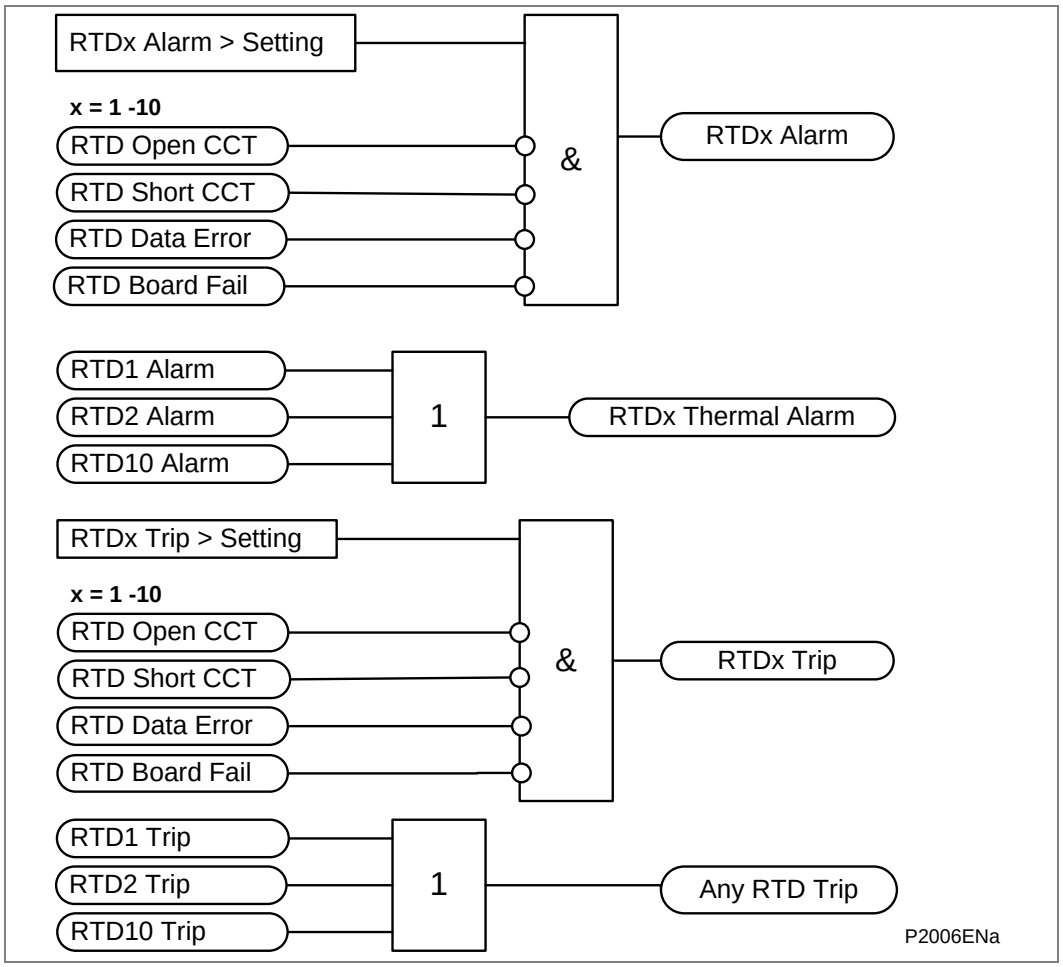


Figure 47 - RTD logic diagram

2.21 Current Loop Inputs and Outputs

2.21.1 Current Loop Inputs

Four analog (or current loop) inputs are provided for transducers with ranges of 0 - 1 mA, 0 - 10 mA, 0 - 20 mA or 4 - 20 mA. The analog inputs can be used for various transducers such as vibration monitors, tachometers and pressure transducers. Associated with each input there are two protection stages, one for alarm and one for trip. Each stage can be individually enabled or disabled and each stage has a definite time delay setting.

The Alarm and Trip stages can be set for operation when the input value falls below the Alarm/Trip threshold **Under** or when the input current is above the input value **Over**. The sample interval is nominally 50 ms per input.

The relationship between the transducer measuring range and the current input range is linear. The maximum and minimum settings correspond to the limits of the current input range. This relationship is shown in the *Relationship between the transducer measuring quantity and the current input range* diagram.

This diagram also shows the relationship between the measured current and the Analog-to-Digital Conversion (ADC) count. The hardware design allows for over-ranging, with the maximum ADC count (4095 for a 12-bit ADC) corresponding to 1.0836 mA for the 0 - 1 mA range, and 22.7556 mA for the 0 - 10 mA, 0 - 20 mA and 4 - 20 mA ranges. The relay will therefore continue to measure and display values beyond the Maximum setting, within its numbering capability (-9999 to 9999).

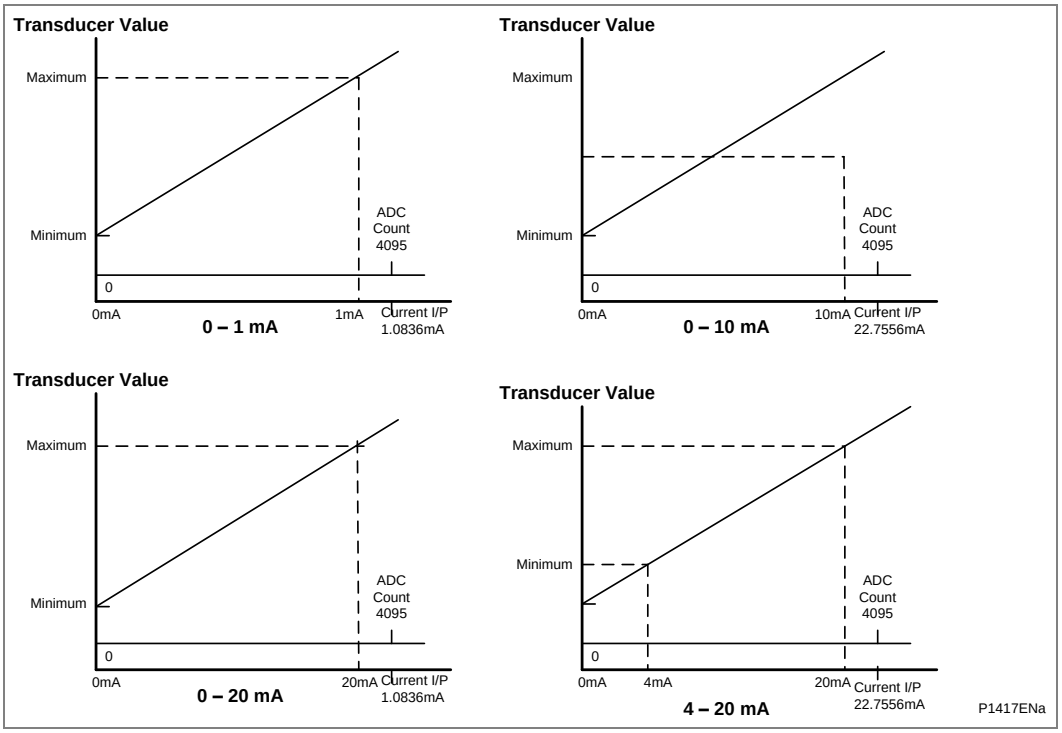


Figure 48 - Relationship between transducer value and current input range

Note	*If the Maximum is set less than the Minimum, the slopes of the graphs will be negative. This is because the mathematical relationship remains the same irrespective of how Maximum and Minimum are set, e.g., for 0 - 1 mA range, Maximum always corresponds to 1 mA and Minimum to 0 mA.*

Power-on diagnostics and continuous self-checking are provided for the hardware associated with the current loop inputs. When a failure is detected, the protection associated with all the current loop inputs is disabled and a single alarm signal (CL Card I/P Fail, DDB 470) is set and an alarm (CL Card I/P Fail) is raised. A maintenance record with an error code is also recorded with additional details about the type of failure.

For the 4 - 20 mA input range, a current level below 4 mA indicates that there is a fault with the transducer or the wiring. An instantaneous under current alarm element is available, with a setting range from 0 to 4 mA. This element controls an output signal (CLI1/2/3/4 I< Fail Alm., DDB 461- 464) which can be mapped to a user defined alarm if required.

Hysteresis is implemented for each protection element. For 'Over' protection, the drop-off/pick-up ratio is 95%, for 'Under' protection, the ratio is 105%.

A timer block input is available for each current loop input stage which will reset the CLI timers of the relevant stage if energized, (DDB 714-717).If a current loop input is blocked the protection and alarm timer stages and the 4 - 20 mA undercurrent alarm associated with that input are blocked. The blocking signals may be useful for blocking the current loop inputs when the CB is open for example.

DDB signals are available to indicate starting an operation of the alarm and trip stages of the each current loop inputs, (CLI1/2/3/4 Alarm Start: DDB 1614-1617, CLI1/2/3/4 Trip Start: DDB 1618-1621, CL Input 1/2/3/4 Alarm: DDB 457-460, CLI Input1/2/3/4 Trip: DDB 1199-1202). The state of the DDB signals can be programmed to be viewed in the **Monitor Bit x** cells of the **COMMISSION TESTS** column in the relay.

The current loop input starts are mapped internally to the ANY START DDB signal – DDB 1312.

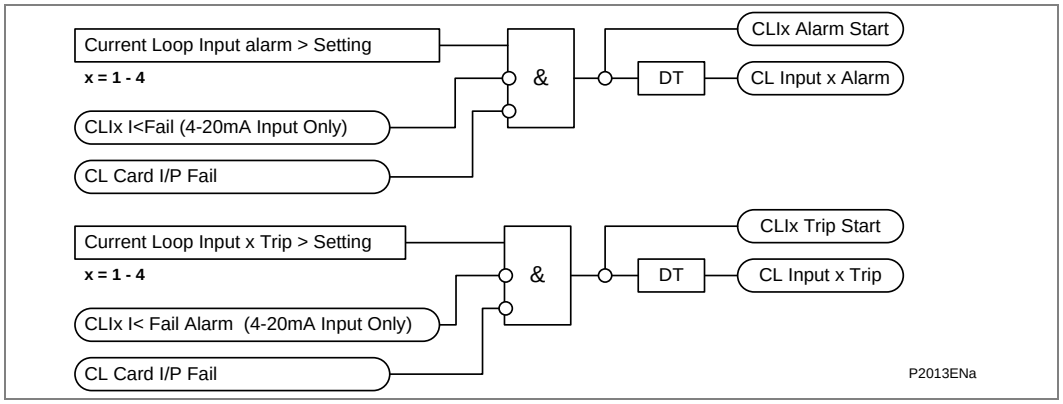


Figure 49 - Current loop input logic diagram

2.21.2 Current Loop Output

Four analog current outputs are provided with ranges of 0 - 1 mA, 0 - 10 mA, 0 - 20 mA or 4 - 20 mA which can alleviate the need for separate transducers. These may be used to feed standard moving coil ammeters for analog indication of certain measured quantities or into a SCADA using an existing analog RTU.

The CLIO output conversion task runs every 50 ms and the refresh interval for the output measurements is nominally 50 ms. The exceptions are marked with an asterisk in the table of current loop output parameters below. Those exceptional measurements are updated once every second.

The user can set the measuring range for each analog output. The range limits are defined by the Maximum and Minimum settings.

This allows the user to "zoom in" and monitor a restricted range of the measurements with the desired resolution. For voltage, current and power quantities, these settings can be set in either primary or secondary quantities, depending on the **CLO1/2/3/4 Set Values** - **Primary/Secondary** setting associated with each current loop output.

The output current of each analog output is linearly scaled to its range limits, as defined by the Maximum and Minimum settings. The relationship is shown in the *Relationship between the current output and the relay measurement* diagram.

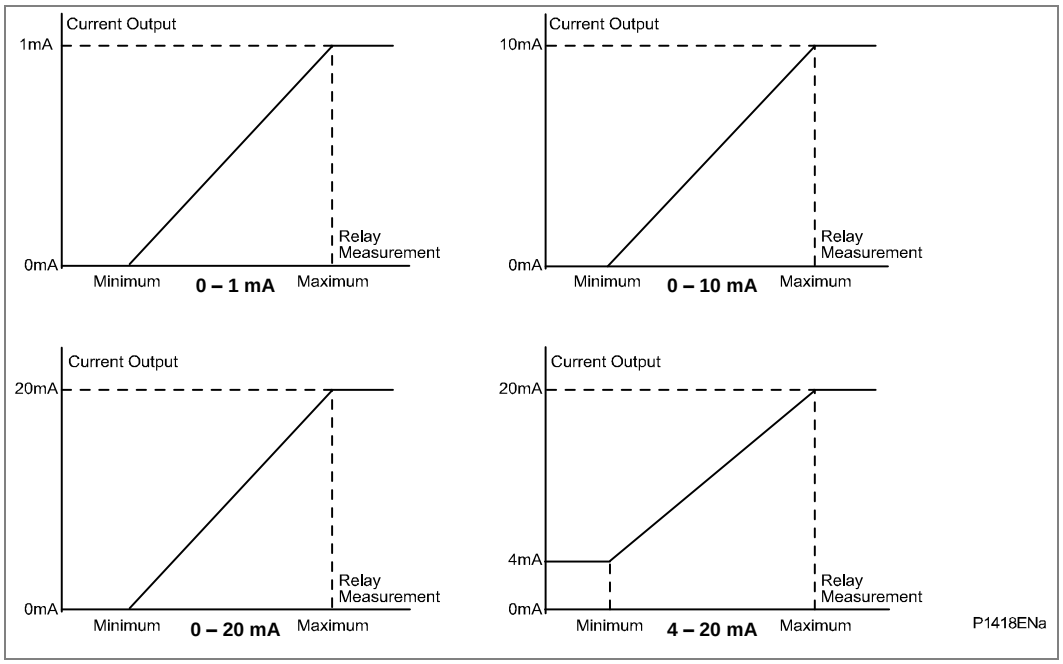


Figure 50 - Relationship between the current output and the relay measurement

Note	*If the Maximum is set less than the Minimum, the slopes of the graphs will be negative. This is because the mathematical relationship remains the same irrespective of how Maximum and Minimum are set, e.g., for 0 - 1 mA range, Maximum always corresponds to 1 mA and Minimum corresponds to 0 mA.*

The relay transducers are of the current output type. This means that the correct value of output will be maintained over the load range specified. The range of load resistance varies a great deal, depending on the design and the value of output current. Transducers with a full-scale output of 10mA will normally feed any load up to a value of 1000Ω (compliance voltage of 10V). This equates to a cable length of 15 km (approximately) for lightweight cable (1/0.6 mm cable). A screened cable earthed at one end only is recommended to reduce interference on the output current signal. The table below gives typical cable impedances/km for common cables. The compliance voltage dictates the maximum load that can be fed by a transducer output. Therefore, the 20mA output will be restricted to a maximum load of 500Ω approximately.

Cable	1/0.6 mm	1/0.85 mm	1/1.38 mm
CSA (mm^2)	0.28	0.57	1.50
R (Ω/km)	65.52	32.65	12.38

Table 21 - Cable sizes

The receiving equipment, whether it be a simple moving-coil (DC milliamp meter) instrument or a remote terminal unit forming part of a SCADA system, can be connected at any point in the output loop and additional equipment can be installed at a later date (provided the compliance voltage is not exceeded) without any need for adjustment of the transducer output.

Where the output current range is used for control purposes, it is sometimes worthwhile to fit appropriately rated diodes, or Zener diodes, across the terminals of each of the units in the series loop to guard against the possibility of their internal circuitry becoming open circuit. In this way, a faulty unit in the loop does not cause all the indications to disappear because the constant current nature of the transducer output simply raises the voltage and continues to force the correct output signal round the loop.

Power-on diagnostics and continuous self-checking are provided for the hardware associated with the current loop outputs. When failure is detected, all the current loop output functions are disabled and a single alarm signal (CL Card O/P Fail) is set and an alarm (CL Card O/P Fail) is raised. A maintenance record with an error code is also recorded with additional details about the type of failure.

Current loop output parameters are shown in this table:

Current loop output parameter	Abbreviation	Units	Range	Step	Default min.	Default Max.
Current Magnitude	IA-1 Magnitude IB-1 Magnitude IC-1 Magnitude IA-2 Magnitude IB-2 Magnitude IC-2 Magnitude IA-3 Magnitude IB-3 Magnitude IC-3 Magnitude IA-4 Magnitude IB-4 Magnitude IC-4 Magnitude IA-5 Magnitude IB-5 Magnitude IC-5 Magnitude IA HV Magnitude IB HV Magnitude IC HV Magnitude IA LV Magnitude IB LV Magnitude IC LV Magnitude IA TV Magnitude (P643/P645) IB TV Magnitude (P643/P645) IC TV Magnitude (P643/P645)	A	0 to 16 A	0.01 A	0 A	1.2 A
Current Magnitude	IN HV Measured Mag IN HV Derived Mag IN LV Measured Mag IN LV Derived Mag IN TV Measured Mag (P643/P645) IN TV Derived Mag (P643/P645)	A	0 to 16 A	0.01 A	0 A	1.2 A
Phase Sequence Current Components	I0-1 Magnitude I1-1 Magnitude I2-1 Magnitude I0-2 Magnitude I1-2 Magnitude I2-2 Magnitude I0-3 Magnitude (P643/P645) I1-3 Magnitude (P643/P645) I2-3 Magnitude (P643/P645) I0-4 Magnitude (P645) I1-4 Magnitude (P645) I2-4 Magnitude (P645) I0-5 Magnitude (P645) I1-5 Magnitude (P645) I2-5 Magnitude (P645)	A	0 to 16 A	0.01 A	0 A	1.2 A
P-P Voltage Magnitude	VAB Magnitude VBC Magnitude VCA Magnitude	V	0 to 200 V	0.1 V	0 V	140 V
P-N voltage Magnitude	VAN Magnitude (P643/P645) VBN Magnitude (P643/P645) VCN Magnitude (P643/P645)	V	0 to 200 V	0.1 V	0 V	80 V
Neutral Voltage Magnitude	VN Derived Mag. (P643/645)	V	0 to 200 V	0.1 V	0 V	80 V
P-P Voltage Magnitude	Vx Magnitude	V	0 to 200 V	0.1 V	0 V	80 V
Phase Sequence Voltage Components	V1 Magnitude V2 Magnitude V0 Magnitude	V	0 to 200 V	0.1 V	0 V	80 V
RMS Phase Voltages	VAN RMS (P643/P645) VBN RMS (P643/P645) VCN RMS (P643/P645)	V	0 to 200 V	0.1 V	0 V	80 V
Frequency	Frequency	Hz	0 to 70 Hz	0.01Hz	45 Hz	65 Hz
RTD Temperatures	RTD 1 through to RTD 10	°C	-40°C to 300°C	0.1°C	0°C	200°C
Current Loop Inputs	CL Input 1 through to CL input 4	-	-9999 to 9999	0.1	0	9999
Overflux element W1	Volts/Hz W1 (P643/P645)	V/Hz	0 to 20	0.01	0	4
	V/Hz W1 Thermal (P643/P645)	%	0 to 200	0.01	0	120
Overflux element W2	Volts/Hz W2	V/Hz	0 to 20	0.01	0	4
	V/Hz W2 Thermal	%	0 to 200	0.01	0	120
Hottest spot temperature	Hot Spot T	°C	-40 to 300	0.1	0	200
Top oil temperature	Top Oil T	°C	-40 to 300	0.1	0	200

Current loop output parameter	Abbreviation	Units	Range	Step	Default min.	Default Max.
Ambient temperature	Ambient T	°C	-40 to 300	0.1	0	200
Loss of life status	LOL Status	hr	1 to 300000	1	1	300000
Note 1 The measurements internal refresh rate is 50 ms.						
Note 2 These settings are for nominal 1 A and 100/120 V versions only. For other nominal versions they need to be multiplied accordingly.						

Table 22 - Current loop output parameters

2.22 Overfluxing Protection (V/f)

Magnetic flux in the transformer core is directly proportional to the voltage and inversely proportional to the frequency. The higher the V/f ratio, the greater the magnetizing current that would lead to heating and possible insulation failure. The overfluxing protection function detects an inadmissibly high flux level in the iron core of transformers as caused by a voltage increase or a frequency decrease, or both. The rise in V/f ratio does not require an immediate trip since this condition may be transient, and the normal condition should be restored within 1 to 2 minutes as a maximum.

The P64x relay provides two four stages overfluxing element. The overfluxing element Volts/Hz W1 gets the voltage signal from the three phase VT input. The overfluxing element Volts/Hz W2 acquires the voltage signal from the single-phase VT input. The protection measures the ratio of phase to phase voltage, (VAB), to frequency, V/Hz, and will operate when this ratio exceeds the setting. One stage can be set to operate with a definite time or inverse time delay (IDMT), this stage can be used to provide the protection trip output. There are also 3 other definite time stages which can be combined with the inverse time characteristic to create a combined multi-stage V/Hz trip operating characteristic using PSL. A blocking signal is provided for the V/Hz>1 stage 1 only, which has the inverse time characteristic option. The blocking signals are BLK W1 VPERHZ>1 (DDB 712) and BLK W2 VPERHZ>1 (DDB 713). This allows a definite time stage to override a section of the inverse time characteristic if required. The blocking signal has the effect of resetting the timer, the start signal and the trip signal.

There is also one definite time alarm stage that can be used to indicate unhealthy conditions before damage has occurred to the transformer.

The P642 has only one overflux element. On the other hand, the P643/P645 has two separate overflux elements for both HV side and LV side respectively.

Overfluxing is a thermal heating based function, therefore the reset timer starts whenever the flux level drops below pickup. The accumulated heat is linearly decreased from the present value down to zero over the course of the reset time. If after half the reset time, another overfluxing condition appears, the heating will restart from half of the previous accumulated level.

A reset command is provided so that the user can reset the element after injection testing. The reset command will reset all start, trip and alarm DDBs of V/Hz. Measurement related to overflux will also be reset. The overfluxing function can be reset by energizing the relevant DDB signal via the PSL (W1 Rest V/Hz: DDB 889, W2 Rest V/Hz: DDB 890).

The V/Hz>1 stages can be blocked by energizing the relevant DDB signals using the PSL (BLK W1 VPERHZ>1: DDB 712, BLK W2 VPERHZ>1: DDB 713). DDB signals are also available to indicate the start and trip of the protection, (Start: DDB 1599-1602, 1604-1607, Trip: DDB 1240-1247). A further DDB **W1 V/Hz> Alarm Start**, **W2 V/Hz> Alarm Start** signals are generated from the overfluxing alarm stage (DDB 1598, DDB 1603). The state of the DDB signals can be programmed to be viewed in the **Monitor Bit x** cells of the **COMMISSION TESTS** column in the relay.

The overfluxing protection starts are mapped internally to the ANY START DDB signal - DDB 1312.

The first trip stage can be set as an IDMT characteristic given as below:

$$t = \frac{TMS}{(M-1)^2}$$

Where:

M = $\frac{V/f}{(V/f\ Trip\ Setting)}$

V = Measured voltage

F = Measured frequency

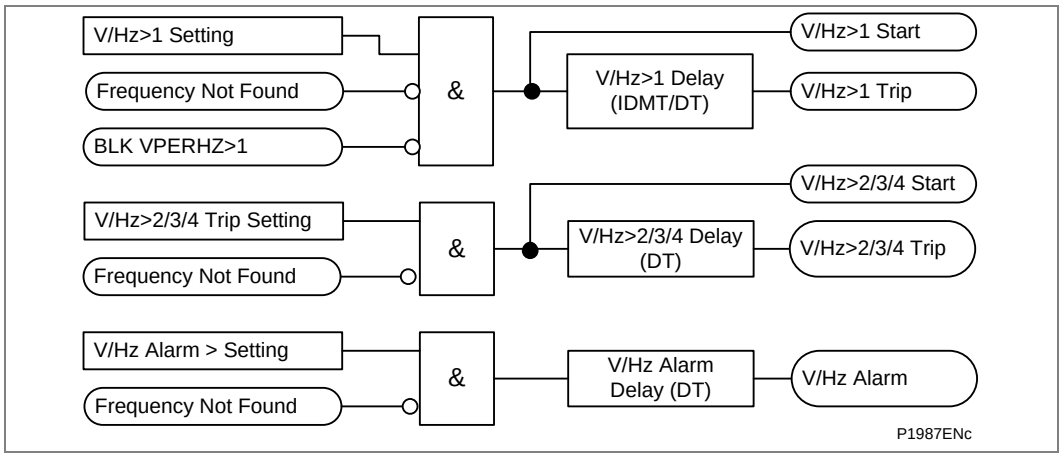


Figure 51 - Overfluxing logic diagram

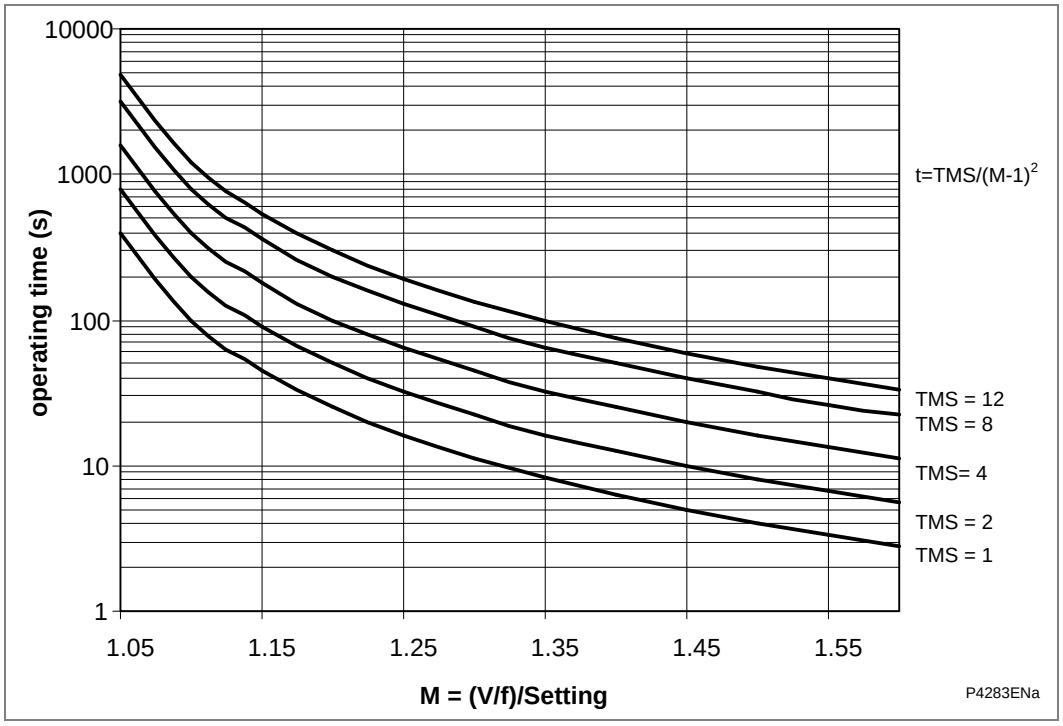


Figure 52 - IDMT overfluxing protection characteristic

The IDMT characteristic is implemented as a thermal function. The internal IDMT timer is treated as a thermal replica with a cooling characteristic. After a V/Hz excursion, the timer should reset according to the reset cooling characteristic. Otherwise, if the unit is subjected to another V/Hz excursion before it has cooled to normal condition, damage could occur before the V/Hz trip point is reached.

A linear reset curve with a Reset Time (V/Hz>x tReset) setting is used for this purpose. The actual reset time left is:

Reset time = tReset * IDMTtimer/tTarget

Where:

tTarget = $TMS/(M-1)^2$

The actual trip time delay is:

Trip delay = tTarget * (1-RESETtimer/tReset)

The following example explains the reset characteristic. It will take tReset time for the thermal replica to reset completely to zero after the thermal replica reaches 100% of V/f>1 Trip at stage 1. If the thermal replica has not reached 100% of V/f>1 Trip, the reset time will be reduced proportionally. For example, if the Reset Time setting is set to 100 s, and the thermal replica has only reached 50% of V/f>1 Trip when V/Hz resets, the reset time will be 50 s, as shown in Stage 2. If another V/Hz excursion appears before the first reset reaches V/f>1 Reset, the V/Hz time delay takes the reset time left into consideration, as shown in Stage 3.

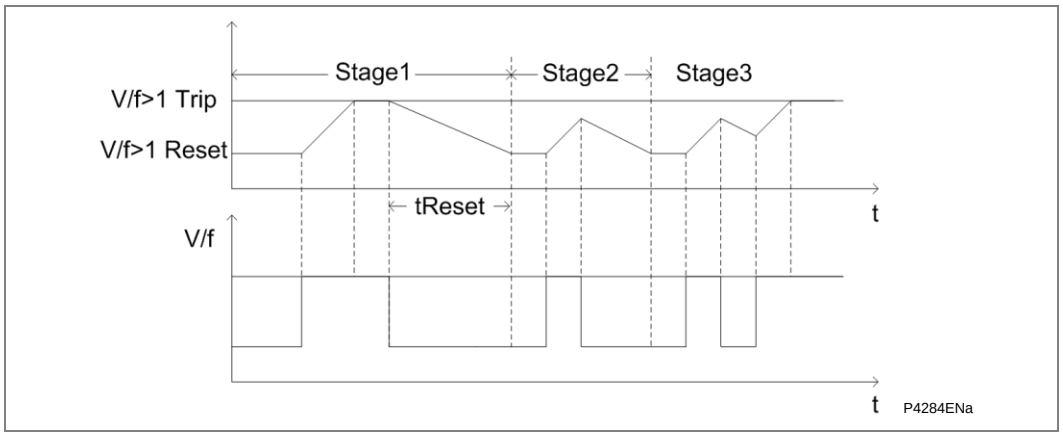


Figure 53 - Reset characteristic

3 OPERATION OF NON-PROTECTION FUNCTIONS

3.1 Current Transformer Supervision (CTS)

Current Transformer Supervision (CTS) is based on the measurement of the ratio of I2/I1 at all ends. When this ratio is not zero, one of these two conditions may be present:

- An unbalanced fault is present on the system - both I2 and I1 are non-zero
- There is a 1 or 2 phase CT problem - both I2 and I1 are non-zero

If the I2/I1 ratio is greater than the set value, CTS I2/I1>2, at all ends, it is almost certainly a genuine fault condition (CTS I2/I1>2 set above maximum unbalanced load and below the minimum unbalanced fault current). Therefore CTS will not operate. If this ratio is detected at one end only, one of the following conditions may be present:

- A CT problem
- A single end fed fault condition

I1 is used to confirm whether it is a CT problem or not. If I1 > CTS I1 is detected at all ends, it must be a CT problem and CTS is allowed to operate. If this condition (I1 > CTS I1) is detected at only one end, it is assumed that either an inrush condition or a single end fed internal fault is present. Therefore, the CTS operation is blocked.

The CTS status under the **CT SUPERVISION** sub-heading can be set either as indication or restraint. In indication mode, the CTS alarm time delay is automatically set to zero. If a CT failure is present, an alarm would be issued without delay, but the differential protection would remain unrestricted. Therefore, the risk of unwanted tripping under load current is present. In restraint mode, the differential protection is blocked for 20 ms after CT failure has been detected. Then the new setting Is-CTS is applied to the differential protection, as shown in the following diagram, the restraint region of the bias characteristic increases. The low impedance REF, earth fault and NPS overcurrent protections are internally blocked by CTS when a CT failure is detected in the CT used by each protection function. Earth fault protection is immune to CTS blocking if **IN> input** is set to **measured**.

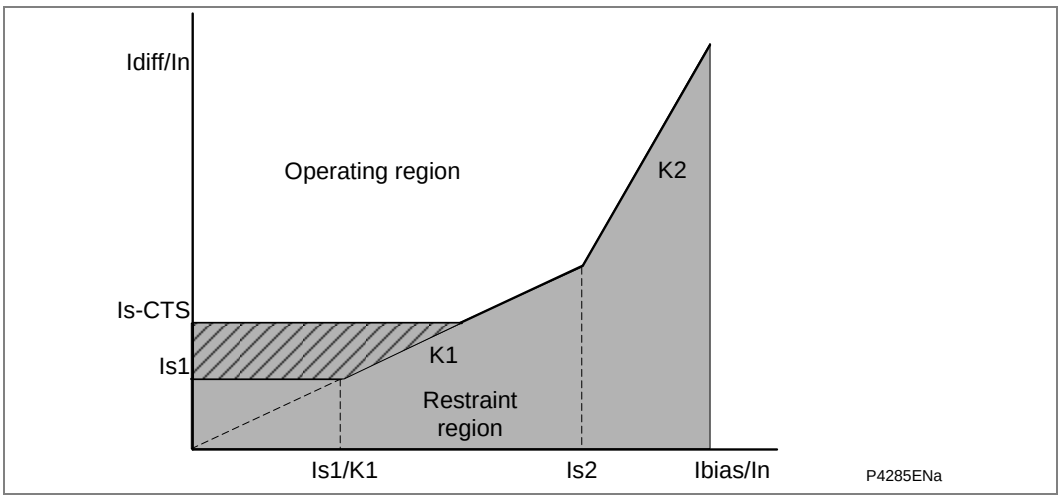


Figure 54 - CTS I1 setting applied to the differential protection

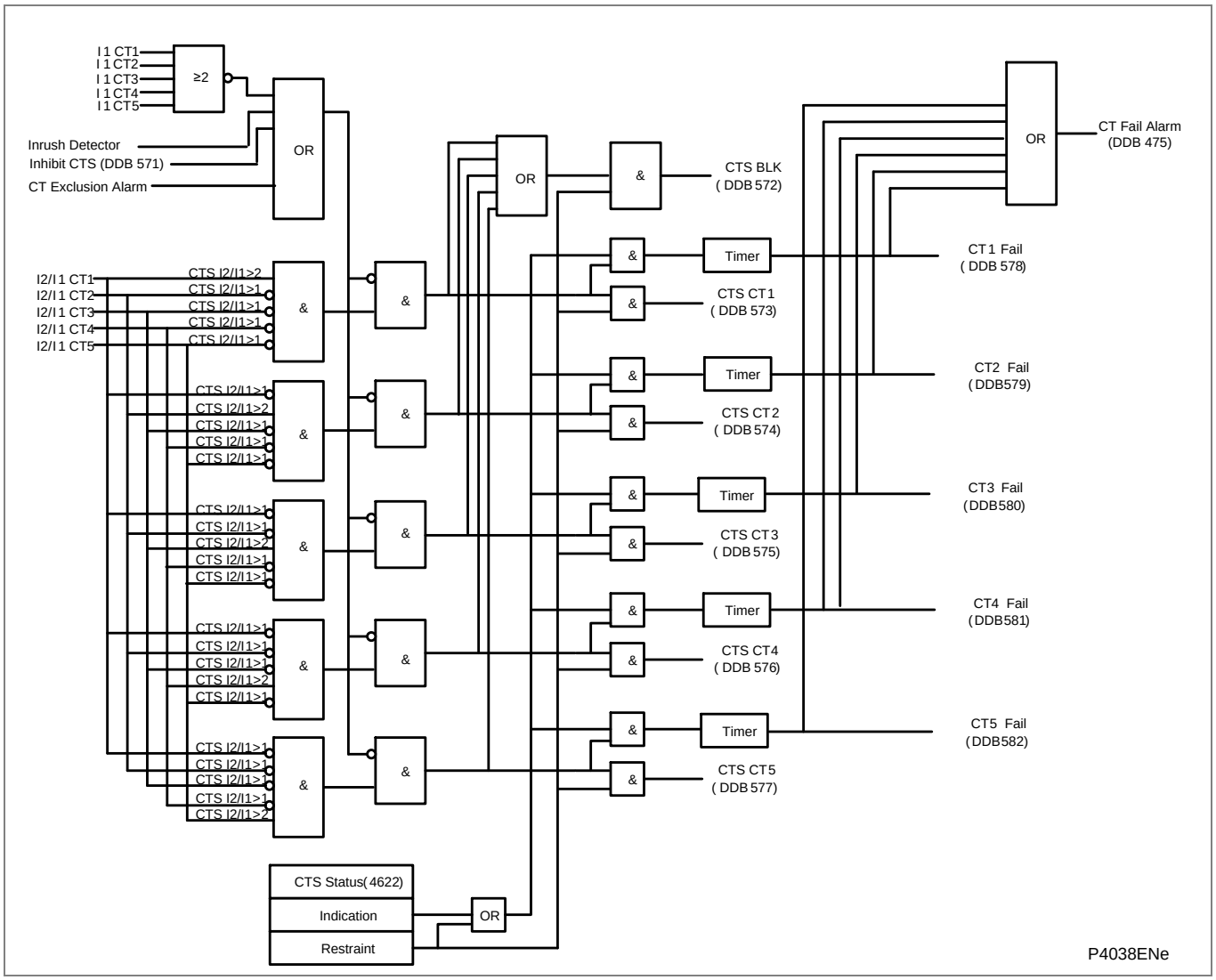


Figure 55 - Differential CTS logic diagram

The previous diagram shows that CTS monitors the positive and negative sequence currents of all ends (2 to 5, depending on the relay model). A faulty CT is determined if the following conditions are present at the same time:

- The positive sequence current in at least two current inputs exceeds the set release threshold I1 (**CTS I1** setting under the **SUPERVISION** menu). This also means that CTS can only operate if minimum load current of the protected object is present.
- On exactly one end a high set ratio of negative to positive sequence current, CTS I2/I1>2, is exceeded.
- On all other ends the ratio of negative to positive sequence current is less than a low set value, CTS I2/I1> 1, or no significant current is present (positive sequence current is below the release threshold I1)

Only a single or double-phase CT failure can be detected by this logic. The probability of symmetrical 3-phase CT failures is very low, therefore in practice this is not a significant problem.

3.2 Current Input Exclusion

It is possible to exclude current inputs from the protection functions in the P643 and P645. Any current input can be excluded as follows:

The appropriate DDB (DDB 737, 738, 739, 740 or 741) is asserted and the undercurrent condition is satisfied.

The DDB 736 is asserted and DDB 737, 738, 739, 740 or 741 is asserted.

When a current input is excluded, the relay sets to zero the current from that input, so that the protection functions considering the excluded current input detect zero current. On the other hand, the relay still measures the current that might be flowing through the excluded current input and compares it against the under current element threshold. The under current threshold is fixed to 0.05 In.

The inputs required are as follows:

Signal name	This signal should be asserted:
CT Exclusion enabled (DDB 736)	to exclude any of the CT inputs without considering the undercurrent elements.
T1 CT Exclusion enabled (DDB 737)	so that T1 CT may be excluded.
T2 CT Exclusion enabled (DDB 738)	so that T2 CT may be excluded.
T3 CT Exclusion enabled (DDB 739)	so that T3 CT may be excluded.
T4 CT Exclusion enabled (DDB 740)	so that T4 CT may be excluded.
T5 CT Exclusion enabled (DDB 741)	so that T5 CT may be excluded.

Table 23 – Inputs

The outputs are as follows:

Signal name	Description
T1 CT Excluded (DDB 704)	When this signal is asserted, T1 CT is excluded from every protection function.
T2 CT Excluded (DDB 705)	When this signal is asserted, T2 CT is excluded from every protection function.
T3 CT Excluded (DDB 706)	When this signal is asserted, T3 CT is excluded from every protection function.
T4 CT Excluded (DDB 707)	When this signal is asserted, T4 CT is excluded from every protection function.
T5 CT Excluded (DDB 708)	When this signal is asserted, T5 CT is excluded from every protection function.
CT exclusion-protection disabled (DDB 1723)	The status of the Tx CT excluded is stored in NVRAM. During the relay initialization after an auxiliary power supply failure, the stored state is compared with the present state. If there is a discrepancy, then this signal is asserted. When this DDB is asserted, all the protection functions using current signals are blocked.
Insufficient number of CTs (DDB 485)	This alarm is asserted when more than one current input is excluded from the P643 or when more than three current inputs are excluded from the P645.

Table 24 – Outputs

Only one current input can be excluded from the P643 and a maximum of three current inputs can be excluded from the P645. An alarm (DDB 485) is issued when more than the maximum number of current inputs is excluded. The status of DDBs 704, 705, 706, 707, and 708 is stored in NVRAM. An alarm (DDB 1723) is raised if the stored statuses do not match the statuses after the power supply is re-established. When DDB 1723 is asserted, the following functions are blocked: differential, REF, Overcurrent, negative phase sequence overcurrent, earth fault, thermal overload, through fault, circuit breaker failure, CT supervision and VT Supervision.

The following diagram shows the current input exclusion logic.

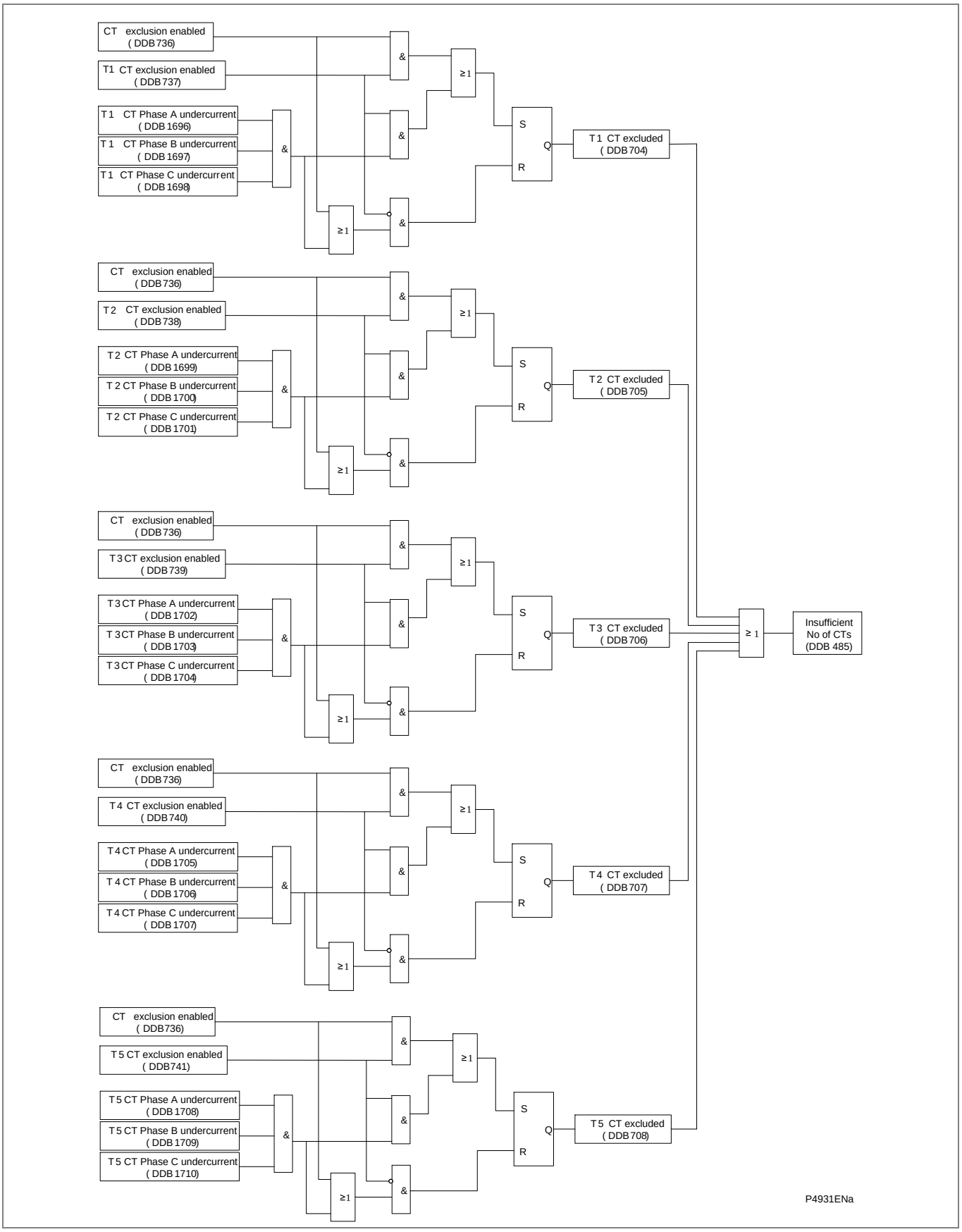


Figure 56 - Current input exclusion logic

3.3 Circuitry Fail Alarm

The circuitry fail alarm logic requires the following settings: **Is-cctfail>**, **K-cctfail** and **tIs-cctfail>**. If the differential current is bigger than **Is-cctfail>** setting and not trip is issued after the **tIs-cctfail>** time delay has elapsed, an alarm would be issued indicating a CT problem.

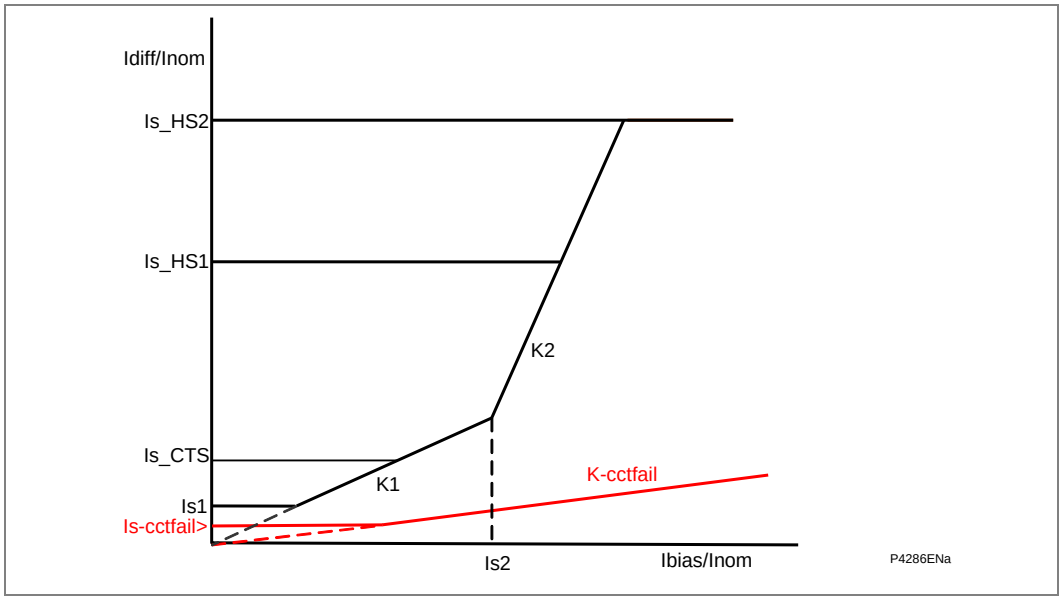


Figure 57 - Circuitry fail alarm fault characteristic

3.4 Voltage Transformer Supervision (VTS)

The Voltage Transformer Supervision (VTS) feature is used to detect failure of the ac voltage inputs to the relay. This may be caused by internal voltage transformer faults, overloading, or faults on the interconnecting wiring to relays. This usually results in one or more VT fuses blowing. Following a failure of the ac voltage input there would be a misrepresentation of the phase voltages on the power system, as measured by the relay, which may result in maloperation.

The VTS status may be set to disabled, blocking or indication. The VTS logic in the relay is designed to detect the voltage failure, and automatically adjust the configuration of protection elements whose stability would otherwise be compromised. A time-delayed alarm output is also available.

VTS can be declared by a Miniature Circuit Breaker (MCB) status input, or by an internal logic using relay measurement.

For the measured method, there are three main aspects to consider regarding the failure of the VT supply. These are defined below:

- Loss of one or two phase voltages
- Loss of all three phase voltages under load conditions
- Absence of three phase voltages upon line energization

The settings **VTS I>Inhibit** and **VTS I2>Inhibi**t are in pu values. The VTS logic considers the current associated to the winding where the VT is located.

- In a P642, the **VTS I>Inhibit** and **VTS I2>Inhibit** settings are always referred to CT1 or CT2 if the VT is located in the HV or LV windings respectively.
- In a P643, the **VTS I>Inhibit** and **VTS I2>Inhibit** settings are always referred to CT1, CT2 or CT3 if the VT is located in the HV, TV or LV windings respectively.
- In a P645, the **VTS I>Inhibit** and **VTS I2>Inhibit** settings are always referred to CT1, CT3 or CT5 if the VT is located in the HV, TV or LV windings respectively. In a P645, if the VT is in the HV winding, and the HV CT Terminals setting is 00011, then T1 CT and T2 CT are associated to the HV winding. The relay compares the HV current on a per-phase basis to the **VTS I>Inhibit** setting, and the HV negative sequence current to the **VTS I2>Inhibit** setting. In this case, the settings are always relative to T1 CT.

3.4.1 Loss of One or Two Phase Voltages

The VTS feature within the relay operates on detection of Negative Phase Sequence (NPS) voltage without the presence of negative phase sequence current. This gives operation for the loss of one or two-phase voltages. Stability of the VTS function is assured during system fault conditions, by the presence of NPS current. The use of negative sequence quantities ensures correct operation even where three-limb or ‘V’ connected VT’s are used.

Negative sequence VTS element:

- The negative sequence thresholds used by the element are V2 = 10 V (V2 drop off is 9.5 V) and I2 = 0.05 to 0.5In settable (defaulted to 0.05 In).

3.4.2 Loss of all Three Phase Voltages under Load Conditions

Under the loss of all three phase voltages to the relay, there will be no negative phase sequence quantities present to operate the VTS function. However, under such circumstances, a collapse of the three phase voltages will occur. If this is detected without a corresponding change in any of the phase current signals (which would be indicative of a fault), a VTS condition will be raised. In practice, the relay detects the presence of superimposed current signals, which are changes in the current applied to the relay. These signals are generated by comparison of the present value of the current with that exactly one cycle previously. Under normal load conditions, the value of superimposed current should therefore be zero. Under a fault condition a superimposed current signal will be generated which will prevent operation of the VTS.

The phase voltage level detectors are fixed and will drop off at 10V (40V on 380/440V relays) and pickup at 30V (120V on 380/440V relays).

The sensitivity of the superimposed current elements is fixed at 0.1 In.

3.4.3 Absence of Three Phase Voltages upon Line Energization

If a VT were inadvertently left isolated prior to line energization, incorrect operation of voltage dependent elements could result. The previous VTS element detected 3-phase VT failure by absence of all 3-phase voltages with no corresponding change in current. On line energization there will, however, be a change in current (as a result of load or line charging current for example). An alternative method of detecting 3-phase VT failure is therefore required on-line energization.

The absence of measured voltage on all three-phases on line energization can be due to:

- A three-phase VT failure
- A close-up 3-phase fault

The first condition would require blocking of the voltage dependent function and the second would require tripping.

To differentiate between these two conditions an overcurrent level detector (***VTS I> Inhibit***) is used which will prevent a VTS block from being issued if it operates. This element should be set in excess of any non-fault based currents on line energization (load, line charging current, transformer inrush current if applicable) but below the level of current produced by a close-up 3-phase fault. If the line is now closed where a 3-phase VT failure is present the overcurrent detector will not operate and a VTS block will be applied. Closing onto a 3-phase fault will result in operation of the overcurrent detector and prevent a VTS block being applied.

This logic will only be enabled during a live line condition (as indicated by the relays pole dead logic) to prevent operation under dead system conditions, where no voltage will be present and the **VTS I> Inhibit** overcurrent element will not be picked up.

Required to drive the VTS logic are a number of dedicated level detectors as follows:

- IA>, IB>, IC>, these level detectors operate in less than 20 ms and their settings should be greater than load current. This setting is specified as the VTS current threshold. These level detectors pick-up at 100% of setting and drop-off at 95% of setting.
- I2>, this level detector operates on negative sequence current and has a user setting. This level detector picks-up at 100% of setting and drops-off at 95% of setting.
- ΔIIA>, ΔIB>, ΔIC>, these level detectors operate on superimposed phase currents and have a fixed setting of 10% of nominal. These level detectors are subject to a count strategy such that 0.5 cycle of operate decisions must have occurred before operation.
- VA>, VB>, VC>, these level detectors operate on phase voltages and have a fixed setting, Pick-up level = 30 V (Vn = 100/120 V), 120V (Vn = 380/480 V), Drop Off level = 10V (Vn = 100/120 V), 40V (Vn = 380/480 V).
- VAB>, VBC>, these level detectors operate on phase-phase voltages and have a fixed setting, Pick-up level = 95 V (Vn = 100/120 V), Drop Off level = 70V (Vn = 100/120 V).
- V2>, this level detector operates on negative sequence voltage, it has a fixed setting of 10V/40 V depending on VT rating (100/120 or 380/480) with pick-up at 100% of setting and drop-off at 95% of setting.

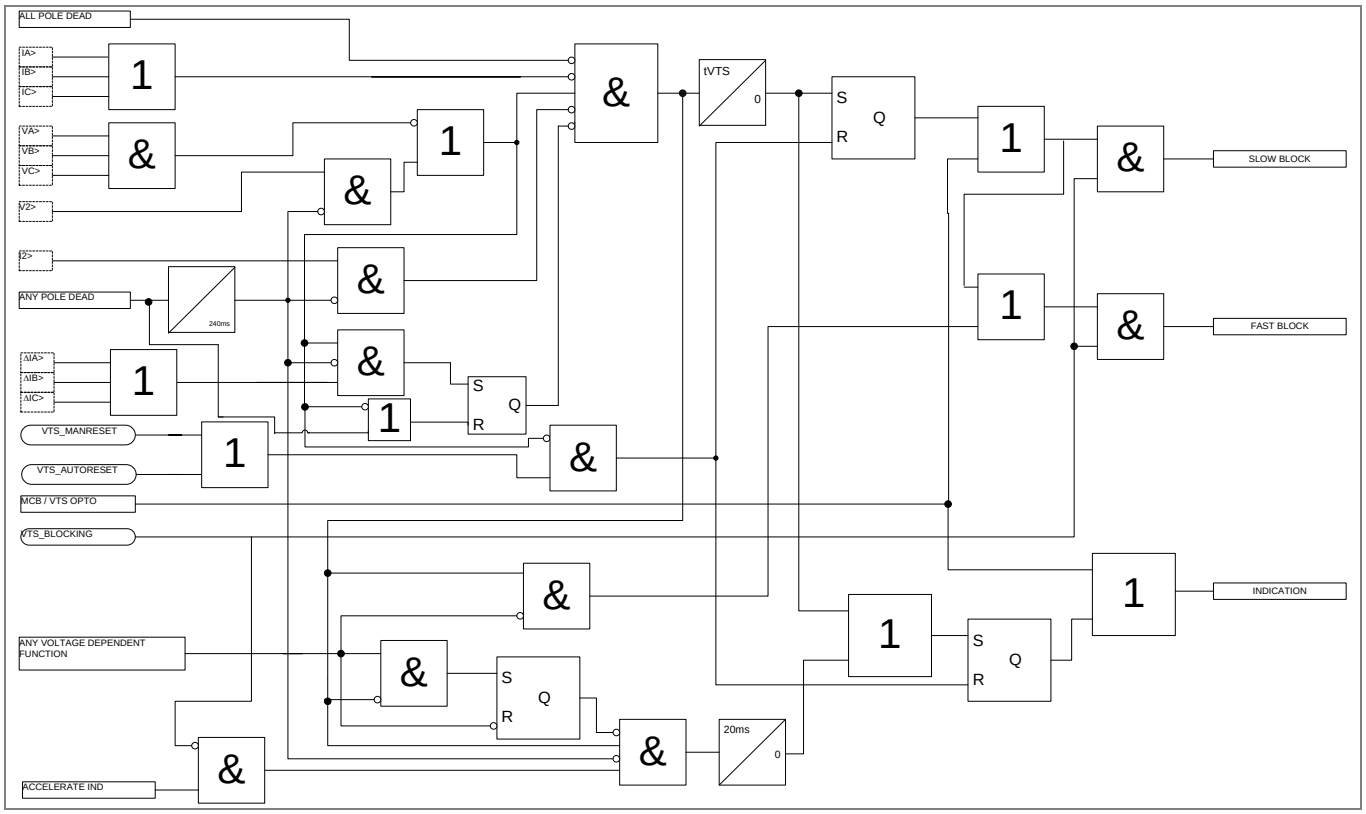


Figure 58 - VTS logic - P645 and P643

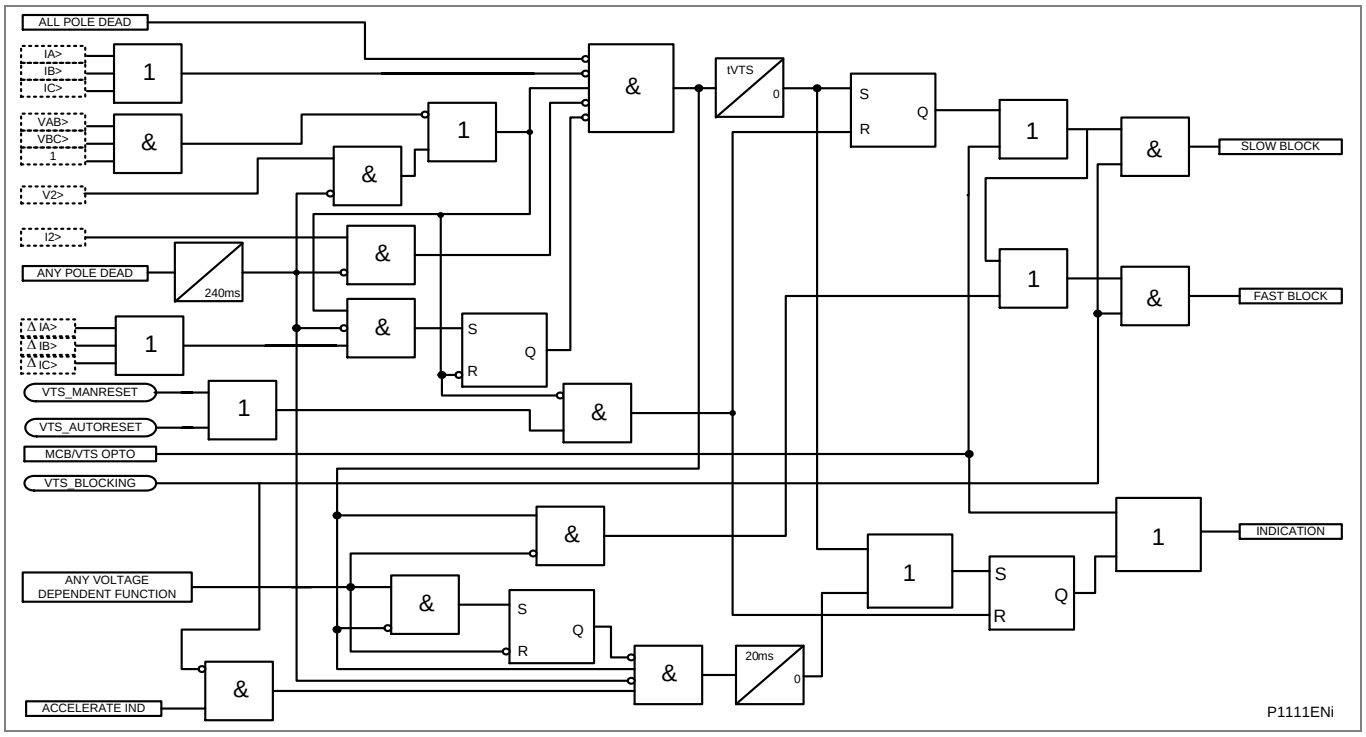


Figure 59 - VTS logic - P642

3.4.3.1 Inputs

Signal name	Description
IA>, IB>, IC>	Phase current levels (Fourier magnitudes)
I2>	I2 level (Fourier magnitude).
ΔIA, ΔIB, ΔIC	Phase current samples (current and one cycle previous)
VA>, VB>, VC>	Phase voltage signals (Fourier magnitudes)
V2>	Negative sequence voltage (Fourier magnitude)
ALL POLE DEAD (DDB 1772)	Breaker is open for all phases (driven from auxiliary contact or pole dead logic).
VTS_MANRESET	A VTS reset performed via front panel or remotely.
VTS_AUTORESET	A setting to allow the VTS to automatically reset after this delay.
MCB/VTS OPTO (DDB 874)	To remotely initiate the VTS blocking using an opto
Any Voltage Dependent Function (DDB 1739)	Output from any function that uses the system voltage, if any of these functions operate before a VTS is detected; the VTS is blocked from operation. The outputs include starts and trips. It is a hidden DDB not available for customer use.
Accelerate Ind (DDB 1738)	Signal from a fast tripping voltage dependent function used to accelerate indications when the indicate only option is selected. It is a hidden DDB not available for customer use.
Any Pole Dead (DDB 1773)	Breaker is open on one or more than one phases (driven from auxiliary contact or pole dead logic)
tVTS	The VTS timer setting for latched operation

Table 25 - Inputs

3.4.3.2 Outputs

Signal name	Description
VTS Fast Block (DDB1 800)	Used to block voltage dependent functions
VTS Slow Block (DDB 1801)	Used to block the Any Pole dead signal

Table 26 - Outputs

3.4.4 Operation

The relay may respond as follows to an operation of any VTS element:

- VTS set to provide alarm indication only (DDB 477 VT Fail Alarm);
- Optional blocking of voltage dependent protection elements (DDB 1800 VTS Fast Block, DDB 1801 VTS Slow Block);
- Optional conversion of directional overcurrent directional earth fault and directional NPS overcurrent elements to non-directional protection (available when set to blocking mode only). These settings are found in the function links cell of the relevant protection element columns in the menu.

Time delayed protection elements (Directional NPS Overcurrent) are blocked after the VTS Time Delay on operation of the VTS Slow Block. Fast operating protection elements (Directional overcurrent, Neutral Voltage Displacement, Undervoltage) are blocked on operation of the VTS Fast Block.

Note	*The neutral voltage displacement protection is only blocked by VTS if the neutral voltage input is set to Derived and not Measured.*

Other protections can be selectively blocked by customizing the PSL, integrating DDB 1800 VTS Fast Block and DDB 1801 VTS Slow Block with the protection function logic.

The VTS I> Inhibit or VTS I2> Inhibit elements are used to override a VTS block in event of a fault occurring on the system which could trigger the VTS logic. Once the VTS block has been established, however, then it would be undesirable for subsequent system faults to override the block. The VTS block will therefore be latched after a user settable time delay **VTS Time Delay**. Once the signal has latched then two methods of resetting are available. The first is manually using the front panel interface (or remote communications) provided the VTS condition has been removed and secondly, when in 'Auto' mode, by the restoration of the three-phase voltages above the phase level detector settings mentioned previously.

A VTS indication will be given after the VTS Time Delay has expired. In the case where the VTS is set to indicate only the relay may potentially mal-operate, depending on which protection elements are enabled. In this case the VTS indication will be given before the VTS time delay expires if a trip signal is given.

Where a Miniature Circuit Breaker (MCB) is used to protect the voltage transformer ac output circuits, it is common to use MCB auxiliary contacts to indicate a 3-phase output disconnection. As previously described, it is possible for the VTS logic to operate correctly without this input. However, this facility has been provided for compatibility with various utilities current practices. Energizing an opto-isolated input assigned to **DDB 362 MCB/VTS** or **MCB Open** on the relay will therefore provide the necessary block.

Where directional overcurrent elements are converted to non-directional protection on VTS operation, it must be ensured that the current pick-up setting of these elements is higher than full load current.

3.5 Pole Dead Logic

The pole dead logic in the P642 requires two single-phase VT inputs. It requires the three phase VT input in the P643 and P645. VAB and VBC are considered in P642 and in P643/P645 VAN, VBN and VCN are considered.

The pole dead logic is only available for the winding where the three-phase VT or two single phase VTs are located. This logic is used by the relay to determine when the circuit breaker poles are open (“pole dead”). This indication may be forced, using status indication from CB auxiliary contacts (52a or 52b), or internally determined by the relay. 52b contacts need to be inverted in the PSL because only the CB closed DDB signal is available for each breaker.

The relay will also initiate a pole dead condition if the following conditions are asserted:

- 3PH_CB_OPEN signal low
- Slow Block VTS signal low
- The line current and voltage fall below a preset threshold

This is necessary so that a pole dead indication is still given even when an upstream breaker is opened. The undervoltage (V<) and undercurrent (I<) thresholds have the following, fixed, pick-up and drop-off levels:

- VA<, VB<, VC<, these level detectors operate on phase voltages and have a fixed setting, Pick-up level = 10 V (Vn = 100/120 V), 40V (Vn = 380/480 V), Drop Off level = 30V (Vn = 100/120 V), 120V (Vn = 380/480 V).
- VAB<, VBC<, these level detectors operate on phase-phase voltages and have a fixed setting, Pick-up level = 70 V (Vn = 100/120 V), Drop Off level = 95V (Vn = 100/120 V).
- IA<, IB<, IC<, these level operate on phase currents and have a fixed setting, Pick-up level = 0.05 In, Drop Off level = 0.055 In.

Note	*If the VT is connected at the busbar side, auxiliary contacts (52a or 52b) must be connected to the relay for a correct pole dead indication. The logic diagrams below show the details:*

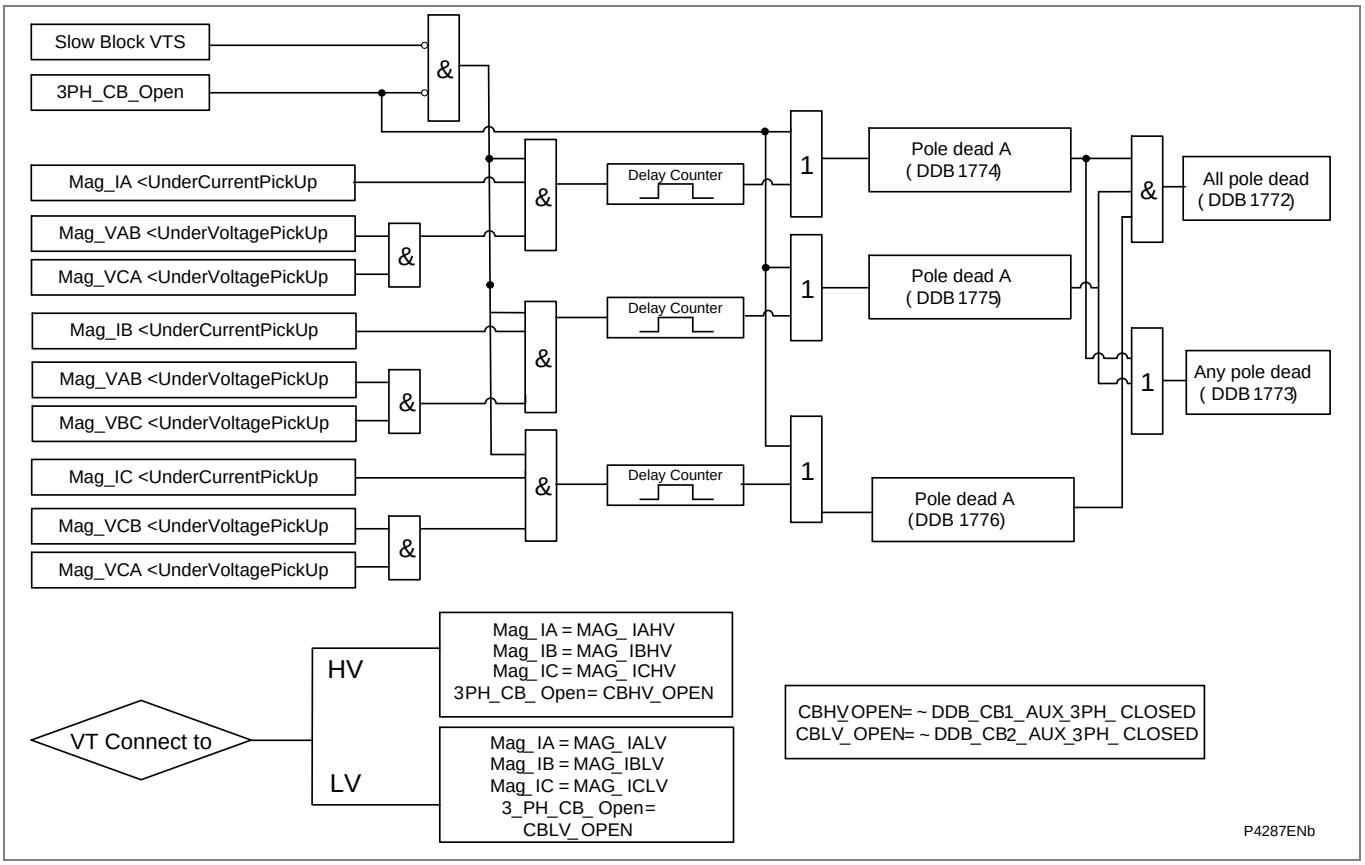


Figure 60 - P642 Pole dead logic

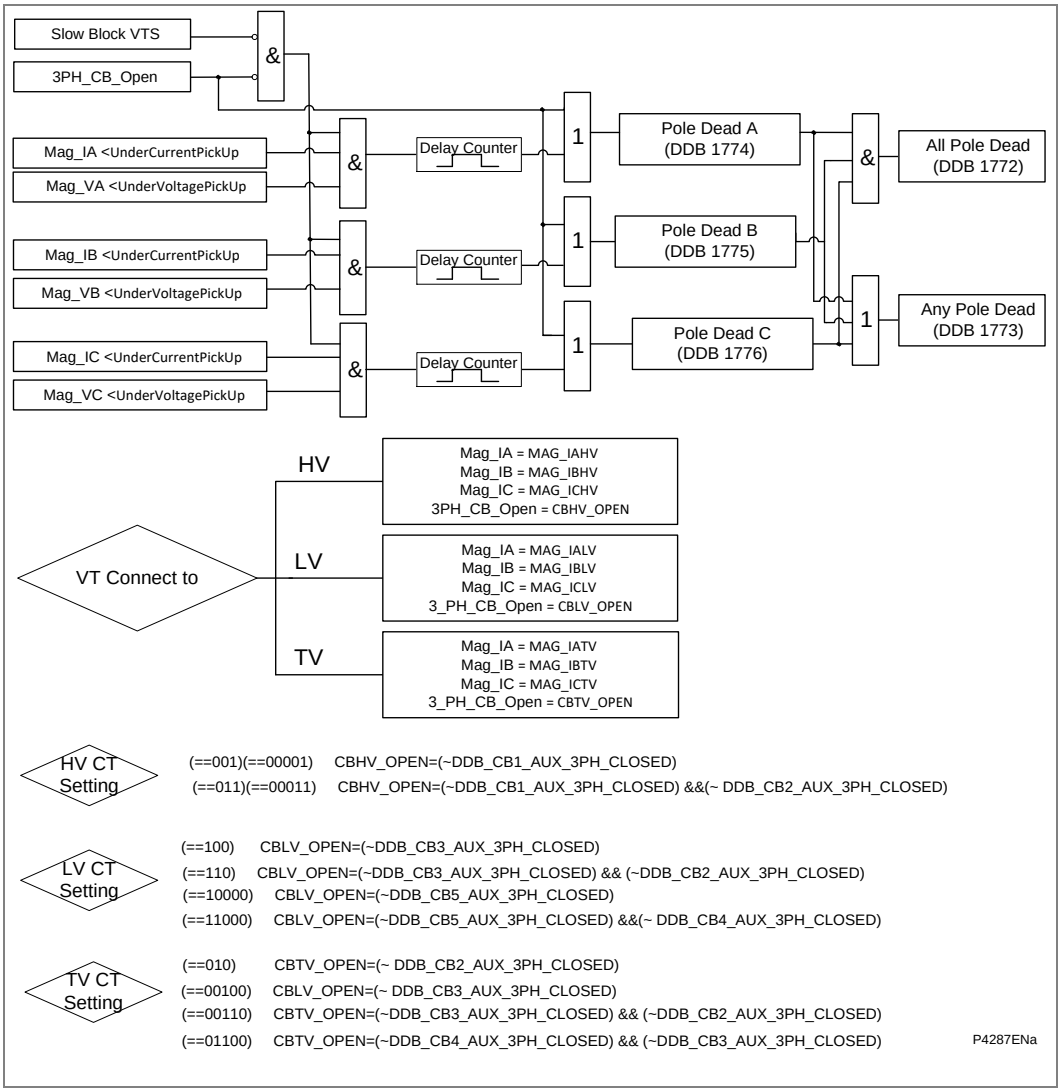


Figure 61 - P643/P645 Pole dead logic

If one or more poles are dead, the relay will indicate which phase is dead and will also assert the ANY POLE DEAD DDB signal (DDB 1773). If all phases were dead the ANY POLE DEAD signal would be accompanied by the ALL POLE DEAD DDB signal (DDB 1772).

If the VT fails a signal is taken from the VTS logic (DDB 1801 - Slow Block) to block the pole dead indications that would be generated by the undervoltage and undercurrent thresholds. However, the VTS logic will not block the pole dead indications if they are initiated by a CB Open signal.

Note	*When no auxiliary contacts are available, the 3PH_CB_OPEN signal must be forced low to avoid a wrong indication of a pole dead condition.*

The 3PH_CB_Open signal is the output of an AND gate. The inputs of this AND gate are the statuses of the breakers associated with the winding where the pole dead logic is available. When no auxiliary contacts are available, the 3PH_CB_Open signal shown in the pole dead logic diagram must be forced low, so that valid all pole dead (DDB 1772) and any pole dead (DDB 1773) conditions are given. In the programmable scheme logic, the relay only has CB closed signals (DDBs 719, 721, 723, 725, 727). If there are no auxiliary breaker contacts, the CB closed signals should be forced high, so that the 3PH_CB_Open signal is low. If the 3PH_CB_Open signal is low, and the VTS Slow Block (DDB 1801) is also low, the relay checks on the currents and voltages to detect an all pole or any pole dead condition.

The following diagram shows a way of forcing the CB closed signals high when there are no auxiliary contacts.

It is important to notice that in the absence of auxiliary breaker contacts, the CB close signals should be forced high. If not, the logic will assert the “all pole dead” and “any pole dead” signals when the winding may still be energized.

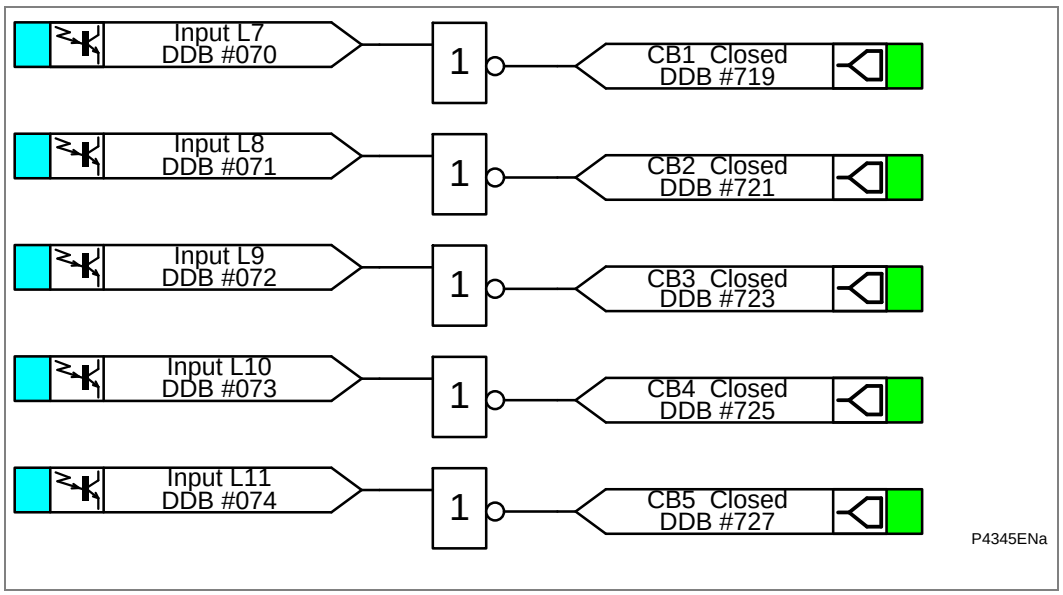


Figure 62 - P643/P645 Pole dead logic - CB closed signals

3.6 User Alarms

Thirty two user alarms are available, the first 16 are self-reset and the next 16 are manual reset. The user alarm labels can be set in the setting file and these labels are displayed in the PSL file as well.

3.7 Changing Setting Groups

The setting groups can be changed using 2 DDB signals or by a menu selection or by using the hotkey menu. In the **Configuration** column if **Setting Group - select via PSL** is selected, DDBs 885 (SG Select 1x) and 884 (SG Select x1), which are dedicated for setting group selection, can be used to select the setting group as shown in the table below. These DDB signals can be connected to opto inputs for local selection or control inputs for remote selection of the setting groups. If **Setting Group - select via menu** is selected, in the **Configuration** column the **Active Settings - Group1/2/3/4** can be used to select the setting group. The setting group can be changed using the hotkey menu providing that **Setting Group - select via menu** is chosen.

SG select 1x	SG select x1	Selected setting group
0	0	1
1	0	2
0	1	3
1	1	4

Table 27 - Setting Group select

Note	*Setting groups comprise both Settings and Programmable Scheme Logic (PSL). Each is independent per group - not shared as common. The settings are generated in the Settings and Records application in MiCOM S1 Studio, or can be applied directly from the relay front panel menu. The PSL can only be set using the PSL Editor application in MiCOM S1 Studio, generating files with extension ".psl".*

Warning **It is essential that where the installation needs application-specific PSL that the appropriate .psl file is downloaded (sent) to the relay, for each and every setting group that will be used. If the user fails to download the required .psl file to any setting group that may be brought into service, then factory default PSL will still be resident. THIS MAY HAVE SEVERE OPERATIONAL AND SAFETY CONSEQUENCES.**

3.8 Control Inputs

The control inputs function as software switches that can be set or reset either locally or remotely. These inputs can be used to trigger any function that they are connected to as part of the PSL. There are three setting columns associated with the control inputs that are: “CONTROL INPUTS”, “CTRL. I/P CONFIG.” and “CTRL. I/P LABELS”. The function of these columns is described below:

Menu Text	Default Setting	Setting Range	Step Size
CONTROL INPUTS			
Ctrl I/P Status	00000000000000000000000000000000		
Control Input 1	No Operation	No Operation, Set, Reset	
Control Input 2 to 32	No Operation	No Operation, Set, Reset	

Table 28 - Control inputs

The Control Input commands can be found in the ‘Control Input’ menu. In the ‘Ctrl. I/P status’ menu cell there is a 32 bit word which represent the 32 control input commands. The status of the 32 control inputs can be read from this 32-bit word. The 32 control inputs can also be set and reset from this cell by setting a 1 to set or 0 to reset a particular control input. Alternatively, each of the 32 Control Inputs can be set and reset using the individual menu setting cells ‘Control Input 1, 2, 3’ etc. The Control Inputs are available through the relay menu as described above and also via the rear communications.

In the programmable scheme logic editor 32 Control Input signals, DDB 1824 - 1855, which can be set to a logic 1 or On state, as described above, are available to perform control functions defined by the user.

The status of the Control Inputs configured as latched is stored in flash memory. Therefore, in the event that the auxiliary supply is interrupted, the status of the control inputs is recorded even if the battery is missing or discharged. Once the auxiliary supply is restored, the control input is set to the same status as before the auxiliary supplied failed.

Menu Text	Default Setting	Setting Range	Step Size
CTRL. I/P CONFIG.			
Hotkey Enabled	11111111111111111111111111111111		
Control Input 1	Latched	Latched, Pulsed	
Ctrl Command 1	SET/RESET	SET/RESET, IN/OUT, ENABLED/DISABLED, ON/OFF	
Control Input 2 to 32	Latched	Latched, Pulsed	
Ctrl Command 2 to 32	SET/RESET	SET/RESET, IN/OUT, ENABLED/DISABLED, ON/OFF	
Menu Text	Default Setting	Setting Range	Step Size
CTRL. I/P LABELS			
Control Input 1	Control Input 1	16 character text	
Control Input 2 to 32	Control Input 2 to 32	16 character text	

Table 29 - Ctrl I/P Config

Menu Text	Default Setting	Setting Range	Step Size
CTRL. I/P LABELS			
Control Input 1	Control Input 1	16 character text	
Control Input 2 to 32	Control Input 2 to 32	16 character text	

Table 30 - Ctrl I/P labels

The **CTRL. I/P CONFIG.** column has several functions one of which allows the user to configure the control inputs as either **latched** or **pulsed**. A latched control input will remain in the set state until a reset command is given, either by the menu or the serial communications. A pulsed control input, however, will remain energized for 10ms after the set command is given and will then reset automatically (i.e. no reset command required).

In addition to the latched/pulsed option this column also allows the control inputs to be individually assigned to the **Hotkey** menu by setting **1** in the appropriate bit in the **Hotkey Enabled** cell. The hotkey menu allows the control inputs to be set, reset or pulsed without the need to enter the **CONTROL INPUTS** column. The **Ctrl. Command** cell also allows the SET/RESET text, displayed in the hotkey menu, to be changed to something more suitable for the application of an individual control input, such as **ON/OFF**, **IN/OUT** etc.

The **CTRL. I/P LABELS** column makes it possible to change the text associated with each individual control input. This text will be displayed when a control input is accessed by the hotkey menu, or it can be displayed in the PSL.

3.9 PSL DATA Column

The relay contains a PSL DATA column that can be used to track PSL modifications. A total of 12 cells are contained in the PSL DATA column, 3 for each setting group. The function for each cell is shown below:

Grp PSL Ref	When downloading a PSL to the relay, the user will be prompted to enter which groups the PSL is for and a reference ID. The first 32 characters of the reference ID will be displayed in this cell. The ⟨ and ⟩ keys can be used to scroll through 32 characters as only 16 can be displayed at any one time.
18 Nov 2002 08:59:32.047	This cell displays the date and time when the PSL was down loaded to the relay.
Grp 1 PSL ID - 2062813232	This is a unique number for the PSL that has been entered. Any change in the PSL will result in a different number being displayed.

Note *The above cells are repeated for each setting group.*

3.10 Auto Reset of Trip LED Indication

The trip LED can be reset when the flags for the last fault are displayed. The flags are displayed automatically after a trip occurs, or can be selected in the fault record menu. The reset of trip LED and the fault records is performed by pressing the c key once the fault record has been read.

Setting **Sys Fn Links** in the **SYSTEM DATA** Column to logic **1** sets the trip LED to automatic reset. Resetting will occur when the circuit is reclosed and the **Any Pole Dead** signal (DDB 1773) has been reset for three seconds. Resetting, however, will be prevented if the **Any start** signal is active after the breaker closes.

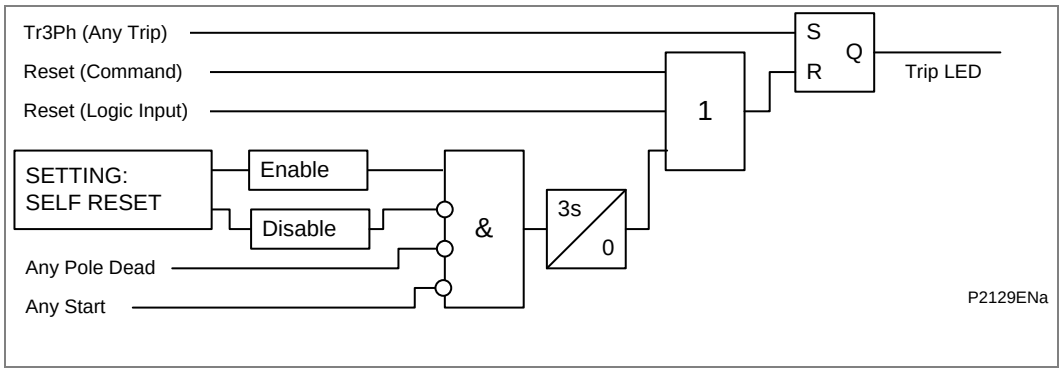


Figure 63 - Trip LED logic diagram

3.11 Reset of Programmable LEDs and Output Contacts

The programmable LEDs and output contacts can be set to be latched in the programmable scheme logic. If there is a fault record then clearing the fault record by pressing the ⓒ key once the fault record has been read will clear any latched LEDs and output contacts. If there is no fault record, then as long as the initiating signal to the LED or output contact is reset the LEDs and contacts can be reset by one of these methods.

- Using the View Records - Reset Indications menu command cell
- Using DDB 876 **Reset Relays/LED** which can be mapped to an Opto Input or a Control Input for example

3.12 Real Time Clock Synchronization via Opto-Inputs

In modern protective schemes it is often desirable to synchronize the relays real time clock so that events from different relays can be placed in chronological order. This can be done using the IRIG-B input, if fitted, or via the communication interface connected to the substation control system. In addition to these methods the P64x range offers the facility to synchronize using an opto-input by routing it in PSL to DDB 881 (Time Sync.). Pulsing this input will result in the real-time clock snapping to the nearest minute if the pulse input is ±3 s of the relay clock time. If the real-time clock is within 3 s of the pulse the relay clock will crawl (the clock will slow down or get faster over a short period) to the correct time. The recommended pulse duration is 20 ms to be repeated no more than once per minute. An example of the time sync. function is shown below:

Time of “Sync. Pulse”	Corrected time
19:47:00 to 19:47:29	19:47:00 This assumes a time format of hh:mm:ss
19:47:30 to 19:47:59	19:48:00

Note	*The above assumes a time format of hh:mm:ss*

Table 31 - Time Sync function

To avoid the event buffer from being filled with unnecessary time sync. events, it is possible to ignore any event that generated by the time sync. opto input. This can be done by applying the following settings:

Menu text	Value
RECORD CONTROL	
Opto Input Event	Enabled
Protection Event	Enabled
DDB 064 - 079 (Opto Inputs)	Set “Time Sync.” associated opto to 0

Table 32 - Record control

To improve the recognition time of the time sync. opto input by approximately 10 ms, the opto input filtering could be disabled. This is achieved by setting the appropriate bit to 0 in the **Opto Filter Cntl** cell in the **OPTO CONFIG** column.

Disabling the filtering may make the opto input more susceptible to induced noise. Fortunately the effects of induced noise can be minimized by using the methods described in the *Product Design* chapter.

3.13 Function Keys

The relay offers users 10 function keys for programming any operator control functionality via PSL. Each function key has an associated programmable tri-colour LED that can be programmed to give the desired indication on function key activation.

These function keys can be used to trigger any function that they are connected to as part of the PSL. The function key commands can be found in the 'Function Keys' menu (see the Settings chapter). In the 'Fn. Key Status' menu cell there is a 10-bit word which represent the 10 function key commands and their status can be read from this 10-bit word.

In the programmable scheme logic editor 10 function key signals, which can be set to a logic 1 or On state, as described above, are available to perform control functions defined by the user.

The "Function Keys" column has 'Fn. Key n Mode' cell which allows the user to configure the function key as either 'Toggled' or 'Normal'. In the 'Toggle' mode the function key DDB signal output will remain in the set state until a reset command is given, by activating the function key on the next key press. In the 'Normal' mode, the function key DDB signal will remain energized for as long as the function key is pressed and will then reset automatically.

A minimum pulse duration can be programmed for a function key by adding a minimum pulse timer to the function key DDB output signal.

The "Fn. Key n Status" cell is used to enable/unlock or disable the function key signals in PSL. The 'Lock' setting has been specifically provided to allow the locking of a function key thus preventing further activation of the key on consequent key presses. This allows function keys that are set to 'Toggled' mode and their DDB signal active 'high', to be locked in their active state thus preventing any further key presses from deactivating the associated function. Locking a function key that is set to the "Normal" mode causes the associated DDB signals to be permanently off. This safety feature prevents any inadvertent function key presses from activating or deactivating critical relay functions.

The "Fn. Key Labels" cell makes it possible to change the text associated with each individual function key. This text will be displayed when a function key is accessed in the function key menu, or it can be displayed in the PSL.

The status of the function keys is stored in battery backed memory. In the event that the auxiliary supply is interrupted the status of all the function keys will be recorded. Following the restoration of the auxiliary supply the status of the function keys, prior to supply failure, will be reinstated. If the battery is missing or flat the function key DDB signals will set to logic 0 once the auxiliary supply is restored.

Note	*The relay will only recognize a single function key press at a time and that a minimum key press duration of approximately 200msec. is required before the key press is recognized in PSL. This deglitching feature avoids accidental double presses.*

Notes:

APPLICATION NOTES

CHAPTER 6

Date:	07/2018
Products covered by this chapter:	This chapter covers the specific versions of the MiCOM products listed below. This includes ***only*** the following combinations of Software Version and Hardware Suffix.
Hardware Suffix:	L (P642) M (P643/P645)
Software Version:	B4 - P64x (P642, P643 & P645)
Connection Diagrams:	10P642xx (xx = 01 to 10) 10P643xx (xx = 01 to 06) 10P645xx (xx = 01 to 09)

CONTENTS

FIGURES

TABLES

Notes:

1 INTRODUCTION

1.1 Transformer Protection

1.1.1 Introduction

The development of modern power systems has been reflected in the advances in transformer design. This has resulted in a wide range of transformers with power rating from a few kVA to several hundred MVA being available for use in a wide variety of applications.

The considerations for transformer protection vary with the application and importance of the transformer. To reduce the effects of thermal stress and electrodynamic forces, the overall protection should minimize the time that a fault is present within a transformer.

On smaller distribution transformers, effective and economically justifiable protection can be achieved by using either fuse protection or IDMT/instantaneous overcurrent relays. Due to the requirements of co-ordination with the downstream power system protection, this results in time-delayed fault clearance for some low-level faults. Time delayed clearance of major faults is unacceptable on larger distribution, transmission and generator transformers, where the effects on system operation and stability must be considered. High speed protection is desirable for all faults.

Transformer faults are generally classified into these categories:

- Winding and terminal faults
- Core faults
- Abnormal operating conditions such as overvoltage, overfluxing and overload
- Sustained or uncleared external faults

All of the above conditions must be considered individually and the transformer protection designed accordingly.

To provide effective protection for faults within a transformer and security for normal operation and external faults, the design and application of transformer protection must consider factors such as:

- Magnetizing inrush current
- Winding arrangements
- Winding connections
- Connection of protection secondary circuits

The way that the protection of larger transformers is typically achieved is best illustrated by examining the protective devices associated with common applications.

1.1.2 Transformer Connections

There are several possible transformer connections but the more common connections are divided into the main groups shown in the following table:

Group	Phase displacement	Transformer connections
Group 1	0° Phase displacement	Yy0 or Dz0 or Dd0
Group 2	180° Phase displacement	Yy6 or Dd6 or Dz6
Group 3	30° lag Phase displacement	Dy1 or Yz1 or Yd1
Group 4	30° lead Phase displacement	Yd11 or Dy11 or Yz11

Table 1 - Four main transformer connection groups

High voltage windings use capital letters and low voltage windings by lower-case letters (reference to high and low is relative). The numbers refer to positions on a clock face and indicate the phase displacement of the low voltage phase to neutral vector with respect to the high voltage phase to neutral vector. For example, Yd1 indicates that the low voltage phase vectors lag the high voltage phase vectors by 30° (-30° phase shift).

Determining transformer connections is best shown with a particular example. These points should be noted:

- The line connections are normally made to the end of the winding which carries the subscript 2, such as: A_2, B_2, C_2 and a_2, b_2, c_2.
- The line terminal designation (both letter and subscript) are the same as those of the phase winding to which the line terminal is connected.

Consider the Yd1 connection. The transformer windings shown in the following diagram should be connected in Yd1 configuration.

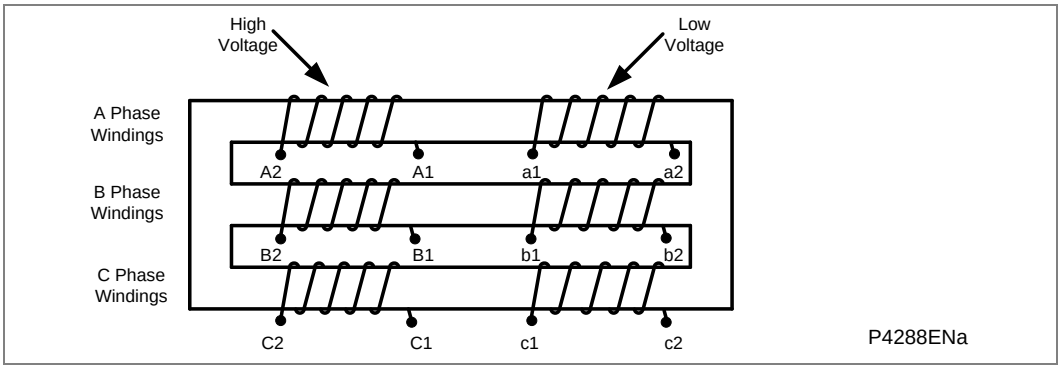


Figure 1 - Transformer windings to be connected in Yd1 configuration

Follow these steps to connect the transformer windings:

1. Draw the primary and secondary phase to neutral vectors showing the required phase displacement.

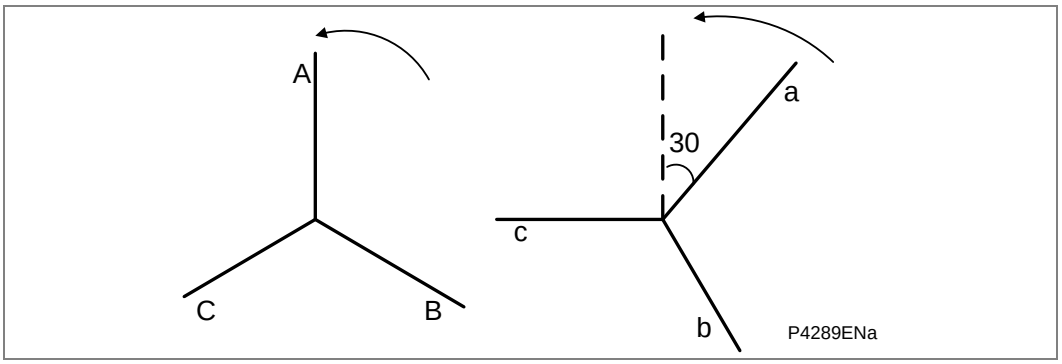


Figure 2 - Phase-neutral voltage vectors

1. Complete the delta winding connection on the secondary side and indicate the respective vector directions. Magnetically coupled windings are drawn in parallel, winding “A” in the star side is parallel to winding “a” in the delta side. The same applies for the other two phases.

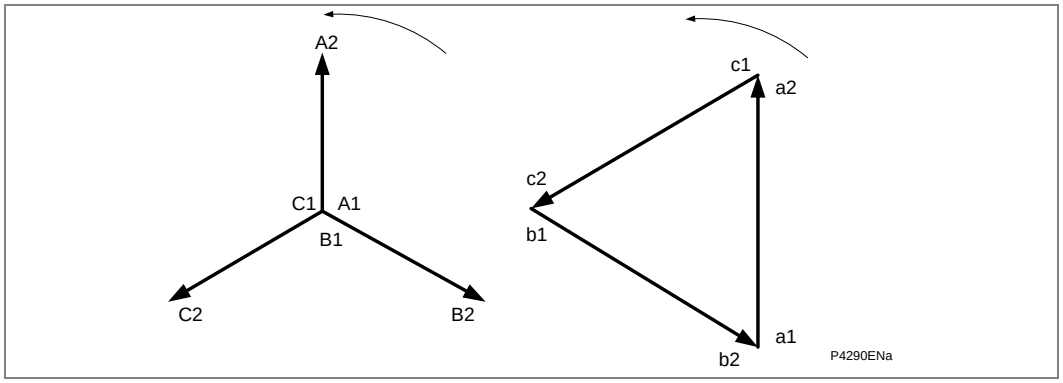


Figure 3 - Draw the delta

1. It is now possible to indicate the winding subscript numbers bearing in mind that if the direction of induced voltage in the high voltage winding at a given instant is from A1 to A2 (or vice versa) then the direction of the induced voltage in the low voltage winding at the same instant will also be from a1 to a2.
1. The delta connection should be made by connecting a2 to c1, b2 to a1 and c2 to b1:

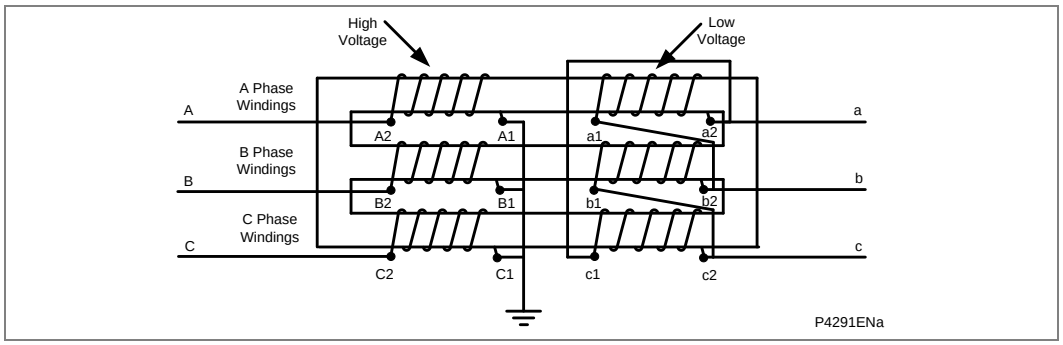


Figure 4 - Yd1 transformer configuration

1.1.3 Overview of Existing Practices

The “Typical transformer protection package” diagram shows typical protection functions for a sub-transmission or large distribution transformer.

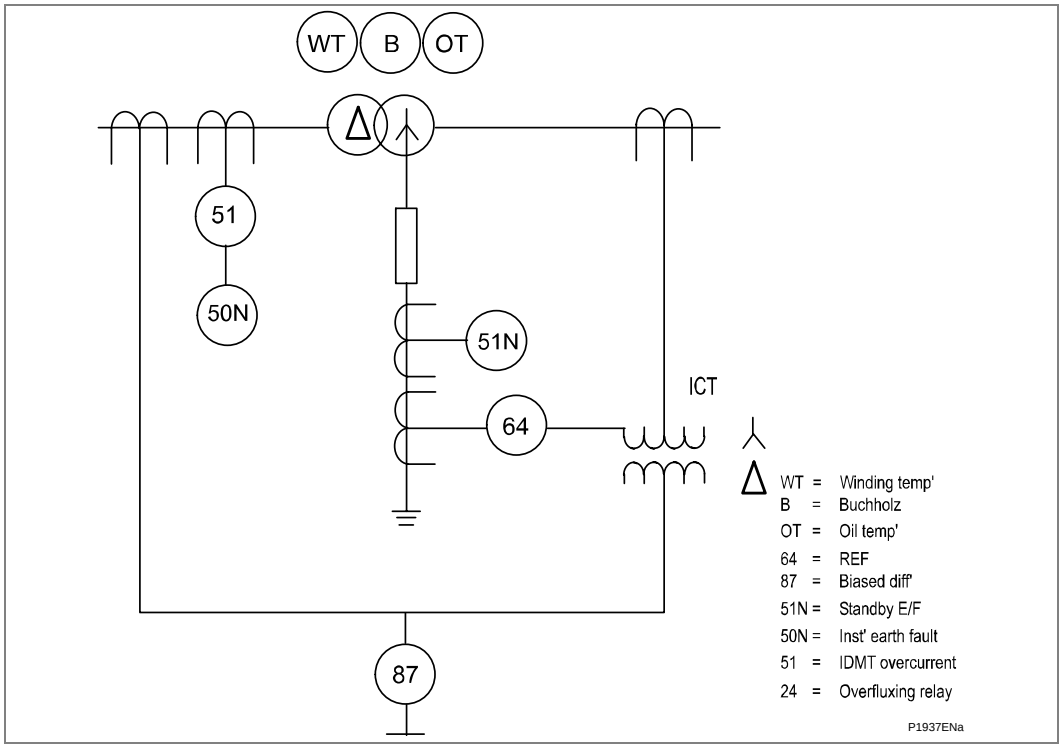


Figure 5 - Typical transformer protection package

High speed protection is provided for faults on both the HV and LV windings by biased differential protection (87). The relay operates on the basic differential principle that HV and LV CT secondary currents entering and leaving the zone of protection can be balanced under load and through fault conditions, whereas under internal fault conditions balance will be lost and a differential current will cause the relay to trip. The zone of protection is clearly defined by the CT locations and, as the protection is stable for through faults, it can be set to operate without any intentional time delay.

The following figure shows the application of the P64x differential relay with software vector group and amplitude matching. This provides phase and ratio correction of CT signals in addition to filtering LV zero sequence current to prevent maloperation of the differential element for external LV earth faults. Interposing CTs (ICTs) are no longer required.

More sensitive high-speed earth fault protection for the LV winding is provided by restricted earth fault protection (64). Due to the limitation of phase fault current on the HV side for LV winding earth faults, and the fact that any unrestricted earth fault protection in the transformer earth path requires a discriminative time delay, restricted earth fault protection is widely applied.

Earth fault protection is provided on the HV winding by the inherently restricted earth fault element associated with the HV overcurrent protection (50N). The delta winding of the transformer draws no HV zero sequence current for LV earth faults and passes no zero sequence current to upstream HV earth faults. Hence, there is no requirement to grade this element with other earth fault protection and it can be set to operate without any intentional time delay. For delta windings this is known as balanced earth fault protection.

Sustained external LV faults are cleared by the IDMT overcurrent protection on the HV winding (51) or by the standby earth fault protection (51N) in the transformer earth connection. The extent of backup protection used will vary according to the transformer installation and application.

The protection scheme may be further enhanced by the use of other protective devices associated with the transformer, such as the Buchholz, pressure relief and winding temperature devices. These devices can act as another main protective system for large transformers. They may also provide clearance for some faults which might be difficult to detect by protection devices operating from line current transformers, for example, winding inter turn faults or core lamination faults. These devices are connected to directly trip the breaker in addition to operating auxiliary relays for indication purposes.

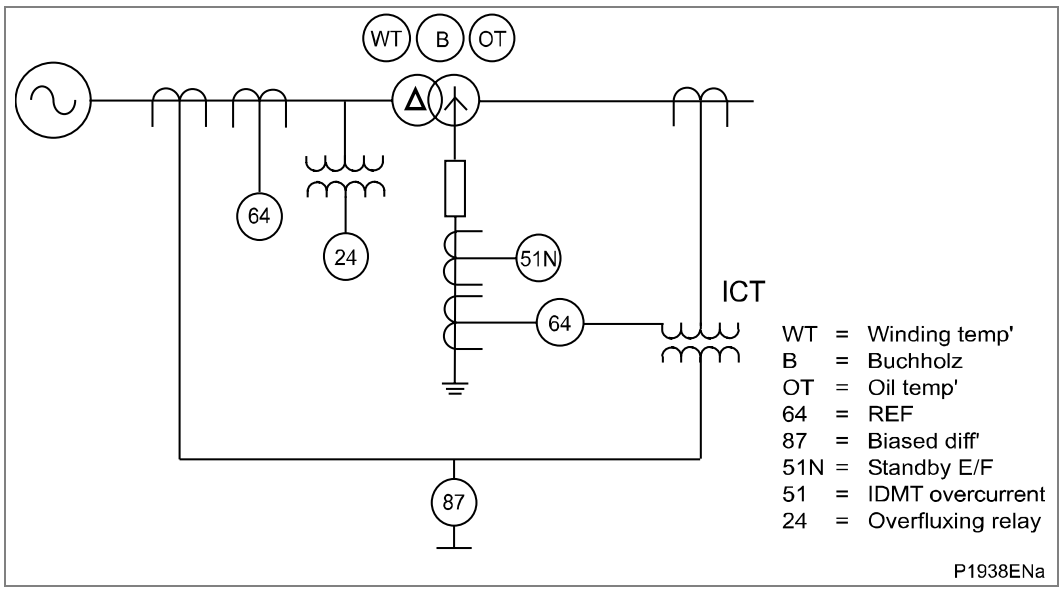


Figure 6 - Typical protection package for a transformer

The protection of a generator transformer is similar to that for any other large transformer.

High speed protection is provided for phase to phase faults by the provision of biased differential protection. In addition, for large generators, the transformer is commonly included within an overall second main differential arrangement, which incorporates the generator and transformer within the overall zone of protection. Earth fault protection is provided by a restricted earth fault element on the star winding.

Overfluxing protection is commonly applied to generator circuits to prevent generator or transformer damage from prolonged overfluxing conditions.

Other protection devices will again complement the main relay protection.

Auto-transformers are commonly used to couple EHV and HV power networks if the ratio of their voltages is moderate. The protection arrangements for an auto-transformer are similar in most respects to the protection of a two-winding transformer. Protection of all windings can be offered by a biased differential relay such as the P64x.

1.2 Protection Relay

The P64x relay has been designed to bring the latest numerical technology to the protection of power transformers. The increased functionality of numerical relays allows enhanced protection functions to be offered for a wide variety of applications, which, when combined with a host of non-protective features, can provide power system control and monitoring requirements.

1.2.1 Protection Functions

The main protection functions offered by the P64x are listed below:

- Biased differential protection (87)
- Restricted earth fault protection for individual transformer windings (64)
- Directional/non-directional instantaneous/time delayed phase overcurrent protection (50/51)
- Derived/measured, directional/non-directional, instantaneous/time delayed earth fault protection (50N/51N)
- Directional/non-directional, instantaneous/time delayed negative phase sequence overcurrent protection (46)
- Thermal overload protection (49)
- Under/overvoltage and residual overvoltage protection (27/59/59N)
- Under/overfrequency protection (81)
- Overfluxing protection (24)
- Stub bus/Winding overcurrent. It is only available in P643/P645.
- Breaker failure
- Opto-isolated inputs and programmable logic for alarm/trip indication of external devices

Note	*Directional overcurrent elements, under/overvoltage and residual overvoltage elements are available on request of the three-phase VT input.*

The biased differential element has a triple slope bias characteristic to ensure sensitivity, with load current, to internal faults and stability under heavy through-fault conditions.

The differential element can be blocked for magnetizing inrush conditions, based on the ratio of second harmonic to fundamental current. Also the differential element can be blocked during transient overfluxing conditions, based on the ratio of fifth harmonic to fundamental current. Fast operating times for heavy internal faults can be achieved using the unrestrained instantaneous differential high set elements.

Restricted earth fault protection, based on the low/high impedance principle, is available for up to three transformer windings to offer increased sensitivity to low-level winding earth faults.

Three four-stage overcurrent protection elements are provided for each transformer winding. Three four-stage earth fault protection elements are provided based on the neutral current of every winding. Hence, each winding has its dedicated earth fault protection elements. The user can select between measured neutral current and derived neutral current. Three four-stage negative phase sequence overcurrent protection elements are provided for each transformer winding.

Thermal overload protection can be used to prevent equipment from operating at temperatures in excess of the designed maximum withstand. Prolonged overloading causes excessive heating, which may result in premature ageing of the insulation, or in extreme cases, insulation failure. The thermal overload protection is based on IEEE Standard C57.91-1995. The trip command is based on either the hot spot temperature or the top oil temperature, each one with three time-delayed stages.

Transformer loads are becoming increasingly non-linear, causing increased current harmonics. Since increased harmonics content raise the winding temperature, the relay incorporates a current based thermal replica, using rms load current to model heating and cooling of the protected transformer. The element can be set with both alarm and trip stages.

The V/f overfluxing element provides protection against transformer damage which may result from prolonged operation at increased voltages or decreased frequency, or both. Independent alarm and trip characteristics are provided to enable corrective action to be undertaken before tripping is initiated.

Stub bus protection is used in a one and a half breaker scheme. When the disconnector associated to a winding is open, the differential, REF, breaker failure and differential CTS elements related to the open winding are affected. The output of the stub bus detection logic can be used to change the trip logic and to trigger an indication if necessary.

It is common practice to install Circuit Breaker Failure (CBF) protection to monitor that the circuit breaker has opened within a reasonable time after the main protection has tripped. If the fault current has not been interrupted following a set time delay from circuit breaker trip initiation, CBF protection will operate. CBF operation can be used to backtrip upstream circuit breakers to ensure that the fault is isolated correctly. CBF operation can also reset all start output contacts, ensuring that any blocks asserted on upstream protection are removed.

Use of the opto-inputs as trip repeat and alarm paths for other transformer protection devices, (Buchholz, Oil pressure, winding temperature) allows operation of these devices to be event-logged. Interrogation of the relay fault, event and disturbance records offers an overall picture of an event or fault, of the transformer protection performance and sequences of operation.

All models of the P64x are 3-phase units with internal phase compensation, CT ratio correction and zero sequence filtering, eliminating the need for external interposing transformers. Up to five biased inputs can be provided to cater for power transformers with more than two windings or more than one set of CTs associated with each winding, such as in mesh or one-and-a-half circuit breaker substation arrangements.

The variety of protective functions offered by the P64x makes it ideal not only for the protection of power transformers but also for a variety of applications where biased differential is commonly applied, these include:

- Overall generator/transformer protection
- Generators
- Reactors
- Motors

1.2.2 Non-Protection Features

In addition to providing all the common relaying requirements for a transformer protection package, the P64x relay shares many common features with the other relays in the MiCOM range.

The P64x offers this variety of additional features due to its digital design and standardization of hardware. These features are listed below:

- Loss of life statistic
- Through-fault monitoring
- CT and VT supervision
- Pole dead. It is only available in P643/P645 on request of the 3-phase VT input
- Fault records (summary of reasons for tripping)
- Event records (summary of alarms and relay events)
- Disturbance records (record of analogue waveforms and operation of opto-inputs and output relays)
- Date and time tagging of all records
- Setting aids
- Remote communications
- High level of continuous self monitoring and diagnostic information

2 APPLICATION OF INDIVIDUAL PROTECTION FUNCTIONS

These sections detail the individual protection functions in addition to where and how they may be applied. Worked examples show how the settings are applied to the relay.

2.1 Overall Differential Protection (87)

In applying the well established principles of differential protection to transformers, a variety of considerations have to be taken into account. These include compensation for any phase shift across the transformer, possible unbalance of signals from current transformers either side of the windings and the effects of the variety of earthing (grounding) and winding arrangements. In addition to these factors, which can be compensated for by correct application of the relay, the effects of normal system conditions on relay operation must also be considered. The differential element must be blocked for system conditions which could result in maloperation of the relay, such as high levels of magnetizing current during inrush conditions or during transient overfluxing.

In traditional transformer differential schemes, the requirements for phase and ratio correction were met by the application of external interposing current transformers, as a secondary replica of the main transformer winding arrangements, or by a delta connection of main CTs (phase correction only). The P64x has settings to allow flexible application of the protection to a wide variety of transformer configurations, or to other devices where differential protection is required, without the need for external interposing CTs or delta connection of secondary circuits.

2.1.1 Biased Elements

The P64x percentage bias calculation is performed 8 times per cycle. A triple slope percentage bias characteristic is implemented. Both the flat and the lower slope provide sensitivity for internal faults. Under normal operation steady state magnetizing current and the use of tap changers result in unbalanced conditions and hence differential current. To accommodate these conditions the initial slope, K1, may be set to 30%. This ensures sensitivity to faults while allowing for mismatch when the power transformer is at the limit of its tap range and CT ratio errors. At currents above rated, extra errors may be gradually introduced as a result of CT saturation, Hence, the higher slope may be set to 80% to provide stability under through fault conditions, during which there may be transient differential currents due to saturation effect of the CTs. The through fault current, in all but ring bus or mesh fed transformers, is given by the inverse of the per unit reactance of the transformer. For most transformers, the reactance varies between 0.05 to 0.2 pu, therefore typical through fault current is given by 5 to 20 I_n.

The number of biased differential inputs required for an application depends on the transformer and its primary connections. It is recommended that, where possible, a set of biased CT inputs is used for each set of current transformers. According to IEEE Std. C37.110-2007 separate current inputs should be used for each power source to the transformer. If the secondary windings of the current transformers from two or more supply breakers are connected in parallel, under heavy through fault conditions, differential current resulting from the different magnetizing characteristics of the current transformers flows in the relay. This current only flows through one current input in the relay and can cause misoperation. If each CT is connected to a separate current input, the total fault current in each breaker provides restraint. It is only advisable to connect CT secondary windings in parallel when both circuits are outgoing loads. In this condition, the maximum through fault level is restricted solely by the power transformer impedance.

There are three basic models of the P64x relay:

- P642 Two biased differential inputs
- P643 Three biased differential inputs
- P645 Five biased differential inputs

Where a P643 or P645 is chosen, it can be programmed to provide 2 or 3 biased inputs.

The following table shows the variety of connections which can be catered for by the range of P64x relays.

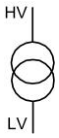
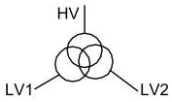
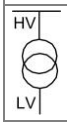
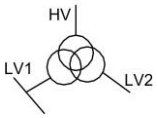
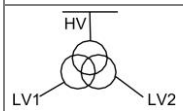
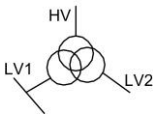
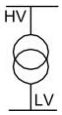
Configuration	No. of CT sets	Recommended relay
	2	P642
	3	P643
	3	P643
	3	P643
	4 or 5	P645
	4 or 5	P645
	4 or 5	P645

Table 2 - Applications of the P64x transformer differential protection relay

The P64x relay achieves stability for through faults in two ways, both of which are essential for correct relay operation. The first is the correct sizing of the current transformers; the second is by providing a relay bias characteristic as shown here:

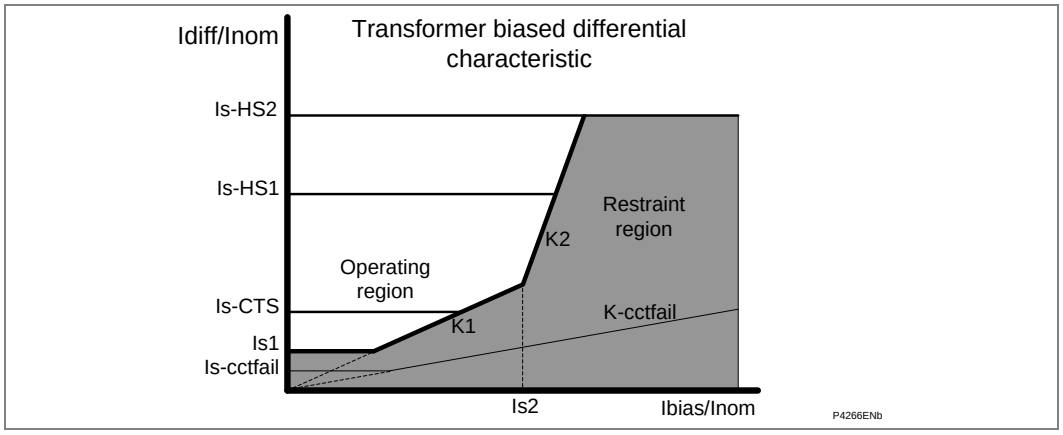


Figure 7 - P64x triple slope (flat, K1, K2) biased differential protection

The flat and lower slope, K1, provides sensitivity for internal faults. The higher slope, K2, provides stability under through fault conditions, during which there may be transient differential currents due to asymmetric CT saturation.

The differential and biased current calculations are done on a per phase basis after amplitude, vector group matching and zero sequence filtering are performed. The following equations are valid for uniformly defined current directions relative to the protected equipment, such that the current directions of all windings are either towards the protected object or away from it.

The differential current, I_{diff}, and the bias current I_{bias} are defined by these expressions:

$$I_{diff} = \left|\vec{I}_1 + \vec{I}_2 + \vec{I}_3 + \vec{I}_4 + \vec{I}_5\right| \qquad I_{bias} = \frac{\left|\vec{I}_1\right| + \left|\vec{I}_2\right| + \left|\vec{I}_3\right| + \left|\vec{I}_4\right| + \left|\vec{I}_5\right|}{2}$$

The differential current, I_{diff}, is the vector sum of the phase currents measured at all ends of the transformer. The mean bias current, I_{bias} is the scalar mean of the magnitude of the currents at all ends of the transformer.

To provide stability for external faults these measures are taken on the bias calculations:

- **Delayed bias**: the bias quantity is the maximum of the bias quantities calculated within the last cycle. This is to maintain the bias level, providing stability during the time when an external fault is cleared. This feature is implemented on a per phase basis.
- **Transient bias**: an additional bias quantity is introduced into the bias calculation, on a per phase basis, if there is a sudden increase in the mean-bias measurement. This quantity will decay exponentially afterwards. The transient bias is reset to zero once the relay has tripped or if the mean-bias quantity is below the Is1 setting. The transient bias algorithm is executed 8 times per cycle.
- **Maximum bias**: the bias quantity used per phase for the percentage bias characteristic is the maximum delayed bias current calculated from all three phases.

$$Ibias_{max} = \text{Maximum}\left[Ia_{bias}, Ib_{bias}, Ic_{bias}\right]$$

For the P64x relays the restraining effect (bias current) never disappears when there is an internal fault; the restraining effect is even reinforced. However, the restraining current factor ½ means that the differential current I_d has twice the value of the restraining current I_{bias}, so that safe and reliable tripping is also guaranteed in the case of multi-end infeed for internal faults.

As shown in the above “P64x triple slope (flat, K1, K2) biased differential protection“ diagram, the tripping characteristic of the differential protection has two knees. The first knee is dependent on the setting of the basic threshold value Is1. The second knee of the tripping characteristic is defined by the setting Is2.

The basic pick up level of the low set differential element, Is1, is dependant on the item of the plant being protected and by the amount of differential current that might be seen during normal operating conditions. A setting of 0.2 pu is generally recommended when the P64x is used to protect a transformer. When protecting generators and other items of the plant, where shunt magnetizing current is not present, a lower differential setting can be used and 0.1 pu is more typical.

The flat section of the tripping curve represents the most sensitive region of the tripping characteristic in the form of the settable basic threshold value Is1. The default setting of 0.2 pu considers the steady state magnetizing current of the transformer, which flows even in a no-load condition and is generally less than 5% of the nominal transformer current.

Characteristic equation:

For $\text{Ibias} < \frac{\text{Is1}}{\text{K1}}$

The flat and K1 slopes of the tripping curve cover the load current range, so that in these sections we must account for not only the transformer steady state magnetizing current, which appears as differential current, but also with differential currents that can be attributed to the transformation errors of the current transformer sets and on load tap changers.

If we calculate the worst case with IEC class 10P current transformers, the maximum allowable amplitude error according to IEC 60044-1 is 3 % for nominal current. The phase-angle error can be assumed to be 2° for nominal current. The maximum allowable total error for nominal current is then obtained, in approximation, as $(0.03 + \sin 2°) \approx 6.5$ %. If the current is increased to the nominal accuracy limit current, the total error for Class 10P current transformers can be 10 % maximum, as may be the case under heavy fault conditions. Beyond the nominal accuracy limit current, the transformation error can be of any magnitude.

The dependence of the total error of a current transformer on current is therefore non-linear. In the operating current range (the current range below the nominal accuracy limit current) we can expect a worst case total error of approximately 10 % per current transformer set.

The first slope section of the tripping characteristic forms a straight line, the slope of which should correspond to the cumulative total error of the participating current transformer sets and on load tap changer. The curve slope, K1, can be set. The default setting for K1 is 30%.

Characteristic equation:

For $\text{Idiff} \geq \text{Is1}$ $\quad \text{Ibias} < \text{Is2}$ $\quad \text{Idiff} >= \text{K1} \times \text{Ibias}$

The second knee point, Is2, is settable. It has a default setting of 1 pu and must be set in accordance with the maximum possible operating current.

Restraining currents that go beyond the set knee point (Is2) are typically considered as through fault currents. For through fault currents, the third section of the tripping characteristic could therefore be given an infinitely large slope. However, a fault can occur in the transformer differential protected zone, therefore a finite slope K2 is provided for the third section of the tripping curve. The default setting for K2 is 80%.

Characteristic equation:

For $\text{Idiff} >= \text{Is2}$ $\quad \text{Idiff} >= \text{K1} \times \text{Is2} + \text{K2} (\text{Ibias} - \text{Is2})$

2.1.2 Ratio Correction

To ensure correct operation of the differential element, it is important that under load and through fault conditions the currents into the differential element of the relay balance. In many cases, the HV and LV current transformer primary ratings will not exactly match the transformer winding rated currents. Ratio correction factors are therefore provided. The CT ratio correction factors are applied to ensure that the signals to the differential algorithm are correct.

A reference power, identical for all windings, is defined in the $\mathbf{S_{ref}}$ setting cell under the **SYSTEM CONFIG** menu heading. For two-winding arrangements, the nominal power is usually the reference power. For three-winding transformers, the nominal power of the highest-power winding should be set as the reference power. The ratio correction factor for each winding of the transformer is calculated by the relay on the basis of the set reference power, the set primary nominal voltages of the transformer and the set primary nominal currents of the current transformers.

$$K_{amp,n} = \frac{I_{primCT,nom,n}}{\frac{S_{prim,ref}}{\sqrt{3}V_{primCT,nom,n}}}$$

Where:

$K_{amp,n}$ = amplitude matching factor for the respective CT input

$I_{primCT,nom,n}$: primary nominal current for the respective CT input

$V_{primCT,nom,n}$: nominal voltage for the respective CT input. Where on-load tap changing is used, the nominal voltage chosen should be that for the mid tap position.

$S_{prim,ref}$: common primary reference value of S for all windings

Therefore, the only data needed for ratio correction or amplitude matching calculations done by the relay are the nominal values read from the generator/transformer nameplate.

For the two-winding transformer shown in the “Ratio Correction or Amplitude Matching Factor” diagram, the phase C amplitude matched currents of the HV and LV windings are the same.

$$I_{amp,HV,C} = K_{amp,HV} \times I_{HV,C}$$

$$I_{amp,LV,C} = K_{amp,LV} \times I_{LV,C}$$

Where:

$I_{amp,\ HV,C}$; HV side phase C amplitude matched current

$K_{amp,HV}$: HV side calculated ratio correction factor

$I_{HV,C}$: HV side phase C current magnitude

$I_{amp,\ LV,C}$; LV side phase C amplitude matched current

$K_{amp,LV}$: LV side calculated ratio correction factor

$I_{LV,C}$: LV side phase C current magnitude

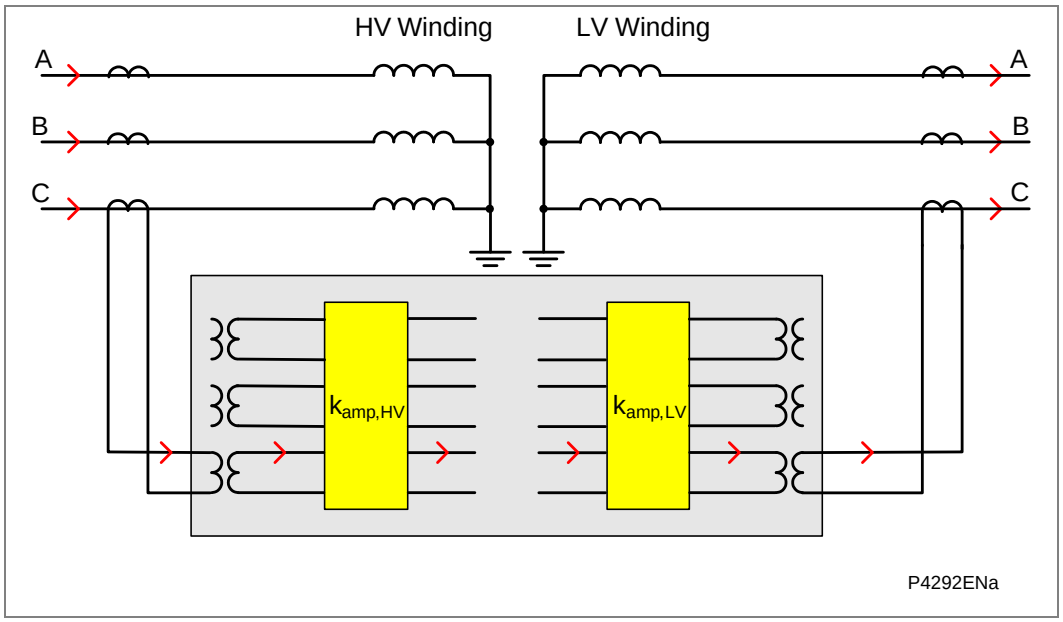


Figure 8 - Ratio correction or amplitude matching factor

Matching factors are displayed by the relay in the **Match Factor CT1**, **Match Factor CT2**, **Match Factor CT3**, **Match Factor CT4** and **Match Factor CT5** data cells under the **SYSTEM CONFIG** menu heading. The relay derives amplitude matching factors automatically so that all biased currents are compared on a like for like basis. The range of the calculated matching factors is from 0.05 to 20.

Caution	***Amplitude matching factors above 20 are not recommended as the probability of tripping due to electrical noise is very high.***

2.1.3 Vector Group Correction

To compensate for any phase shift between two windings of a transformer it is necessary to provide vector group correction. This was traditionally provided by the appropriate connection of physical interposing current transformers, as a replica of the main transformer winding arrangements, or by a delta connection of main CTs. This matching operation can be carried out regardless of the phase winding connections, since the phase relationship is described unambiguously by the characteristic vector group number.

Hence, vector group matching is performed by mathematical phasor operations on the amplitude-matched phase currents of the *low-voltage side* as per the characteristic vector group number. The vector group is the clock-face hour position of the LV A-phase voltage, with respect to the A-phase HV voltage at 12-o'clock (zero) reference. Phase correction is provided in the P64x using **SYSTEM CONFIG** then **LV Vector Group** for phase shift between HV and LV windings and **SYSTEM CONFIG** then **TV Vector Group** for phase shift between HV and TV windings. This is shown in the following diagram for vector group characteristic number 5, where vector group Yd5 is used as the example:

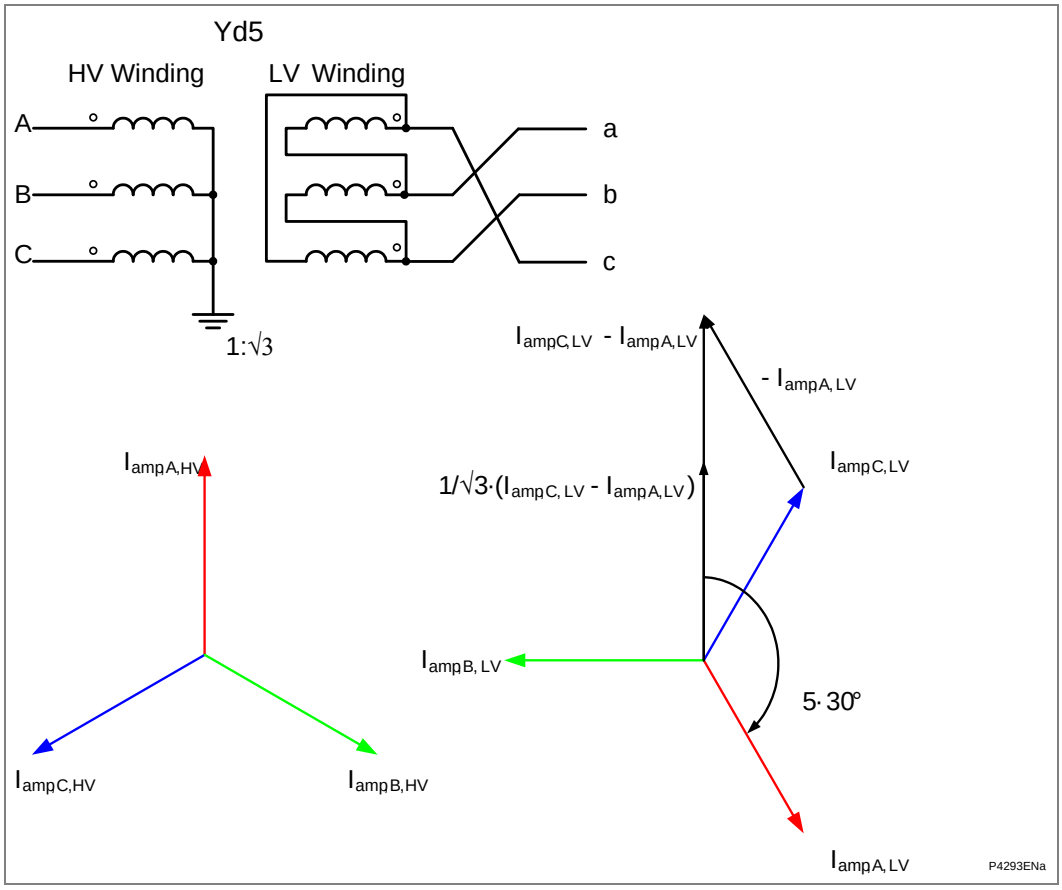


Figure 9 - Yd5 transformer example

The angle of positive sequence primary current is used as a default; therefore no vector correction is applied to the high voltage side.

As shown in the above *Yd5 transformer example* diagram, the positive sequence current at the low voltage end is shifted by 150° clockwise for ABC (anti-clockwise) rotation. Therefore, the relay setting, **LV Vector Group**, equal to "5" rotates back the current at the low side for 150° in an anti-clockwise direction. This assures that the primary and secondary currents are in phase for load and external fault conditions. The vector correction also considers amplitude matching. If the vector group is any odd number, the calculated current will be greater by $\sqrt{3}$; therefore this current will be automatically divided by $\sqrt{3}$. Hence, this effect does not need to be taken into account when CT correction compensation is automatically calculated or set.

Setting the vector group matching function is very simple and does not require any calculations. Only the characteristic vector group number needs to be set in **LV Vector Group** and **TV Vector Group**.

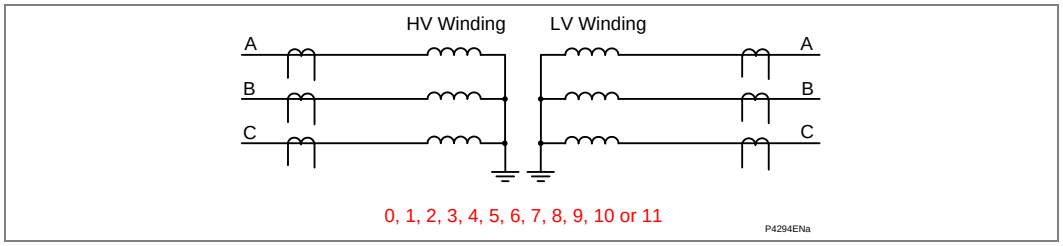


Figure 10 - Vector group selection

Other nameplate designations may be used instead of the clock notation.
Common examples are:

Alternatives		Equivalent standard	LV group setting
D_{AB}/Y	D_{AB} – Y	Dy1	1
D_{AC}/Y	D_{AC} – Y	Dy11	11
Y/Y	Y_0 - Y0	Yy0	0
Y/Y	Y_0 - Y6	Yy6	6

Table 3 - Examples of nameplate designations

2.1.4 Zero Sequence Filter

In addition to mimicking the phase shift of the protected transformer, it is also necessary to mimic the distribution of primary zero sequence current in the protection scheme. The necessary filtering of zero sequence current has also been traditionally provided by appropriate connection of interposing CTs or by delta connection of main CT secondary windings. In the relay, the user does not need to decide which windings need zero sequence filtering. The user just needs to set which windings are grounded using a Yn, Zn or in zone-earthing transformer. The relay will adjust itself accordingly. In the advanced setting mode, it is possible to override the self adaptive setting with the zero sequence filtering enabled/disabled setting.

Where a transformer winding can pass zero sequence current to an external earth fault, it is essential that some form of zero sequence current filtering is used. This ensures that out of zone earth faults will not cause the relay to maloperate.

An external earth fault on the star side of a Dyn11 transformer will result in zero sequence current flowing in the current transformers associated with the star winding. However, due to the effect of the delta winding, there will be no corresponding zero sequence current in the current transformers associated with the delta winding.

To ensure stability of the protection, the LV zero sequence current must be eliminated from the differential current. Traditionally this has been achieved by either delta connected line CTs or by the inclusion of a delta winding in the connection of an interposing current transformer.

In accordance with its definition, the zero-sequence current is determined as follows from vector and amplitude matched phase currents:

$$\vec{I}_0 = \frac{1}{3}.\left(\vec{I}_{A,vector\_comp} + \vec{I}_{B,vector\_comp} + \vec{I}_{C,vector\_comp}\right)$$

The current that is used in the differential equation is the filtered current per phase:

$$\vec{I}_{A,filtered} = \vec{I}_{A,vector\_comp} - \vec{I}_0$$

$$\vec{I}_{B,filtered} = \vec{I}_{B,vector\_comp} - \vec{I}_0$$

$$\vec{I}_{C,filtered} = \vec{I}_{C,vector\_comp} - \vec{I}_0$$

Setting the zero-sequence current filtering function is very simple and does not require any calculations. Zero-sequence current filtering should only be activated for those ends where there is operational earthing (grounding) of a neutral point:

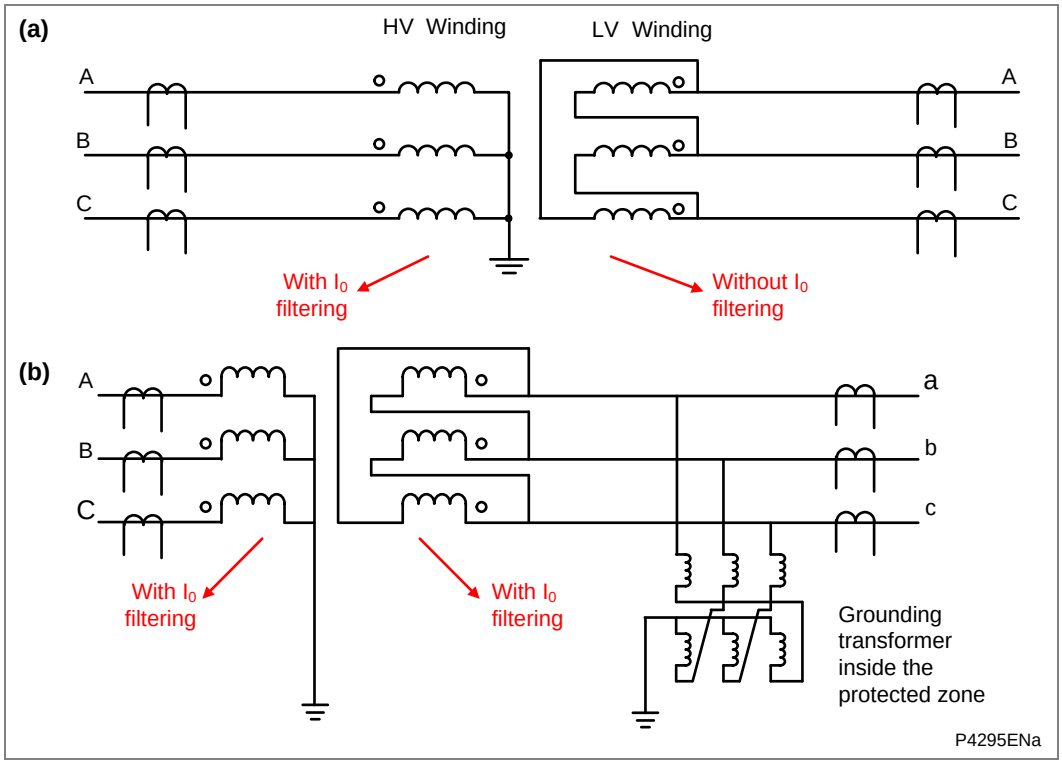


Figure 11 - Zero sequence current filtering

The following figure shows the current distribution for an AN fault on the delta side of a Yd1 transformer with a grounding transformer inside the protected zone.

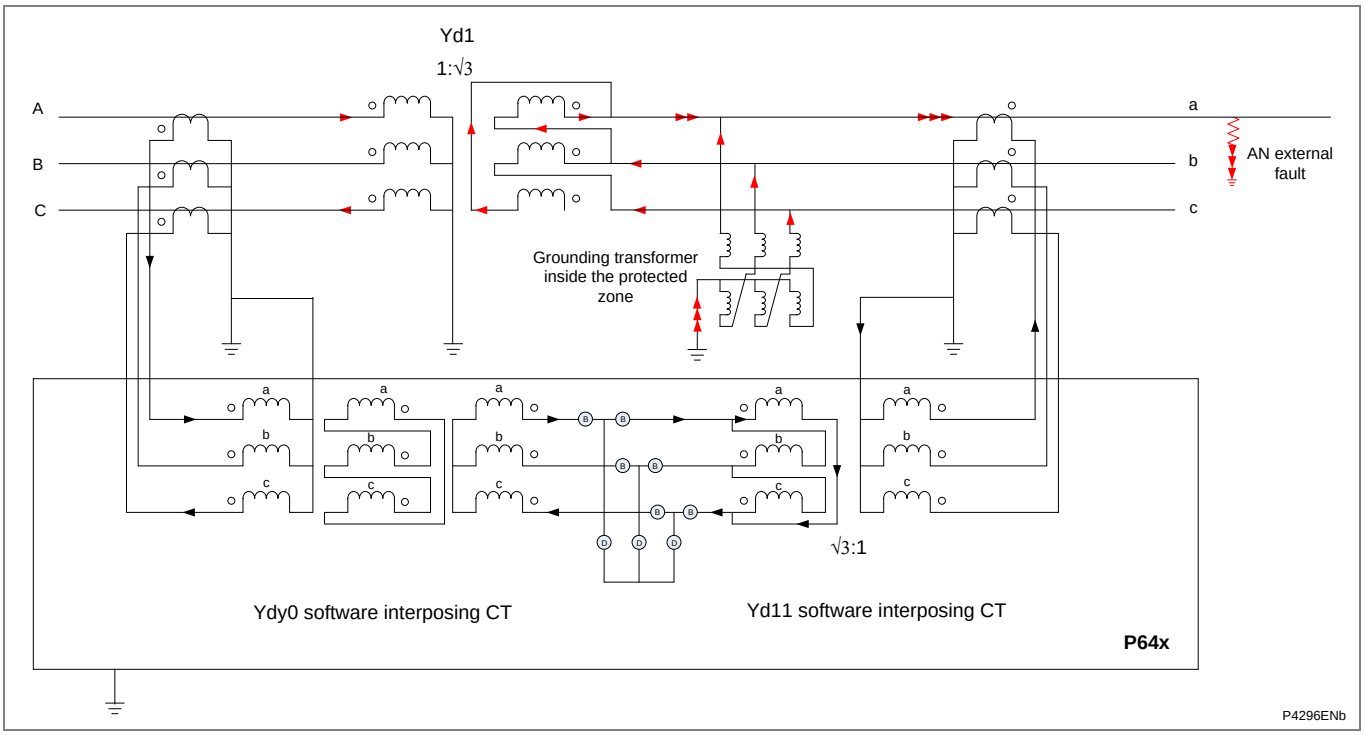


Figure 12 - Current distribution for AN external fault on delta side of Yd1 transformer

2.1.5 Magnetizing Inrush Stabilization

When a transformer is first energized, a transient magnetizing current flows, which may reach instantaneous peaks of 8 to 30 times the full load current. The factors controlling the duration and magnitude of the magnetizing inrush are:

- Size of the transformer bank
- Size of the power system
- Resistance in the power system from the source to the transformer bank
- Residual flux level
- Type of iron used for the core and its saturation level.

There are three conditions which can produce a magnetizing inrush effect:

- First energization
- Voltage recovery following external fault clearance
- Sympathetic inrush due to a parallel transformer being energized.

The following diagram shows under normal steady state conditions the flux in the core changes from maximum negative value to maximum positive value during one half of the voltage cycle, which is a change of 2.0 maximum.

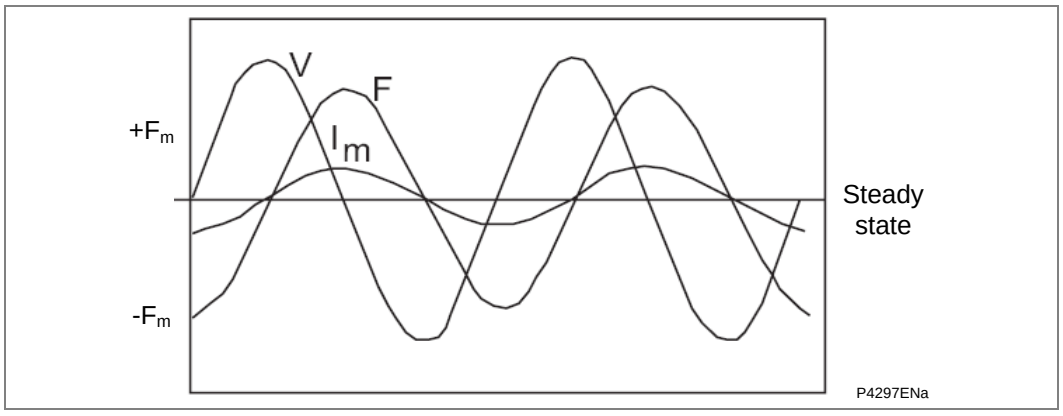


Figure 13 - Steady state magnetizing inrush current

If the transformer is energized at a voltage zero when the flux would normally be at its maximum negative value, the flux will rise to twice its normal value over the first half cycle of voltage. To establish this flux, a high magnetizing inrush current is required. The first peak of this current can be as high as 30 times the transformer rated current. This initial rise could be further increased if there was any residual flux in the core at the moment the transformer was energized.

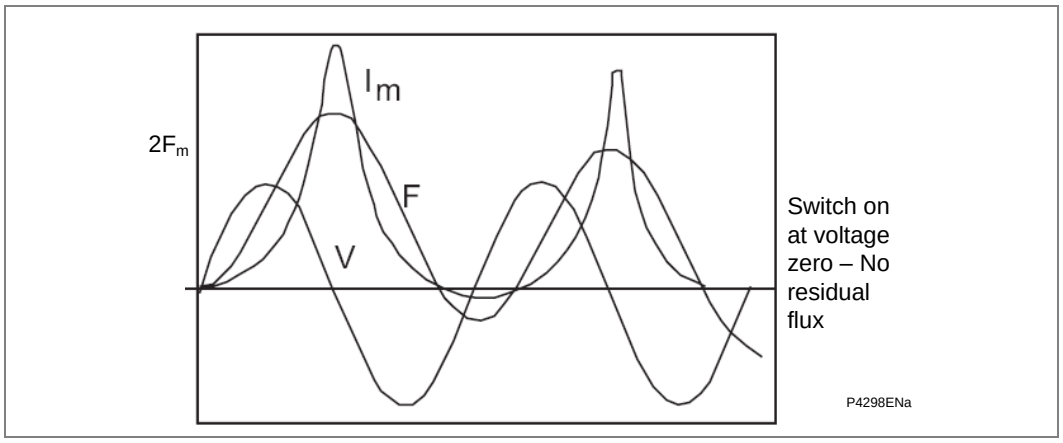


Figure 14 - Magnetizing inrush current during energization

As the flux enters the highly saturated portion of the magnetizing characteristic, the inductance falls and the current rises rapidly. Magnetizing impedance is of the order of 2000% but under heavily saturated conditions this can reduce to around 40%, which is an increase in magnetizing current of 50 times normal. This figure can represent 5 or 6 times normal full load current.

Analysis of a typical magnitude inrush current wave shows (fundamental = 100%):

Component	-DC	2nd H	3rd H	4th H	5th H	6th H	7th H
	55%	63%	26.8%	5.1%	4.1%	3.7%	2.4%

The offset in the wave is only restored to normal by the circuit losses. The time constant of the transient can be quite long, typically 0.1 second for a 100 KVA transformer and up to 1 second for larger units. The initial rate of decay is high due to the low value of air core reactance. When below saturation level, the rate of decay is much slower. The following graph shows the rate of decay of the DC offset in a 50 Hz or 60 Hz system in terms of amplitude reduction factor between successive peaks.

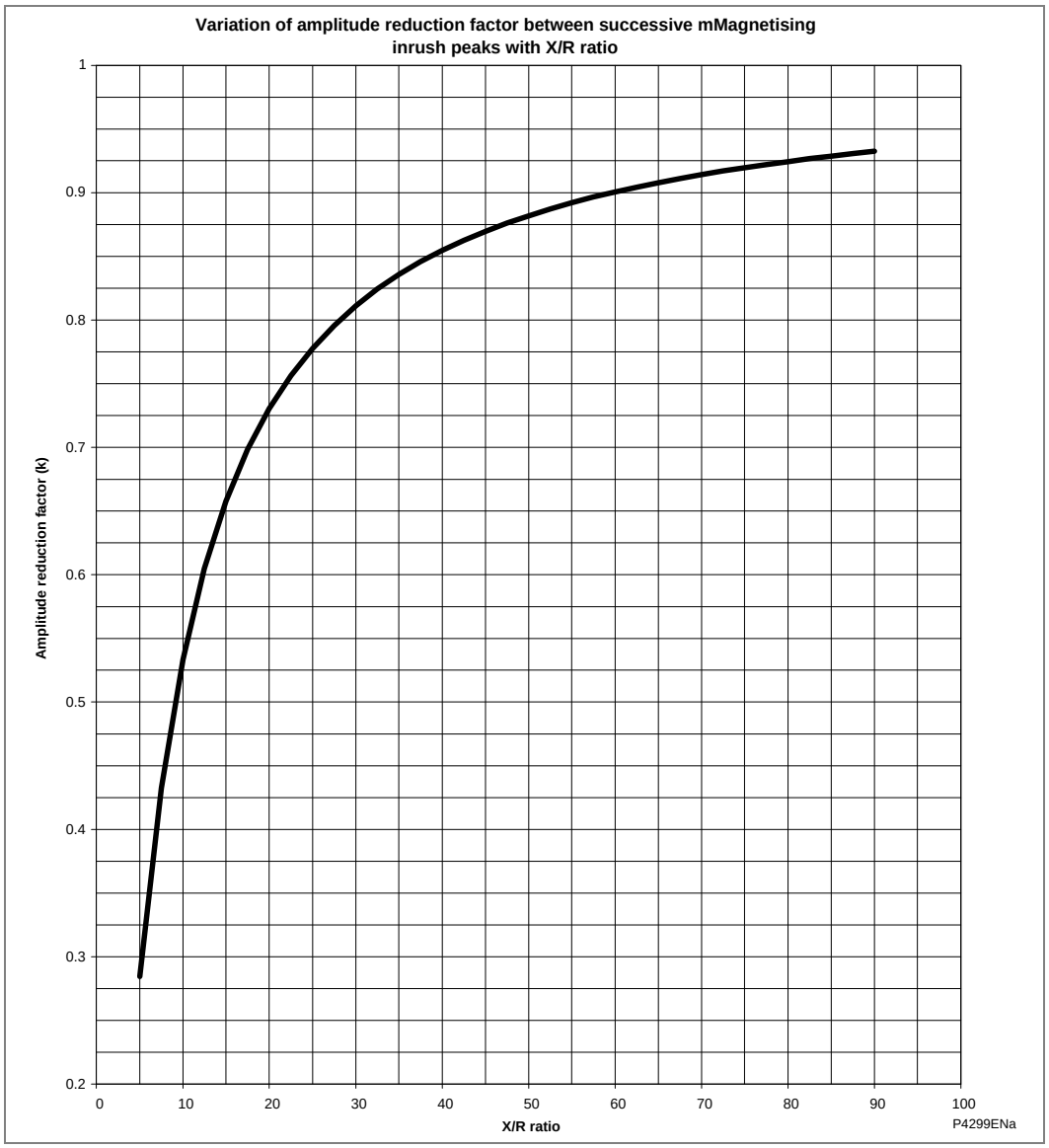


Figure 15 - Variation of amplitude reduction factor

The magnitude of the inrush current is limited by the air core inductance of the windings under extreme saturation conditions. A transformer with concentric windings will draw a higher magnetizing current when energized from the LV side, since this winding is usually on the inside and has a lower air core inductance. Sandwich windings have approximately equal magnitude currents for both LV and HV. Resistance in the source will reduce the magnitude current and increase the rate of decay.

The magnetizing inrush phenomenon is associated with a transformer winding which is being energized where no balancing current is present in the other winding(s). This current appears as a large operating signal for the differential protection. Therefore, special measures are taken with the relay design to ensure that no maloperation occurs during inrush. The fact that the inrush current has a high proportion of harmonics having twice the system frequency offers a possibility of stabilization against tripping by the inrush current.

The second harmonic blocking may not be effective in all applications with all types of transformers. The relay filters the differential current. The fundamental $I_{diff}(f_0)$ and second harmonic components $I_{diff}(2*f_0)$ of the differential current are determined. If the ratio $I_{diff}(2*f_0)/I_{diff}(f_0)$ exceeds a specific adjustable value (typical setting 20%) in at least one phase, the low-set differential element is blocked optionally in one of these modes:

- Across all three phases if cross blocking is selected
- Selectively for one phase because the harmonic blocking is phase segregated
- There is no blocking if the differential current exceeds the high set thresholds Is-HS1 or Is-HS2.

2.1.6 CT Saturation and no Gap Detection

No settings are required by the CT saturation and no gap detection features. It is only possible to either enable or disable them on the **CTSat and NoGap** setting cell. It is recommended to enable **CTSat and NoGap** because faster operating times are achievable under CT saturation with fault levels below Is-HS1 threshold. The assertion of CTSat and NoGap prevents the second harmonic element from blocking the low set differential element. Therefore, at fault levels below Is-HS1 threshold fast fault clearance is achievable even with CT saturation.

The following two figures are the same AN internal fault.

- The “CT saturation and no gap detection enabled” diagram shows the disturbance record from a P64x with CT saturation and no gap detection enabled. The second harmonic blocking is asserted due to CT saturation. Therefore, the operation of the low set differential element (bias element trip) is prevented. Once the No gap detection is asserted the low set differential element is allowed to operate. The operating time is 32 ms.
- The “CT saturation and no gap detection disabled” diagram shows the disturbance record from a P64x with CT saturation and no gap detection disabled. The second harmonic blocking is asserted due to CT saturation. Therefore, the operation of the low set differential element (bias element trip) is prevented until the second harmonic blocking de-asserts. In this case, the operating time is 56 ms.

  Enabling the CT saturation and no gap detection logics enhance the relay operating time. In this example, the relay is 24 ms faster if the CT saturation and no gap detection logics are enabled.

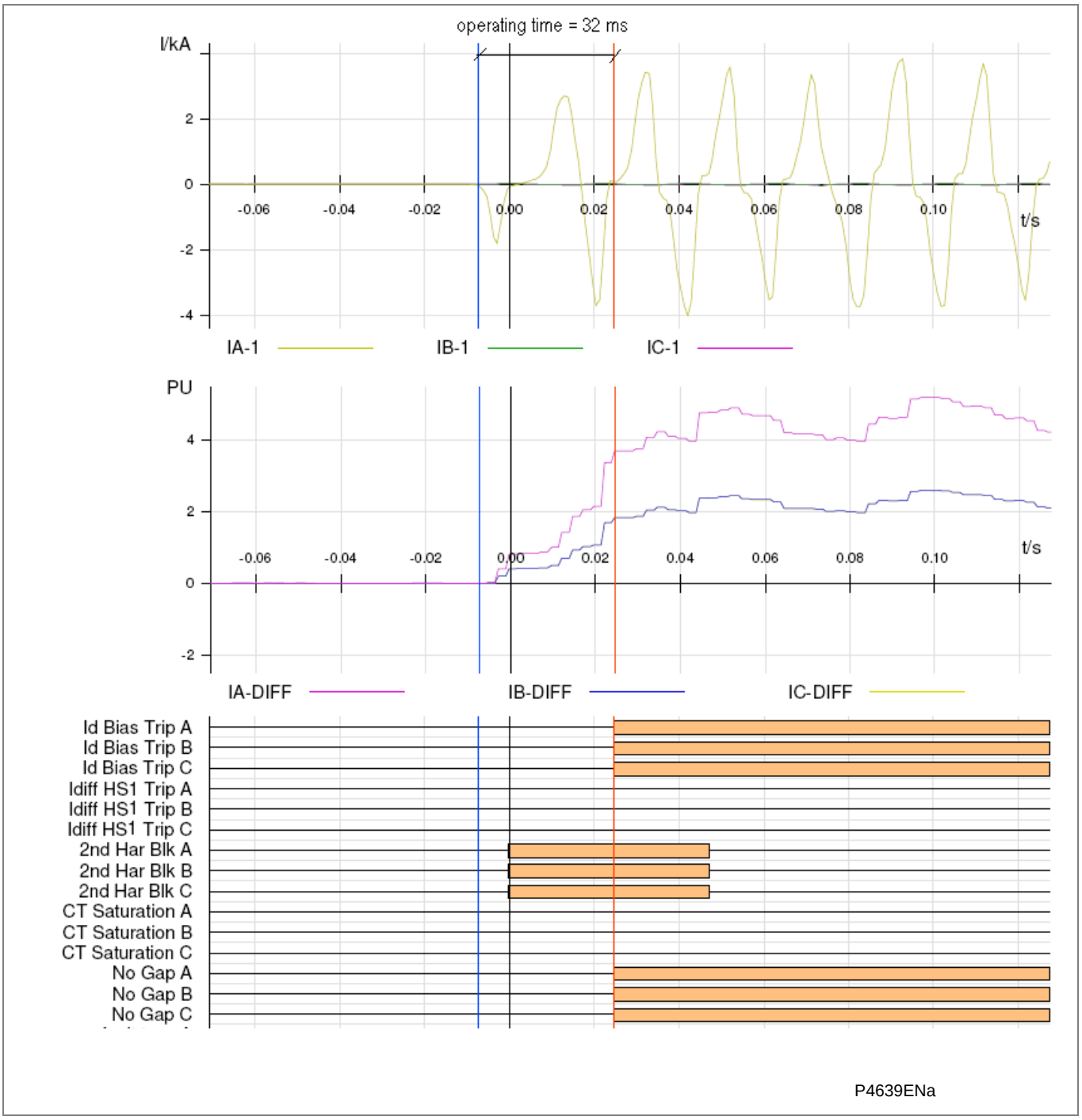


Figure 16 - CT saturation and no gap detection enabled

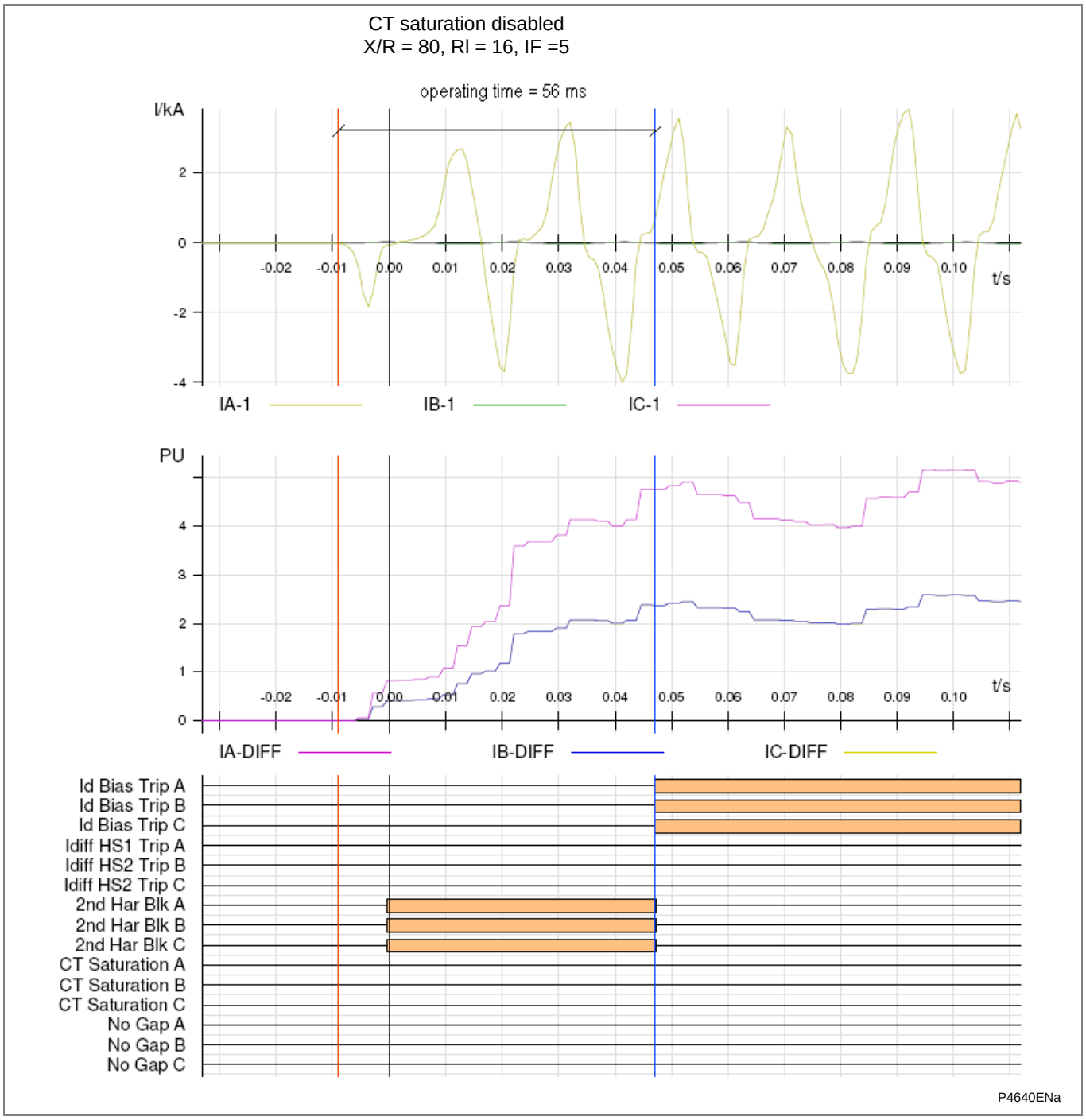


Figure 17 - CT saturation and no gap detection disabled

The following two diagrams shows the same AN internal fault.

- The “CT saturation and no gap detection enabled” diagram shows the disturbance record from a P64x with CT saturation and No gap detection enabled, the operating time of the low set differential element is 28 ms. It can be observed that both the CT saturation logic and the no gap detection logic are asserted. The CT saturation and No gap detection logics complement each other.
- The “CT saturation and no gap detection disabled” diagram shows the disturbance record from a P64x with CT saturation and No gap detection disabled. The operating time is 57 ms. The P64x is 29 ms faster if the CT saturation and No gap detection is enabled.

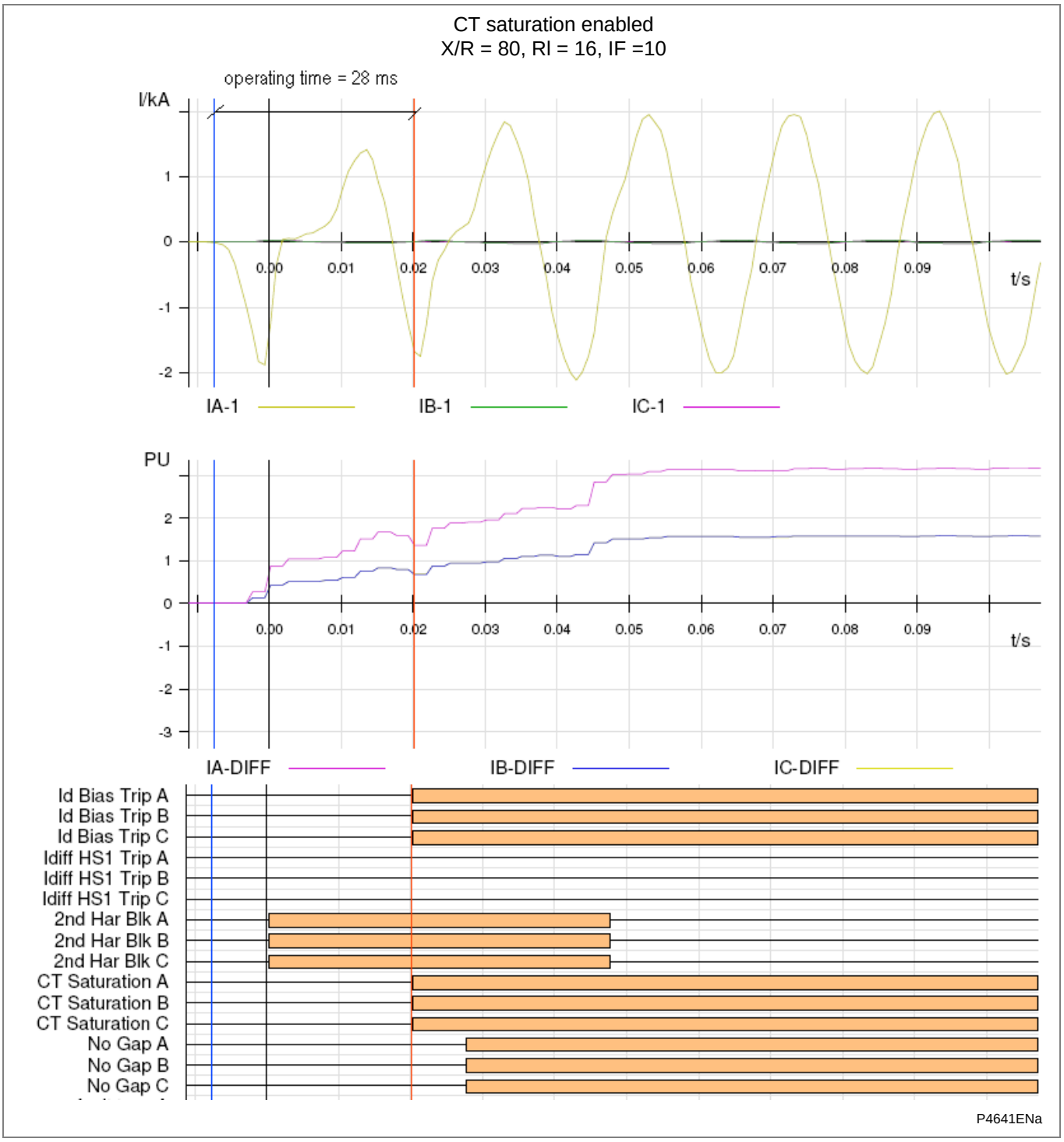


Figure 18 - CT saturation and no gap detection enabled

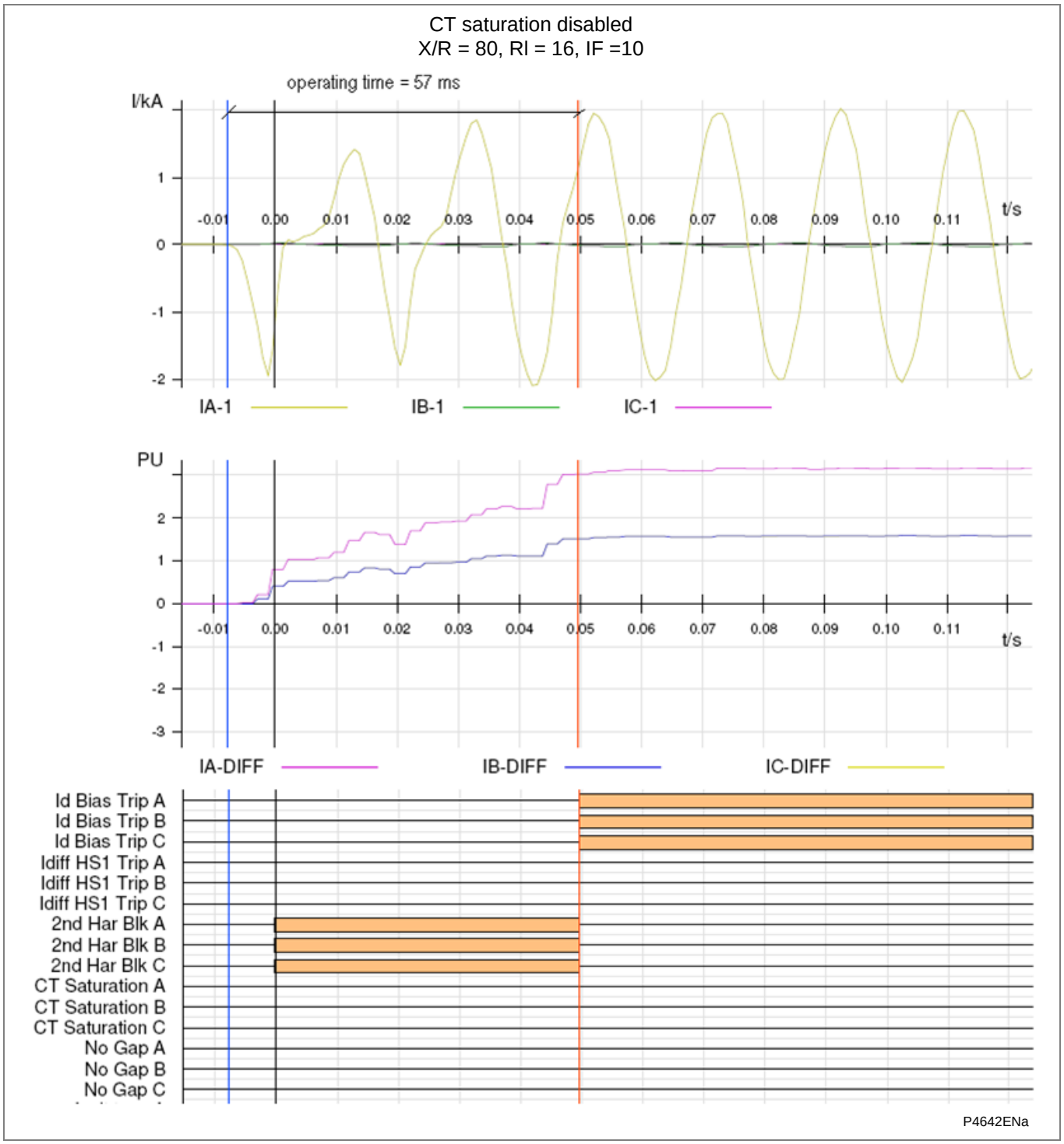


Figure 19 - CT saturation and no gap detection disabled

2.1.7 High Set Operation

The relay incorporates independent differential high set elements, Is-HS1 and Is-HS2 to complement the protection provided by the biased differential low set element. The instantaneous high set offers faster clearance for heavy internal faults and it is not blocked for magnetizing inrush or transient overfluxing conditions.

Stability is provided for heavy external faults, but the operating threshold of the high set differential element must be set to avoid operation with inrush current.

When a transformer is energized, a high magnetizing inrush current is drawn. The magnitude and duration of this inrush current depends on several factors including:

- Size and impedance of the transformer
- Point on wave of switching
- Remnant flux in the transformer
- Number of transformers connected in parallel

It is difficult to accurately predict the maximum anticipated level of inrush current. Typical waveform peak values are of the order of 8x to 30x rated current. A worst-case estimation of inrush could be made by dividing the transformer full load current by the per-unit leakage reactance quoted by the transformer manufacturer. In the simple mode, the relay calculates the setting for Is-HS1 as the reciprocal of the transformer reactance.

A setting range of 2.5 to 32 pu is provided on the P64x relay for Is-HS1 and Is-HS2. Both elements should be set in excess of the anticipated or estimated peak value of inrush current after ratio correction.

The Is-HS2 element uses the fundamental component of the differential current. This element is not restrained by the bias characteristic, so the P64x will trip regardless of the restraining current. Is-HS2 should be set so that the relay will not maloperate during external faults. When through fault current is limited by the transformer impedance, Is-HS2 can be set as $1.3 \times (1/X_t)$. In breaker and a half, ring bus or mesh applications, the through fault current is not limited by the transformer impedance but by the system source impedance. This current can be higher than $1.3 \times (1/X_t)$, therefore the user should consider the actual through fault current when setting Is-HS2. To avoid high values of spurious differential current due to CT saturation during through fault conditions, it is important to equalize the burden on the CT secondary circuits.

2.1.8 Setting Guidelines for Transformer Biased Differential Protection

The differential setting, **Configuration/Diff Protection**, should be set to **Enable**.

The basic pick up level of the low set differential element, Is1, is variable between 0.1 pu and 2.5 pu in 0.01 pu steps. The setting chosen is dependant on the item of plant being protected and by the amount of differential current that might be seen during normal operating conditions. When the P64x is used to protect a transformer, a setting of 0.2 In is generally recommended.

When protecting generators and other items of plant, where shunt magnetizing current is not present, a lower differential setting can be used and 0.1 pu would be more typical.

The biased low-set differential protection is blocked under magnetizing inrush conditions and during transient over fluxing conditions if the appropriate settings are enabled. The second harmonic measurement and blocking are phase segregated. If cross blocking is set to enabled, phases A, B and C of the low set differential element are blocked when an inrush condition is detected. The fifth harmonic measurement and blocking are also phase segregated, but no cross blocking is available.

As shown in the “Tap changer and CT combined errors” diagram below, the first slope is flat and depends on the Is1 setting. It ensures sensitivity to internal faults. The second slope, K1, is user settable. K1 ensures sensitivity to internal faults up to full load current. It allows for the 15% mismatch which can occur at the limit of the transformer’s tap-changer range and an additional 5% for any CT ratio errors. The K1 slope should be set above the errors due to CT mismatch, load tap changers and steady state magnetizing current. The errors slope, which is the combined tap changer (T/C) and current transformer (CT) error, should always be below the K1 slope to avoid mal operations. It is recommended to set K1 to 30%, as long as the errors slope is below the K1 slope by a suitable margin. The second slope, K2, is also user settable, and it is used for bias currents above the rated current. To ensure stability under heavy through fault conditions, which could lead to increased differential current due to asymmetric saturation of CTs, K2 is **recommended to be** set to 80%.

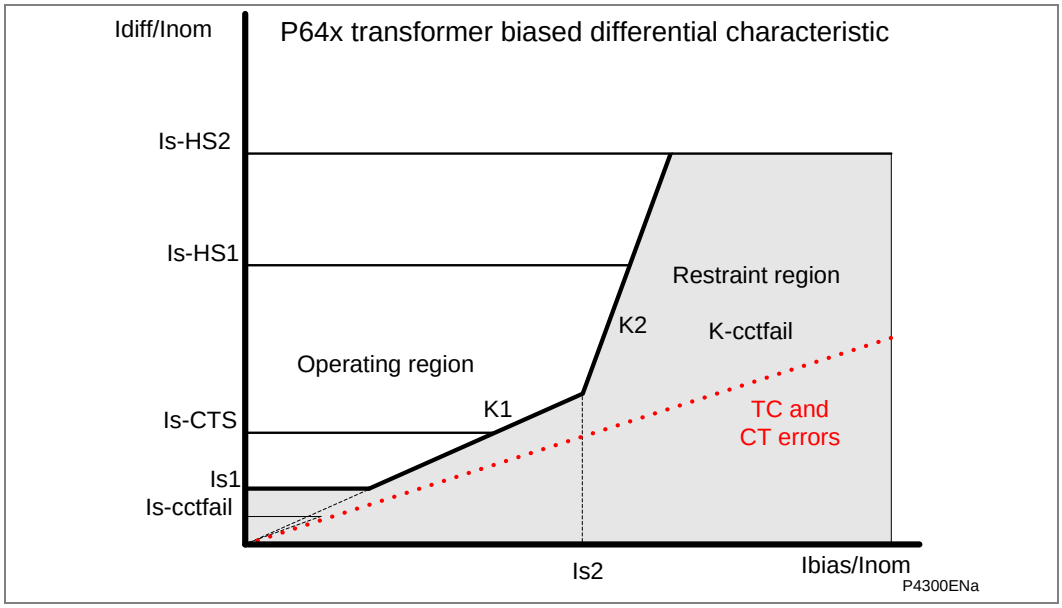


Figure 20 - Tap changer and CT combined errors

2.1.8.1 Example 1: Two Winding Transformer (P642) - no Tap Changer

The following diagram shows the application of P642 to protect a two winding transformer. The power transformer data has been given: 90 MVA Transformer, Ynd9, 132/33 kV. The current transformer ratios are as follows: HV CT ratio - 400/1, LV CT ratio - 2000/1.

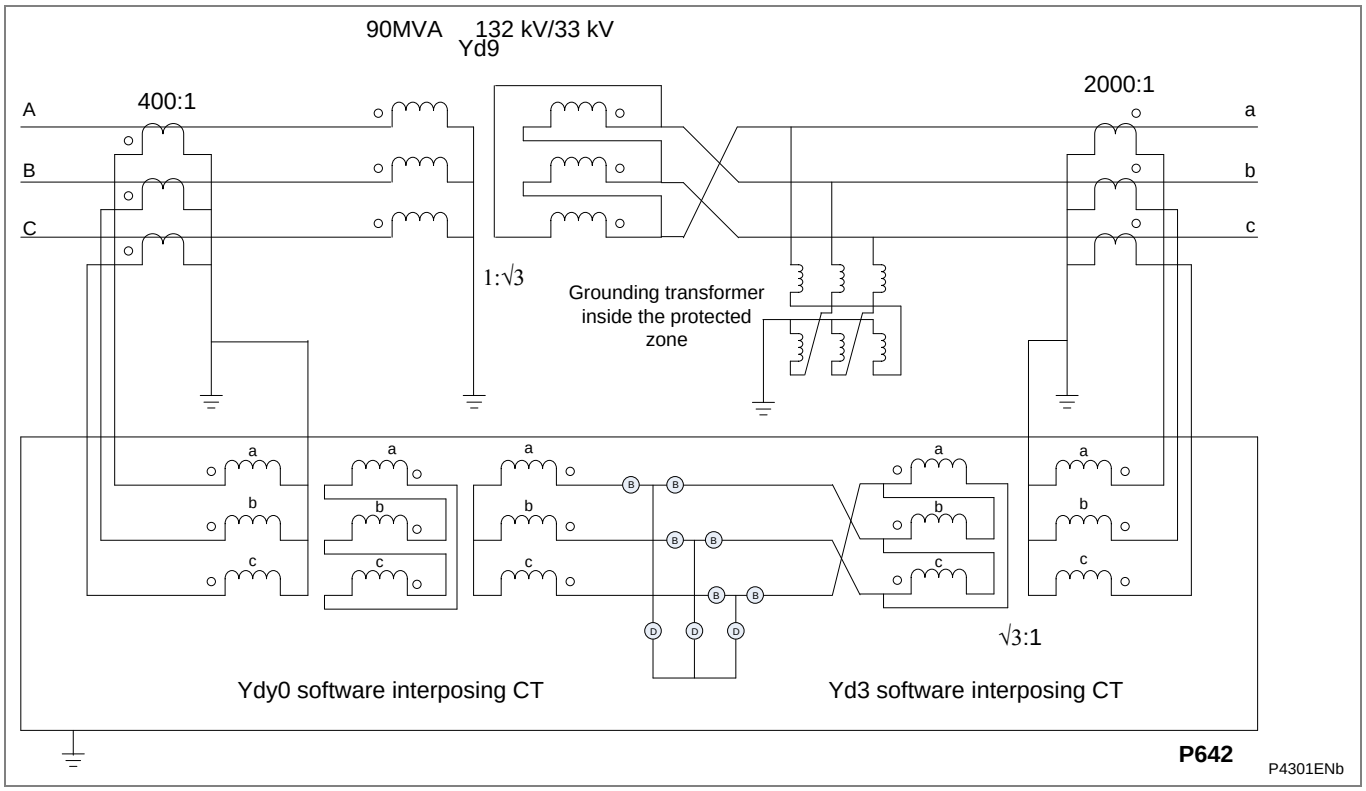


Figure 21 - P642 used to protect a two winding transformer

The relay always calculates and sets the amplitude matching factors. As explained previously no vector correction is applied to the high voltage side. Vector correction is done by setting **SYSTEM CONFIG** then **LV Vector Group** to **9**. The zero sequence filtering is done by setting **SYSTEM CONFIG** then **HV Grounding** to **Grounded** and **SYSTEM CONFIG** then **LV Grounding** to **Grounded**. The following screenshot shows the SYSTEM CONFIG settings for the P642.

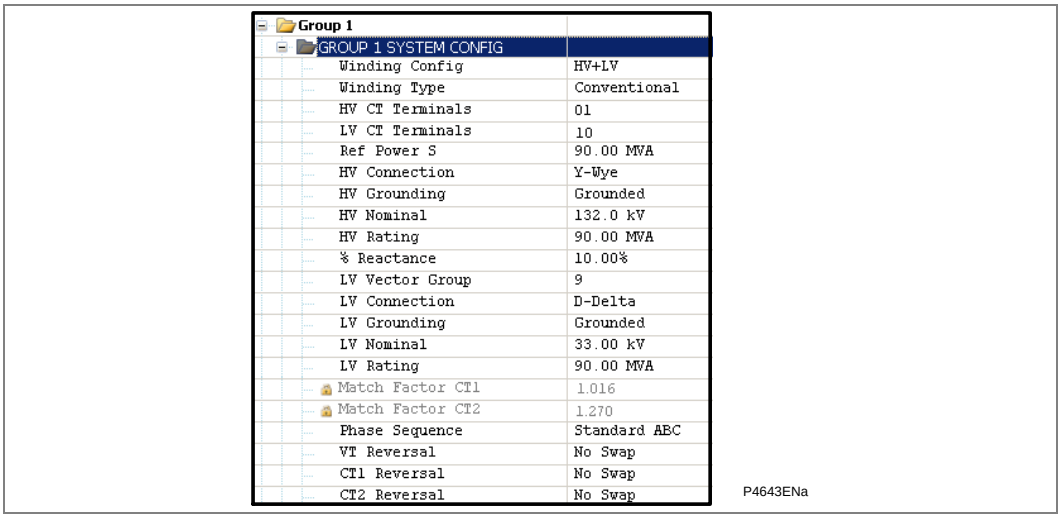


Figure 22 - P642 System Config settings

The ratio correction factors are calculated by the relay as follows:

$$K_{amp,T1CT} = \frac{I_{nom,T1CT}}{\frac{S_{ref}}{\sqrt{3}V_{nom,HV}}} = \frac{400}{\frac{90 \times 10^6}{\sqrt{3} \times 132 \times 10^3}} = 1.016$$

$$K_{amp,T2CT} = \frac{I_{nom,T2CT}}{\frac{S_{ref}}{\sqrt{3}V_{nom,LV}}} = \frac{2000}{\frac{90 \times 10^6}{\sqrt{3} \times 33 \times 10^3}} = 1.270$$

Where:

S_{ref}: common reference power for all ends

$K_{am,\ T1CT,\ T2CT}$: ratio correction factor of T1 CT or T2 CT windings

$I_{nom,\ T1CT,\ T2CT}$: primary nominal currents of the main current transformers

$V_{nom,\ HV,LV}$: primary nominal voltage of HV or LV windings

The recommended settings for the differential function (Is1, Is2, K1, K2, second and fifth harmonic blocking) were discussed in previous sections. See the P642 Diff Protection Settings diagram shown below.

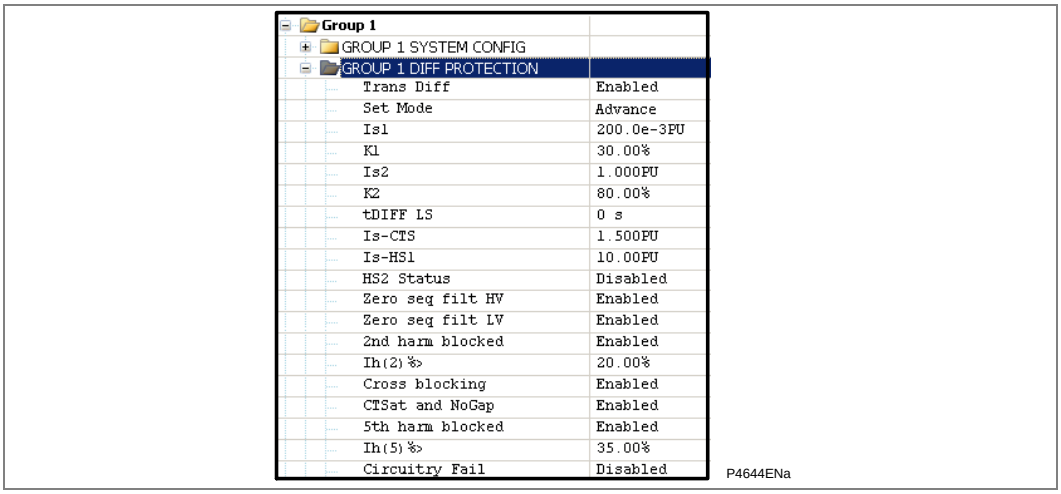


Figure 23 - P642 Diff Protection settings

2.1.8.2 Example 2: Autotransformer (P645) - Load Tap Changer

The following diagram shows the application of a P645 to protect an autotransformer.

The power transformer data has been given: 175/175/30 MVA Autotransformer, YNyn0d1, 230/115/13.8 kV.

The current transformer ratios are as follows: HV CT ratio - 800/5, LV CT ratio - 1200/5 and TV CT ratio 2000/5.

Since the transformer has an on load tap changer on the HV side, the nominal voltage of the HV winding must be set to the mid tap voltage level. According to the nameplate data, the mid tap voltage is 218.5 kV. The mid tap voltage can also be calculated as follows:

$$\text{Mid tap position} = \frac{100 + \frac{(5 - 15)}{2}}{100} \times 230 = 218.5kV$$

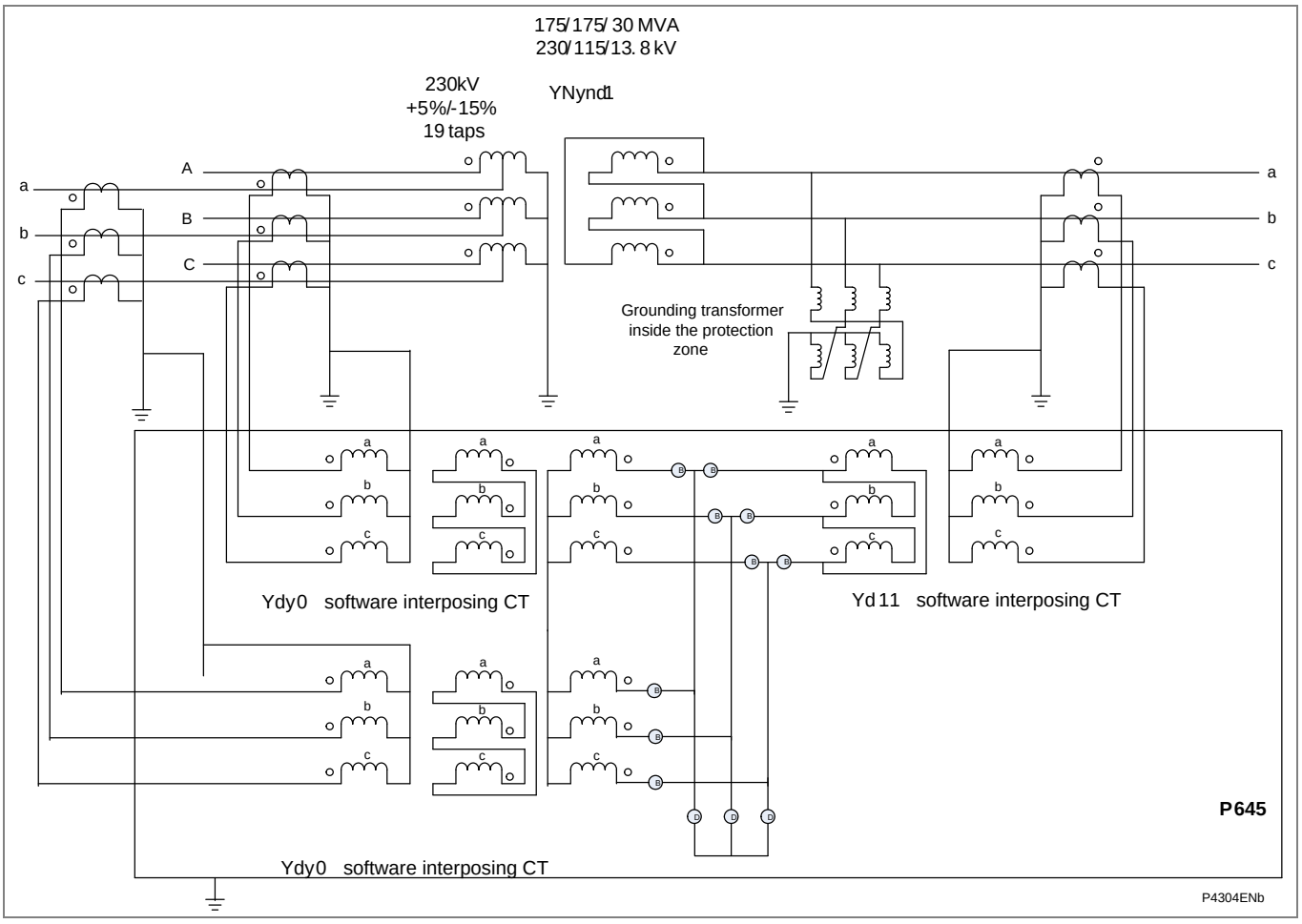


Figure 24 - P645 used to protect an autotransformer with load tap changer

Ratio Correction:

The relay calculates the ratio correction factors as follows:

$$K_{amp,T1CT} = \frac{I_{nom,T1CT}}{\frac{S_{ref}}{\sqrt{3}V_{nom,HV}}} = \frac{800}{\frac{175\times10^6}{\sqrt{3}\times218.5\times10^3}} = 1.730$$

$$K_{amp,T5CT} = \frac{I_{nom,T5CT}}{\frac{S_{ref}}{\sqrt{3}V_{nom,LV}}} = \frac{1200}{\frac{175\times10^6}{\sqrt{3}\times115\times10^3}} = 1.366$$

$$K_{amp,T3CT} = \frac{I_{nom,T3CT}}{\frac{S_{ref}}{\sqrt{3}V_{nom,TV}}} = \frac{2000}{\frac{175\times10^6}{\sqrt{3}\times13.8\times10^3}} = 0.273$$

To check that the differential protection does not misoperate due to errors introduced by the on load tap changer, the user may perform the following calculations.

Transformer Nominal Rating

Calculate HV full load current at both tap extremities and LV and TV full load current.

$$\text{HV full load current on tap 1 (5\%)} = \frac{175\times10^6}{\sqrt{3}\times241500} = 418.37A \quad \text{primary}$$

$$\text{HV full load current on tap 1 (5\%)} = \frac{418.37}{160} = 2.615A \quad \text{secondary}$$

$$\text{HV corrected current on tap 1} = 1.730\times2.615 = 4.524A \quad \text{secondary}$$

$$\text{HV full load current on tap 19 (-15\%)} = \frac{175\times10^6}{\sqrt{3}\times195.510^3} = 516.810A \quad \text{primary}$$

$$\text{HV full load current on tap 19 (-15\%)} = \frac{516.810}{160} = 3.230A \quad \text{secondary}$$

$$\text{HV corrected current on tap 19} = 1.730\times3.230 = 5.588A \quad \text{secondary}$$

$$\text{LV full load current} = \frac{145\times10^6}{\sqrt{3}\times115\times10^3} = 727.963A \quad \text{primary}$$

$$\text{LV full load current} = \frac{727.963}{240} = 3.033A \quad \text{secondary}$$

$$\text{TV full load current} = \frac{30\times10^6}{\sqrt{3}\times13.8\times10^3} = 1255.109A \quad \text{primary}$$

$$\text{TV full load current} = \frac{1255.109}{400} = 3.138A \quad \text{secondary}$$

Determine Idiff at both tap extremities (with mid tap correction).

$$\text{LV corrected current} = 1.366 \times 3.033 = 4.143$$

$$\text{TV corrected current} = 0.273 \times 3.138 = 0.857$$

$$\text{Idiff at tap } 1 = \left|4.524 - 4.143 - 0.857\right| = 0.476A = \frac{0.476}{5} = 0.095pu$$

$$\text{Idiff at tap } 19 = \left|5.588 - 4.143 - 0.857\right| = 0.588A = \frac{0.588}{5} = 0.118pu$$

Determine Ibias at both tap extremities (with mid tap correction). The currents used in the Ibias calculation are the currents after ratio and vector correction.

$$\text{Ibias at tap } 1 = \frac{4.524 + 4.143 + 0.857}{2} = 4.762A = \frac{4.762}{5} = 0.9524pu$$

$$\text{Ibias at tap } 19 = \frac{5.588 + 4.143 + 0.857}{2} = 5.294A = \frac{5.294}{5} = 1.059pu$$

Determine relay differential current.

Iop = Is1, (Ibias $\leq$ Is1/K1)

Iop = K1$\times$ Ibias, (Is1/K1 $\leq$ Ibias $\leq$ Is2)

Iop = K1 $\times$ Is2 + K2 $\times$ (Ibias - Is2), (Ibias $\geq$ Is2)

Ibias at tap 1 is less than 5 A (1 pu) and greater than 3.33 A (0.667 pu); since Is_2 is set to the rated current (5 A), Iop is calculated as follows:

Iop = 0.3 $\times$ 4.762 = 1.429 A

Ibias at tap 19 is greater than 5 A; since Is_2 is set to the rated current (5 A), Iop is calculated as follows:

Is2 = 1 pu = 1 $\times$ 5 = 5 A

Iop = 0.3 $\times$ 5 + 0.8 $\times$ (5.294 - 5) = 1.735 A

Check Idiff < Iop by a 10% margin for each tap extremity and adjust Is1 and/or K1 as necessary.

Tap 1: Since Idiff = 0.476A and 0.9Iop at tap 1 = 0.9 x 1.429 = 1.286 A

Therefore there is sufficient safety margin with K1 = 30% and Is1 = 0.2 pu.

Tap 19: Since Idiff = 0.588A and 0.9Iop at tap 19 = 0.9 x 1.735 = 1.562 A

Therefore there is sufficient safety margin with K1 = 30% and Is1 = 0.2 pu.

66.7% of transformer nominal rating

Calculate HV, LV and TV load current at 66.7% of the nominal MVA rating.
The 66.7% is the interception between Is1 and K1.
It is determined as Is1/K1 × 100% = (0.2/0.3) × 100 = 66.7%.

$$\text{HV full load current on tap 1(5\%)} = 0.667 \times \frac{175 \times 10^6}{\sqrt{3} \times 241500} = 279.05A \quad \text{primary}$$

$$\text{HV full load current on tap 1(5\%)} = \frac{279.05}{160} = 1.744A \quad \text{secondary}$$

$$\text{HV corrected current on tap 1} = 1.730 \times 1.744 = 3.017\,A \quad \text{sec}\,ondary$$

$$\text{HV full load current on tap19 (-15\%)} = 0.667 \times \frac{175 \times 10^6}{\sqrt{3} \times 195.510^3} = 344.71A \quad \text{primary}$$

$$\text{HV full load current on tap 19 (-15\%)} = \frac{344.71}{160} = 2.154A \quad \text{secondary}$$

$$\text{HV corrected current on tap 19} = 1.730 \times 2.154 = 3.727A \quad \text{sec}\,ondary$$

$$\text{LV full load current} = 0.667 \times \frac{145 \times 10^6}{\sqrt{3} \times 115 \times 10^3} = 485.551A \quad \text{primary}$$

$$\text{LV full load current} = \frac{485.551}{240} = 2.023A \quad \text{secondary}$$

$$\text{TV full load current} = 0.667 \times \frac{30 \times 10^6}{\sqrt{3} \times 13.8 \times 10^3} = 837.158A \quad \text{primary}$$

$$\text{TV full load current} = \frac{837.158}{400} = 2.093A \quad \text{secondary}$$

Determine Idiff at both tap extremities (with mid tap correction).

$$\text{LV corrected current} = 1.366 \times 2.023 = 2.763A$$

$$\text{TV corrected current} = 0.273 \times 2.093 = 0.571A$$

$$\text{Idiff at tap 1} = |3.017 - 2.763 - 0.571| = 0.317A = \frac{0.317}{5} = 0.063pu$$

$$\text{Idiff at tap 19} = |3.727 - 2.763 - 0.571| = 0.393A = \frac{0.393}{5} = 0.0786pu$$

Determine Ibias at both tap extremities (with mid tap correction). The currents used in Ibias calculation are the currents after ratio and vector correction.

$$\text{Ibias at tap 1} = \frac{3.017 + 2.763 + 0.571}{2} = 3.176A = \frac{3.176}{5} = 0.635pu$$

$$\text{Ibias at tap 19} = \frac{3.727 + 2.763 + 0.571}{2} = 3.531A = \frac{3.531}{5} = 0.706pu$$

Determine relay differential current.

Iop = Is1, (Is1/K1 ≤ Ibias)

Iop = K1× Ibias, (Is1/K1 ≤ Ibias ≤ Is2)

Iop = K1 × Is2 + K2 × (Ibias - Is2), (Ibias ≥ Is2)

Ibias at tap 1 is less than 3.33 A (0.667 pu); then Iop = 0.2 pu = 1 A

Ibias at tap 1 is less than 5 A (1 pu) and greater than 3.33 A (0.667 pu); since Is_2 is set to the rated current (5 A), Iop is calculated as follows:

Iop = 0.3 × 3.531 = 1.059 A

Check Idiff < Iop by a 10% margin for each tap extremity and adjust Is1 and/or K1 as necessary:

Tap 1: Since Idiff = 0.317 A and 0.9Iop at tap 1 = 0.9 x 1 = 0.9 A

Therefore there is sufficient safety margin with K1 = 30% and Is1 = 0.2 pu.

Tap 19: Since Idiff = 0.393 A and 0.9Iop at tap 19 = 0.9 x 1.059 = 0.953 A

Therefore there is sufficient safety margin with K1 = 30% Is1 = 0.2 pu.

The following diagram shows the bias characteristic, the CT and tap changer errors (assumed as 20%), and the bias, differential coordinates corresponding to full load current and 66.7% of full load current. It can also be seen that it is necessary to check the safety margin at the two knee-points of the bias characteristic.

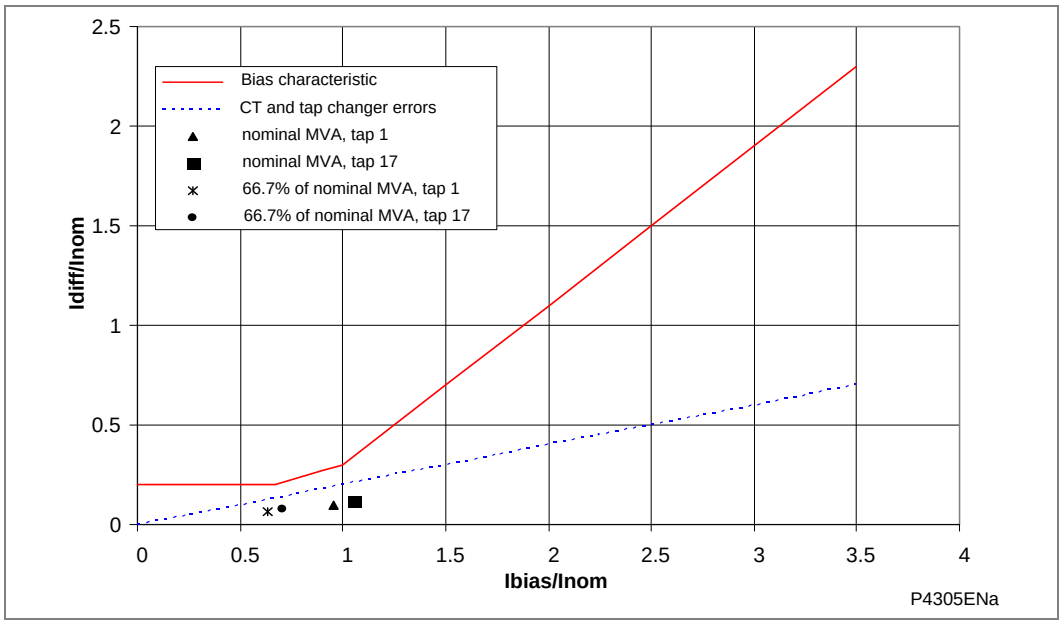


Figure 25 - Safety margin at the two knee-points of the bias characteristic

Vector correction and zero sequence filtering

Vector correction is done by setting **LV Vector Group** in **SYSTEM CONFIG** to **0** and **TV Vector Group** in **SYSTEM CONFIG** to **1**. The zero sequence filtering is done by setting **HV Grounding**, **LV Grounding** and **TV Grounding** in **SYSTEM CONFIG** to **Grounded**. The TV winding is grounded using a grounding transformer inside the protected zone.

The system configuration and differential protection settings are shown in the following diagram:

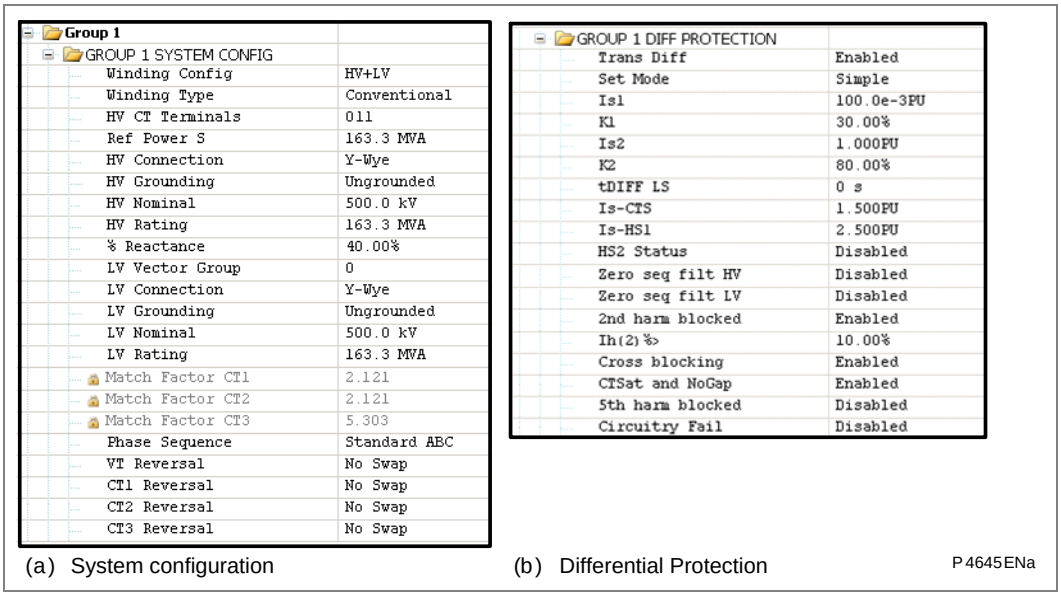


Figure 26 - P645 System Config (a) and Diff Protection settings (b) - Autotransformer

2.1.8.3 Example 3: Autotransformer (P643) - Delta Not Connected

The following diagram shows the application of a P645 to protect an autotransformer. The power transformer data has been given: 175/175/30 MVA Autotransformer, YNyn0d1, 230/115/13.8 kV. The delta winding is not loaded. The current transformer ratios are as follows: HV CT ratio - 1200/5, LV CT ratio - 1200/5, CTs in each phase at the neutral end of the winding 1200/5.

The winding configuration is set to HV + LV + TV. The CT on the HV line side is connected to T1 CT, the CT on the HV neutral side is connected to T2 CT, and the CT on the LV side is connected to T3 CT.

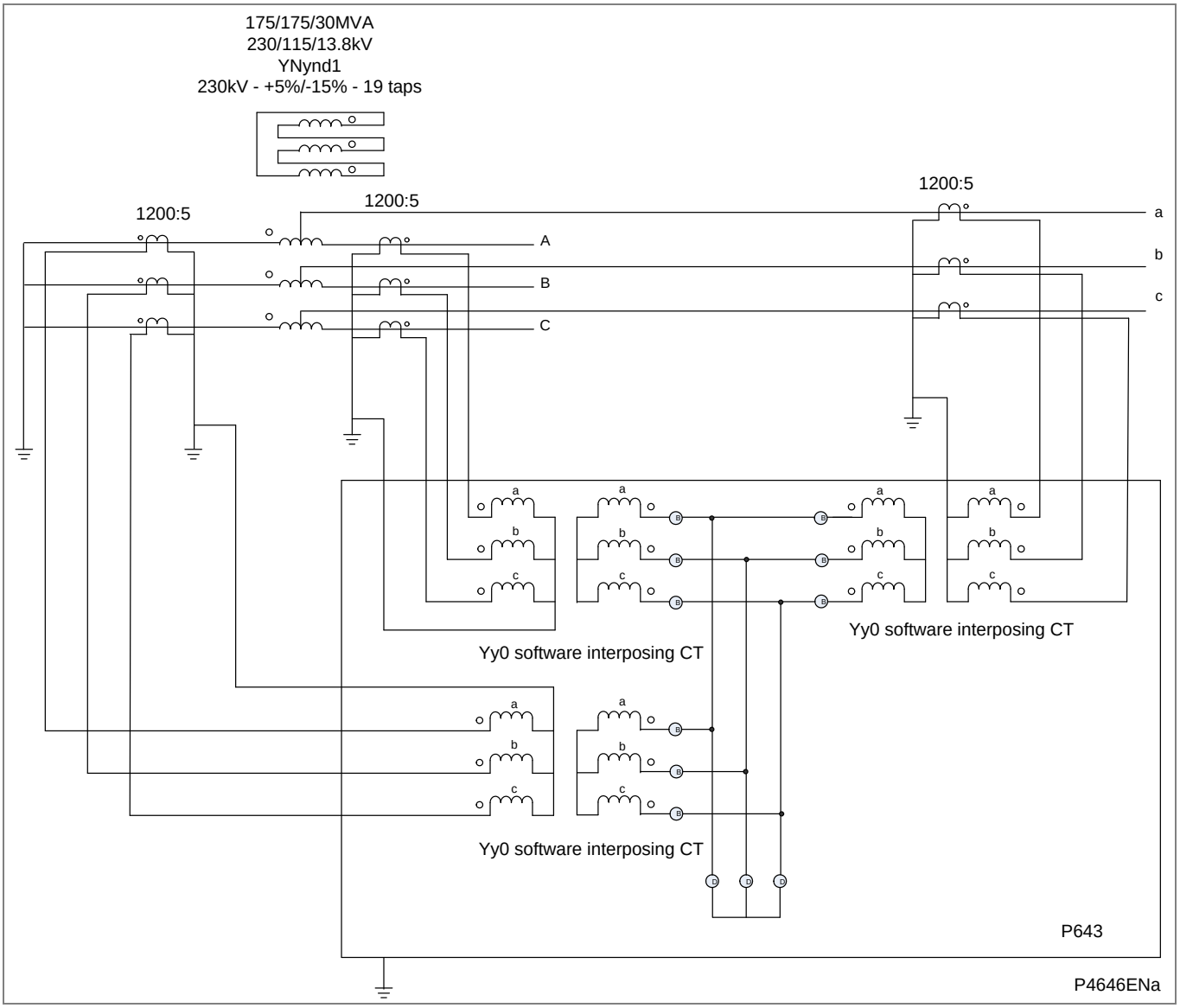


Figure 27 - P643 used to protect an autotransformer - delta not connected

Ratio Correction:

It is preferred that the ratio correction factors are close or equal to 1. In this example, it is possible to achieve ratio correction factors equal to 1 because current transformers are available in each phase at the neutral end and all the current transformer ratios are the same. This configuration is studied applying Kirchoff's current law. Consider that full load current is flowing and that an equivalent source is connected to the HV winding and an equivalent load is connected to the LV winding. The current distribution is as follows:

$$I_{FLC\text{-}HV} = \frac{S}{\sqrt{3}\, V_{non,HV}} = \frac{175 \times 10^6}{\sqrt{3} \times 230 \times 10^3} = 439A$$

$$I_{FLC\text{-}LV} = \frac{S}{\sqrt{3}\, V_{non,LV}} = \frac{175 \times 10^6}{\sqrt{3} \times 115 \times 10^3} = 878A$$

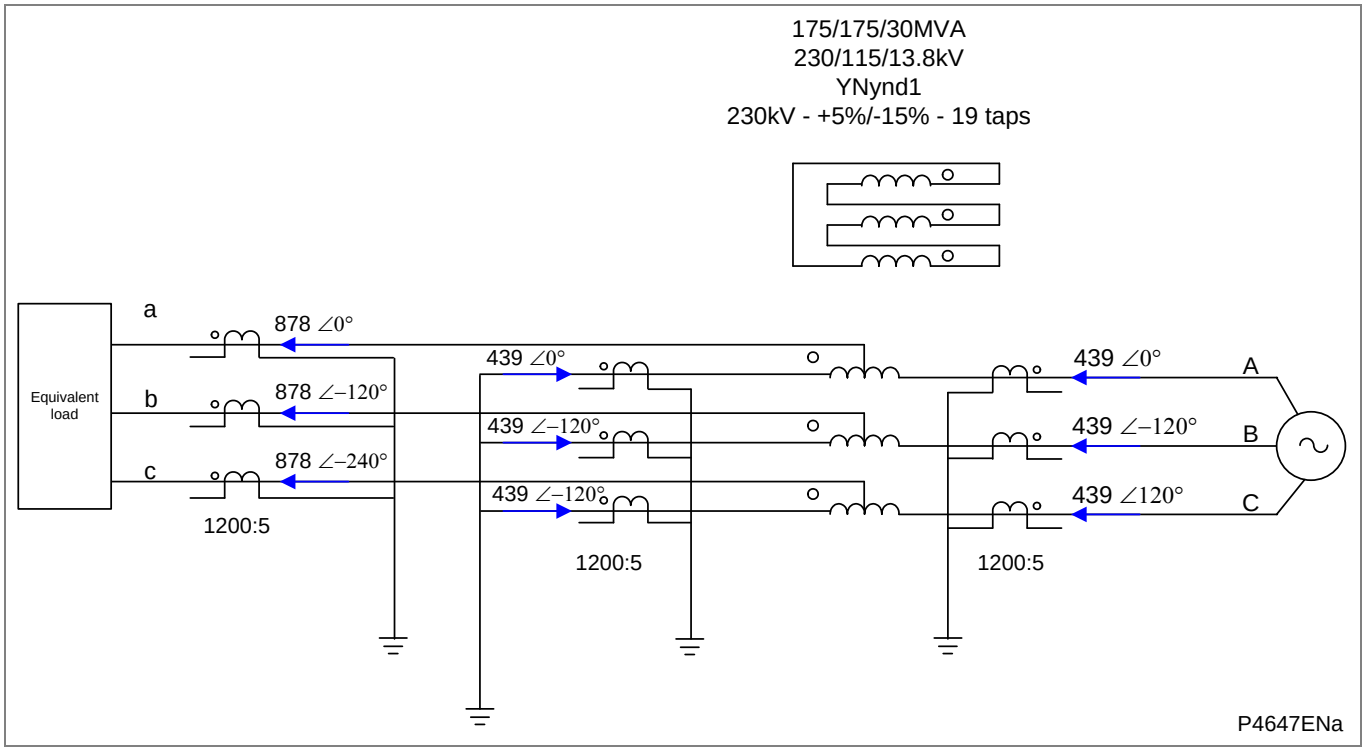


Figure 28 - P643 protect an autotransformer – delta not connected – current distribution

The reference power is set to 478 MVA and the nominal voltage in HV, LV and TV windings is set to 230 kV. Note that in this application, even though, there is an on-load tap changer on the HV side, it is not required to consider the mid-tap voltage. It is appropriate to set the reference power to a value other than the one given in the transformer nameplate data because the reference power is used to convert the currents to a common base.

The relay calculates the ratio correction factors as follows:

$$K_{amp,T1CT} = K_{amp,T2CT} = K_{amp,T3CT} = \frac{I_{nom,T1CT}}{\frac{S_{ref}}{\sqrt{3}V_{nom}}} = \frac{1200}{\frac{478 \times 10^6}{\sqrt{3} \times 230 \times 10^3}} = 1$$

Vector Correction and Zero Sequence Filtering

Vector correction is done by setting **LV Vector Group** in **SYSTEM CONFIG** to **0** and then **TV Vector Group** in **SYSTEM CONFIG** to 0. The zero sequence filtering is done by setting **HV Grounding**, **LV Grounding** and **TV Grounding** in **SYSTEM CONFIG** to **ungrounded**.

The system configuration and differential protection settings are shown in the following diagram:

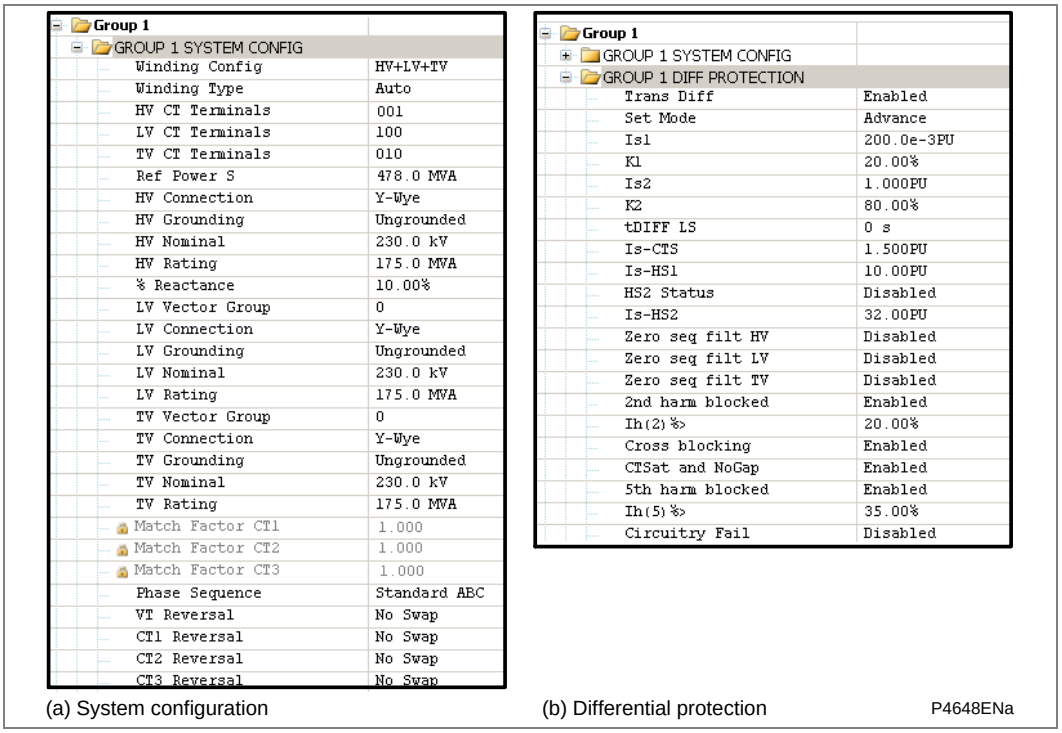


Figure 29 - P643 System Config (a) and Diff Protection settings (b) – Autotransformer

The differential element does not protect the tertiary winding. Unloaded delta-connected tertiary windings are often not protected. If protection is required, the delta winding can be earthed at one point through a current transformer used to provide instantaneous overcurrent protection for the tertiary winding.

2.1.9 Setting Guidelines for Short-Interconnector Biased Differential Protection

The P645 can be used to protect short interconnectors. Consider the five feeders - single bus scheme and its differential protection zone shown in the following diagram:

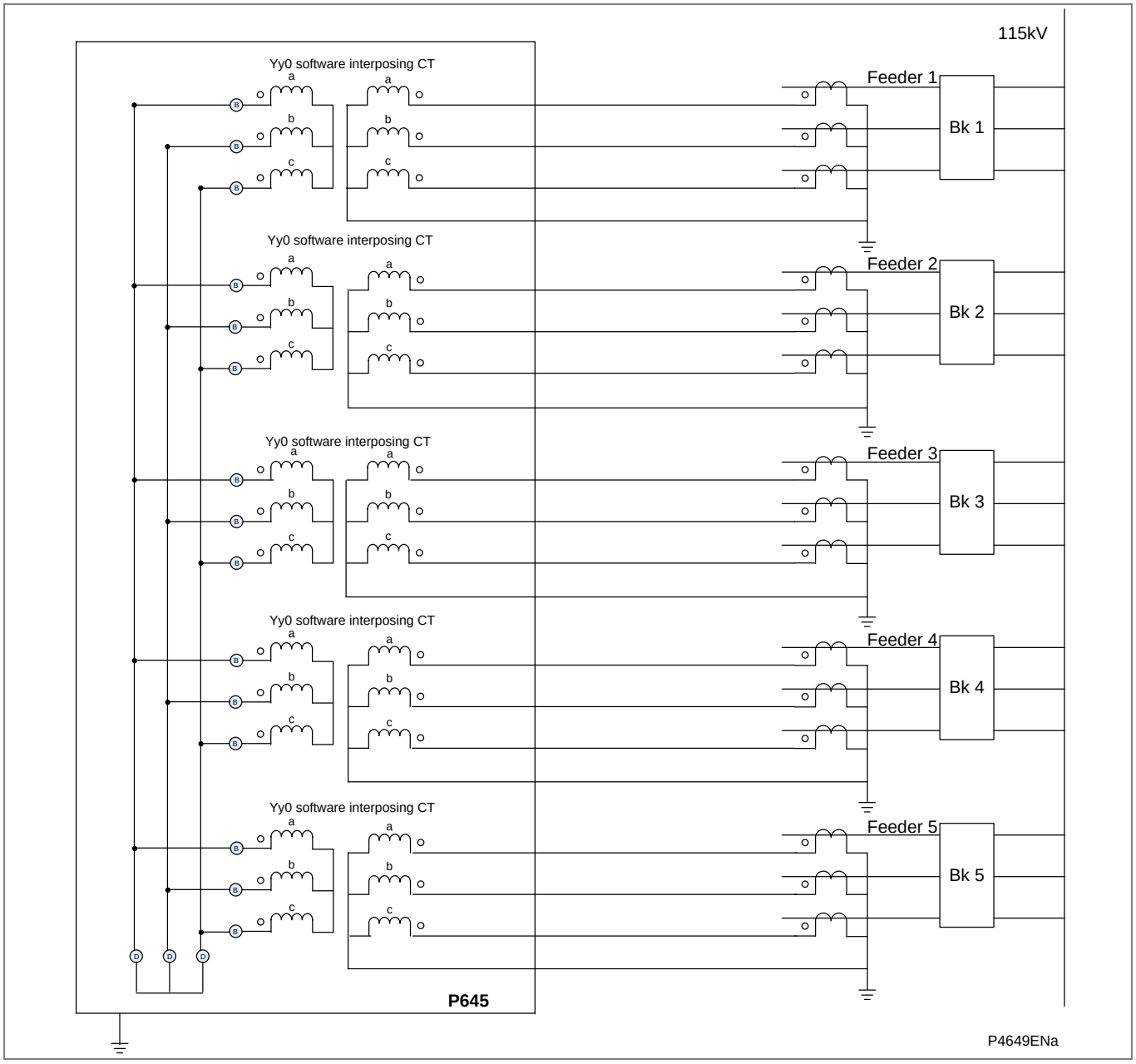


Figure 30 - Single bus differential protection zone

- Five biased current inputs are required. Consider that feeder 1 CT is connected to biased current input 1 (T1 CT), feeder 2 CT is connected to biased current input 2 (T2 CT), feeder 3 CT is connected to biased current input 3 (T3 CT), feeder 4 CT is connected to biased current input 4 (T4 CT), feeder 5 CT is connected to biased current input 5 (T5 CT).
- Set the Reference power **Ref Power S** equal to the maximum load (including overloads) in MVA that would be handled by the busbar.

- Set HV Connection, LV Connection and TV Connection as Y-Wye.
  Set HV Grounding, LV Grounding and TV Grounding as Ungrounded, so that the zero sequence filters are disabled.
- Set **HV Nominal**, **LV Nominal** and **TV Nominal** to the system voltage.
- Set **HV Rating**, **LV Rating** and **TV Rating** equal to the Reference power **Ref Power S**. This setting has no impact on the differential protection; it is used by other functions such as the thermal and through-fault monitoring elements which are not required for busbar protection.
- Set the LV Vector Group and TV Vector Group to 0.
- It is highly recommended that you use the following settings:
  - Is1 = 1.2pu
  - K1 = 20%
  - K2 = 80%
  - Is2 = 0.4pu
  - Is-HS1 = 10pu
  - Is-HS2 = disabled
  - 2nd harmonic blocked = disabled
  - 5th harmonic blocked = disabled
- Is1 should be set to $1.2 \times \text{highest load} \le \text{Is1} \le 0.8 \times \text{minimum fault level}$.
- Set the **Circuitry Fail** alarm to **Enabled**. Set **K-cctfail** to **15%** to allow the maximum composite error of 10% that may be introduced by class 10P current transformers. **Is-cctfail** is typically set between 5 to 20% to prevent detecting noise coming from the CTs and spurious differential current that may be caused by the maximum load unbalance. This element is typically delayed by 5 s.
- It is recommended to apply CT supervision to prevent maloperation of the biased differential protection when there is an open circuited CT secondary. The CTS feature can be used to desensitize the biased differential protection. Desensitization is achieved by raising the differential current pickup setting Is1 to the value of Is-CTS.

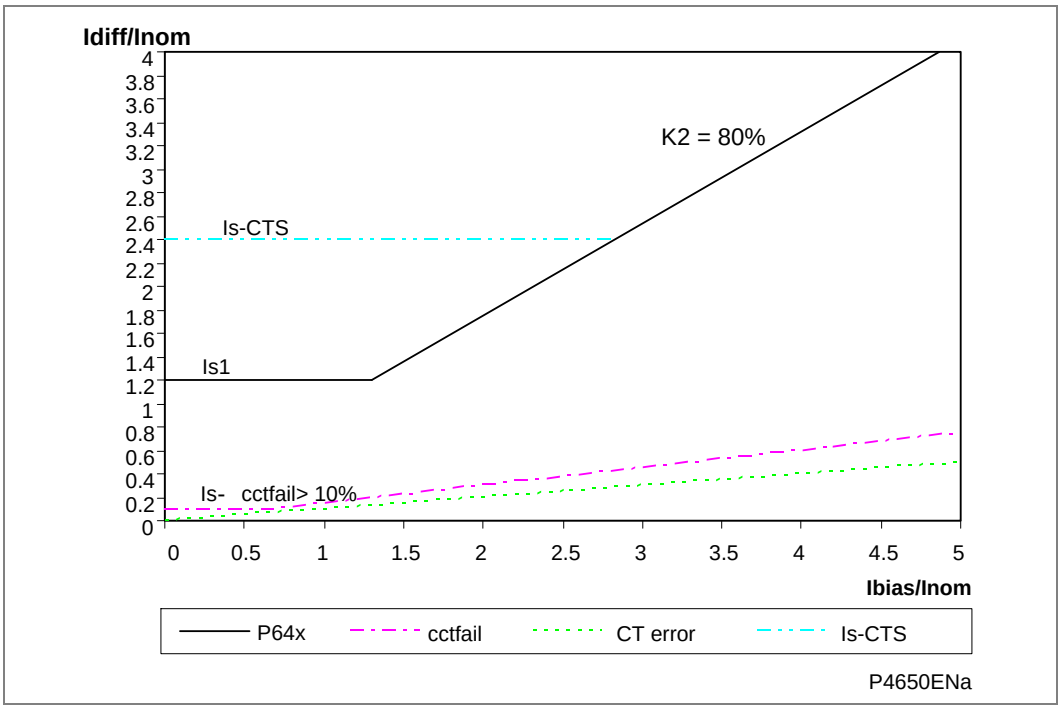


Figure 31 - Busbar biased differential protection

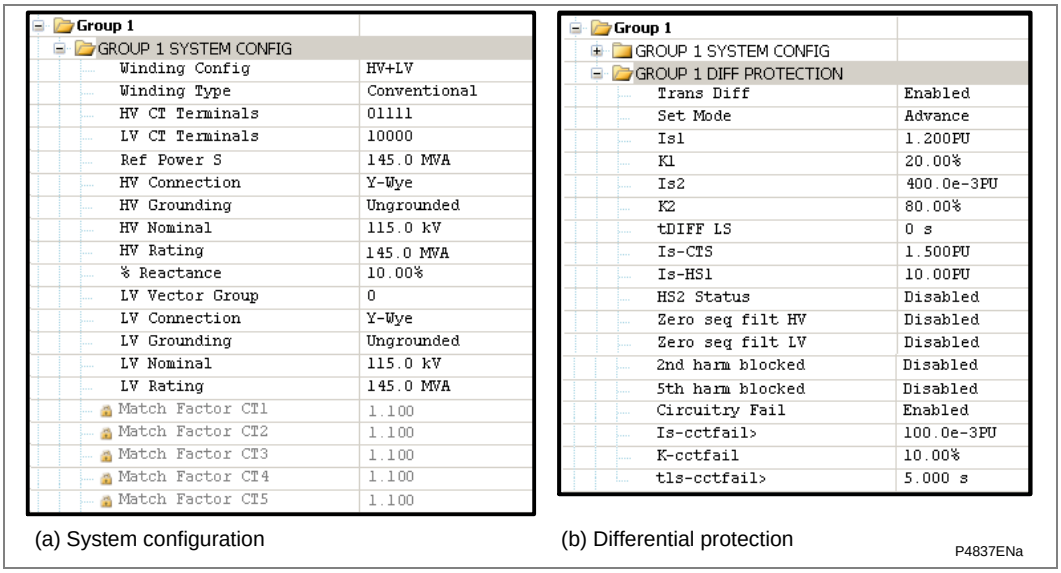


Figure 32 - P645 System Config (a) and Diff Protection settings (b) - Short Interconnector

2.1.10 Setting Guidelines for Short-Interconnector Biased Differential Protection

Reactors are commonly used in the power system:

- To reduce the fault current level in grounded neutrals
- To reduce the phase fault current level when the reactor is connected in series to a line.
- To compensate for the capacitive reactance of long transmission lines or cables when the reactor is connected in shunt. The shunt reactor absorbs the VARs generated by the line capacitive reactance as the power system generally cannot absorb it.

According to IEEE Std. C37.109-2006 one of the main difficulties with shunt reactor protection is that the relay may mal-operate during iron-core reactor energization and de-energization. A shunt reactor is typically switched in and out regularly depending on the power system load. The iron-core shunt reactor energization current contains dc offset with long time constant and low frequency components as shown in the “Reactor energization current” diagram shown below. These current waveforms cause a certain level of remanent flux in the CT magnetic core. During normal reactor operation the current is generally the nominal current which is not high enough to reduce the flux level in the CT. In the next switch in operation, the flux may either increase or decrease depending on the point on energization. The regular switch in and out of the reactor causes CT saturation; therefore, it is recommended that the current transformers on both sides of the reactor have similar excitation characteristics to reduce the risk of unwanted operations. A high impedance differential scheme is generally recommended over a low impedance differential scheme, because it is not affected by CT saturation.

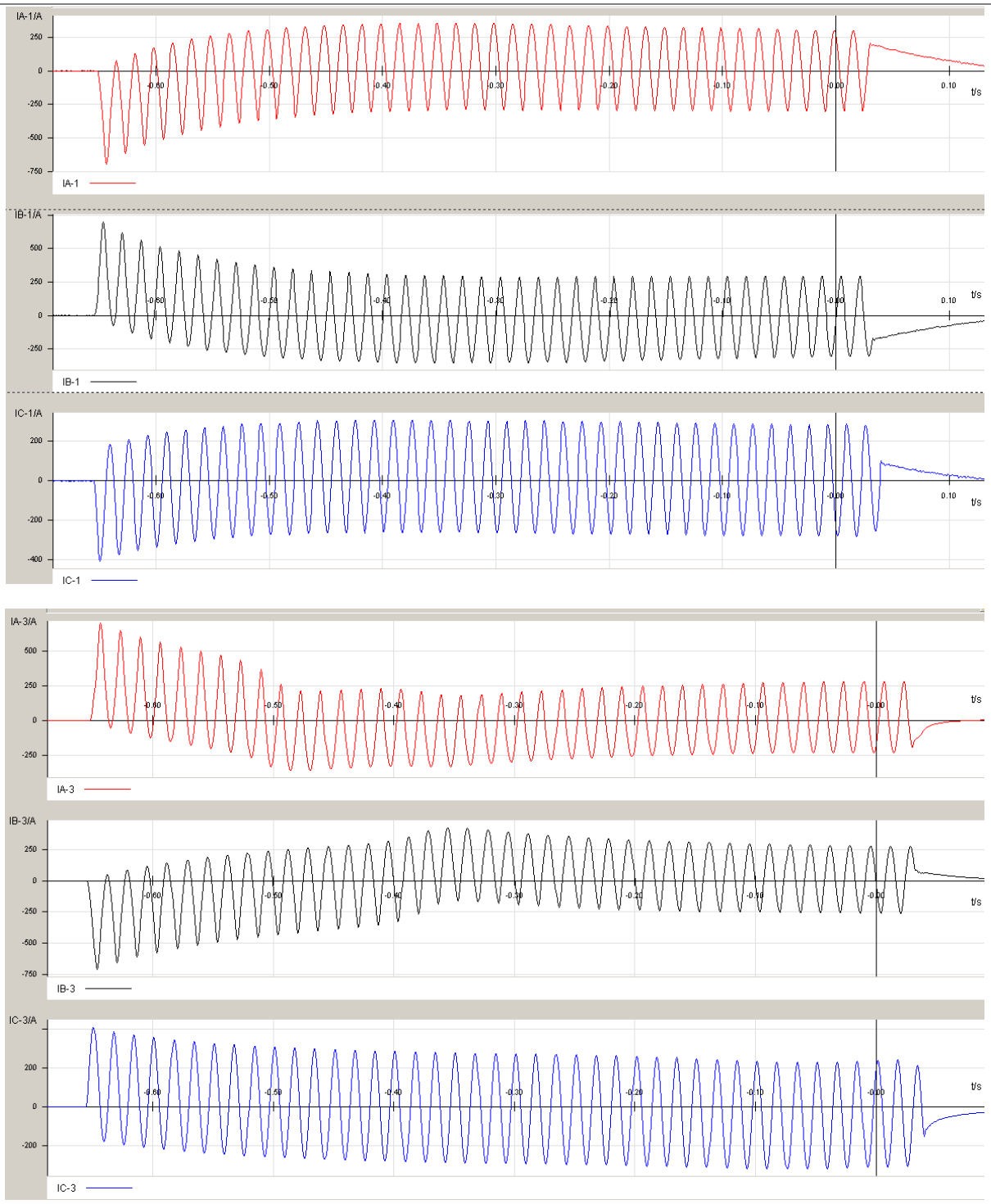


Figure 33 - Reactor energization current

As per the IEEE Std. C37.109-2006 the properties of shut reactors are summarized as:

- Dry air-air core type reactors: no magnetizing inrush during energization as there is no iron core. The peak current during energization might be as high as $2 \times \sqrt{2} \times I_{nominal}$ due to transient offset.
- Oil-immersed type reactors: the gapped iron-core type might experience severe energizing inrush. The coreless type experiences less severe magnetizing inrush.

2.1.10.1 Example 1: Shunt Reactor Differential Protection

Consider the shunt reactor shown in the “Reactor single line” diagram below:

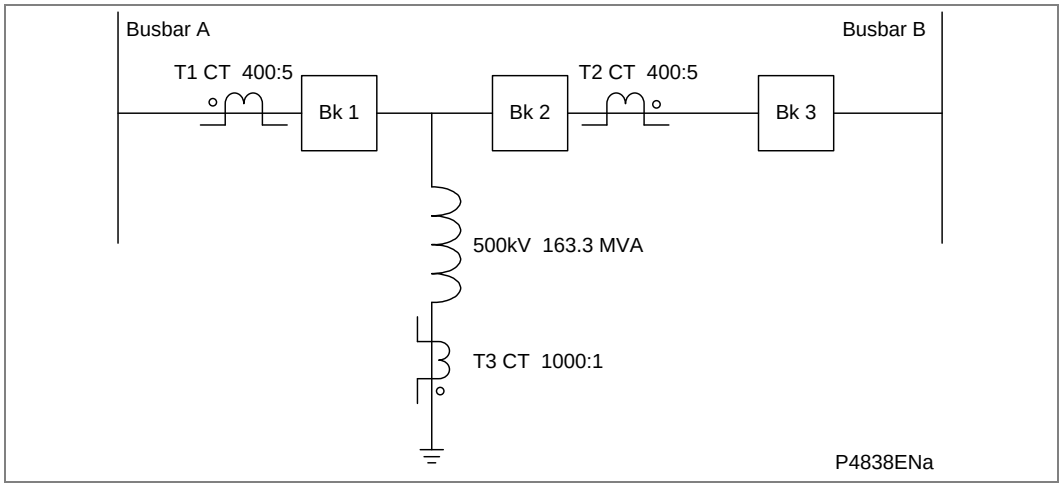
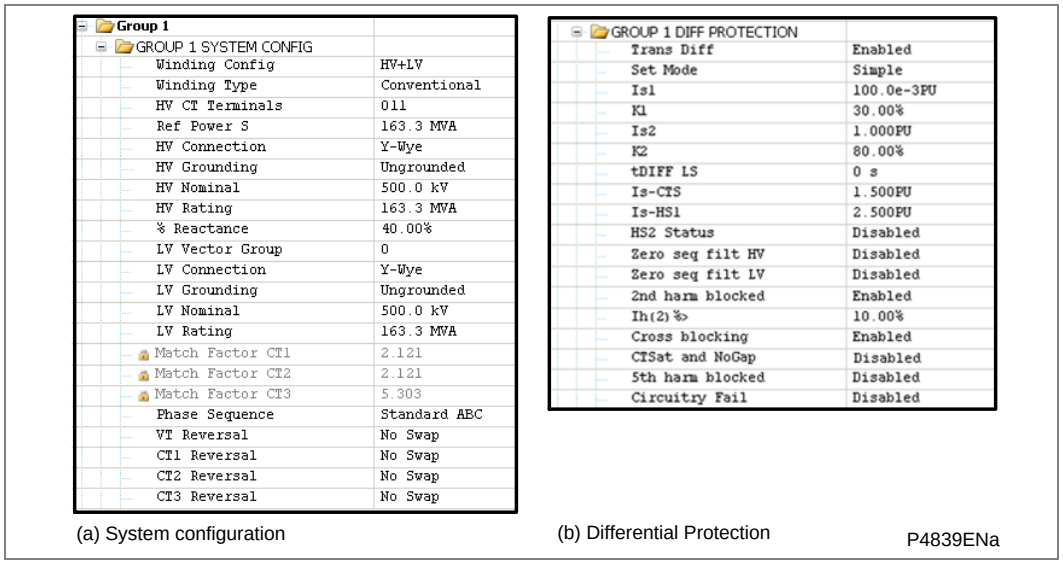


Figure 34 - Reactor single line diagram

The bias differential element in the P643 would be used to protect the reactor. In a reactor application the low set differential element, Is1, should be set between 10%-15%. The second harmonic blocking can be set as low as 10%. This is to enhance the relay stability during energization. The high set 1 differential element, Is-HS1, can be set to 250% of the reactor current at rated voltage.



Group 1	
GROUP 1 SYSTEM CONFIG	
Winding Config	HV+LV
Winding Type	Conventional
HV CT Terminals	011
Ref Power S	163.3 MVA
HV Connection	Y-Wye
HV Grounding	Ungrounded
HV Nominal	500.0 kV
HV Rating	163.3 MVA
% Reactance	40.00%
LV Vector Group	0
LV Connection	Y-Wye
LV Grounding	Ungrounded
LV Nominal	500.0 kV
LV Rating	163.3 MVA
Match Factor CT1	2.121
Match Factor CT2	2.121
Match Factor CT3	5.303
Phase Sequence	Standard ABC
VT Reversal	No Swap
CT1 Reversal	No Swap
CT2 Reversal	No Swap
CT3 Reversal	No Swap

(a) System configuration

GROUP 1 DIFF PROTECTION	
Trans Diff	Enabled
Set Mode	Simple
Is1	100.0e-3PU
K1	30.00%
Is2	1.000PU
K2	80.00%
tDIFF LS	0 s
Is-CTS	1.500PU
Is-HS1	2.500PU
HS2 Status	Disabled
Zero seq filt HV	Disabled
Zero seq filt LV	Disabled
2nd harm blocked	Enabled
Ih(2)%>	10.00%
Cross blocking	Enabled
CTSat and NoGap	Disabled
5th harm blocked	Disabled
Circuitry Fail	Disabled

(b) Differential Protection

Figure 35 - P643 system config (a) and diff protection settings (b) – Reactor

2.2 Possible Misindication of the Unfaulted Phases due to Fault Current Distribution

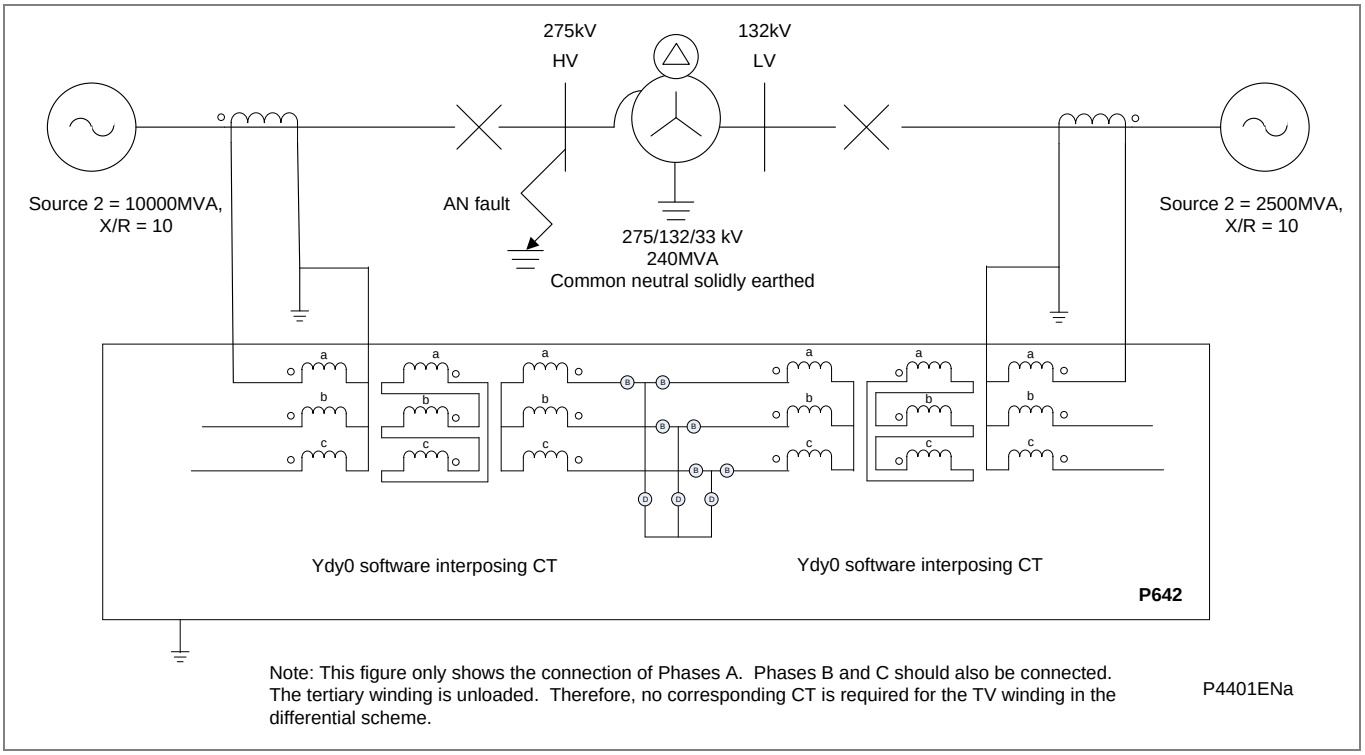


Figure 36 - AN fault in the HV side of an autotransformer

The positive, negative and zero sequence impedances of the transformer windings using 240 MVA as base are as follows:

	HV	LV	TV
Positive Sequence	j 0.134 pu	j 0.075 pu	-j 0.024 pu
Negative Sequence	j 0.134 pu	j 0.075 pu	-j 0.024 pu
Zero Sequence	j 0.067 pu	j 0.0375 pu	-j 0.012 pu

Table 4 - Positive, negative and zero sequence impedances of transformer windings

The X/R ratio determines the angle of the source impedances, so this angle is $\tan^{-1}(10) = 84^\circ$.

The magnitude of source 1 impedance is $1 \times \frac{240}{10000} = 0.024\text{pu}$.

The magnitude of source 2 impedance is $1 \times \frac{240}{2500} = 0.096\text{pu}$

Consider the internal AN fault on the HV side of the autotransformer shown in the above diagram. The disturbance record and events obtained from the relay indicate that the phase C also tripped, even though the fault was on phase A.

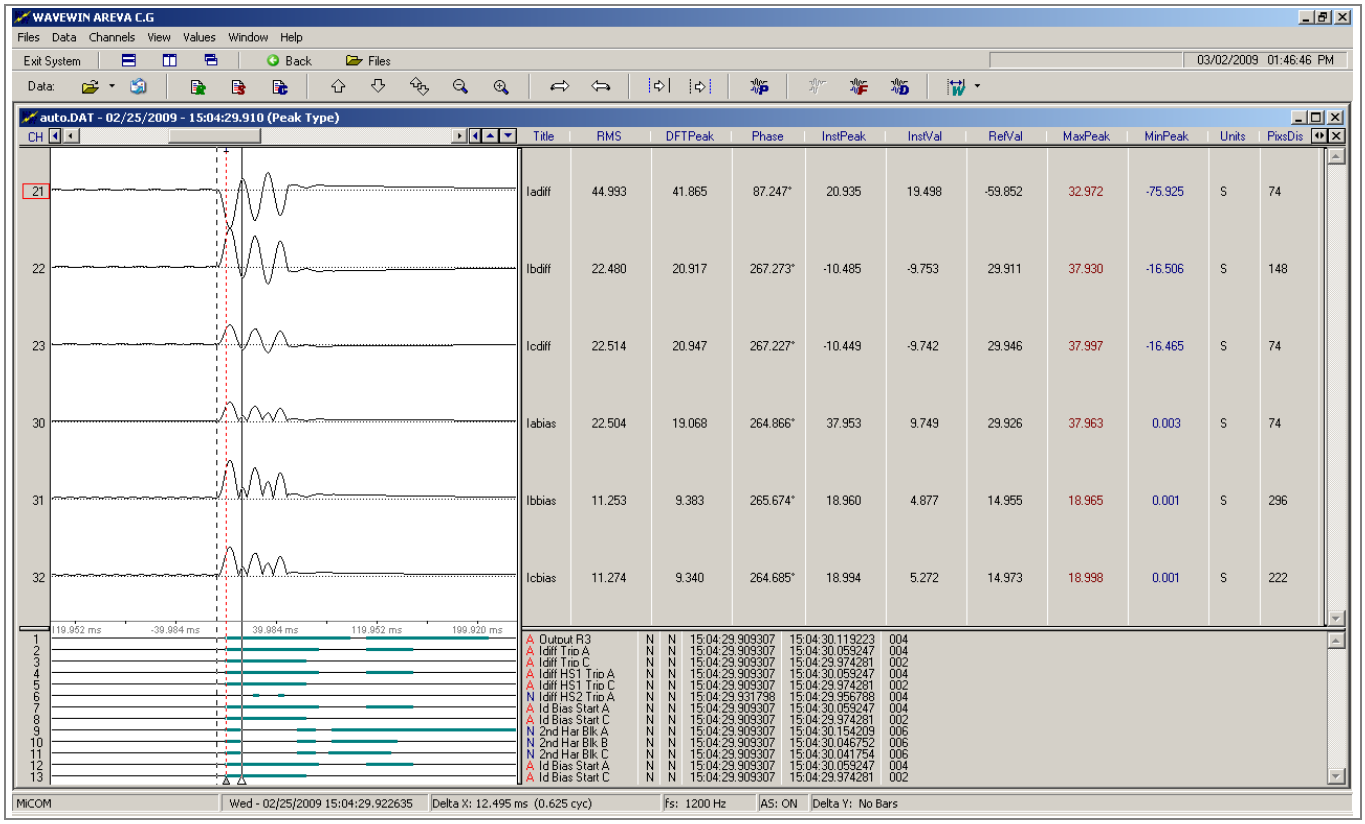


Figure 37 - Relay disturbance record

The following analysis explains why the phase C differential element also tripped. The sequence networks for an AN fault are shown in the following “Sequence Networks” diagram. All the quantities are in pu.

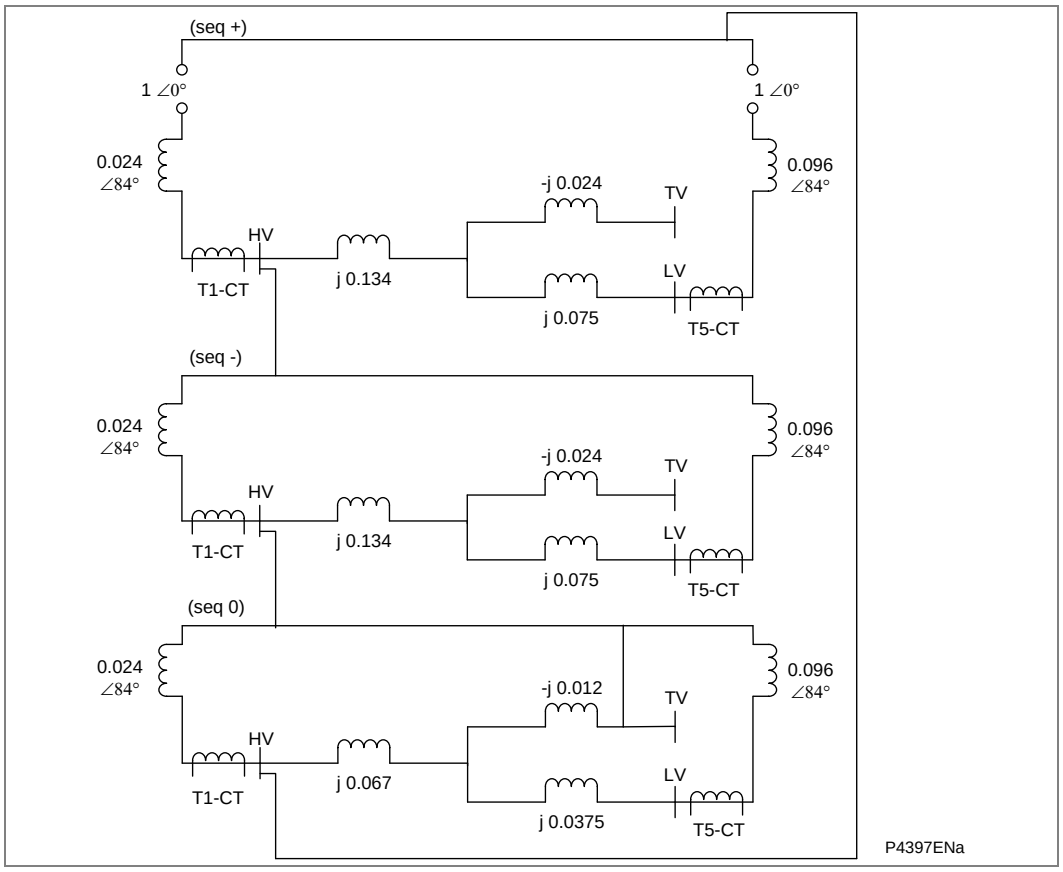


Figure 38 - Sequence networks

The positive sequence network is simplified as follows:

$$0.096\angle 84^\circ + j0.075 + j0.0134 = 0.305\angle 88.1^\circ pu$$

The negative sequence network is simplified as follows:

$$0.096\angle 84^\circ + j0.075 + j0.0134 = 0.305\angle 88.1^\circ pu$$

The zero sequence network is simplified as follows:

$$0.096\angle 84^\circ + j0.0375 = 0.133\angle 85.7^\circ pu$$

$$\frac{\left(0.133\angle 85.7^\circ\right)\left(-j0.012\right)}{0.133\angle 85.7^\circ + \left(-j0.012\right)} = 0.013\angle -89.6^\circ pu$$

$$j0.067 + 0.013\angle -89.6^\circ = 0.054\angle 89.9^\circ pu$$

Therefore the sequence networks in the above “Sequence Networks” diagram are simplified as follows:

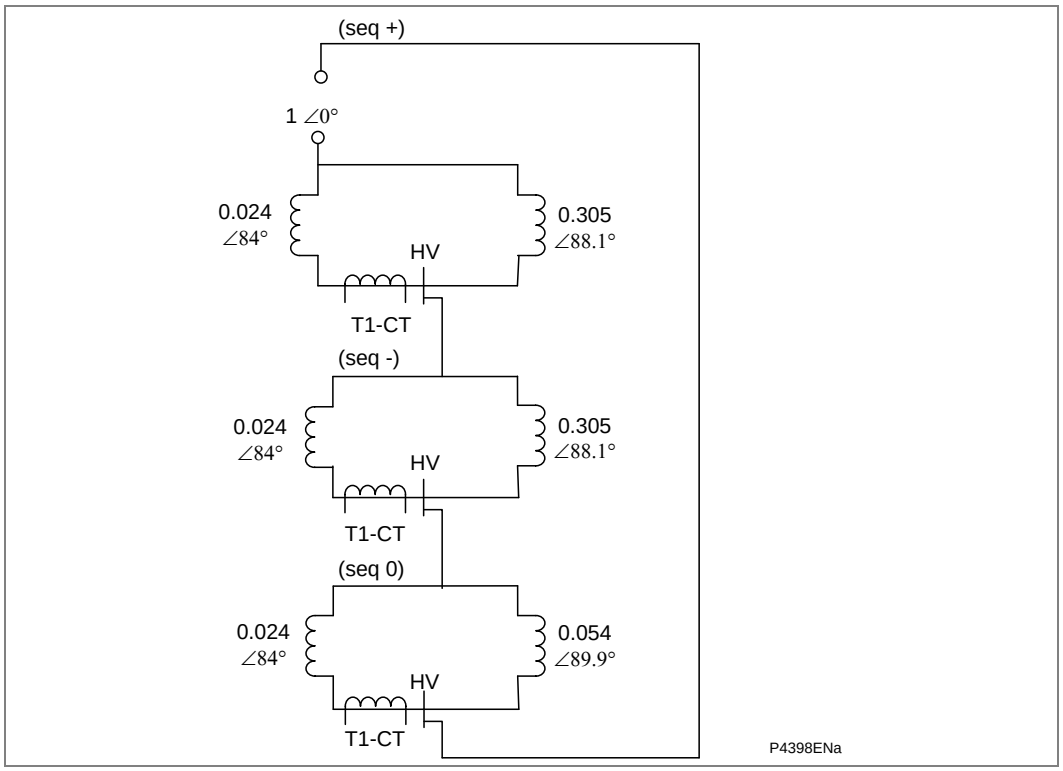


Figure 39 - Simplified sequence networks

From the above “Simplified sequence networks” diagram, the equivalent sequence networks impedances are calculated as follows:

Positive sequence equivalent impedance:

$$\frac{\left(0.024\angle 84^\circ\right)\left(0.305\angle 88.1^\circ\right)}{0.024\angle 84^\circ + 0.305\angle 88.1^\circ} = 0.022\angle 84.3^\circ \text{pu}$$

The negative sequence equivalent impedance is the same as the positive sequence equivalent impedance:

$$\frac{\left(0.024\angle 84^\circ\right)\left(0.305\angle 88.1^\circ\right)}{0.024\angle 84^\circ + 0.305\angle 88.1^\circ} = 0.022\angle 84.3^\circ \text{pu}$$

Zero sequence equivalent impedance:

$$\frac{\left(0.024\angle 84^\circ\right)\left(0.054\angle 89.9^\circ\right)}{0.024\angle 84^\circ + 0.054\angle 89.9^\circ} = 0.017\angle 85.8^\circ \text{pu}$$

The sequence networks are now represented by the equivalent impedances in series:

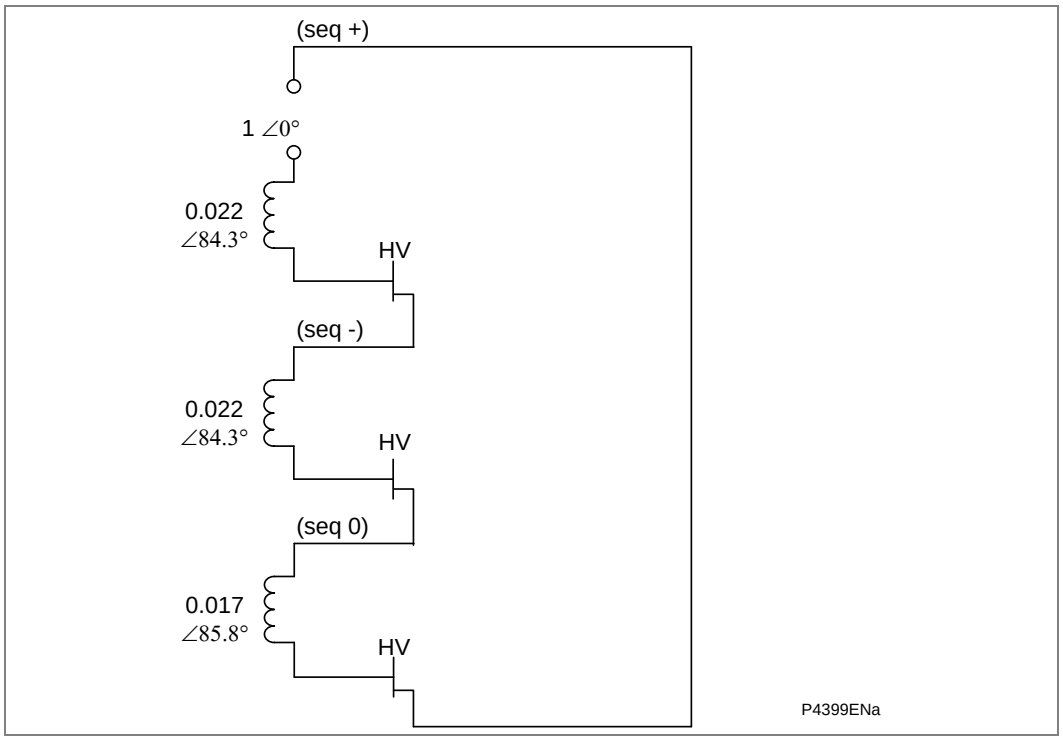


Figure 40 - Sequence networks

The equivalent impedance is:

$$0.022\angle 84.3^\circ + 0.022\angle 84.3^\circ + 0.017\angle 85.8^\circ = 0.061\angle 84.7^\circ \text{pu}$$

The positive, negative and zero sequence currents are:

$$I_0 = I_1 = I_2 = \frac{1}{0.061\angle 84.7^\circ} = 16.4\angle -84.7^\circ \text{pu}$$

The positive sequence currents on the HV side are calculated using a current division:

$$16.4\angle -84.7^\circ \times \frac{0.305\angle 88.1^\circ}{0.024\angle 84^\circ + 0.305\angle 88.1^\circ} = 15.21\angle -84.4^\circ \text{pu}$$

The positive sequence currents on the LV side are calculated using a current division:

$$16.4\angle -84.7^\circ \times \frac{0.024\angle 84^\circ}{0.024\angle 84^\circ + 0.305\angle 88.1^\circ} = 1.2\angle -88.5^\circ \text{pu}$$

The negative sequence currents on the HV and LV side are the same as the positive sequence currents on the HV and LV side respectively.

The zero sequence currents on the HV side are calculated using a current division:

$$16.4\angle -84.7^\circ \times \frac{0.054\angle 89.9^\circ}{0.024\angle 84^\circ + 0.054\angle 89.9^\circ} = 11.4\angle -82.9^\circ \text{pu}$$

The zero sequence currents on the LV side are calculated using a current division:

$$16.4\angle -84.7^\circ \times \frac{0.024\angle 84^\circ}{0.024\angle 84^\circ + 0.054\angle 89.9^\circ} = 5.1\angle -88.8^\circ \text{pu}$$

$$5.1\angle -88.8^\circ \times \frac{-j0.012}{-j0.012 + 0.133\angle 85.7^\circ} = 0.51\angle 95.9^\circ \text{pu}$$

The current distribution in the sequence networks is shown in the following “Current distribution in the sequence networks” diagram:

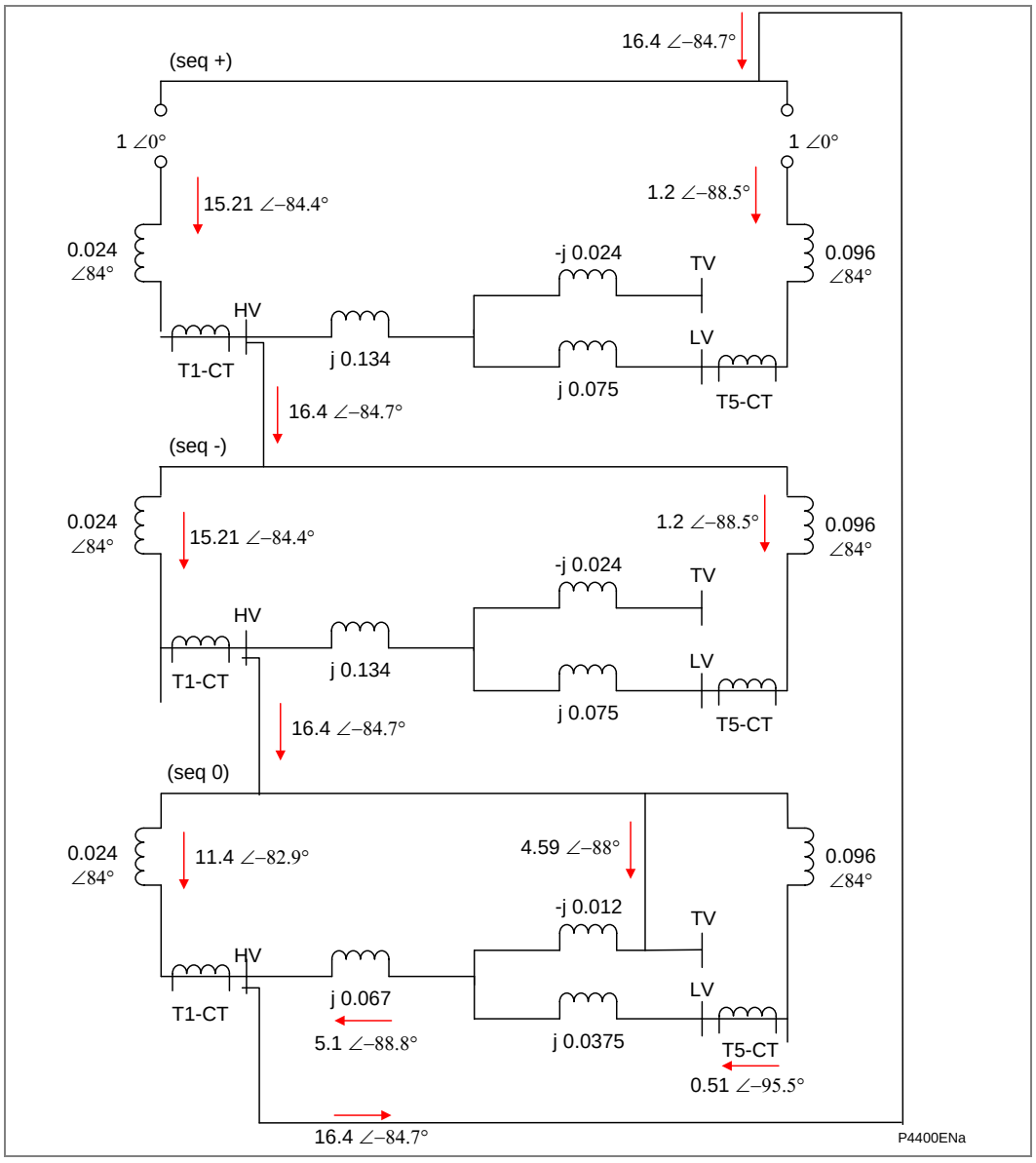


Figure 41 - Current distribution in the sequence networks

The currents on the HV and LV side seen by the current transformers T1-CT and T5-CT are calculated as follows using the following matrix:

$$\begin{bmatrix} Ia \\ Ib \\ Ic \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix} \times \begin{bmatrix} I_0 \\ I_1 \\ I_2 \end{bmatrix}$$

Current calculations on the HV side:

$$Ia = I_0 + I_1 + I_2 = 11.4\angle -82.9^\circ + 15.21\angle -84.4^\circ + 15.21\angle -84.4^\circ = 41.8\angle -84^\circ \text{pu}$$

$$Ib = I_0 + a^2 \times I_1 + a \times I_2$$

$$Ib = 11.4\angle -82.9^\circ + 1\angle 240^\circ \times 15.21\angle -84.4^\circ + 1\angle 120^\circ \times 15.21\angle -84.4^\circ = 3.82\angle 91.1^\circ \text{pu}$$

$$Ic = I_0 + a \times I_1 + a^2 \times I_2$$

$$Ib = 11.4\angle -82.9^\circ + 1\angle 120^\circ \times 15.21\angle -84.4^\circ + 1\angle 240^\circ \times 15.21\angle -84.4^\circ = 3.82\angle 91.1^\circ \text{pu}$$

Current calculations on the LV side:

$$Ia = I_0 + I_1 + I_2 = 0.51\angle 95.9^\circ + 1.2\angle -88.5^\circ + 1.2\angle -88.5^\circ = 1.89\angle -89.7^\circ \text{ pu}$$

$$Ib = I_0 + a^2 \times I_1 + a \times I_2$$

$$Ib = 0.51\angle 95.9^\circ + 1\angle 240^\circ \times 1.2\angle -88.5^\circ + 1\angle 120^\circ \times 1.2\angle -88.5^\circ = 1.71\angle 92.8^\circ \text{ pu}$$

$$Ic = I_0 + a \times I_1 + a^2 \times I_2$$

$$Ib = 0.51\angle 95.9^\circ + 1\angle 120^\circ \times 1.2\angle -88.5^\circ + 1\angle 240^\circ \times 1.2\angle -88.5^\circ = 1.71\angle 92.8^\circ \text{ pu}$$

The ratio correction factors as calculated by the relay are 2.382 on the HV side, and 1.143 on the LV side. These factors can be calculated by the user taking into consideration the CT primary nominal current and the winding full load current at the reference power.

$$\text{HV ratio correction factor} = \frac{1200}{\left(\frac{240 \text{ x } 10^6}{\sqrt{3} \text{ x } 275 \text{ x } 10^3}\right)} = 2.382$$

$$\text{LV ratio correction factor} = \frac{1200}{\left(\frac{240 \text{ x } 10^6}{\sqrt{3} \text{ x } 132 \text{ x } 10^3}\right)} 1.143$$

Since it is an autotransformer, HV and LV winding are effectively grounded star. The software interposing CTs are Ydy on each winding as shown in the "AN fault in the HV side of an autotransformer" diagram shown above. Therefore the zero sequence current is filtered on the HV and LV sides.

Note	*In this example, since the currents have been calculated in pu at the transformer base MVA, the differential calculation has been simplified by comparing the HV and LV pu currents. Therefore the ratio correction factors are not needed for this example.*

The differential currents on each phase is calculated as follows:

$$Iadiff = \left(\vec{Ia}_{HV} - \vec{I}_{0-HV}\right) + \left(\vec{Ia}_{LV} - \vec{I}_{0-LV}\right)$$

$$Iadiff = \left(41.8\angle -84^\circ - 11.4\angle -82.9^\circ\right) + \left(1.89\angle -89.7^\circ - 0.51\angle 95.9^\circ\right) = 32.8\angle -84.7^\circ \text{ pu}$$

$$Ibdiff = \left(\vec{Ib}_{HV} - \vec{I}_{0-HV}\right) + \left(\vec{Ib}_{LV} - \vec{I}_{0-LV}\right)$$

$$Ibdiff = \left(3.82\angle 91.1^\circ - 11.4\angle -82.9^\circ\right) + \left(1.71\angle 92.8^\circ - 0.51\angle 95.9^\circ\right) = 16.4\angle -95.3^\circ \text{ pu}$$

$$Icdiff = \left(\vec{Ic}_{HV} - \vec{I}_{0-HV}\right) + \left(\vec{Ic}_{LV} - \vec{I}_{0-LV}\right)$$

$$Icdiff = \left(3.82\angle 91.1^\circ - 11.4\angle -82.9^\circ\right) + \left(1.71\angle 92.8^\circ - 0.51\angle 95.9^\circ\right) = 16.4\angle -95.3^\circ \text{ pu}$$

The mean bias currents are calculated as follows:

$$Iabias = 0.5 \times \left(\left| \vec{Ia}_{HV} - \vec{I}_{0-HV} \right| + \left| \vec{Ia}_{LV} - \vec{I}_{0-LV} \right| \right)$$

$$Iabias = 0.5 \times \left(\left| 41.8\angle -84^\circ - 11.4\angle -82.9^\circ \right| + \left| 1.89\angle -89.7^\circ - 0.51\angle 95.9^\circ \right| \right) = 16.4pu$$

$$Ibbias = 0.5 \times \left(\left| \vec{Ib}_{HV} - \vec{I}_{0-HV} \right| + \left| \vec{Ib}_{LV} - \vec{I}_{0-LV} \right| \right)$$

$$Ibbias = 0.5 \times \left(\left| 3.82\angle 91.1^\circ - 11.4\angle -82.9^\circ \right| + \left| 1.71\angle 92.8^\circ - 0.51\angle 95.9^\circ \right| \right) = 8.2pu$$

$$Icbias = 0.5 \times \left(\left| \vec{Ic}_{HV} - \vec{I}_{0-HV} \right| + \left| \vec{Ic}_{LV} - \vec{I}_{0-LV} \right| \right)$$

$$Icbias = 0.5 \times \left(\left| 3.82\angle 91.1^\circ - 11.4\angle -82.9^\circ \right| + \left| 1.71\angle 92.8^\circ - 0.51\angle 95.9^\circ \right| \right) = 8.2pu$$

The current distribution within the P642 is shown in the “Current distribution within the P642” diagram shown below:

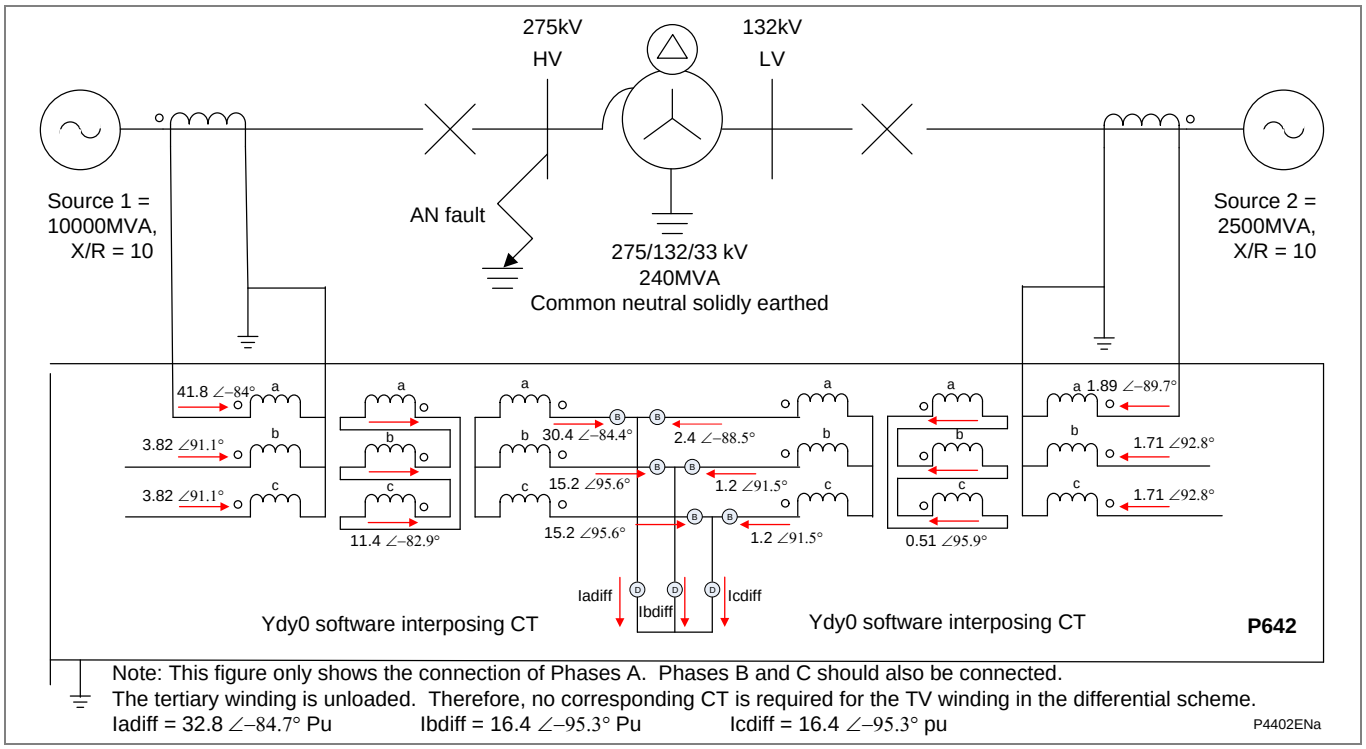


Figure 42 - Current distribution within the P642

The bias current used by the relay for all the phases is the maximum bias current. In this case the relay will use Iabias.

From the above calculations it can be observed that all three phases are much greater than the high set one element (Is-HS1), which has been set to 4.9 pu. As mentioned in the operation chapter, for the relay to trip for Is-HS1, the differential current should be above the Is-HS1 setting and in the operating region of the bias characteristic. Therefore, due to the current distribution during the internal AN fault, the differential elements for phases B and C may trip even though these phases are not faulted.

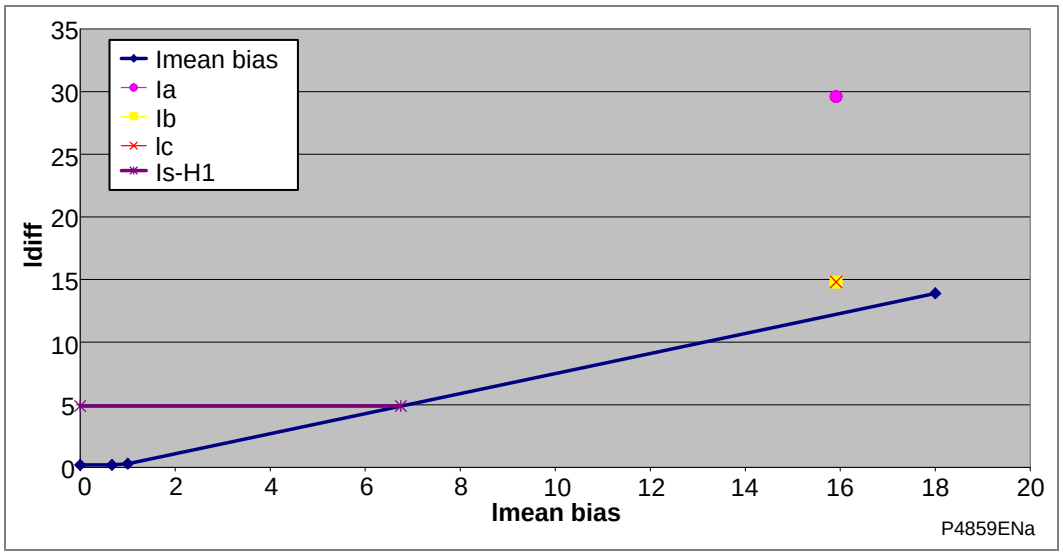


Figure 43 - Differential characteristic

It is important to note that all the calculations have only taken into consideration the mean bias and mean differential currents. The relay also adds an additional transient bias quantity to the operating current. It should be noted that due to transient bias if the differential calculations of the non-faulted phases are close to the bias characteristic, then these un-faulted phases may not operate.

The current distribution in this system is shown in the following "Current distribution" diagram. The positive, negative and zero sequence currents in the HV terminal were calculated already, and they are:

- Positive sequence = 1.2 ∠ - 88.5° pu
- Negative sequence = 1.2 ∠ - 88.5° pu
- Zero sequence = 5.1 ∠ - 88.8° pu

The phase currents in the autotransformer HV terminal are calculated as follows:

$Ia = I_0 + I_1 + I_2 = 5.1\angle -88.8° + 1.2\angle -88.5° + 1.2\angle -88.5° = 7.5\angle -88.7pu$

$Ib = I_0 + a^2I_1 + aI_2$

$Ib = 5.1\angle -88.8° + 1\angle 240° \times 1.2\angle -88.5° + 1\angle 120° \times 1.2\angle -88.5° = 3.9\angle -88°pu$

$Ic = I_0 + aI_1 + a^2I_2$

$Ib = 5.1\angle -88.8° + 1\angle 120° \times 1.2\angle -88.5° + 1\angle 240° \times 1.2\angle -88.5° = 3.9\angle -88°pu$

To analyse the current distribution of the autotransformer, the current values need to be converted from pu to amperes. Then Kirchoff's current law is then applied.

$$\text{The base current in the 275kV side is} = \frac{240 \times 10^6}{\sqrt{3} \times 275 \times 10^3} = 504A$$

$$\text{The base current in the 132kV side is} = \frac{240 \times 10^6}{\sqrt{3} \times 132 \times 10^3} = 1050A$$

The currents flowing from source 1 are:

$Ia = 41.8\angle -84pu = 41.8\angle -84° \times 504 = 21067\angle -84° A$

$Ib = 3.82\angle 91.1pu = 3.82\angle 91.1° \times 504 = 1925\angle 91.1° A$

$Ic = 3.82\angle 91.1pu = 3.82\angle 91.1° \times 504 = 1925\angle 91.1° A$

$3I0 = 3x11.4\angle -82.9° = 34.2\angle -82.9°pu = 34.2\angle -82.9° \times 504 = 17237\angle -82.9° A$

The currents flowing from source 2 to the autotransformer LV terminal are:

$Ia = 1.89\angle -89.7pu = 1.89\angle -89.7° \times 1050 = 1985\angle -89.7° A$

$Ib = 1.71\angle 92.8pu = 1.71\angle 92.8° \times 1050 = 1796\angle 92.8° A$

$Ic = 1.71\angle 92.8pu = 1.71\angle 92.8° \times 1050 = 1796\angle 92.8° A$

$3I0 = 3x0.51\angle 95.9° = 1.53\angle 95.9°pu = 1.53\angle 95.9° \times 1050 = 1607\angle 95.5° A$

The currents flowing from the autotransformer HV terminal are:

Ia = 7.5∠-88.7pu = 7.5∠-88.7° x 504 = 3780∠-88.7° A

Ib = 3.9∠-88pu = 3.9∠-88° x 504 = 1966∠-88° A ≈ 1925∠91.1° A

Ic = 3.9∠-88pu = 3.9∠-88° x 504 = 1966∠-88° A ≈ 1925∠91.1° A

3I0 = 3x5.1∠-88.8° = 15.3∠-88.8°pu = 15.3∠-88.8° x 1504 = 7610∠-88.8° A

As expected, the currents in phases B and C in the autotransformer HV terminal are the same as the currents in phases B and C in source 1.

The current in the ground of the autotransformer is the subtraction of $3I_{0\text{-}HV}$ minus $3I_{0\text{-}LV}$:

$3I_{0\text{-}HV} - 3I_{0\text{-}LV}$ = 7610∠-88.8° - 1607∠95.5° = 9213∠-88.8

The zero sequence current trapped in the delta is calculated using current division as follows:

$$5.1\angle -88.8° \times \frac{0.133\angle 85.7°}{-j0.012 + 0.133\angle 85.7°} = 5.6\angle -88.4° \text{pu}$$

$$\text{The base current in the 33kV side is} = \frac{240 \times 10^6}{\sqrt{3} \times 33 \times 10^3} = 4199\text{A}$$

Therefore, the current trapped in the delta is 5.6∠-88.4° × 4199 = 23514 ∠-88.4° A.

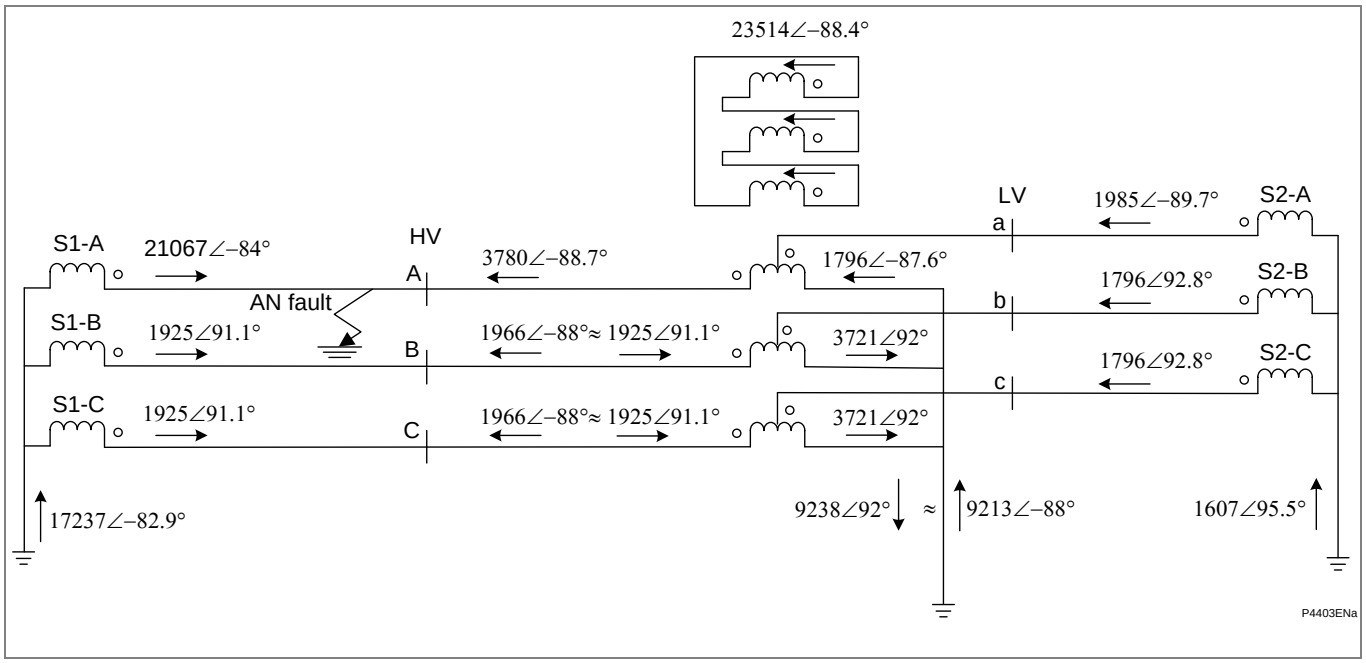


Figure 44 - Current distribution

2.3 Restricted Earth Fault (REF) Protection

2.3.1 Basic Principles

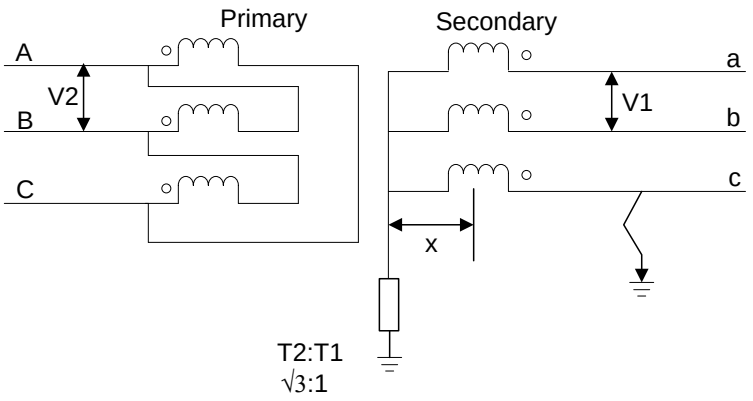
An earth fault is the most common type of fault that occurs in a transformer. These conditions must be satisfied for an earth fault current to flow:

- A path exists for the current to flow into & out of the windings (zero sequence path)
- The ampere turns balance is maintained between the windings

The magnitude of earth fault current depends on the method of earthing (solid or resistance) and the transformer connection.

Consider the resistance earthed star winding shown in the following diagram. An earth fault on such a winding causes a current which depends on the earthing impedance value. This earth fault current is proportional to the distance of the fault from the neutral point since the fault voltage is directly proportional to this distance.

The ratio of transformation between the primary winding and the short-circuited turns also varies with the position of the fault. Therefore, the current that flows through the transformer terminals is proportional to the square of the fraction of the winding which is short-circuited.



The earthing resistor is rated to pass full load current $\frac{V_1}{\sqrt{3}R} = I_{FLC}$

Assuming that V1 = V2 then:

$V1\phi = T1$

$V2\phi = T2$

$$\frac{V1}{V2} = \frac{\sqrt{3}\cdot V1\phi}{V2\phi} = \frac{\sqrt{3}\cdot T1}{T2}$$

$$1 = \frac{\sqrt{3}\cdot T1}{T2} \Rightarrow T2 = \sqrt{3}\cdot T1$$

For a fault at x pu distance from the neutral If is $I_f = \frac{x.V_1}{\sqrt{3}R}$

The secondary fault current referred to the primary is $I\,\text{primary} = \frac{x\cdot V_1}{\sqrt{3}R}\,\frac{x\cdot T_1}{T_2}$

$$= x^2\cdot I_{FLC}\frac{1}{\sqrt{3}}$$

P4307ENa

Figure 45 - Star winding resistance earthed

If the fault in the previous diagram is a single end fed fault, the primary current should be greater than 0.2 pu (Is1 default setting) for the differential protection to operate.
Therefore, $(x^2 / \sqrt{3}) > 20\%$
This table shows that 41% of the winding is protected by the differential element.

x	Idiff in %	
10	0.58	59% of unprotected winding
20	2.31	
30	5.20	
40	9.24	
50	14.43	
59	20.00	
70	28.29	41% of protected winding
80	36.95	
90	46.77	
100	57.74	

Table 5 - % of winding protected by differential element

In a solidly earthed star winding, the fault current is limited only by the leakage reactance of the winding, which varies in a complex manner with the position of the fault. For most of the winding the fault current is approximately 3 x I_{FLC}, reaching a maximum of 5 x I_{FLC}.

Earth faults occurring on a transformer winding or terminal may be of limited magnitude, either due to the impedance present in the earth path or by the percentage of transformer winding that is involved in the fault. It is common to apply standby earth fault protection fed from a single CT in the transformer earth connection - this provides time-delayed protection for a transformer winding or terminal fault. In general, particularly as the size of the transformer increases, it becomes unacceptable to rely on time delayed protection to clear winding or terminal faults as this would lead to an increased amount of damage to the transformer. A common requirement is therefore to provide instantaneous phase and earth fault protection. Applying differential protection across the transformer may fulfill these requirements. However, an earth fault occurring on the LV winding, particularly if it is of a limited level, may not be detected by the differential relay, as it is only measuring the corresponding HV current. Therefore, instantaneous protection that is restricted to operating for transformer earth faults only is applied. This is referred to as Restricted Earth Fault (REF) Protection.

Note	*REF can also be referred to as restricted, or balanced, earth fault protection (REF or BEF). The BEF terminology is usually used when the protection is applied to a delta winding.*

The P64x uses biased differential protection to provide fast clearance for faults within the protected zone. The value of earth fault current, however, may be limited by any impedance in the earth path or by the percentage of the winding involved in the fault. The P64x offers a REF element for up to 3 windings of the protected transformer to provide greater sensitivity for earth faults which will not change with load current.

The levels of fault current available for relay measurement are shown below. If an earth fault is considered on an impedance earthed star winding of a Dyn transformer (see the “Fault Limitation on an Impedance Earthed System” diagram below), the value of current flowing in the fault (If) depends on two factors. These are the value of earthing impedance and the fault point voltage, which is governed by the fault location. The value of fault current (If) is directly proportional to the location of the fault as shown in the diagram below. A REF element (64) is connected to measure If directly, to provide more SEF protection. The overall differential protection is less sensitive, since it only measures the HV current Is. The value of Is is limited by the number of faulty secondary turns in relation to the HV turns.

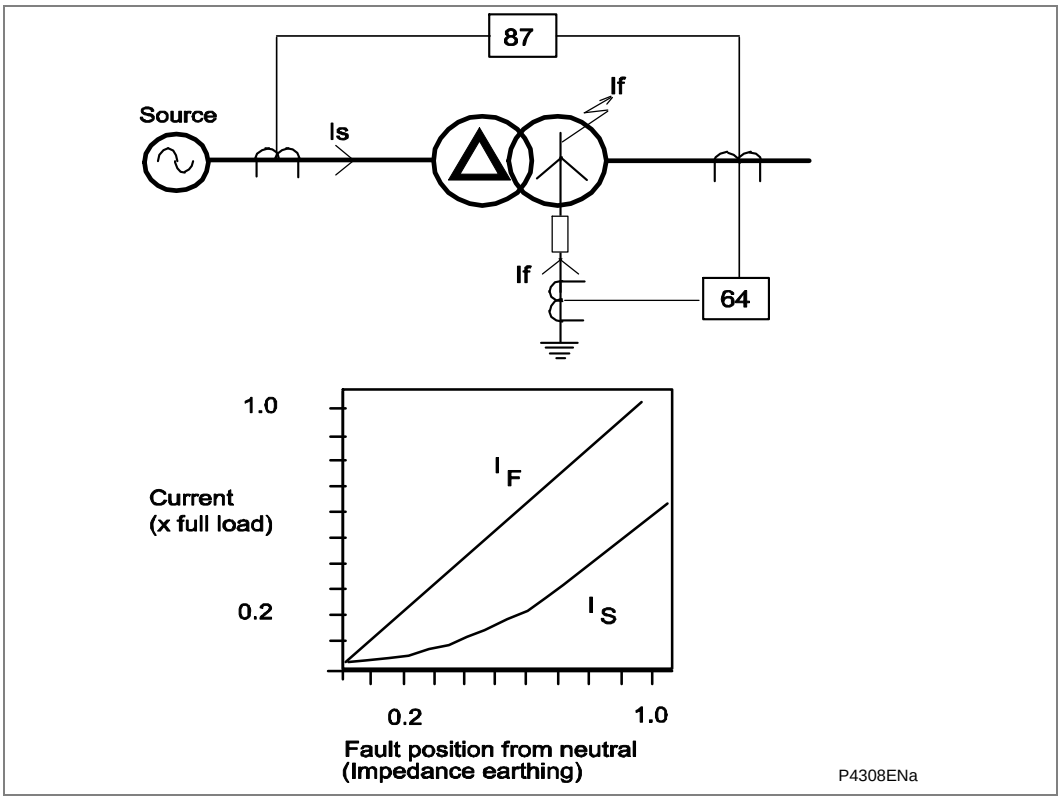


Figure 46 - Fault limitation on an impedance earthed system

If a fault on a solidly earthed star winding (as shown in the “Fault Limitation on a Solidly Earthed System” diagram below) is considered, the fault current is limited by the leakage reactance of the winding, any impedance in the fault path and by the fault point voltage. The value of fault current varies in a complex manner with fault location. As in the case of the impedance earthed transformer, the value of current available as an overall differential protection operating quantity is limited. More SEF protection is provided by a REF relay (64), which is arranged to measure If directly. Although more sensitive protection is provided by REF, the operating current for the overall differential protection is still significant for faults over most of the winding. For this reason, independent REF protection may not have previously been considered necessary for a solidly earthed winding, especially where an additional relay would have been required. With the P64x, the REF protection is available at no extra cost if a neutral CT is available.

REF protection is also commonly applied to Delta windings of large power transformers, to improve the operating speed and sensitivity of the protection package for winding earth faults. When applied to a Delta winding this protection is commonly referred to as “balanced earth fault protection”. It is inherently restricted in its zone of operation when it is stabilized for CT spill current during inrush or during phase faults. The value of the fault current flowing depends on system earthing arrangements and the fault point voltage.

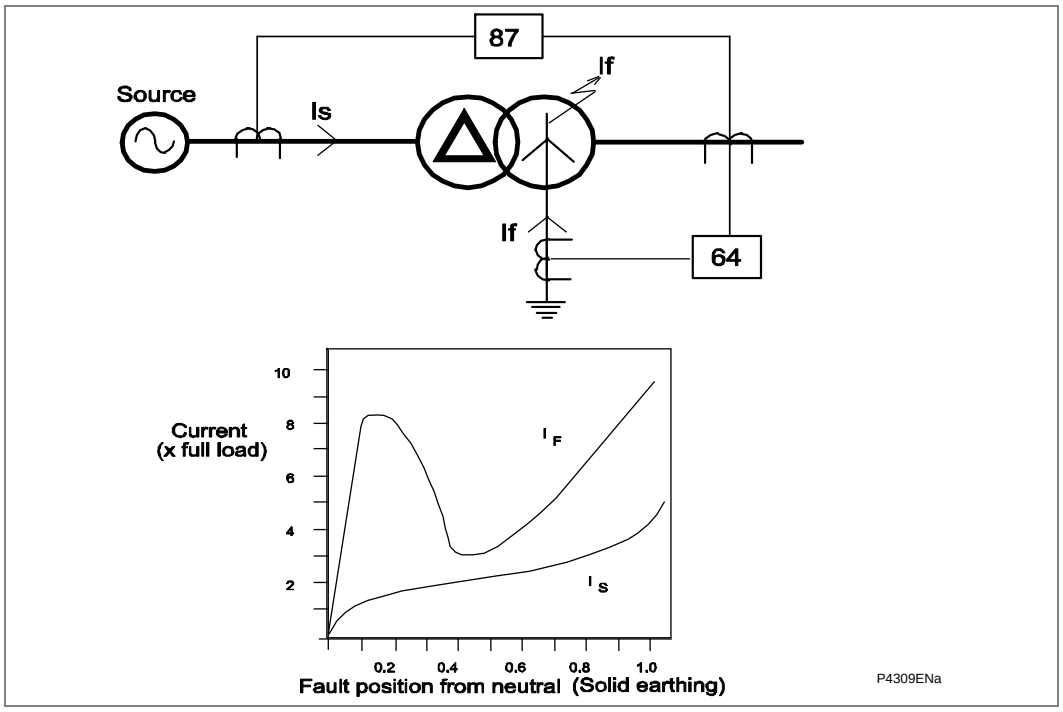


Figure 47 - Fault limitation on a solidly earthed system

2.3.2 Low Impedance REF Operating Mode

When applying differential protection such as REF, some suitable means must be used to give the protection stability under external fault conditions, ensuring that relay operation only occurs for faults on the transformer winding or connections. The P64x uses the bias technique which operates by measuring the level of through current flowing and altering the relay sensitivity accordingly. In addition, the P64x uses transient bias to improve the stability of REF during external faults.

Low impedance REF with a triple slope biased characteristic is provided in the P64x. One low impedance REF protection function is available for each transformer winding. It can also be used in 1.5 breaker and autotransformer applications. Low impedance REF is based on comparing the vector sum of phase currents of the transformer winding to the neutral point current measured directly.

The differential current and bias current are given by the expressions:

$$I_{bias} = \frac{1}{2}\left\{\max\left[\left|I_{A\,CT_n}\right|, \left|I_{B\,CT_n}\right|, \left|I_{C\,CT_n}\right|\right] + I_N \times K\right\}$$

$$I_{diff} = \left[\left(\vec{I}_{A\,CT_n} + \vec{I}_{B\,CT_n} + \vec{I}_{C\,CT_n}\right) + \vec{I}_N \times K\right]$$

Scaling factor = K = Neutral CT ratio / CT_n ratio

The REF biased characteristic is shown in the “REF Biased Characteristic” diagram.

Low impedance biased REF settings are similar to those of the biased differential protection function. The low impedance REF is blocked by CTS.

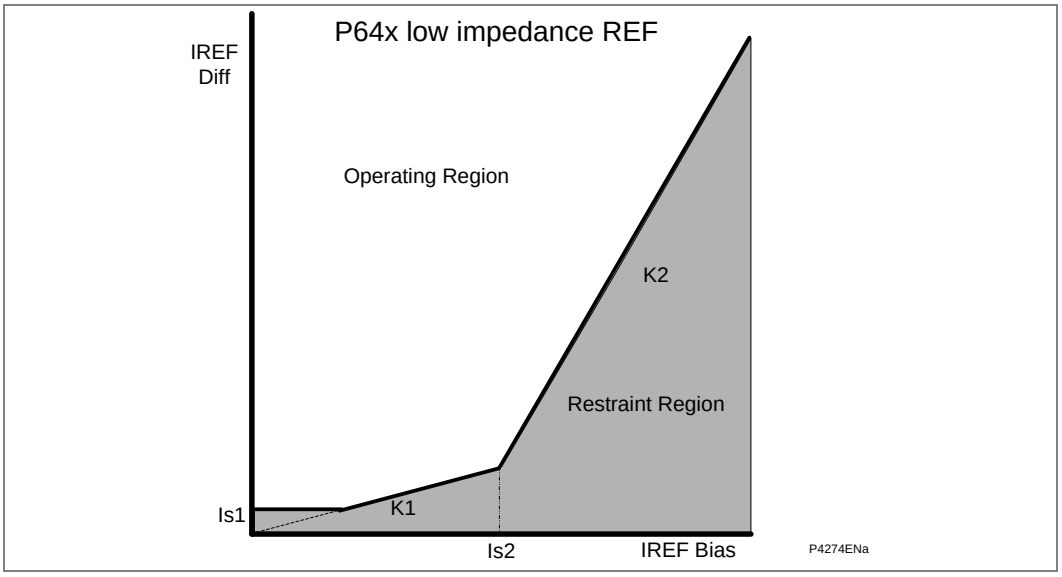


Figure 48 - P64x restricted earth fault biased characteristic

2.3.3 Setting Guidelines for Low Impedance Biased REF Protection

Two bias settings are provided in the REF protection in the P64x. The IREF K1 level of bias is applied up to through currents of Is2 Set, which is normally set to the rated current of the transformer. IREF> K1 is normally set to 0% to give optimum sensitivity for internal faults. However, if any differential spill current is present under normal conditions due to CT mismatch, IREF K1 may be increased accordingly to compensate. Then a setting of 20% is recommended.

IREF> K2 bias is applied for through currents above Is2 Set and may typically be set to 150% to ensure adequate restraint for external faults.

The neutral current scaling factor which automatically compensates for differences between neutral and phase CT ratios relies on the relay having been programmed with the correct CT ratios. It must therefore be ensured that these CT ratios are entered into the relay, in the **CT RATIOS** menu, for the scheme to operate correctly.

Typical settings for Is1 Set according to ESI 48-3 1977 are 10-60% of the winding rated current when solidly earthed and 10-25% of the minimum earth fault current for a fault at the transformer terminals when resistance earthed.

The following diagram shows the relay connections for the P64x relay applied for biased REF protection.

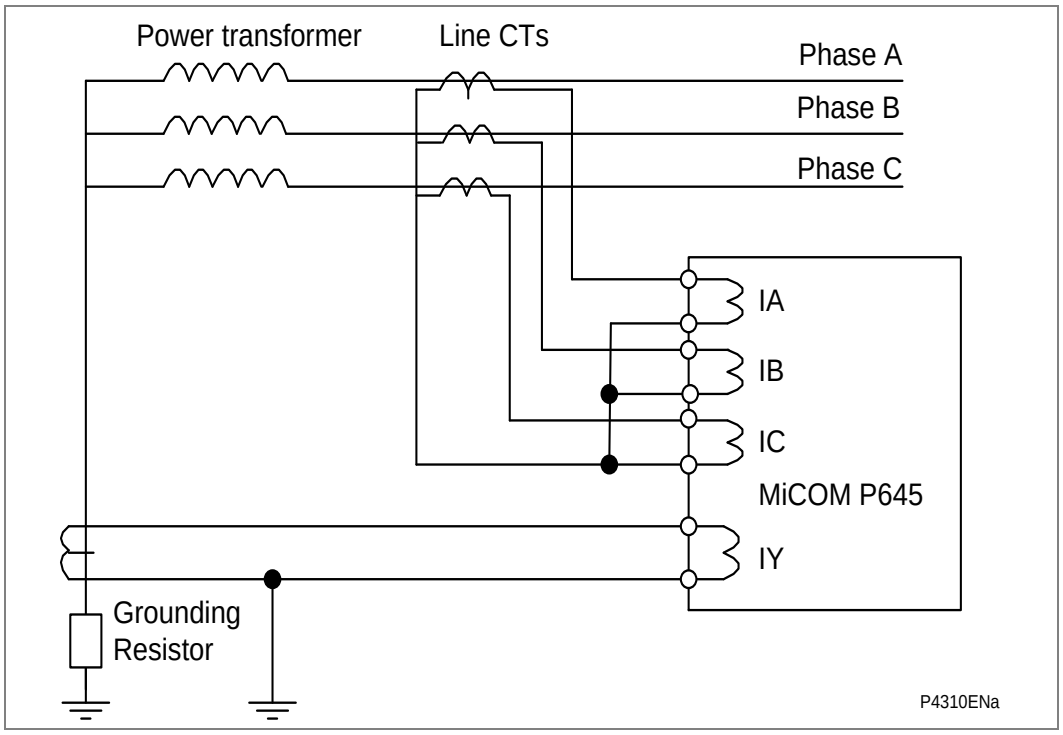


Figure 49 - P64x connections for biased REF protection

In the “Connections for Biased REF Protection” diagram shown above, the three line CTs are connected to the three phase CTs in the normal manner. The neutral CT is then connected to the I_Y input. These currents are then used internally to derive both a bias and a differential current quantity for use by the low impedance REF protection.

The actual operating characteristic of the element is shown in the “REF Scaling Factor” diagram shown below. The advantage of this mode of connection is that the line and neutral CTs are not differentially connected so the neutral CT can also be used to drive the 51N protection to provide Standby Earth Fault Protection. Also, no external equipment such as stabilizing resistors or Metrosils are required, as is the case with high impedance protection.

Where it is required that the neutral CT also drives the 51N protection element to provide standby earth fault protection, it may be a requirement that the neutral CT has a lower ratio than the line CTs to provide better earth fault sensitivity. If this was not accounted for in the REF protection, the neutral current value used would be incorrect. The relay automatically calculates the scaling factor that matches in amplitude the summation of line currents to the neutral current. This is shown in the “REF Scaling Factor” diagram.

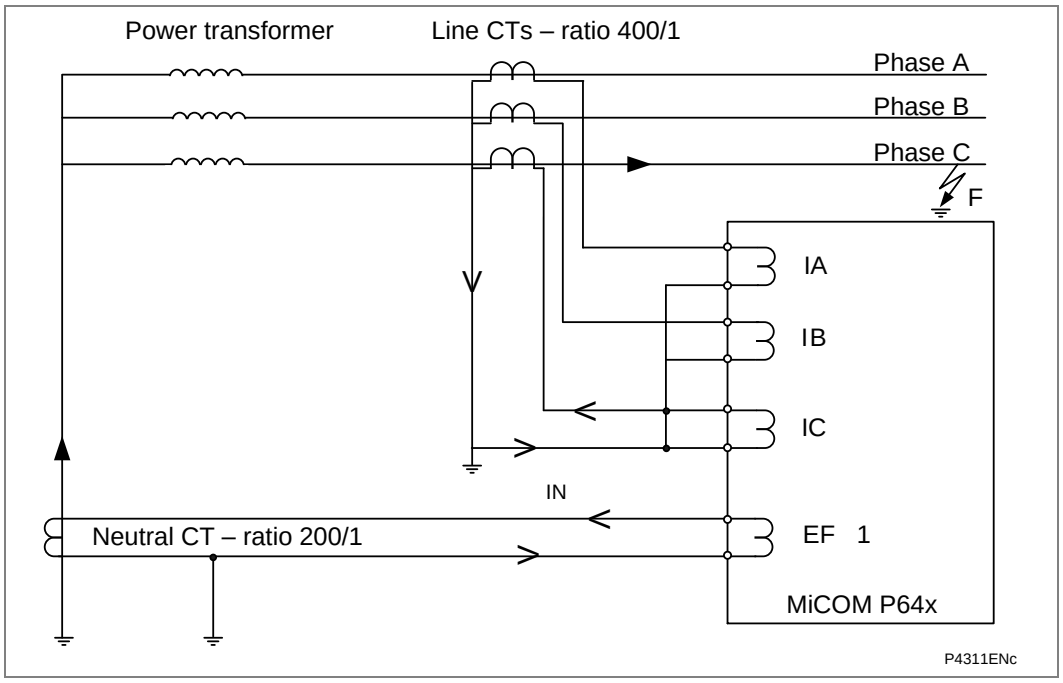


Figure 50 - P64x REF scaling factor

$$I_{REF,\,diff} = \left[\left(\vec{I}_{A\,CT_n} + \vec{I}_{B\,CT_n} + \vec{I}_{C\,CT_n}\right) + \vec{I}_N \times K\right]$$

$$I_{REF,\,bias} = \frac{1}{2}\left\{\max\left[\vec{I}_{A\,CT_n}, \vec{I}_{B\,CT_n}, \vec{I}_{C\,CT_n}\right] + I_N \times K\right\}$$

Scaling factor = K = Neutral CT ratio / CT_n ratio

Example 1: Consider a solidly earthed 90 MVA transformer which has a star winding protected by the REF function in the P64x. Consider 400:1 line CTs.

Is1 Set is set to 10% of the winding nominal current:

$$\text{Is1 Set} = 0.1 \times \frac{90 \times 10^6}{\sqrt{3} \times 132 \times 10^3} = 39\text{A primary} = \frac{39}{400} = 0.98\text{A secondary}$$

Is2 is set to the rated current of the transformer:

$$\text{Is2 Set} = \frac{90 \times 10^6}{\sqrt{3} \times 132 \times 10^3} = 390\text{A primary} = \frac{390}{400} = 1\text{A secondary}$$

As recommended previously K1 may be set to 0% and K2 to 150%.

2.3.4 High Impedance REF Operating Mode

The REF protection is a high impedance differential scheme which balances zero sequence current flowing in the transformer neutral against zero sequence current flowing in the transformer phase windings. Any unbalance for in-zone fault will result in an increasing voltage on the CT secondary and thus will activate the REF protection.

The high impedance differential technique ensures that the impedance of the circuit is sufficiently high such that the differential voltage that may occur under external fault conditions is lower than the voltage required to drive setting current through the relay. This ensures stability against external fault conditions and then the relay will operate only for faults occurring inside the protected zone.

This scheme is very sensitive and can then protect against low levels of fault current in resistance grounded systems where the earthing impedance and the fault voltage limit the fault current. In this application, the **HV/LV/TV/Auto Is1 Set** setting should be chosen to provide a primary operating current less than 10-25% of the minimum earth fault level.

This scheme can also be used in a solidly grounded system. It provides a more sensitive protection, even though the overall differential scheme provides a protection for faults over most of the windings. In this application, the **HV/LV/TV/Auto Is1 Set** setting should be chosen to provide a primary operating current between 10% and 60 % of the winding rated current.

The following three figures show how the P64x is used in REF, BEF and autotransformer REF applications.

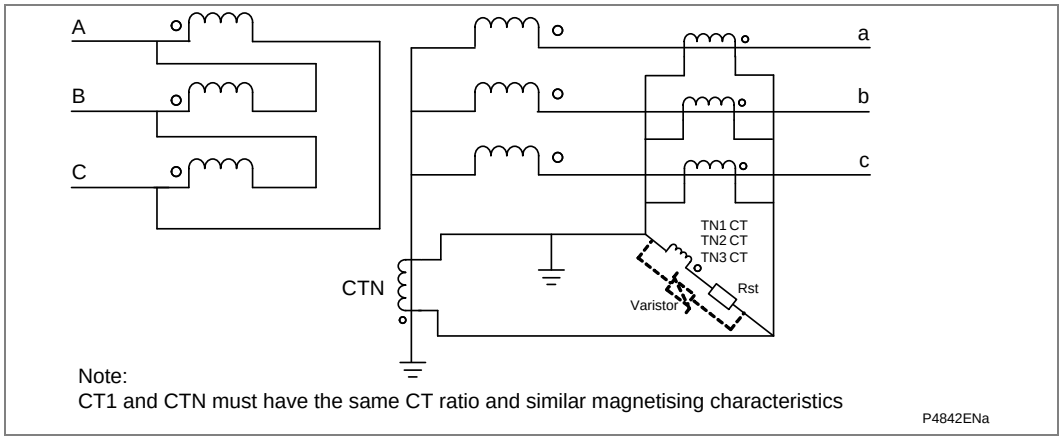


Figure 51 - P64x high impedance REF of the grounded star winding of a power transformer

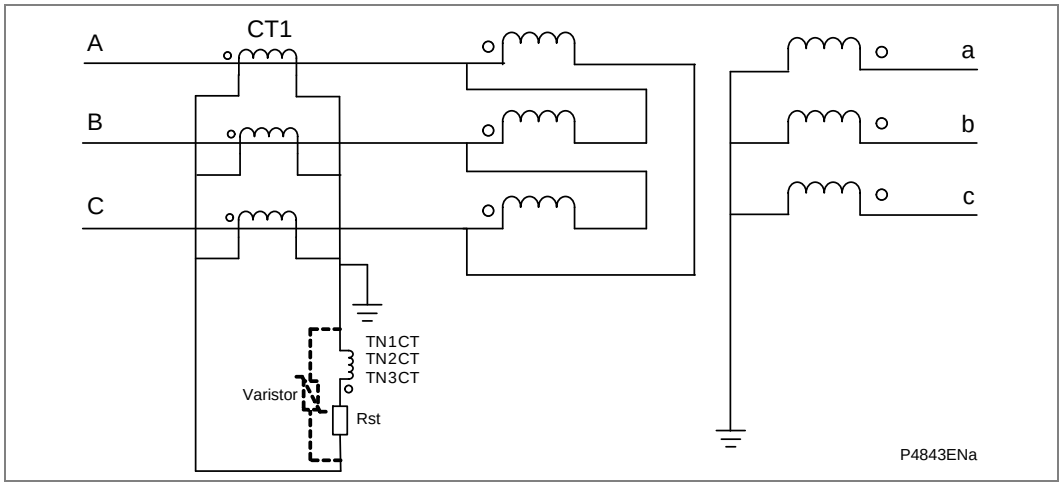


Figure 52 - P64x high impedance BEF of the delta winding of a power transformer with supply system earthed

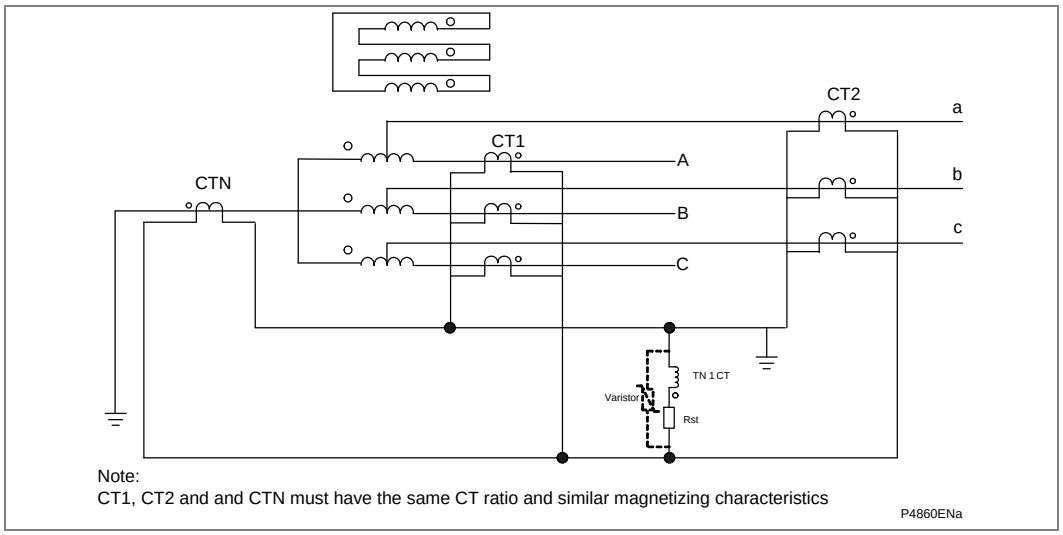


Figure 53 - P64x Autotransformer high impedance REF

2.3.5 Setting Guidelines for High Impedance REF Protection

This diagram shows the application of a high impedance REF to protect the LV winding of a power transformer.

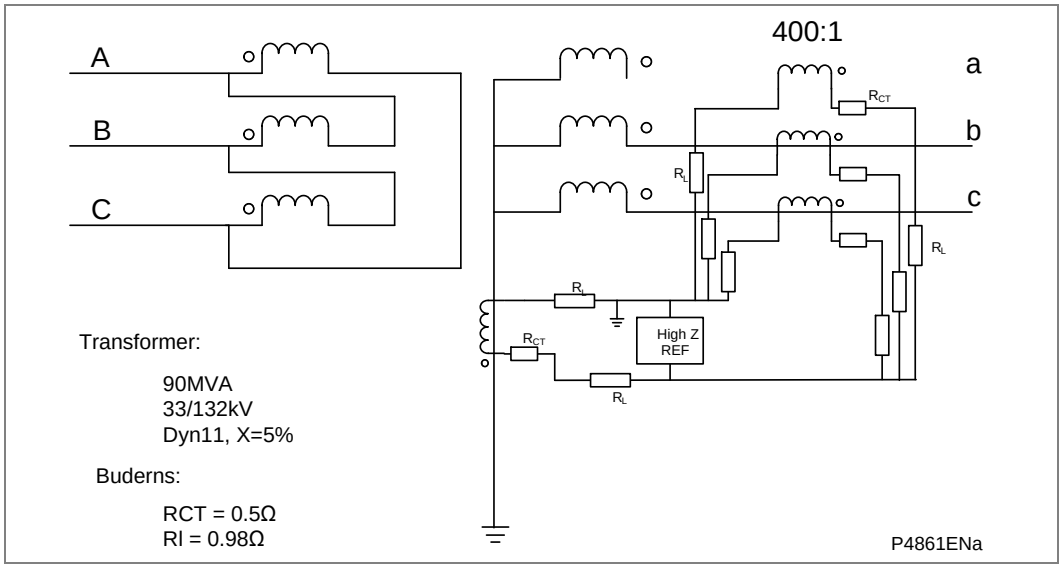


Figure 54 - Restricted earth fault protection on a transformer

2.3.5.1 Stability Voltage Calculation

The transformer Full Load Current (FLC), I_{FLC}, is:

$$I_{FLC} = \frac{90 \times 10^6}{\sqrt{3} \times 132 \times 10^3} = 394A$$

To calculate the stability voltage the maximum through fault level should be considered. The maximum through fault level, ignoring the source impedance, I_F, is:

$$I_F = \frac{I_{FLC}}{X_{TC}} = \frac{394A}{0.05} = 7873A$$

Required relay stability voltage, V_S, and assuming one CT saturated is:

$V_S = KI_F (R_{CT} + 2R_L)$

$V_S = 1 \times I_F R_{CT} + 2R_L = 1 \times 7873 \times 1/400 (0.5 + 2 \times 0.98) = 48.5V$

The CTs knee point voltage should be at least 4 times V_S so that an average operating time of 40 ms is achieved.

2.3.5.2 Primary Operating Current Calculation

The primary operating current should be between 10 and 60 % of the winding rated current. Assuming the relay effective setting or primary operating current is approximately 30% of the full load current, the calculation below shows that a setting of less than 0.3A is required on the relay.

$$\text{Relay Effective Setting} = 0.3 \times \frac{I_{FLC}}{CT_{ratio}} = 0.3 \times \frac{394A}{400} = 0.3A$$

2.3.5.3 Stabilising Resistor Calculation

Assuming a setting of 0.1A is selected the value of the stabilizing resistor R_{ST}, needed is:

$$R_{ST} = \frac{V_S}{\text{HV Is1 Set}} = \frac{48.5}{0.1} = 485\Omega$$

To achieve an average operating time of 40 ms, Vk/Vs should be 4.

Kneepoint Voltage $V_K = 4V_S = 4 \times 48.5 = 194$ V

2.3.5.4 Current Transformers

The effective relay setting or primary operating current is:

$$I_P = N \times (I_S + nI_e)$$

By re-arranging this equation, the excitation current for each of the current transformers at the relay stability voltage can be calculated:

CT Magnetising current at stability voltage:

$$I_e \leqslant \frac{1}{n} \times \left(\frac{I_P}{N} - I_S \right) \leqslant \frac{0.3 - 0.1}{4} \leqslant 0.05A$$

In summary, the current transformers used for this application must have a kneepoint voltage of 194 V or higher, with a secondary winding resistance of 0.5 Ω or lower and a magnetizing current at 48.5 V of less than 0.05 A.

2.3.5.5 Non-Linear Resistors

If the peak voltage developed across the relay circuit under maximum internal fault conditions exceeds 3000 V peak then a suitable non-linear resistor should be connected across the relay and stabilizing resistor, to protect the insulation of the CTs, relay and interconnecting leads. To calculate the maximum fault voltage assuming no CT saturation, use this equation:

$V_F = I'_F (R_{CT} + 2R_L + R_{ST} + R_r) = 7873 \times 1/400 (0.5 + 2 \times 0.98 + 485) = 9594V$

Assuming a CT kneepoint voltage of 200 V, the peak voltage can be estimated as:

$V_P = 2\sqrt{2V_K (V_F - V_K)} = 2\sqrt{2x200(9594-200)} = 3876V$

This value is above the peak voltage of 3000 V and therefore a non-linear resistor is required.

Note	*The kneepoint voltage value used in the above formula should be the actual voltage obtained from the CT magnetizing characteristic and not a calculated value.*

One stabilizing resistor, Schneider Electric part No. ZB9016 756, and one varistor, Schneider Electric part No. 600A/S1/S256 would be suitable for this application.

2.4 Overfluxing Protection and Blocking

2.4.1 Basic Principles

Overfluxing or overexcitation of a transformer connected to the terminals of a generator, can occur if the ratio of voltage to frequency exceeds certain limits. High voltage or low frequency, causing a rise in the V/f ratio, will produce high flux densities in the magnetic core of the transformer. This could cause the core of the transformer to saturate and stray flux to be induced in unlaminated components that have not been designed to carry flux. The resulting eddy currents in solid components (core bolts and clamps) and end of core laminations can cause rapid overheating and damage.

The P64x relays provide a four-stage overfluxing element. One stage can be set to operate with a definite time or inverse time delay (IDMT), this stage can be used to provide the protection trip output. There are also three other definite time stages which can be combined with the inverse time characteristic to create a combined multi-stage V/Hz trip operating characteristic using PSL. An inhibit signal is provided for the V/Hz>1 stage 1 only, which has the inverse time characteristic option. This allows a definite time stage to override a section of the inverse time characteristic if required. The inhibit has the effect of resetting the timer, the start signal and the trip signal. There is also one definite time alarm stage that can be used to indicate unhealthy conditions before damage has occurred to the machine.

The P64x relay offers an overfluxing protection element which can be used to raise an alarm or initiate tripping in the event of prolonged periods of transformer overfluxing. In addition, a differential current 5th harmonic blocking feature is also provided within the P64x, which can be used to prevent possible maloperation of the differential element under transient overfluxing conditions.

To make use of the time delayed overfluxing protection, the P64x relay must be supplied with a voltage signal which is representative of the primary system voltage on the source side of the transformer. The 5th harmonic blocking feature does not require a voltage signal. A 5th harmonic signal is derived from the differential current wave form on each phase and blocking of the low set biased characteristic is on a per phase basis.

2.4.2 Transformer Overfluxing

Transformer overfluxing might arise for the following reasons:

- High system voltage
- Generator full load rejection
- Ferranti effect with light loading transmission lines
- Low system frequency
- Generator excitation at low speed with AVR in service
- Geomagnetic disturbance
- Low frequency earth current circulation through a transmission system

The initial effects of overfluxing will be to increase the magnetizing current for a transformer. This current will be seen as a differential current. If it reaches a high level there would be a risk of differential protection tripping.

Persistent overfluxing may result in thermal damage or degradation of a transformer as a result of heating caused by eddy currents that may be induced in non-laminated metalwork of a transformer. The flux levels in such regions would normally be low, but excessive flux may be passed during overfluxed operation of a transformer.

The following protection strategy is proposed to address potential overfluxing conditions:

- Maintain protection stability during transient overfluxing
- Ensure tripping for persistent overfluxing

In most applications, the recommended minimum differential trip threshold for P64x, its filtering action and possible operation of the inrush detector will ensure stability of the differential element. If more difficult situations exist, the P64x relay is offered with a 5th harmonic differential current blocking facility. This facility could be applied with some study of the particular problem.

To ensure tripping for persistent overfluxing, due to high system voltage or low system frequency, the P64x is provided with time delayed Volts per Hertz protection. Where there is any risk of persistent geomagnetic overfluxing, with normal system voltage and frequency, the 5th harmonic differential current facility could be used to initiate tripping after a long time delay. This time delay would need to be programmed in the PSL as shown in the following PSL diagram.

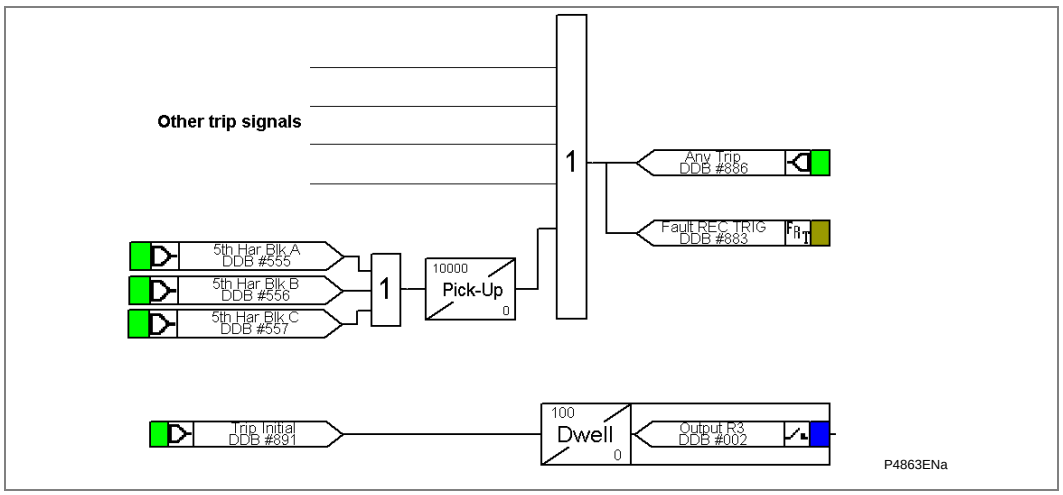


Figure 55 - Fifth harmonic tripping

2.4.3 Time Delayed Overfluxing Protection

Two overfluxing elements for HV and LV transformer sides are provided in the P643 and P645. One overfluxing element is available in the P642.

The following functions are provided:

- Alarm stage with definite time delay
- Trip stage V/Hz>1 with DT or IDMT time delay
- Trip stage V/Hz>2/3/4 with DT delay

The settings of the alarm stage should be such that the alarm signal can be used to prompt automatic or manual corrective action.

Protection against damage due to prolonged overfluxing is offered by a V/f protection element with a variable time tripping characteristic. The setting flexibility of this element, by adjustment of the time delay at various V/f values, makes it suitable for various applications. The manufacturer of the transformer or generator should be able to supply information about the short-time over-excitation capabilities, which can be used to determine appropriate settings for the V/f tripping element. The variable time overfluxing protection would be used to trip the transformer directly.

If preferred, the V/f tripping element can be set with a definite time characteristic.

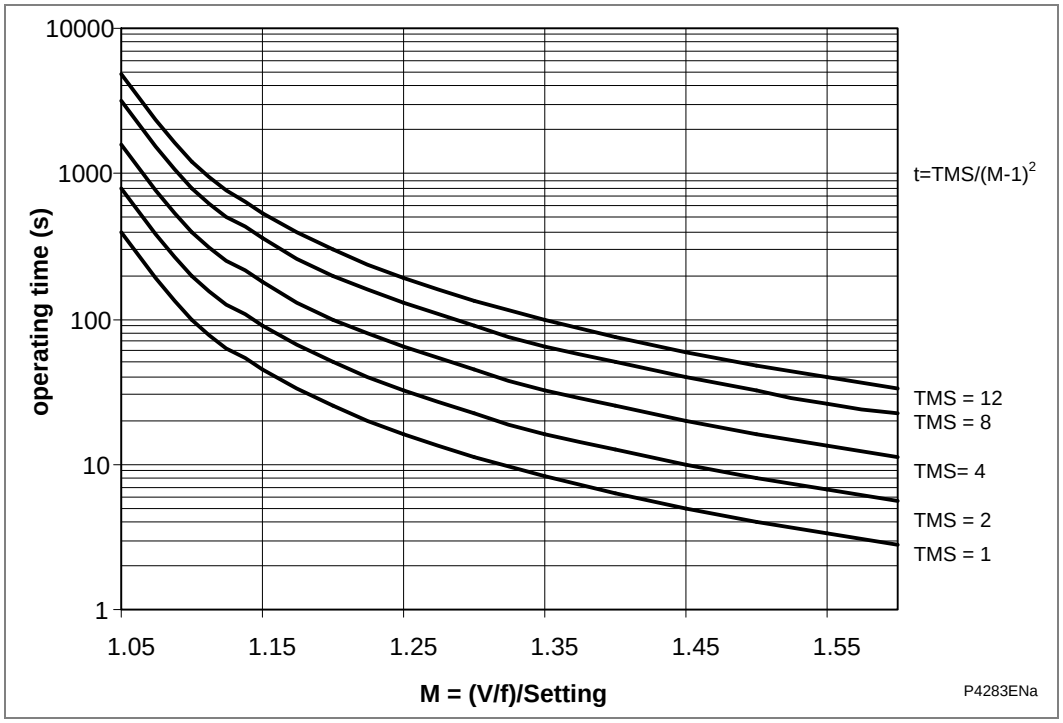


Figure 56 - Variable time overfluxing protection characteristic

2.4.4 Setting Guidelines for Overfluxing Protection

The V/Hz>1 overfluxing protection element trip stage can be selected by setting the V/Hz Trip Func cell to the required time delay characteristic: DT for definite time operation, IDMT, for inverse time operation. In the **V/Hz>x Status** cells, the four overfluxing protection trip stages can be set to **Enable** or **Disable**.

In the **V/Hz Alarm Status** cell, the overfluxing protection alarm stage can be set to **Enable** or **Disable**.

The pick up for the overfluxing elements depends on the nominal core flux density levels. Generator transformers are generally run at higher flux densities than transmission and distribution transformers, so they require a pick up setting and shorter tripping times which reflect this. Transmission transformers can also be at risk from overfluxing conditions and withstand levels should be consulted when deciding on the required settings.

IEEE Standard C37.91-2000 states that overexcitation of a transformer can occur whenever the ratio of the per unit voltage to per unit frequency (V/Hz) at the secondary terminals of a transformer exceeds its rating of 1.05 per unit (PU) on transformer base at full load, 0.8 power factor, or 1.1 PU at no load. Refer to subclause 4.1.6 in IEEE Std C57.12.00-2006 for further discussion on the capability of a transformer to operate above rated voltage and below rated frequency.

The element is set in terms of the actual ratio of voltage to frequency; the overfluxing threshold setting, **V/Hz>x Trip Set**, can therefore be calculated as shown below:

A 1.05 p.u. setting = 110/50 x 1.05 = 2.31

Where:

- The VT secondary voltage at rated primary volts is 110 V
- The rated frequency is 50 Hz

The overfluxing alarm stage threshold setting, **V/Hz Alarm Set**, shall be set lower than the trip stage setting to provide an indication that abnormal conditions are present and to alert an operator to adjust system parameters accordingly.

The time delay settings should be chosen to match the withstand characteristics of the protected transformer. If an inverse time characteristic is selected, select the time multiplier setting, **V/Hz>1 Trip TMS** so the operating characteristic closely matches the withstand characteristic of transformer. If a definite time setting is chosen for the trip stages the time delay is set in the **V/Hz>x Trip Delay** cells. The alarm stage time delay is set in the **V/Hz Alarm Delay** cell.

The three definite time stages and one DT/IDMT stage can be combined to create a combined multi-stage V/Hz trip operating characteristic using PSLThe “Multi-stage overfluxing characteristic” is shown in the next graph. The “Scheme Logic for Multi-Stage Overfluxing Characteristic” is shown in the next diagram.

Refer to manufacturers’ withstand characteristics before formulating these settings.

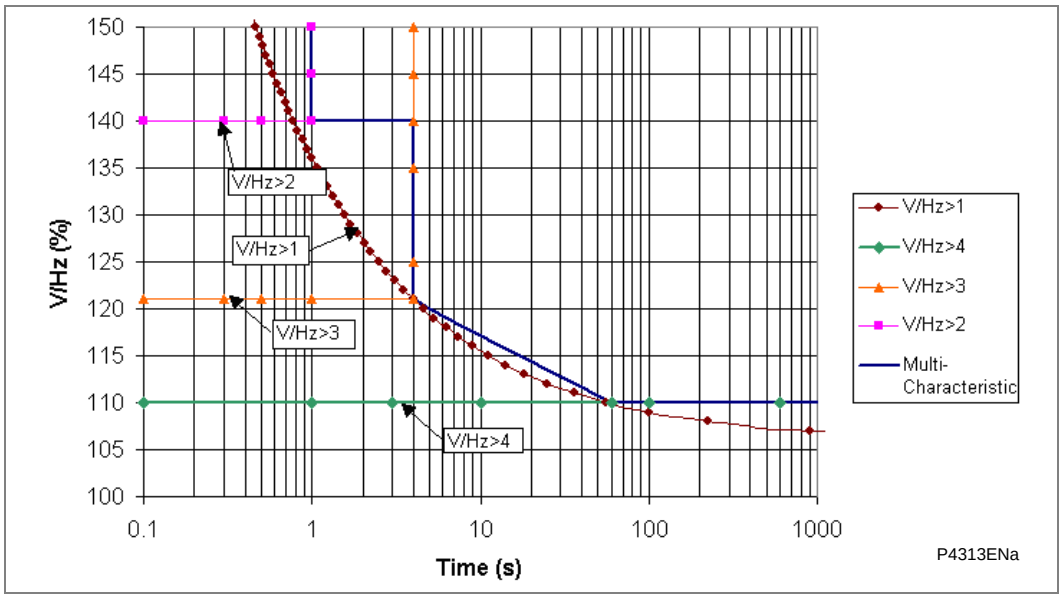


Figure 57 - Multi-stage overfluxing characteristic

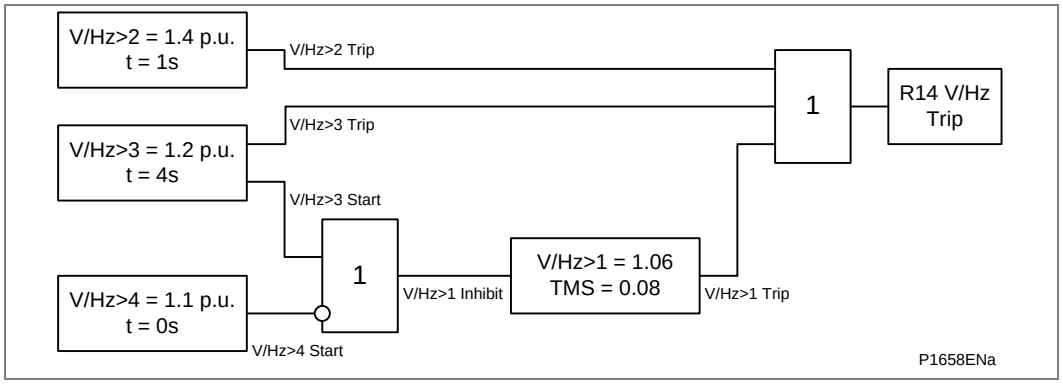


Figure 58 - Scheme logic for multi-stage overfluxing characteristic

2.4.5 5th Harmonic Blocking

The fifth Harmonic blocking feature is available for possible use to prevent unwanted operation of the low set differential element under transient overfluxing conditions.

When overfluxing occurs, the transformer core becomes partially saturated and the resultant magnetizing current waveforms increase in magnitude and become harmonically distorted. Such waveforms have a significant fifth harmonic content, which can be extracted and used as a means of identifying the abnormal operating condition.

The fifth harmonic blocking threshold is adjustable between 5 - 100%. The threshold should be adjusted so that blocking will be effective when the magnetizing current rises above the chosen threshold setting of the low-set differential protection.

For example, when a load is suddenly disconnected from a power transformer the voltage at the input terminals of the transformer may rise by 10-20% of the rated value. Since the voltage increases, the flux, which is the integral of the excitation voltage, also increases. As a result, the transformer steady state excitation current becomes higher. The resulting excitation current flows in one winding only and therefore appears as differential current which may rise to a value high enough to operate the differential protection. A typical differential current waveform during such a condition is shown in the Typical overflux current waveform diagram shown below. A typical setting for **Ih(5)%>** is 35%

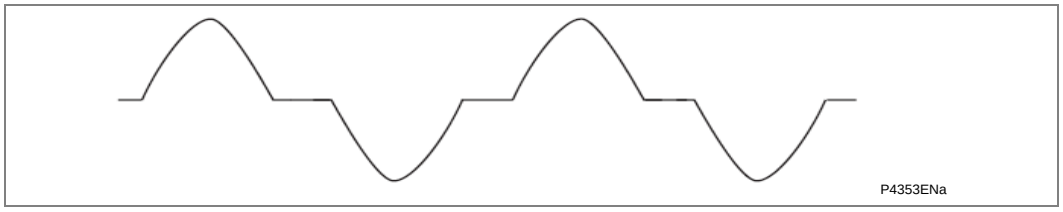


Figure 59 - Typical overflux current waveform

To offer some protection against damage due to persistent overfluxing that might be caused by a geomagnetic disturbance, the fifth harmonic blocking element can be routed to an output contact using an associated timer. Operation of this element could be used to give an alarm to the network control centre. If such alarms are received from a number of transformers, they could serve as a warning of geomagnetic disturbance so that operators could take some action to safeguard the power system. Alternatively this element can be used to initiate tripping in the event of prolonged pick up of a fifth harmonic measuring element. It is not expected that this type of overfluxing condition would be detected by the AC overfluxing protection. This form of time delayed tripping should only be applied in regions where geomagnetic disturbances are a known problem and only after proper evaluation through simulation testing.

Note	*The P64x determines the fundamental components and the fifth harmonic components from the line differential currents and provide fifth harmonic blocking option when the setting cell [3133: 5th harm blocked] under the* ***GROUP 1 DIFF PROTECTION*** *menu is set to* ***Enabled****.*

2.5 Phase Fault Overcurrent Protection (50/51)

A fault external to a transformer can result in damage to the transformer. If the fault is not cleared promptly, the resulting overload on the transformer can cause severe overheating and failure. Overcurrent relays may be used to clear the transformer from the faulted bus or line before the transformer is damaged. Overcurrent relays are often the only form of protection applied to small transformers. They are used for backup protection for larger transformers and both instantaneous and time delayed overcurrent can be applied.

The overcurrent inverse time characteristic on the HV side of the transformer must grade with the overcurrent inverse time characteristic on the LV side which in turn must grade with the LV outgoing circuits. The overcurrent function provides limited protection for internal transformer faults because sensitive settings and fast operation times are usually not possible. Sensitive settings are not possible because the pickup should allow overloading of the transformer when required. Fast operating times are not possible because of the grading required with respect to downstream overcurrent relays. To allow fast operating times, phase instantaneous overcurrent functions with low transient overreach are required.

The pickup of the time delayed overcurrent element can be set to 125-150% of the maximum MVA rating to allow overloading of the transformer according to IEEE Std. C37.91-2000.

As recommended by IEEE Std. C37.91-2000, the instantaneous overcurrent element should be set to pick up at a value higher than the maximum asymmetrical through fault current. This is usually the fault current through the transformer for a low-side three-phase fault. For instantaneous elements subject to transient overreach, a pickup of 175% (variations in settings of 125–200% are common) of the calculated maximum low-side three-phase symmetrical fault current generally provides sufficient margin to avoid false tripping for a low-side bus fault, while still providing protection for severe internal faults. Due to low transient overreach of the third and fourth overcurrent stages in the P64x, the instantaneous overcurrent element may be set to 120-130% of the through fault level of the transformer ensuring that the relay is stable for through faults. The instantaneous pickup setting should also consider the effects of transformer magnetizing inrush current.

Under fault conditions, currents are distributed in different ways according to winding connections. It is important to understand the fault current distribution under faults to set the overcurrent element. The following diagrams show various current distributions.

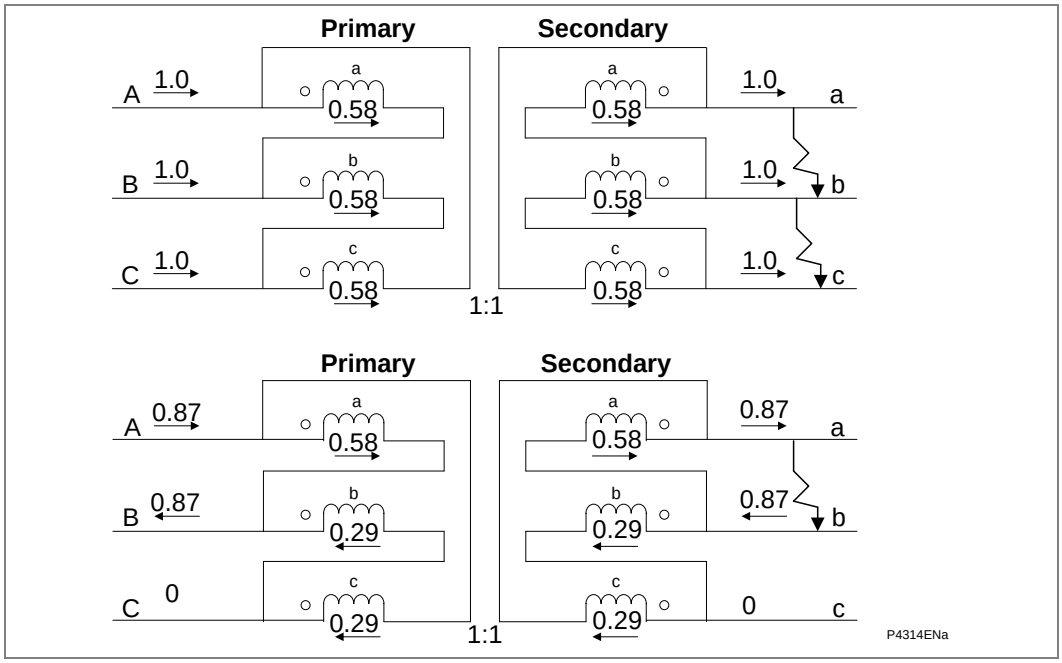


Figure 60 - Current distribution for Δ-Δ connected transformers

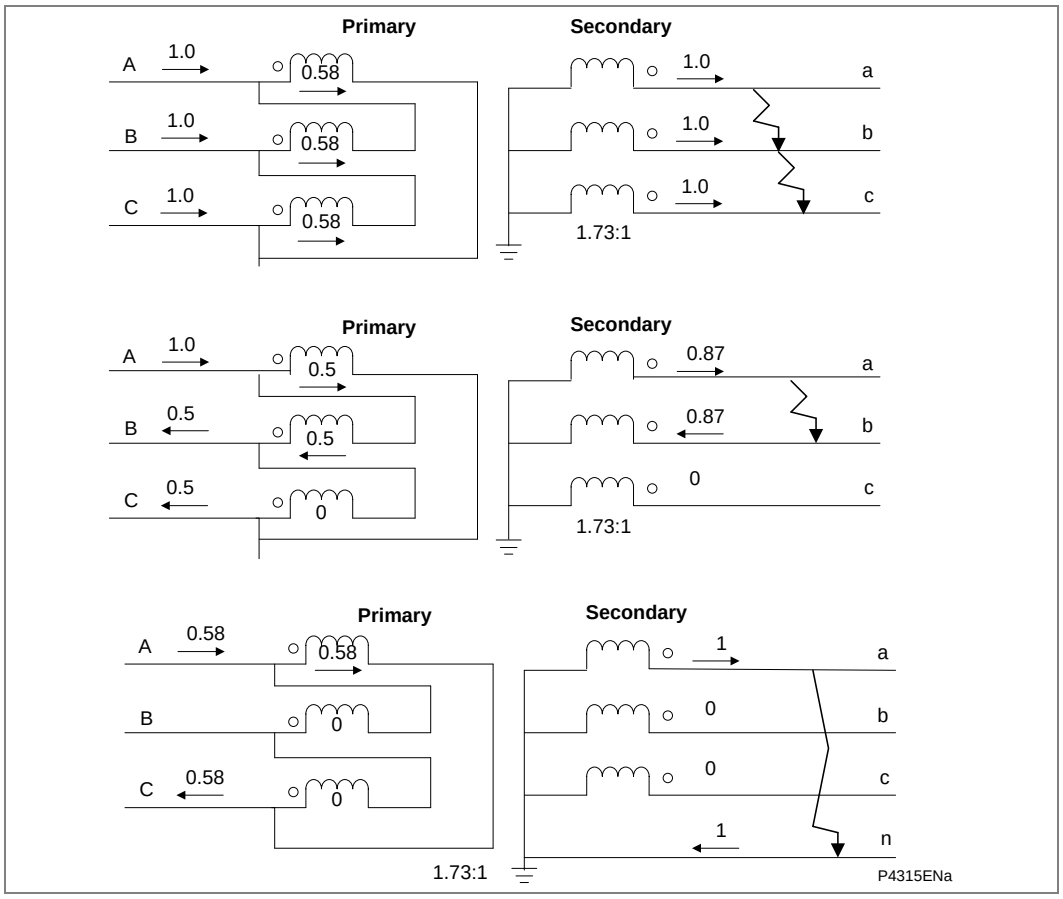


Figure 61 - Current distribution for Δ-Y connected transformers

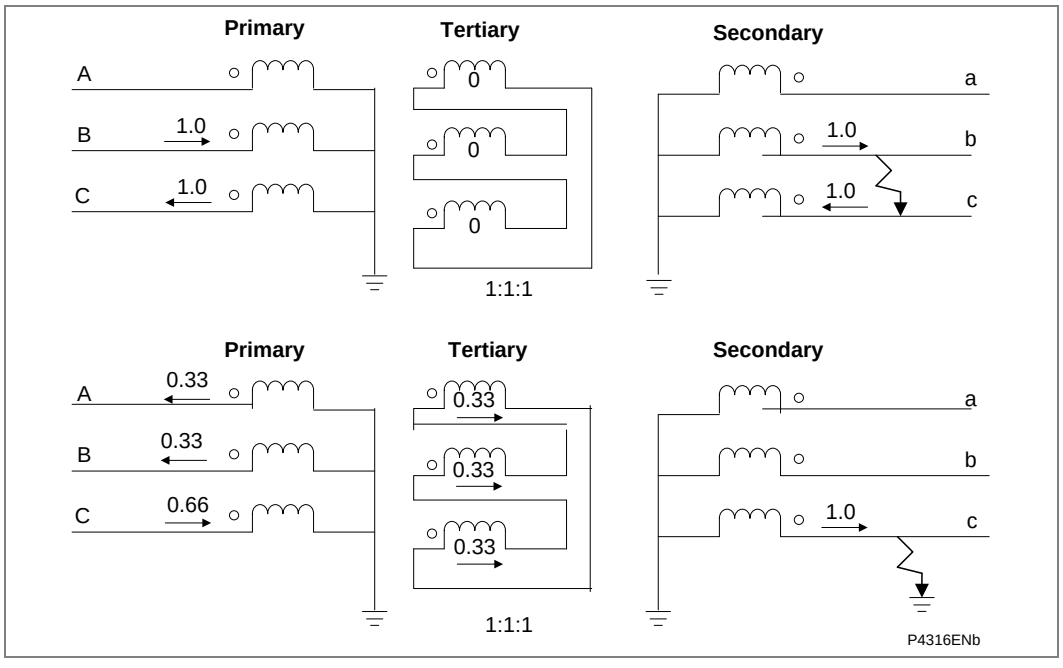


Figure 62 - Current distribution for Y-Δ-Y connected transformers

Transformers are mechanically and thermally limited in their ability to withstand short-circuit current for finite periods of time. For proper backup protection, the relays should operate before the transformer is damaged by an external fault. In setting transformer overcurrent relays, the short-time overload capability of the transformer in question should not be exceeded. Low values of 3.5 or less times normal base current may result from overloading rather than faults. Also the overcurrent characteristic should always be below the transformer damage curve.

A four-stage directional/non-directional overcurrent element is provided. This element can be used to provide time-delayed backup protection for the system and instantaneous protection providing fast operation for transformer faults.

The first two stages have a time delayed characteristic that can be set as either Inverse Definite Minimum Time (IDMT) or Definite Time (DT). The third and fourth stages have a definite time delay, which can be set to zero to produce instantaneous operation. Each stage can be selectively enabled or disabled.

In summary, there are a few application considerations to make when applying overcurrent relays to protect a transformer:

- When applying overcurrent protection to the HV side of a power transformer it is usual to apply a high set instantaneous overcurrent element in addition to the time delayed low-set, to reduce fault clearance times for HV fault conditions. Typically, this will be set to approximately 1.3 times the LV fault level, so that it will only operate for HV faults. A 30% safety margin is sufficient due to the low transient overreach of the third and fourth overcurrent stages. Transient overreach defines the response of a relay to DC components of fault current and is quoted as a percentage. A relay with a low transient overreach will be largely insensitive to a DC offset and may therefore be set more closely to the steady state AC waveform.
- The second requirement for this element is that it should remain inoperative during transformer energization, when a large primary current flows for a transient period. In most applications, the requirement to set the relay above the LV fault level will automatically result in settings that will be above the level of magnetizing inrush current.

All four overcurrent stages operate on the Fourier fundamental component. Therefore, for the third and fourth overcurrent stages in P64x relays, it is possible to apply settings corresponding to 40% of the peak inrush current while maintaining stability for the condition.

Where an instantaneous element is required to accompany the time delayed protection, as described above, the third or fourth overcurrent stage of the P64x relay should be used, as they have wider setting ranges.

2.5.1 Application of Timer Hold Facility

This feature may be useful in certain applications, for example when grading with electromechanical overcurrent relays which have inherent reset time delays. Setting of the hold timer to a value other than zero, delays the resetting of the protection element timers for this period therefore allowing the element to behave similarly to an electromechanical relay.

Another situation where the timer hold facility may be used to reduce fault clearance times is where intermittent faults may be experienced. An example of this may occur in a PVC insulated cable. In this application the fault energy can melt and reseal the cable insulation, extinguishing the fault.

When the reset time of the overcurrent relay is instantaneous, the relay will be repeatedly reset and not be able to trip until the fault becomes permanent. By using the timer hold facility the relay will integrate the fault current pulses, reducing fault clearance time.

The timer hold facility for the first and second overcurrent stages is settings **I>1 tReset** and I**>2 tReset**, respectively. This cell is not visible for the IEEE/US curves if an inverse time reset characteristic has been selected, as the reset time is then determined by the programmed time dial setting.

2.5.2 Setting Guidelines for Overcurrent Protection

The first or second stage of overcurrent protection can be selected by setting **I>1 Status** or **I>2 Status** to **Enabled**. The first or second stage are disabled if **I>1 Status** or **I>2 Status** are set to **Disabled**.

The first or second stage can provide backup protection for faults on the transformer and the system. It should be coordinated with downstream protection to provide discrimination for system faults, setting the current threshold **I>1/2 Current Set** and the time delay.

I>1 TMS	For IEC curves;
I>1 Time Dial	For US/IEEE curves;
I>1 Time Delay	For definite time accordingly.

The third and fourth stages of overcurrent protection can be enabled by setting **I>3 Status** or **I>4 Status** to **Enabled**, providing a definite time operating characteristic. The third and fourth stages are disabled if **I>3 Status** or **I>4 Status** are set to **Disabled**. The third or fourth stage can be set as an instantaneous overcurrent protection, providing protection against internal faults on the transformer. The overcurrent function has low transient overreach. It should be set to 120-130% of the through fault level of the transformer to ensure stability for through faults. Care must also be taken to ensure that it does not operate under magnetizing inrush conditions.

The directionality of the overcurrent element can be chosen by setting **I>1/2/3/4 Direction**.

2.5.3 Setting Guidelines for Voltage Controlled Overcurrent Protection

Two voltage controlled overcurrent elements are available. They can be set as directional or non-directional and definite time or inverse time. The voltage controlled overcurrent element threshold is reduced when the voltage is below a settable undervoltage threshold. **VCO>1 Curr' Set** and **VCO>1 K Setting** are set on the basis of the minimum fault-current condition independent of any load current requirements. This element is controlled by an undervoltage threshold, **VCO>1 V<Setting**. The undervoltage threshold is set below the normal minimum system load voltage, but above the maximum expected fault voltage. As a result, sensitive phase fault protection is provided with no risk of tripping due to load current.

2.6 Directional Phase Fault Overcurrent Protection (67)

If fault current can flow in both directions through a relay location, it is necessary to add directionality to the overcurrent relays to obtain correct co-ordination. Typical systems which require such protection are parallel feeders (both plain and transformer) and ring main systems, each of which are relatively common in distribution networks.

To give directionality to an overcurrent relay, it is necessary to provide it with a suitable reference, or polarizing, signal. The reference generally used is the system voltage, as its angle remains relatively constant under fault conditions. The phase fault elements of the relays are internally polarized by the quadrature phase-phase voltages, as shown here.

Phase of protection	Operating current	Polarizing voltage
A Phase	IA	VBC
B Phase	IB	VCA
C Phase	IC	VAB

Table 6 - Phase of protection, operating currents and polarizing voltages

It is therefore important to ensure the correct phasing of all current and voltage inputs to the relay, in line with the supplied application diagram.

Under system fault conditions, the fault current vector will lag its nominal phase voltage by an angle dependent on the system X/R ratio. It is a requirement that the relay operates with maximum sensitivity for currents lying in this region. This is achieved using the Relay Characteristic Angle (RCA) setting; this defines the angle by which the current applied to the relay must be displaced from the voltage applied to the relay to obtain maximum relay sensitivity. This is set in cell **I>Char Angle** in the **OVERCURRENT** menu.

A common application which requires the use of directional relays is considered below.

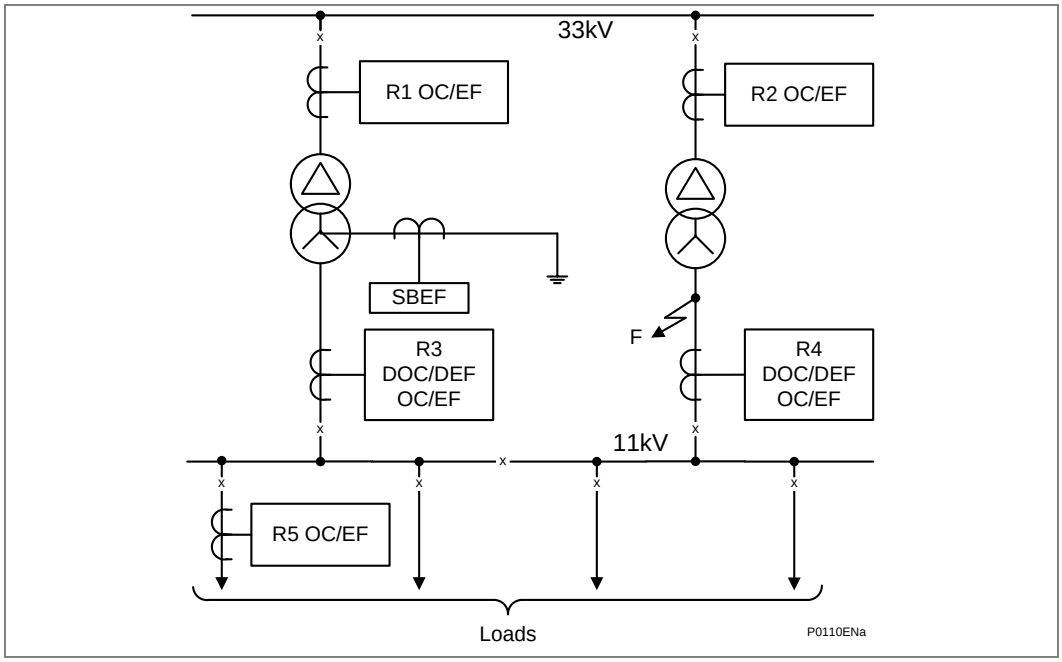


Figure 63 - Typical distribution system using parallel transformers

The above diagram shows a typical distribution system using parallel power transformers. In such an application, a fault at 'F' could result in the operation of both R3 and R4 relays and the subsequent loss of supply to the 11 kV busbar. Therefore with this system configuration it is necessary to apply directional relays at these locations set to look into their respective transformers. These relays should co-ordinate with the non-directional relays, R1 and R2; ensuring discriminative relay operation during such fault conditions.

In such an application, relays R3 and R4 may commonly require non-directional overcurrent protection elements to provide protection to the 11 kV busbar, in addition to providing a back-up function to the overcurrent relays on the outgoing feeders (R5).

When applying the P64x relays in the above application, stage 1 of the overcurrent protection of relays R3 and R4 would be set non-directional and time graded with R5, using an appropriate time delay characteristic. Stage 2 could then be set directional, looking back into the transformer, also having a characteristic which provides correct coordination with R1 and R2. IDMT or DT characteristics are selectable for both stages 1 and 2 and directionality of each of the overcurrent stages is set in cell **I>x Direction**.

Note	*The principles previously outlined for the parallel transformer application are equally applicable for plain feeders which are operating in parallel.*

2.7 Standby Earth Fault Protection (SBEF)

The parallel transformer application previously shown in the previous "Typical distribution system using parallel transformers" diagram requires Directional Earth Fault (DEF) protection at locations R3 and R4, to provide discriminative protection. However, to provide back-up protection for the transformer, busbar and other downstream earth fault devices, StandBy Earth Fault (SBEF) protection is also commonly applied. This function is fulfilled by a separate earth fault current input, fed from a single CT in the transformer earth connection. The HV, LV and TV earth fault elements of the P643 and P645 relay may be used to provide both the DEF and SBEF functions, respectively.

Where a Neutral Earthing Resistor (NER) is used to limit the earth fault level to a particular value, it is possible that an earth fault condition could cause a flashover of the NER and hence a dramatic increase in the earth fault current. For this reason, it may be appropriate to apply two-stage SBEF protection. The first stage should have suitable current and time characteristics which coordinate with downstream earth fault protection. The second stage may then be set with a higher current setting but with zero time delay, providing fast clearance of an earth fault which gives rise to an NER flashover.

The remaining two stages are available for customer-specific applications.

2.8 Directional Earth Fault (DEF) Protection

2.8.1 Residual Voltage Polarization

With earth fault protection, the polarizing signal needs to be representative of the earth fault condition. As residual voltage is generated during earth fault conditions, this quantity is commonly used to polarize DEF elements. The P643 and P645 relay internally derives this voltage from the 3-phase voltage input which must be supplied from either a five-limb or three single phase VTs. These types of VT design allow the passage of residual flux and consequently permit the relay to derive the required residual voltage. In addition, the primary star point of the VT must be earthed. A three-limb VT has no path for residual flux and is therefore unsuitable to supply the relay.

It is possible that small levels of residual voltage will be present under normal system conditions due to system imbalances, VT inaccuracies and relay tolerances. Hence, the relay includes a user-settable threshold **IN>VNPol set** which must be exceeded for the DEF function to be operational. The residual voltage measurement provided in the MEASUREMENTS 1 column of the menu may assist in determining the required threshold setting during the commissioning stage, as this will indicate the level of standing residual voltage present.

Note	*Residual voltage is nominally 180° out of phase with residual current. Consequently, the DEF elements are polarised from the -Vres quantity. This 180° phase shift is automatically introduced in the P64x relay.*

2.8.2 Negative Sequence Polarization

In certain applications, the use of residual voltage polarization of DEF may either be not possible to achieve, or problematic. An example of the former case would be where a suitable type of VT was unavailable, for example if only a three limb VT was fitted. An example of the latter case would be an HV/EHV parallel line application where problems with zero sequence mutual coupling may exist.

In either of these situations, the problem may be solved by the use of Negative Phase Sequence (NPS) quantities for polarization. This method determines the fault direction by comparison of NPS voltage with NPS current. The operating quantity, however, is still residual current.

This is available for selection on both the derived and measured standard earth fault elements. It requires a suitable voltage and current threshold to be set in cells **IN>V2pol set** and **IN>I2pol set**, respectively.

Negative sequence polarizing is not recommended for impedance earthed systems regardless of the type of VT feeding the relay. This is due to the reduced earth fault current limiting the voltage drop across the negative sequence source impedance (V2pol) to negligible levels. If this voltage is less than 0.5 volts the relay will cease to provide DEF protection.

2.8.3 General Setting Guidelines for DEF

When setting the Relay Characteristic Angle (RCA) for the directional overcurrent element, a positive angle setting was specified. This was because the quadrature polarizing voltage lagged the nominal phase current by 90°. The position of the current under fault conditions was leading the polarizing voltage so a positive RCA was required. With DEF, the residual current under fault conditions lies at an angle lagging the polarizing voltage. Therefore, negative RCA settings are required for DEF applications. This is set in the cell **I>Char Angle** in the relevant earth fault menu.

The following angle settings are recommended for a residual voltage polarized relay:

- Resistance earthed systems = 0°
- Distribution systems (solidly earthed) = –45°
- Transmission systems (solidly earthed) = –60°

For negative sequence polarization, the RCA settings must be based on the angle of the NPS source impedance, much the same as for residual polarizing. Typical settings are:

- Distribution systems –45°
- Transmission systems –60°

2.9 Negative Phase Sequence (NPS) Overcurrent Protection (46OC)

When applying traditional phase overcurrent protection, the overcurrent elements must be set higher than maximum load current, thereby limiting the element's sensitivity. Most protection schemes also use an earth fault element operating from residual current, which improves sensitivity for earth faults. However, certain faults may arise which can remain undetected by such schemes.

Any unbalanced fault condition will produce negative sequence current of some magnitude. Thus, a Negative Phase Sequence (NPS) overcurrent element can operate for both phase-to-phase and phase-to-earth faults.

- NPS overcurrent elements give greater sensitivity to resistive phase-to-phase faults, where phase overcurrent elements may not operate
- In certain applications, residual current may not be detected by an earth fault relay due to the system configuration. For example, an earth fault relay applied on the delta side of a delta-star transformer is unable to detect earth faults on the star side. However, negative sequence current will be present on both sides of the transformer for any fault condition, irrespective of the transformer configuration. Therefore, a NPS overcurrent element may be employed to provide time-delayed back-up protection for any uncleared asymmetrical faults downstream
- Where rotating machines are protected by fuses, loss of a fuse produces a large amount of negative sequence current. This is a dangerous condition for the machine due to the heating effects of NPS current and hence an upstream NPS overcurrent element may be applied to provide back-up protection for dedicated motor protection relays
- It may be required to simply alarm for the presence of NPS currents on the system. Operators may then investigate the cause of the unbalance

2.9.1 Setting Guidelines for NPS Overcurrent Protection

Since the NPS overcurrent protection does not respond to balanced-load or three-phase faults, negative sequence overcurrent relays may provide the desired overcurrent protection. This is particularly applicable to Δ−Y grounded transformers where only 58% of the secondary per unit phase-to-ground fault current appears in any one primary phase conductor. Backup protection can be particularly difficult when the Y is impedance-grounded.

2.9.1.1 Negative Phase Sequence (NPS) Current Threshold

A negative sequence relay can be connected in the primary supply to the transformer and set as sensitively as required to protect for secondary phase-to-ground or phase-to-phase faults. This function will also provide better protection than the phase overcurrent function for internal transformer faults. The NPS overcurrent protection should be set to coordinate with the low-side phase and ground relays for phase-to-ground and phase-to-phase faults. The current pickup threshold must also be set higher than the negative sequence current because of unbalanced loads. This can be set practically at the commissioning stage, making use of the relay measurement function to display the standing negative phase sequence current, and setting at least 20% above this figure.

Where the NPS element is required to operate for specific uncleared asymmetric faults, a precise threshold setting would have to be based on an individual fault analysis for that particular system due to the complexities involved. However, to ensure operation of the protection, the current pick-up setting must be set approximately 20% below the lowest calculated NPS fault current contribution to a specific remote fault condition.

Note	*In practice, if the required fault study information is unavailable, the setting must adhere to the minimum threshold previously outlined, employing a suitable time delay for co-ordination with downstream devices, this is vital to prevent unnecessary interruption of the supply resulting from inadvertent operation of this element.*

2.9.1.2 Time Delay for the NPS Overcurrent Element

As stated above, correct setting of the time delay for this function is vital. It should also be noted that this element is applied primarily to provide backup protection to other protective devices, or to provide an alarm or used in conjunction with neutral voltage displacement protection for interturn protection. Therefore in practice it would be associated with a long time delay if used to provide backup protection or an alarm.

Where the protection is used for backup protection or as an alarm it must be ensured that the time delay is set greater than the operating time of any other protective device (at minimum fault level) on the system which may respond to unbalanced faults, such as:

- Phase overcurrent elements
- Earth fault elements

2.9.1.3 Directionalizing the Negative Phase Sequence (NPS) Overcurrent Element

Where NPS current may flow in either direction through a relay location, such ring main systems, directional control of the element should be used.

Directionality is achieved by comparison of the angle between the NPS voltage and the NPS current and the element may be selected to operate in either the forward or reverse direction. A suitable relay characteristic angle setting (**I2> Char Angle**) is chosen to provide optimum performance. This setting should be set equal to the phase angle of the negative sequence current with respect to the inverted negative sequence voltage (–V2), to be at the center of the directional characteristic.

The angle that occurs between V2 and I2 under fault conditions is directly dependent on the negative sequence source impedance of the system. However, typical settings for the element are as follows:

- For a transmission system the RCA should be set equal to –60°
- For a distribution system the RCA should be set equal to –45°

For the NPS directional elements to operate, the relay must detect a polarizing voltage above a minimum threshold, **I2> V2pol Set**. This must be set in excess of any steady state NPS voltage. This may be determined during the commissioning stage by viewing the NPS measurements in the relay.

2.10 Undervoltage Protection Function (27)

Undervoltage conditions may occur on a power system for a variety of reasons, some of which are outlined below:

- Increased system loading. Generally, some corrective action would be taken by voltage regulating equipment such as AVRs or On Load Tap Changers, to bring the system voltage back to its nominal value. If the regulating equipment is unsuccessful in restoring healthy system voltage, tripping with an undervoltage relay will be required following a suitable time delay.
- Faults occurring on the power system result in a reduction in voltage of the phases involved in the fault. The proportion by which the voltage decreases is directly dependent on the type of fault, method of system earthing and its location with respect to the relaying point. Consequently, co-ordination with other voltage and current-based protection devices is essential to achieve correct discrimination.
- Complete loss of busbar voltage. This may occur due to fault conditions present on the incomer or busbar itself, resulting in total isolation of the incoming power supply. For this condition, it may be a requirement for each of the outgoing circuits to be isolated, so that when supply voltage is restored, the load is not connected. Therefore, the automatic tripping of a feeder on detection of complete loss of voltage may be required. This may be achieved by a three-phase undervoltage element.
- Where outgoing feeders from a busbar are supplying induction motor loads, excessive dips in the supply may cause the connected motors to stall, and should be tripped for voltage reductions which last longer than a pre-determined time. Both the under and overvoltage protection functions can be found in the relay menu Volt Protection.

2.10.1 Setting Guidelines for Undervoltage Protection

The undervoltage protection is an optional feature within the P64x. It is available on request of the three-phase VT input.

The undervoltage protection can be set to operate from phase-phase or phase-neutral voltage as selected by **V< Measur't Mode**. Single or three-phase operation can be selected in **V< Operate Mode**. When Any Phase is selected, the element will operate if any phase voltage falls below setting, when Three-phase is selected the element will operate when all three-phase voltages are below the setting.

In most applications, undervoltage protection is not required to operate during system earth fault conditions. If this is the case, the element should be selected in the menu to operate from a phase to phase voltage measurement, as this quantity is less affected by single-phase voltage depressions due to earth faults.

The voltage threshold setting for the undervoltage protection should be set at some value below the voltage excursions that may be expected under normal system operating conditions. This threshold is dependent upon the system in question but typical healthy system voltage excursions may be in the order of -10% of nominal value.

Similar comments apply regarding a time setting for this element, i.e. the required time delay is dependent upon the time for which the system is able to withstand a depressed voltage. As mentioned earlier, if motor loads are connected, then a typical time setting may be in the order of 0.5 seconds.

Stage 1 may be selected as either IDMT (for inverse time delayed operation), DT (for definite time delayed operation) or Disabled, in the **V<1 Function** cell. Stage 2 is definite time only and is **Enabled** or **Disabled** in the **V<2 Status** cell. The time delay (**V<1 TMS** for IDMT curve; **V<1 Time Delay**, **V<2 Time Delay** for definite time) should be adjusted accordingly.

Stage 2 can be set as an alarm stage to warn the user of unusual voltage conditions so that corrections can be made.

If only a single phase VT signal is available and the user requires an undervoltage alarm, then the P643/P645 (three-phase VT input required) may provide this alarm as long as the VTS status is set to disable. Setting the VTS status to disable will prevent the Fast VTS Block signal from blocking the undervoltage element. The V< Measur't Mode is set Phase-Neutral and the V< Operate Mode is set Three Phase.

2.11 Overvoltage Protection (59)

As previously discussed, undervoltage conditions are relatively common, as they are related to fault conditions. However, overvoltage conditions are also a possibility and are generally related to loss of load conditions.

- Under conditions of load rejection, the supply voltage will increase in magnitude. This situation would normally be rectified by voltage regulating equipment such as AVRs or on-load tap changers. However, failure of this equipment to bring the system voltage back within prescribed limits leaves the system with an overvoltage condition which must be cleared to preserve the life of the system insulation. Hence, overvoltage protection that is suitably time-delayed to allow for normal regulator action may be applied.
- Also, during earth fault conditions on a power system, there may be an increase in the healthy phase voltages. Ideally the system should be designed to withstand such overvoltages for a defined period.

Overvoltage protection prevents insulation damage due to excessive voltages. Some of the causes of overvoltage at system frequency are listed below:

- Sudden loss of load caused by the disconnection of a heavily loaded power line
- Lightly loaded long transmission lines with high capacitance
- Phase to earth faults in unearthed or high impedance earthed systems
- Incorrect operation of a voltage regulator or wrong settings under manual voltage
- Overspeed of generator when disconnected from the network and incorrect operation of the machine AVR control

Transformers must not be subject to prolonged overvoltage because the insulation would be damaged. For maximum efficiency they are operated near the knee of their saturation curve, so at voltages above about 110% of rated, the exciting current becomes very high. A few percent increase in voltage results in a very large increase in exciting current. These large currents can destroy the unit if not reduced promptly. Protection against overvoltage is seldom applied directly, but it is included in regulating and control devices for the power system. On the other hand, overvoltage for generator-transformer units is more likely to occur, therefore an overvoltage protection may be considered.

2.11.1 Setting Guidelines for Overvoltage Protection

The overvoltage protection is an optional feature in the P64x. It is available on request of the three-phase VT input.

The inclusion of the two stages and their respective operating characteristics allows for a number of possible applications:

- Use of the IDMT characteristic gives the option of a longer time delay if the overvoltage condition is only slight but results in a fast trip for a severe overvoltage. As the voltage settings for both of the stages are independent, the second stage could then be set lower than the first to provide a time delayed alarm stage if required .
- Alternatively, if preferred, both stages could be set to definite time and configured to provide the required alarm and trip stages.
- If only one stage of overvoltage protection is required, or if the element is required to provide an alarm only, the remaining stage may be disabled within the relay menu.

This type of protection must be co-ordinated with any other overvoltage relays at other locations on the system. This should be carried out in a similar manner to that used for grading current operated devices.

Stage 1 may be selected as either IDMT (for inverse time delayed operation), DT (for definite time delayed operation) or Disabled, in the **V>1 Function** cell. Stage 2 has a definite time delayed characteristic and is Enabled or Disabled in the **V>2 Status** cell. The time delay (**V>1 TMS** for IDMT curve; **V>1 Time Delay**, **V>2 Time Delay** - for definite time) should be selected accordingly.

The overvoltage protection can be set to operate from Phase-Phase or Phase-Neutral voltage as selected by the **V> Measur't Mode** cell. Single or three-phase operation can be selected in the **V> Operate Mode** cell. When **Any Phase** is selected the element will operate if any phase voltage is above setting; when **Three-phase** is selected the element will operate when all three-phase voltages are above the setting.

Transformers can typically withstand a 110% overvoltage condition continuously. The withstand times for higher overvoltages should be declared by the transformer manufacturer.

To prevent operation during earth faults, the element should operate from the phase-phase voltages. To achieve this **V>1 Measur't Mode** can be set to **Phase-Phase** with **V>1 Operating Mode** set to **Three-phase**. The overvoltage threshold **V>1 Voltage Set** should typically be set to 100% - 120% of the nominal phase-phase voltage seen by the relay. The time delay **V>1 Time Delay** should be set to prevent unwanted tripping of the delayed overvoltage protection function due to transient over voltages that do not pose a risk to the transformer. The typical delay to be applied would be 1s - 3s, with a longer delay being applied for lower voltage threshold settings.

The second stage can be used to provide instantaneous high-set over voltage protection. The typical threshold setting to be applied, **V>2 Voltage Set**, would be 130 - 150% of the nominal phase-phase voltage seen by the relay, depending on transformer manufacturers' advice and the utilities practice. For instantaneous operation, the time delay, **V>2 Time Delay**, should be set to 0 s.

If phase to neutral operation is selected, care must be taken to ensure that the element will grade with other protections during earth faults, where the phase-neutral voltage can rise significantly.

2.12 Residual Overvoltage/Neutral Voltage Displacement Protection Function (59N)

On a healthy three phase power system, the addition of each of the three phase to earth voltages is nominally zero, as it is the vector addition of three balanced vectors at 120° to one another. However, when an earth (ground) fault occurs on the primary system this balance is upset and a '**residual**' voltage is produced.

Note	*This condition causes a rise in the neutral voltage with respect to earth which is commonly referred to as **neutral voltage displacement** or NVD.*

In the P643 and P645, the residual overvoltage is an optional feature. It is calculated by adding up the three-phase voltage vectors corresponding to the optional three-phase voltage input. Hence, a residual voltage element can be used to offer earth fault protection on such a system. This condition causes a rise in the neutral voltage with respect to earth that is commonly referred to as Neutral Voltage Displacement or NVD.

2.12.1 Setting Guidelines for Residual Overvoltage/Neutral Voltage Displacement Protection

Stage 1 may be selected as either **IDMT** (inverse time operating characteristic), **DT** (definite time operating characteristic) or **Disabled**, in the **VN>1 Function** cell. Stage 2 operates with a definite time characteristic and is **Enabled** or **Disabled** in the **VN>2 Status** cell. The time delay. (**VN>1 TMS** for IDMT curve; **V>1 Time Delay**, **V>2 Time Delay** for definite time) should be selected in accordance with normal relay coordination procedures to ensure correct discrimination for system faults.

It must be ensured that the voltage setting of the element is set above any standing level of residual voltage that is present on the system. A typical setting for residual overvoltage protection is 5 V.

The second stage of protection can be used as an alarm stage on unearthed or very high impedance earthed systems where the system can be operated for an appreciable time under an earth fault condition.

2.13 Negative Phase Sequence (NPS) Overvoltage Protection (47)

Where an incoming feeder is supplying a switchboard that is feeding rotating plant (e.g. a motor), correct phasing and balance of the ac supply is essential. Incorrect phase rotation could result in any connected machines rotating in the wrong direction. For some hydro machines, two-phases can be swapped to allow the machine to rotate in a different direction to act as a generator or a motor pumping water.

Any unbalanced condition occurring on the incoming supply will result in the presence of Negative Phase Sequence (NPS) components of voltage. In the event of incorrect phase rotation, the supply voltage would effectively consist of 100% NPS voltage only.

The P643 and P645 relays include a NPS overvoltage element that responds to NPS voltage that may result from a fault or misconnection in a balanced three-phase system. This element monitors the input voltage rotation and magnitude (normally from a bus connected voltage transformer).

The NPS overvoltage element can also be used to provide an additional check to indicate a phase-earth or phase-phase fault is present for the voltage controlled overcurrent protection in the PSL as shown in the *NPS overvoltage control – PSL configuration* diagram below. In this application the NPS overvoltage protection can be accelerated when the CB operating time is <60 ms) to prevent incorrect operation when closing the CB due to pole scattering. However, when the CB is closed there is no need to inherently slow the protection start (typical accelerated operating time is <40 ms). The V2>1 Accelerate signal (DDB 663) connected to CB Closed signal (DDB 719, 721, 723, 725, 727) can be used to accelerate the protection start as shown in the *V2>1 Accelerate – PSL configuration* diagram below.

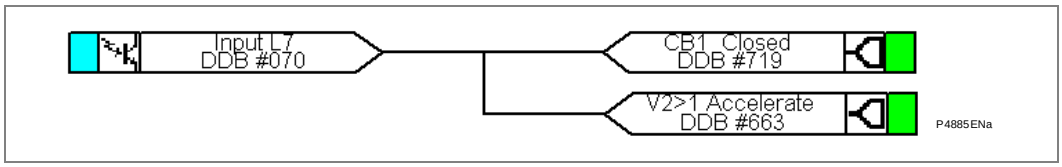


Figure 64 - V2>1 Accelerate – PSL configuration

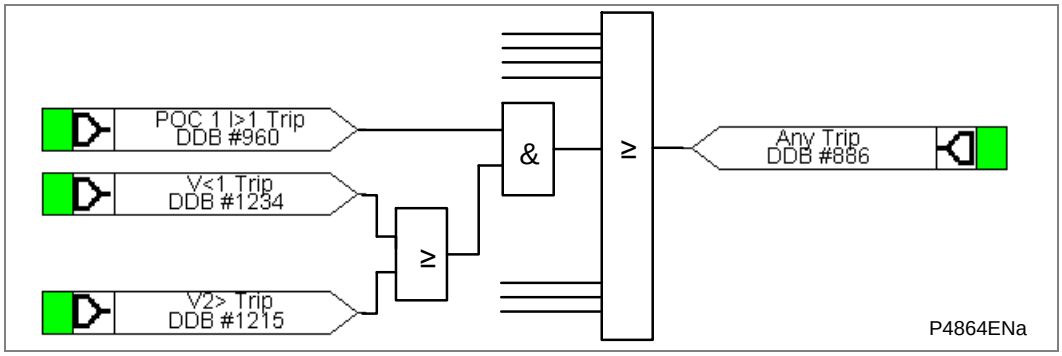


Figure 65 - NPS overvoltage control – PSL configuration

2.13.1 Setting Guidelines

As the primary concern is the detection of incorrect phase rotation (rather than small unbalances), a sensitive setting is not required. You must ensure that the setting is above any standing NPS voltage that may be present due to imbalances in the measuring VT, relay tolerances etc. A setting of approximately 15% of rated voltage may be typical.

Note	*Standing levels of NPS voltage (V2) are displayed in "Measurements 1" column of the relay menu, labeled "V2 Magnitude".*

Hence, if more sensitive settings are required, they may be determined during the commissioning stage by viewing the actual level that is present.

The operation time of the element is highly dependent on the application. A typical setting would be in the region of 5 s. If the NPS overvoltage element is used to provide an additional check for the voltage controlled overcurrent element, set the time delay to 0 s.

2.14 Underfrequency Protection (81U)

Generation and utilization need to be well balanced in any industrial, distribution or transmission network. As load increases, the generation needs to be stepped up to maintain frequency of the supply because there are many frequency-sensitive electrical apparatus that can be damaged when network frequency departs from the allowed band for safe operation. At times, when sudden overloads occur, the frequency drops at a rate decided by the system inertia constant, magnitude of overload, system damping constant and various other parameters. Unless corrective measures are taken at the appropriate time, frequency decay can go beyond the point of no return and cause widespread network collapse. In a wider scenario, this can result in “Blackouts”. To put the network back in healthy condition, a considerable amount of time and effort is required to resynchronize and re-energize.

Protective relays that can detect a low frequency condition are generally used in such cases to disconnect unimportant loads to save the network, by re-establishing the “generation-load equation”. However, with such devices, the action is initiated only after the event and while some salvaging of the situation can be achieved, this form of corrective action may not be effective enough and cannot cope with sudden load increases, causing large frequency decays in very short times. In such cases a device that can anticipate the severity of frequency decay and act to disconnect loads before the frequency actually reaches dangerously low levels, can become very effective in containing damage.

During severe disturbances, the frequency of the system oscillates as various generators try to synchronize on to a common frequency. The measurement of instantaneous rate of change of frequency can be misleading during such a disturbance. The frequency decay needs to be monitored over a longer period to make the correct decision for load shedding.

Normally, generators are rated for a lifetime operation in a particular band of frequency and operation outside this band can cause mechanical damage to the turbine blades. Protection against such contingencies is required when frequency does not improve even after load shedding steps have been taken and can be used for operator alarms or turbine trips in case of severe frequency decay.

While load shedding leads to an improvement in the system frequency, the disconnected loads need to be reconnected after the system is stable again. Loads should only be restored if the frequency remains stable for some period of time, but minor frequency excursions can be ignored during this time period. The number of load restoration steps are normally less than the load shedding steps to reduce repeated disturbances while restoring load.

Four independent definite time-delayed stages of underfrequency protection are offered.

2.14.1 Setting Guidelines for Underfrequency Protection

To minimize the effects of underfrequency on a system, a multi-stage load-shedding scheme may be used with the plant loads prioritized and grouped. During an underfrequency condition, the load groups are disconnected sequentially depending on the level of underfrequency, with the highest priority group being the last one to be disconnected.

The effectiveness of each stage of load shedding depends on what proportion of the power deficiency it represents. If the load shedding stage is too small compared to the prevailing generation deficiency, the improvement in frequency may be non-existent. This aspect should be considered when forming the load groups.

Time delays should be sufficient to override any transient dips in frequency, as well as to provide time for the frequency controls in the system to respond. This should be balanced against the system survival requirement since excessive time delays may cause the system stability to be in jeopardy. Time delay settings of 5 to 20 s are typical.

Each stage of under frequency protection may be selected as **Enabled** or **Disabled** in the **F<x Status** cells. The frequency pickup setting, **F<x Setting**, and time delays, **F<x Time Delay**, for each stage should be selected accordingly.

The under frequency protection function could be used to initiate local system load shedding when required. Four stages under frequency/load shedding can be provided.

2.15 Overfrequency Protection Function (81O)

Overfrequency running of a generator arises when the mechanical power input to the machine exceeds the electrical output. This could happen, for instance, when there is a sudden loss of load due to tripping of an outgoing feeder from the plant to a load centre. Under such over speed conditions, the governor should respond quickly to obtain a balance between the mechanical input and electrical output, thereby restoring normal frequency. Over frequency protection is required as a backup to cater for slow response of frequency control equipment.

The relay has two independent time-delayed stages of overfrequency protection.

2.15.1 Setting Guidelines for Overfrequency Protection

Following faults on the network, or other operational requirements, it is possible that various subsystems will be formed within the power network and it is likely that each of these subsystems will suffer from a generation to load imbalance. The “islands” where generation exceeds the existing load will be subject to over frequency conditions, the level of frequency being a function of the percentage of excess generation. Severe over frequency conditions may be unacceptable to many industrial loads, since running speeds of motors will be affected. The overfrequency element of the P64x can be suitably set to sense this contingency.

The settings for the overfrequency element depend on the maximum frequency that the equipment can tolerate for a given time period.

Each stage of overfrequency protection may be selected as **Enabled** or **Disabled** in the **F>x Status** cells. The frequency pickup setting **F>x Setting** and time delays **F>x Time Delay** for each stage should be selected accordingly.

2.16 Circuit Breaker Fail (CBF) Protection

Following inception of a fault one or more main protection devices will operate and issue a trip output to the circuit breaker(s) associated with the faulted circuit. Operation of the circuit breaker is essential to isolate the fault, and prevent damage / further damage to the power system. For transmission/sub-transmission systems, slow fault clearance can also threaten system stability. It is therefore common practice to install Circuit Breaker Failure (CBF) protection, which monitors that the circuit breaker has opened within a reasonable time. If the fault current has not been interrupted following a set time delay from circuit breaker trip initiation, CBF protection will operate.

CBF operation can be used to backtrip upstream circuit breakers to ensure that the fault is isolated correctly. CBF operation can also reset all start output contacts, ensuring that any blocks asserted on upstream protection are removed.

2.16.1 Reset Mechanisms for Breaker Fail Timers

It is common practice to use low set undercurrent elements in protection relays to indicate that Circuit Breaker (CB) poles have interrupted the fault or load current, as required. This covers the following situations:

- Where CB auxiliary contacts are defective, or cannot be relied on to definitely indicate that the CB has tripped.
- Where a CB has started to open but has become jammed. This may result in continued arcing at the primary contacts, with an additional arcing resistance in the fault current path. Should this resistance severely limit fault current, the initiating protection element may reset. Therefore reset of the element may not give a reliable indication that the CB has opened fully.

For any protection function requiring current to operate, the relay uses operation of undercurrent elements (I<) to detect that the necessary circuit breaker poles have tripped and reset the CB fail timers. However, the undercurrent elements may not be reliable methods of resetting circuit breaker fail in all applications. For example:

- Where non-current operated protection, such as under/overvoltage or under/overfrequency, derives measurements from a line connected voltage transformer. Here, I< only gives a reliable reset method if the protected circuit would always have load current flowing. Detecting drop-off of the initiating protection element might be a more reliable method.
- Where non-current operated protection, such as under/overvoltage or under/overfrequency, derives measurements from a busbar connected voltage transformer. Again, using I< would rely on the feeder normally being loaded. Also, tripping the circuit breaker may not remove the initiating condition from the busbar, so drop-off of the protection element may not occur. In such cases, the position of the circuit breaker auxiliary contacts may give the best reset method.

2.16.2 Setting Guidelines for CBF Protection

2.16.2.1 Breaker Fail Timer Settings

The following “Breaker failure time chart” diagram shows the time chart during normal and breaker failure operation. The maximum clearing time should be less than the critical clearing time which is determined by a stability study. The CBF back-up trip time delay considers the maximum breaker clearing time, the CBF reset time and a safety margin. Typical circuit breakers clearing times are 1.5 or 3 cycles. The CBF reset time should be short enough to avoid CBF back-trip during normal operation. Phase and ground undercurrent elements must be asserted for the CBF to reset. The assertion of the undercurrent elements might be delayed due to the subsidence current that might be flowing through the secondary AC circuit. The subsidence current is the result of the decaying flux in the CT core once the primary current has been interrupted. The delay in asserting the undercurrent elements will cause an unwanted breaker failure operation. In the P64x, a zero crossing detection technique has been implemented to avoid this unwanted operation.

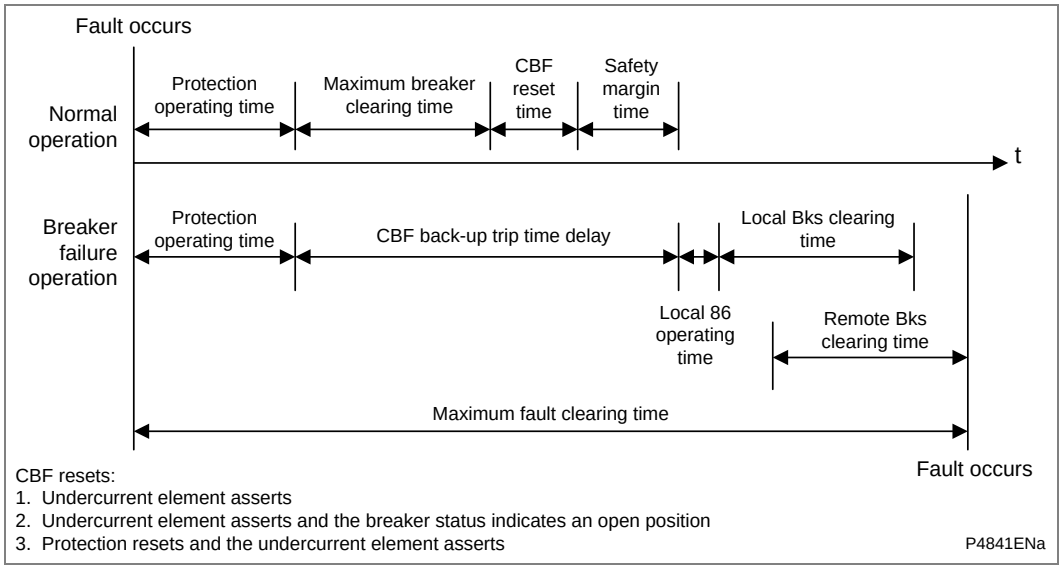


Figure 66 - Breaker failure time chart

Typical timer settings to use are as follows:

CB fail reset mechanism	tBF time delay	Typical delay for 2 cycle circuit breaker
Initiating element reset	CB interrupting time + element reset time (max.) + error in tBF timer + safety margin	50 + 50 + 10 + 50 = 160 ms
CB open	CB auxiliary contacts opening/ closing time (max.) + error in tBF timer + safety margin	50 + 10 + 50 = 110 ms
Undercurrent elements	CB interrupting time + undercurrent element (max.) + safety margin operating time	50 + 25 + 50 = 125 ms

Table 7 - Typical timer settings

Note	*All CB Fail resetting involves the operation of the undercurrent elements. Where element reset or CB open resetting is used the undercurrent time setting should still be used if this proves to be the worst case.*

The examples above consider direct tripping of a 2½ -cycle circuit breaker.

Note	*Where auxiliary tripping relays are used, an additional 10 to 15 ms must be added to allow for trip relay operation.*

2.16.2.2 Breaker Fail Undercurrent Settings

The phase undercurrent settings (I<) must be set less than load current, to ensure that I< operation indicates that the circuit breaker pole is open. A typical setting for overhead line or cable circuits is 20% In, with 5% In common for generator circuit breaker CBF.

2.16.3 Example 1

Consider an application having two breakers on the HV side and two breakers on the LV side. Overcurrent1 has been set to HV winding and Overcurrent2 to LV winding. Stages 1 of Overcurrent1 and 2 are used as back-up protection. The HV breakers must open when Overcurent1 is asserted but not Overcurrent2. The LV breakers must open when Overcurent2 is asserted but not Overcurrent1. The circuit breaker failure timers of breakers 1 and 2 should not be initiated when Overcurrent2/Stage 1 is asserted, and the circuit breaker failure timers of breakers 4 and 5 should not be initiated when Overcurrent1/Stage 1 is asserted. As indicated in the CB fail logic given in the Operation Chapter, the Any Trip signal starts all the breaker failure timers. POC 1 I>1 Trip and POC 2 I>1 Trip signals should be removed from the any trip mapping in PSL. This is to avoid starting the HV circuit breaker failure timers due to POC 2 I>1 Trip and starting the LV circuit breaker failure timers due to POC 1 I>1 Trip. From the circuit breaker Our scheme requires the HV breakers to trip on Idiff, HV I>1, and HV IN>1. The LV breakers trip on Idiff, LV I>1 and LV IN>1.

Removing POC 1 I>1 Trip and POC 2 I>1 Trip from the any trip mapping prevents lighting the any trip led when POC 1 I>1 Trip or POC 2 I>1 Trip is asserted.

To generate fault records due to POC 1 I>1 Trip and POC 2 I>1 Trip, this signals should be configured in the fault record trigger in PSL.

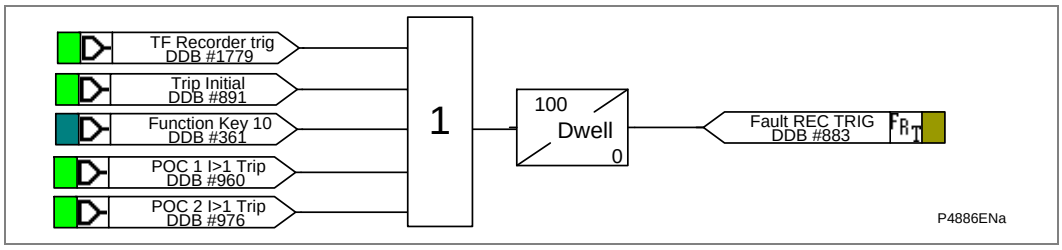


Figure 67 - Fault record trigger configuration

Configure POC 1 I>1 Trip to Extern CB1 trip and Extern CB2 trip in PSL to initiate HV circuit breaker failure timers. Configure POC 2 I>1 Trip to Extern CB4 trip and Extern CB5 trip in PSL to initiate LV circuit breaker failure timers.

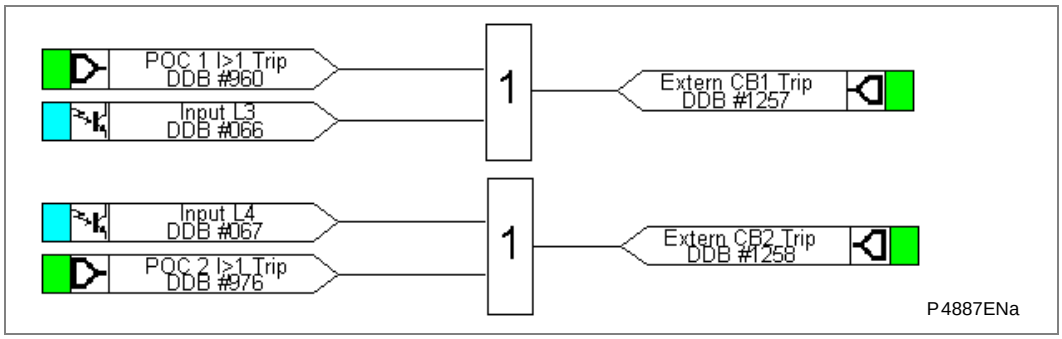


Figure 68 - External CB Trip

2.17 Resistive Temperature Device (RTD) Thermal Protection

Prolonged overloading of transformers may cause their windings to overheat, resulting in premature ageing of the insulation, or in extreme cases, insulation failure. To protect against any general or localized overheating, the relay can accept inputs from up to 10 - 3-wire Type A PT100 Resistive Temperature Device (RTD) sensors.

Such probes can be strategically placed in areas of the equipment that are susceptible to overheating or heat damage. This could protect against winding hot spot overheating or overtemperature in the bulk of the insulating oil.

Typically, a PT100 RTD probe can measure temperature in the range –40° to +300°C. The resistance of these devices changes with temperature, at 0°C they have a resistance of 100 Ω. The temperature at each probe location can be determined by the relay, and is available for:

- Temperature monitoring, displayed locally, or remotely using the relay communications
- Alarming, if a temperature threshold is exceeded for longer than a set time delay
- Tripping, if a temperature threshold is exceeded for longer than a set time delay

If the measured resistance is outside the permitted range, an RTD failure alarm will be raised, indicating an open or short circuit RTD input.

Note	*Direct temperature measurement can provide more reliable thermal protection than devices that use a thermal replica energized from phase current. The latter is susceptible to inaccuracies in time constants used by the replica model, and also inaccuracies due to the variation in ambient temperature.*

See the *Installation* chapter for recommendations on RTD connections and cables.

2.17.1 Setting Guidelines for RTD Thermal Protection

Each RTD can be enabled by setting the relevant bit in **Select RTD**. For example if Select RTD is set to 0000000111, then RTD1, RTD2 and RTD3 would be enabled and the associated settings would be visible in the menu.

The temperature setting for the alarm stage for each RTD can be set in the **RTD x Alarm Set** cells and the alarm time delay in the **RTD x Alarm Dly** cell.

The temperature setting for the trip stage for each RTD can be set in the **RTD x Trip Set** cells and the trip stage time delay in the **RTD x Trip Dly** cell.

Typical operating temperatures for protected plant are given in the table below. These are provided as a guide, actual figures MUST be obtained from the equipment manufacturers:

Parameter	Typical service temperature	Short term overloading at full load
Bearing temperature generators	60 - 80°C, depending on the type of bearing.	60 - 80°C+
Top oil temperature of transformers	80°C (50 - 60°C above ambient).	A temperature gradient from winding temperature is usually assumed, so that top oil RTDs can provide winding protection
Winding hot spot temperature	98°C for normal ageing of insulation.	140°C+ during emergencies

Table 8 - Typical operating temperatures of plant

2.18 Thermal Overload Protection (49)

Transformer overheating can be caused due to failures of the cooling system, external faults that are not clear promptly, overload and abnormal system conditions. These abnormal conditions include low frequency, high voltage, non-sinusoidal load current, or phase-voltage unbalance.

Overheating shortens the life of the transformer insulation in proportion to the duration and magnitude of the high temperature. Overheating can generate gases that could result in electrical failure. Furthermore, excessive temperature may result in an immediate insulation failure. Also, the transformer coolant may be heated above its flash temperature, therefore a fire can be caused.

Results suggest that the life of insulation is approximately halved for each 10°C rise in temperature above the rated value. However, the life of insulation is not wholly dependent on the rise in temperature but on the time the insulation is maintained at this elevated temperature. Due to the relatively large heat storage capacity of a transformer, infrequent overloads of short duration may not damage it. However, sustained overloads of a few percent may result in premature ageing and failure of insulation.

The thermal overload protection in the P64x is based on IEEE Standard C57.91-1995. Thermal overload trip can be based on hot spot temperature, Θ_H, or top oil temperature, Θ_{TO}. Top oil temperature can be calculated or can be measured directly when either CLIO or RTD are available. Hot spot temperature is only calculated.

It is important to consider ambient temperature to determine the load capability of a transformer. The ambient temperature is the temperature of the air in contact with the transformer's radiators. To determine the operating temperature, the temperature rise due to load is added to the ambient temperature. IEEE Standard C57.91-1995 states that transformer ratings are based on 24 hour average ambient temperature of 30°C. If the ambient temperature can be measured, then it should be averaged over a 24 hour period. In the P64x relays, the ambient temperature, Θ_A, can be measured directly or an average value can be set by the user.

The simplest application of overload protection employs I^2t characteristic. Time constants such as the winding time constant at hot spot location, τ_W, and top oil rise time constant, τ_{TO}, are set, so that the thermal model can follow the correct exponential heating and cooling profile, replicating the winding hotspot temperature. Transformer loads are becoming increasingly non-linear; hence, the P64x uses rms current values to replicate the winding hotspot temperature.

2.18.1 Setting Guidelines

The following tables are examples of the thermal data given by the transformer manufacturer. This data is required to set the thermal overload function.

Notes	*In the following tables:* *OD (oil directed) indicates that oil from heat exchangers (radiators) is forced to flow through the windings.* *WF states that the oil is externally cooled by pumped water.*

Thermal characteristic 735 MVA 300 kV +7% to -18% / 23kV ODWF cooled generator transformer	
No load losses (core losses)	340 kW
Load losses at nominal tap	1580 kW
Load losses at maximum current tap	1963 kW
Oil time constant	2.15 hr
Oil exponent	1.0
Top oil rise over ambient temperature at rated load	33.4 K
Winding time constant at hot spot location	14 mins
Winding hottest spot rise over top oil temperature at rated load	30.2 K
Winding exponent	2.0

Table 9 - Example of thermal data given by transformer manufacturer

Thermal characteristic 600 MVA 432/23.5 kV ODWF cooled generator transformer	
No load losses (core losses)	237 kW
Load losses at nominal tap	1423 kW
Load losses at maximum current tap	1676 kW
Oil time constant	2.2 hr
Oil exponent	1.0
Top oil rise over ambient temperature at rated load	46.6 K
Winding time constant at hot spot location	9 mins
Winding hottest spot rise over top oil temperature at rated load	33.1K
Winding exponent	2.0

Table 10 - Example of thermal data given by transformer manufacturer

Thermal characteristic IEC60354 figures based on medium-large power transformers OD cooled	
Oil time constant	1.5 hr
Oil exponent	1.0
Top oil rise over ambient temperature at rated load	49 K
Winding time constant at hot spot location	5-10 mins
Winding hottest spot rise over top oil temperature at rated load	29 K
Winding exponent	2.0

Table 11 - Example of thermal data given by transformer manufacturer

The monitor winding can be set either to HV, LV, TV or biased current. It is recommended to set it to biased current so an overall thermal condition of the transformer is provided. The ambient temperature can be set to average (average ambient temperatures covers 24-hour time periods), or it can be measured directly using a CLI or RTD input. Top oil temperature may be set as calculated or measured. IB is the load in pu, and it is recommended to set it at rated load, of 1.0 pu. The following parameters should be provided by the transformer manufacturer:

- The ratio of load loss at rated load to no load loss (Rated NoLoadLoss). For example, if the no load losses are 340 kW and load losses at rated are 1580 kW, the rated NoLoadLoss is 1580/340 = 4.6.

The losses in a transformer are shown in the following “Transformer losses” diagram:

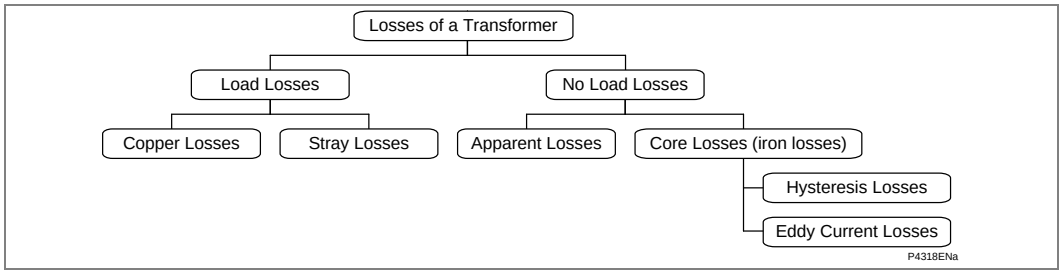


Figure 69 - Transformer losses

No-load losses are mainly iron losses. The loss that is due to the magnetizing current in the primary winding is called the apparent loss. The flow of the magnetizing current through the resistance of the winding does create a real I^2R loss and voltage drop, although both are generally quite small. Time-varying fluxes produce losses in ferromagnetic materials, known as core losses. These iron losses are divided into hysteresis losses and eddy-current losses.

The sum of copper losses and the stray losses is called the load losses. Copper losses are due to the flow of load currents through the primary and secondary windings. They are equal to I^2R, and they heat up the wires and cause voltage drops. Stray losses are due to the stray capacitance and leakage inductance. Stray capacitance exists between turns, between one winding and another, and between windings and the core.

- Winding hottest-spot rise over top oil at rated load (Hot Spot overtop)
- Top oil rise over ambient temperature at rated load (Top Oil overamb). It can also be determined by actual test as per IEEE Std. C57.12.90-1993.
- Winding exponent (Winding exp m) and oil exponent (Oil exp n)

As shown in the IEEE Std. C57.91-1995, this table suggests winding and oil exponents.

Type of cooling	m (winding exponent)	n (oil exponent)
OA	0.8	0.8
FA	0.8	0.9
Non-directed FOA or FOW	0.8	0.9
Directed FOA or FOW	1.0	1.0

Note *OA=Oil/Air* *FA=Forced Air*
FOA=Forced Oil and Air *FOW=Forced Oil and Water*

Table 12 - Suggested winding and oil exponents

ONAN or OA stands for Oil/Air: the cooling system transfers heat using oil to air without using pumps or fans. ONAF or FA stands for Forced Air: the cooling is aided by fans, but without any pumps to circulate the oil. With both these systems the oil circulates through the radiators or heat exchangers by normal convection only. OFAF or FOA stands for Forced Oil and Air: the cooling system uses both pumps and fans to cool the oil. OFWF or FOW stands for Forced Oil and Water: the heat exchanger is water-cooled and does not have the typical radiator configuration. The cooler is normally a chamber with many tubes inside where the oil and water exchange heat energy. In non-directed flow transformers, the pumped oil flows freely through the tank. In directed flow transformers, the pumped oil is forced to flow through the windings.

These exponents are empirically derived and are required to calculate the variation of $\Delta\Theta H$ and $\Delta\Theta_{TO}$ with load changes. The value of m has been selected for each mode of cooling to approximately account for effects of changes in resistance and off viscosity with changes in load. The value of n has been selected for each mode of cooling to approximately account for effects of change in resistance with change in load.

- Winding time constant at hot spot location (Hot spot rise co). It may also be estimated from the resistance cooling curve during thermal tests.
- Oil time constant (Top oil rise co)

The P64x has up to three hot spot stages and up to three top oil stages. The tripping signal, Top Oil T>x Trip, is asserted when the top oil (measured or calculated) temperature is above the setting, **Top Oil>x Set**, and the time delay, **tTop Oil>x Set** has elapsed. Also, the tripping signal, Hot Spot>x Trip, is asserted when the hottest-spot (calculated only) temperature is above the setting, **Hot Spot>x Set**, and the time delay, **tHot Spot>x Set** has elapsed.

When setting the hot spot and top oil stages take into consideration the suggested temperature limits (IEEE Std. C57.91-1995):

Suggested limits of temperature for loading above nameplate distribution transformers with 65°C rise	
Top oil temperature	120°C
Hot spot conductor temperature	200°C

Suggested limits of temperature for loading above nameplate power transformers with 65°C rise (refer to IEEE Std. C57.91-1995 to consider the four types of loading)	
Top oil temperature	110°C
Hot spot conductor temperature	180°C

Table 13 - Suggested temperature limits (IEEE Std. C57.91-1995)

2.19 Loss of Life (LoL)

As stated in IEEE Std. C57.91-1995, aging of insulation is a time function of temperature, moisture and oxygen content. The moisture and oxygen contributions to insulation deterioration are minimized due to modern oil preservation systems. Therefore, temperature is the key parameter in insulation ageing. Temperature distribution is not uniform; the part with the highest temperature undergoes the greatest deterioration. Therefore, the hottest spot temperature is considered in loss of life calculations.

2.19.1 Setting Guidelines

Set the life hours at reference hottest spot temperature. According to IEEE Std. C57.91-1995, the normal insulation life at the reference temperature in hours or years must be arbitrarily defined. The following table extracted from IEEE Std. C57.91-1995 gives values of normal insulation life for a well-dried, oxygen-free 65°C average winding temperature rise insulation system at the reference temperature of 110°C.

Basis	**Normal insulation life**	
	Hours	**Years**
50% retained tensile strength of insulation (former IEEE Std C57.92-1981 criterion)	65000	7.42
25% retained tensile strength of insulation	135000	15.41
200 retained degree of polymerization in insulation	150000	17.12
Interpretation of distribution transformer functional life test data (former IEEE Std. C57.91-1981)	180000	20.55

Notes *Tensile strength or degree of polymerization (D.P.) retention values were determined by sealed tube aging on well-dried insulation samples in oxygen-free oil.*
Refer to I.2 in annex I of the IEEE Std. C57.91-1995 for discussion of the effect of higher values of water and oxygen and also for the discussion on the basis given above.

Table 14 - Normal insulation life based on different factors

The Designed HS temp should be set to 110°C if the transformer is rated 65°C average winding rise. If the transformer is rated 55°C average winding rise, set the Designed HS temp to 95°C.

As recommended by IEEE Std. C57.91-1995, the Constant B Set should be set to 15000 based on modern experimental data.

If the ageing acceleration factor calculated by the relay is greater than the setting **FAA> Set** and the time delay **tFAA> Set** has elapsed, the FAA alarm (DDB 479) would be activated.

If the loss of life calculated by the relay is greater than the setting **LOL>1 Set** and the time delay **tLOL> Set** has elapsed, the LOL alarm (DDB 480) would be activated.

The following is an example on how to set the loss of life function. Consider a new 65°C average winding rise rated transformer whose life hours at designed hottest spot temperature is 180,000 hrs. As a result, Life Hours at HS is set to 180,000, and the Designed HS temp is set to 110.0°C. The Constant B Set is 15,000 as recommended by IEEE from experimental data. The aging acceleration factor takes into consideration the constant B and the hottest spot temperature calculated by the thermal function. For a distribution transformer, IEEE suggests 200°C as the limit for the hottest spot temperature (refer to the thermal overload function to determine the hottest spot temperature for a power transformer). The aging acceleration factor alarm may be asserted when 70% of the 200°C is reached. The aging acceleration factor is calculated as follows:

$$FAA = e^{\left[\frac{B}{383} - \frac{B}{\text{hottest spot temp} + 273}\right]} = e^{\left[\frac{B}{383} - \frac{B}{0.7*200+273}\right]} = 17.2$$

Therefore FAA>set is 17.2. The tFAA> Set may be set to 10.00 min. The LOL>1 Set may be set to 115,000 hrs, if it is considered that the transformer has 65,000 hrs left (Life Hours at HS – hours left = 180,000 – 65,000 = 115,000 hrs). The tLOL> Set may be set to 10.00 min. Finally, the Reset Life Hours setting determines the value of the LOL measurement once the Reset LOL command is executed. The default value is zero because considering a new transformer, after testing the thermal function in the P64x, the LOL measurement should be reset to zero.

Certain tests should be performed to determine the age of an old transformer. Advice from the transformer manufacturer should be requested.

2.20 Through Fault Monitoring

According to IEEE Std C57.109-1993(R2008), mechanical effects are more significant than thermal effects for fault-current magnitudes near the design capability of the transformer. However, at fault-current magnitudes close to the overload range, mechanical effects are less important unless the frequency of fault occurrence is high. Note that mechanical effects are more important in large kVA transformers. The maximum duration limit for the worst case of mechanical duty is 2 s.

The IEEE Std C57.109-1993(R2008) indicates that the transformer categories are as follows:

Transformer Categories		
Category	**Single phase (kVA)**	**Three-phase (kVA)**
I	5 to 500	15 to 500
II	501 to 1667	501 to 5000
III	1668 to 10000	5001 to 30000
IV	Above 10000	Above 30000

Table 15 - Transformer Categories

Category I and II transformer maximum through fault current only considers the transformer short-circuit impedance. Category III and IV transformer maximum through fault current considers the transformer short-circuit impedance and the system short-circuit impedance at the transformer location. The short-circuit impedances are expressed in percent on the transformer rated voltage and rated base kVA.

The P64x through fault monitoring element can monitor the HV, the LV or the TV winding. In three winding applications, monitor the winding through which the highest current would flow during an external fault. Fault studies are required to determine the maximum through fault current and which winding carries the most current. For example, consider the autotransformer shown in the “P645 used to protect an autotransformer with load tap changer” diagram. Consider that an equivalent source and load are connected to the 230 kV terminal. Also an equivalent source and load are connected to the 115 kV terminal and only the load is connected to the 13.8 kV terminal. An external fault on the 230 kV side would be fed by the source on the 115 kV side. Therefore, the current would mainly flow from the 115 kV side to the 230 kV side. If the external fault occurs on the 115kV side, the through fault current would flow from the 230 kV side to the 115 kV side. If an external fault occurs on the 13.8 kV side, the through fault current would flow from the 230 kV and 115 kV sides to the 13.8 kV side. The source and transformer impedances determine the fault current level. Monitor the winding through which the maximum through fault current flows.

Set the **TF I> Trigger** above the maximum overload. According to IEEE Std. C57.109-1993, values of 3.5 or less times normal base current may result from overloads instead of faults. TF I> may be set to 3.85 pu. If the monitored current is above this level and no differential element has started, then the I^2t is calculated.

To set the **TF I^2t> Trigger**, consider the maximum through fault current and the maximum time duration. The maximum through fault current may be determined as 1/X, where X is the transformer impedance. This approximation is valid when the source is strong, so that its impedance is small compared to the transformer impedance. If the transformer has an impedance of 10%, the maximum through fault current may be calculated as 1/X = 1/0.1 = 10 pu. Set **TF I^2t> Trigger** to $(10)^2$ = 100 pu. Therefore, if 10 pu flow through the transformer for 1 s, a through fault alarm is issued.

2.21 Current Loop Inputs and Outputs (CLIO) Protection

2.21.1 Current Loop Inputs

Four analog or current loop inputs are provided for transducers with ranges of 0 to 1 mA, 0 to 10 mA, 0 to 20 mA or 4 to 20 mA. The analog inputs can be used for various transducers such as vibration monitors, tachometers and pressure and temperature transducers. Associated with each input there are two protection stages, one for alarm and one for trip. Each stage can be individually enabled or disabled and each stage has a Definite Time delay setting. The Alarm and Trip stages can be set for operation when the input value falls below the Alarm/Trip threshold **Under** or when the input current is above the input value **Over**. The 4 to 20 mA input range, has an undercurrent alarm element which can be used to indicate that there is a fault with the transducer or the wiring.

Power-on diagnostics and continuous self-checking are provided for the hardware associated with the current loop inputs.

An instantaneous under current alarm element is available, with a setting range from 0 to 4 mA. This element controls an output signal (CLI1/2/3/4 I< Fail Alm, DDB 461-464) which can be mapped to a user defined alarm if required.

2.21.2 Setting Guidelines for Current Loop Inputs

For each analog input, the user can define the following:

- The current input range: 0 – 1 mA, 0 – 10 mA, 0 – 20 mA, 4 – 20 mA
- The analog input function and unit, this is in the form of a 16-character input label
- Analog input Minimum value (setting range from –9999 to 9999)
- Analog input Maximum value (setting range from –9999 to 9999)
- Alarm threshold, range within the maximum and minimum set values
- Alarm function - over or under
- Alarm delay
- Trip threshold, range within maximum and minimum set values
- Trip function - over or under
- Trip delay

Each current loop input can be selected as Enabled or Disabled as can the Alarm and Trip stage of each of the current loop input. The Alarm and Trip stages can be set for operation when the input value falls below the Alarm/Trip threshold 'Under' or when the input current is above the input value 'Over' depending on the application. One of four types of analog inputs can be selected for transducers with ranges of 0 to 1 mA, 0 to 10 mA, 0 to 20 mA or 4 to 20 mA.

The Maximum and Minimum settings allow the user to enter the range of physical or electrical quantities measured by the transducer. The settings are unit-less; but you can enter the transducer function and the unit of the measurement using the 16-character user-defined CLI Input Label. For example, if the analog input is used to monitor a power measuring transducer, the appropriate text could be "Active Power(MW)".

The alarm and trip threshold settings should be set within the range of physical or electrical quantities defined by the user. The relay will convert the current input value into its corresponding transducer measuring value for the protection calculation.

For example, if the CLI Minimum is -1000 and the CLI Maximum is 1000 for a 0 to 10 mA input, an input current of 10 mA is equivalent to a measurement value of 1000, 5 mA is 0 and 1 mA is -800. If the CLI Minimum is 1000 and the CLI Maximum is -1000 for a 0 to 10 mA input, an input current of 10 mA is equivalent to a measurement value of -1000, 5 mA is 0 and 1 mA is 800. These values are available for display in the **CLIO Input 1/2/3/4** cells in the **MEASUREMENTS 3** menu. The top line shows the CLI Input Label and the bottom line shows the measurement value.

2.21.3 Current Loop Outputs

Four analog current outputs are provided with ranges of 0 to 1 mA, 0 to 10 mA, 0 to 20 mA or 4 to 20 mA, which can alleviate the need for separate transducers. These may be used to feed standard moving coil ammeters for analog indication of certain measured quantities or into a SCADA using an existing analog RTU.

The outputs can be assigned to any of the following relay measurements:

- Magnitudes of IA, IB, IC of every CT input
- Magnitudes of IA, IB, IC at HV, LV and TV sides of the transformer
- Magnitudes of IN Measured and IN Derived of every winding
- Magnitudes of I1, I2, I0 at HV, LV and TV sides of the transformer
- Magnitudes of VAB, VBC, VCA, VAN, VBN, VCN, VN Measured, VN Derived
- Magnitude of Vx
- VAN RMS, VBN RMS, VCN RMS
- Frequency
- CL Inputs 1-4
- RTD 1-10

The user can set the measuring range for each analog output. The range limits are defined by the Maximum and Minimum settings. This allows the user to “zoom in” and monitor a restricted range of the measurements with the desired resolution. For voltage, current and power quantities, these settings can be set in either primary or secondary quantities, depending on the **CLO1/2/3/4 Set Values** then **Primary** or **Secondary** setting associated with each current loop output.

Power-on diagnostics and continuous self-checking are provided for the hardware associated with the current loop outputs.

2.21.4 Setting Guidelines for Current Loop Outputs

Each current loop output can be selected as Enabled or Disabled.
One of four types of analog output can be selected for transducers with ranges of 0-1 mA, 0-10 mA, 0-20 mA or 4-20 mA. The 4-20 mA range is often used so that an output current is still present when the measured value falls to zero. This is to give a fail-safe indication and may be used to distinguish between the analog transducer output becoming faulty and the measurement falling to zero.

The Maximum and Minimum settings allow the user to enter the measuring range for each analog output. The range, step size and unit corresponding to the selected parameter is shown in the table in the Operations chapter. This allows the user to “zoom in” and monitor a restricted range of the measurements with the desired resolution.

For voltage, current and power quantities, these settings can be set in either primary or secondary quantities, depending on the **CLO1/2/3/4 Set Values** then **Primary** or **Secondary** setting associated with each current loop output.

The relationship of the output current to the value of the measurand is of vital importance and needs careful consideration. Any receiving equipment must, of course, be used within its rating but, if possible, some kind of standard should be established.

One of the objectives must be to have the capability to monitor the voltage over a range of values, so an upper limit must be selected, typically 120%. However, this may lead to difficulties in scaling an instrument.

The same considerations apply to current transducers outputs and with added complexity to watt transducers outputs, where both the voltage and current transformer ratios must be taken into account.

Some of these difficulties do not need to be considered if the transducer is only feeding, for example, a SCADA outstation. Any equipment which can be programmed to apply a scaling factor to each input individually can accommodate most signals. The main consideration will be to ensure that the transducer is capable of providing a signal right up to the full-scale value of the input, that is, it does not saturate at the highest expected value of the measurand.

3 APPLICATION OF NON-PROTECTION FUNCTIONS

3.1 Voltage Transformer Supervision (VTS)

The Voltage Transformer Supervision (VTS) feature is used to detect failure of the ac voltage inputs to the relay. This may be caused by internal voltage transformer faults, overloading, or faults on the interconnecting wiring to relays. This usually results in one or more VT fuses blowing. Following a failure of the ac voltage input there would be a misrepresentation of the phase voltages on the power system, as measured by the relay, which may result in mal-operation.

The VTS logic in the relay is designed to detect the voltage failure, and automatically adjust the configuration of protection elements whose stability would otherwise be compromised. A time-delayed alarm output is also available.

There are three main aspects to consider regarding the failure of the VT supply:

- Loss of one or two phase voltages
- Loss of all three phase voltages under load conditions
- Absence of three phase voltages on line energization

3.1.1 Loss of One or Two Phase Voltages

The VTS feature within the relay operates on detection of Negative Phase Sequence (NPS) voltage without the presence of NPS current. This gives operation for the loss of one or two phase voltages. Stability of the VTS function is assured during system fault conditions, by the presence of NPS current. The use of negative sequence quantities ensures correct operation even where three-limb or 'V' connected (open delta) VTs are used.

Negative Sequence VTS Element:

The negative sequence thresholds used by the element are V2 = 10 V and I2 = 0.05 to 0.5 In settable (defaulted to 0.05 In).

3.1.2 Loss of all Three Phase Voltages Under Load Conditions

Under the loss of all three phase voltages to the relay, there will be no negative phase sequence quantities present to operate the VTS function. However, under such circumstances, a collapse of the three phase voltages will occur. If this is detected without a corresponding change in any of the phase current signals (which would be indicative of a fault), a VTS condition will be raised. In practice, the relay detects the presence of superimposed current signals, which are changes in the current applied to the relay. These signals are generated by comparison of the present value of the current with that exactly one cycle previously. Under normal load conditions, the value of superimposed current should therefore be zero. Under a fault condition a superimposed current signal will be generated which will prevent operation of the VTS.

The phase voltage level detectors are fixed and will drop off at 10 V and pickup at 30 V.

The sensitivity of the superimposed current elements is fixed at 0.1 In.

3.1.3 Absence of Three Phase Voltages On Line Energization

If a VT were inadvertently left isolated prior to line energization, incorrect operation of voltage dependent elements could result. The previous VTS element detected 3-phase VT failure by absence of all 3-phase voltages with no corresponding change in current. On line energization there will, however, be a change in current (as a result of load or line charging current for example). An alternative method of detecting 3-phase VT failure is therefore required on-line energization.

The absence of voltage measurements on all three phases with line energized can result of two conditions:

- A 3-phase VT failure
- A close up 3-phase fault

The first condition would require blocking of the voltage dependent function and the second would require tripping.

To differentiate between these two conditions, an overcurrent level detector ("VTS Imax> Inh") will prevent a VTS block from being issued if it operates. This element should be set in excess of any non-fault based currents on line energization (load, line charging current, transformer inrush current if applicable), but below the level of current produced by a close up three phase fault. If the line is now closed where a 3-phase VT failure is present, the overcurrent detector will not operate and a VTS block will be applied. Closing onto a 3-phase fault will result in operation of the overcurrent detector and prevent a VTS block being applied.

This logic will only be enabled during a live line condition (as indicated by the relays pole dead logic) to prevent operation under dead system conditions, where no voltage will be present and the **VTS I> Inhibit** overcurrent element will not be picked up.

3.1.4 Setting the VT Supervision Element

The **VTS Status** setting **Blocking/Indication** determines whether these operations will occur on detection of VTS:

- VTS set to provide alarm indication only;
- Optional blocking of voltage dependent protection elements;
- Optional conversion of directional overcurrent elements to non-directional protection (available when set to Blocking mode only). These settings are found in the Function Links cell of the overcurrent protection.

A VTS indication will be given after the VTS Time Delay has expired. In the case where the VTS is set to indicate only the relay may potentially maloperate, depending on which protection elements are enabled. In this case the VTS indication will be given prior to the VTS time delay expiring if a trip signal is given.

Where a Miniature Circuit Breaker (MCB) is used to protect the voltage transformer ac output circuits, it is common to use MCB auxiliary contacts to indicate a three-phase output disconnection. It is possible for the VTS logic to operate correctly without this input. However, this facility has been provided for compatibility with various utilities current practices. Energizing an opto-isolated input assigned to MCB/VTS (DDB 874) on the relay will therefore provide the necessary block.

Where directional overcurrent elements are converted to non-directional protection on VTS operation, it must be ensured that the current pick-up setting of these elements is higher than full load current.

The **VTS I> Inhibit** or **VTS I2> Inhibit** elements are used to override a VTS block in event of a fault occurring on the system which could trigger the VTS logic. Once the VTS block has been established, however, then it would be undesirable for subsequent system faults to override the block. Therefore the VTS block will be latched after a user settable time delay VTS Time Delay. Once the signal has latched the resetting method is determined by a menu setting Manual or Auto. The first is manually using the front panel interface (or remote communications) provided the VTS condition has been removed. The second method is automatically when VTS Reset Mode is set to Auto mode, provided the VTS condition has been removed and the three phase voltages have been restored above the phase level detector settings for more than 240 ms.

The **VTS I> Inhibit** overcurrent setting is used to inhibit the voltage transformer supervision in the event of a loss of all three phase voltages caused by a close up 3-phase fault occurring on the system following closure of the CB to energize the line. This element should be set in excess of any non-fault based currents on line energization (load, line charging current, transformer inrush current if applicable) but below the level of current produced by a close up 3-phase fault.

This **VTS I2> Inhibit** NPS overcurrent setting is used to inhibit the voltage transformer supervision in the event of a fault occurring on the system with negative sequence current above this setting.

The NPS current pick-up threshold must be set higher than the negative phase sequence current due to the maximum normal load unbalance on the system. This can be set practically at the commissioning stage, making use of the relay measurement function to display the standing negative phase sequence current, and setting at least 20% above this figure.

3.2 Current Transformer Supervision (CTS)

The Current Transformer Supervision (CTS) feature is used to detect failure of one or more of the ac phase current inputs to the relay. Failure of a phase CT or an open circuit of the interconnecting wiring can result in incorrect operation of any current operated element. Additionally, interruption in the ac current circuits risks dangerous CT secondary voltages being generated.

3.2.1 Setting the CT Supervision Element

The positive sequence current in at least two current inputs exceeds the **CTS I1** setting. The **CTS I1** setting should be below the minimum load current of the protected object. Therefore, 10% of the rated current might be used.

The high set ratio of negative to positive sequence current, **CTS I2/I1>2**, should be set below the ratio of negative sequence to positive sequence current when the secondary circuit of any phase of any of the CT inputs is disconnected. For example, consider that balanced full load current is flowing and that the secondary of phase A CT1 is disconnected. The currents measured by the relay are:

$I_A = 0$

$I_B = 1\angle - 120°$ pu

$I_C = 1\angle - 240°$ pu

The positive and negative sequence currents are calculated as:

$$I_1 = \left| \frac{1}{3} x \left(I_A + aI_B + a^2 I_C \right) \right| = \left| \frac{1}{3} x \left(a \times 1\angle -120° + a^2 \times 1\angle -240° \right) \right| = \frac{2}{3}$$

$$I_2 = \left| \frac{1}{3} x \left(I_A + a^2 I_B + aI_C \right) \right| = \left| \frac{1}{3} x \left(a^2 \times 1\angle -120° + a \times 1\angle -240° \right) \right| = \frac{1}{3}$$

The ratio of negative to positive sequence current is 50%. A typical setting of 40% might be used.

The low set ratio of negative to positive sequence current, **CTS I2/I1> 1**, should be set above the maximum load unbalance. In practice, the levels of standing negative phase sequence current present on the system govern this minimum setting. This can be determined from a system study, or by making use of the relay measurement facilities at the commissioning stage. If the latter method is adopted, it is important to take the measurements during maximum system load conditions, to ensure that all single-phase loads are accounted for. A 20% setting might be used.

If the following information is recorded by the relay during commissioning:

Ifull load = 500 A

I2 = 50 A

Therefore I2/I1 ratio is given by I2/I1 = 50/500 = 0.1

To allow for tolerances and load variations a setting of 20% of this value may be typical. Therefore, set CTS I2/I1>1 = 20%.

After the **CTS Time Delay** expires the CT Fail Alarm is asserted. The default setting of 2 sec is appropriate.

3.3 CT Input Exclusion

When a current input is excluded, the current associated to the input is set to zero. As a result, all the protection functions considering the current from the excluded input are not affected. The CT input exclusion might be useful during maintenance. In the following “CT input exclusion – 1.5 Bk application” diagram, the adjacent isolators to CB1 are open and locked because of maintenance work on CB1.

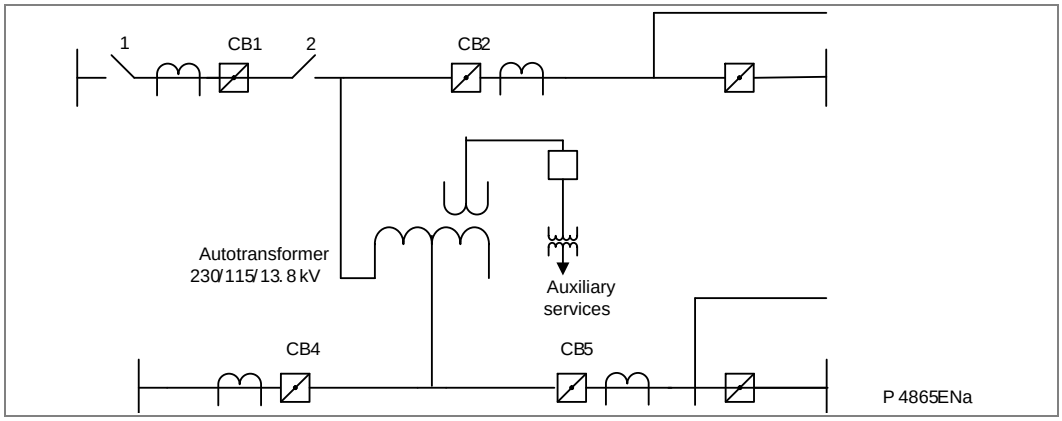


Figure 70 - CT input exclusion – 1.5 Bk application

The current transformer associated to CB1 has been connected to T1 CT input in P645. As shown in the following “CT input exclusion“ diagram, auxiliary contacts from CB1 isolators 1 and 2 must be connected to an opto-input in P645 configured as CT1 Exclu Ena (DDB 704) in PSL.

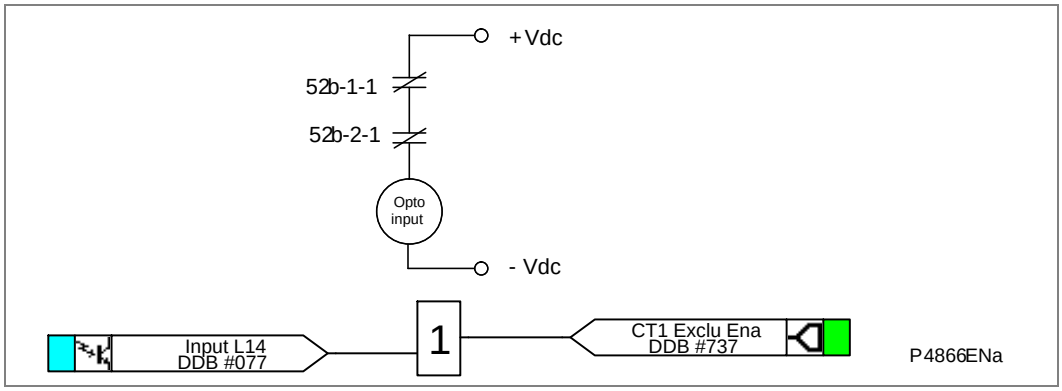


Figure 71 - CT input exclusion

When isolators 1 and 2 are open the opto-input L14 is energized and CT1 Exclu Ena is asserted. To set T1 CT excluded (DDB 704), T1 CT Phase A, B and C undercurrent elements must also be asserted.

3.4 User Alarms

Thirty-two configurable self-reset or manual reset user alarms are available in the P64x. Transformer protection such as Buchholz, temperature, oil level can be configured to a user alarm as follows:

USER ALARMS	
Manual Reset	00000000000000000000000000001011
Labels	
User Alarm 1	Buchholz
User Alarm 2	Oil level
User Alarm 3	Oil tempt alarm
User Alarm 4	Oil tempt trip
User Alarm 5	User Alarm 5
User Alarm 6	User Alarm 6
User Alarm 7	User Alarm 7
User Alarm 8	User Alarm 8
User Alarm 9	User Alarm 9
User Alarm 10	User Alarm 10
User Alarm 11	User Alarm 11
User Alarm 12	User Alarm 12
User Alarm 13	User Alarm 13
User Alarm 14	User Alarm 14
User Alarm 15	User Alarm 15
User Alarm 16	User Alarm 16
User Alarm 17	User Alarm 17
User Alarm 18	User Alarm 18
User Alarm 19	User Alarm 19
User Alarm 20	User Alarm 20
User Alarm 21	User Alarm 21
User Alarm 22	User Alarm 22
User Alarm 23	User Alarm 23
User Alarm 24	User Alarm 24
User Alarm 25	User Alarm 25
User Alarm 26	User Alarm 26
User Alarm 27	User Alarm 27
User Alarm 28	User Alarm 28
User Alarm 29	User Alarm 29
User Alarm 30	User Alarm 30
User Alarm 31	User Alarm 31
User Alarm 32	User Alarm 32

P2681ENa

Figure 72 - User alarm settings

Buchholz, temperature and oil level trips can be executed by the P64x if the user alarm is configured to the any trip signal (DDB 886) as follows:

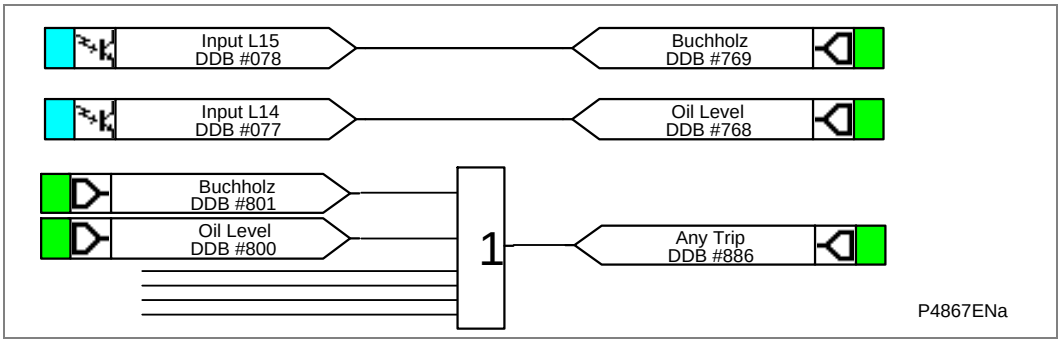


Figure 73 - User alarm configuration

DDBs 768 and 800 are user alarm 1 output and input signal respectively. Both signals have been labeled as Oil Level in the setting file. Whenever opto-input 14 is energized DDB 768 is asserted. The user alarm output always follows the status of the signal configured to it in PSL. In this example, DDB 768 follows the status of opto-input 14 and DDB 769 follows the status of opto-input 15. If user alarm 1 is set as manual reset, then DDB 800 is latched but DDB 768 is not. Similarly if user alarm 2 is set as manual reset, DDB 801 is latched but DDB 769 is not.

3.5 Trip Circuit Supervision (TCS)

The trip circuit, in most protective schemes, extends beyond the IED enclosure and passes through components such as fuses, links, relay contacts, auxiliary switches and other terminal boards. This complex arrangement, coupled with the importance of the trip circuit, has led to dedicated schemes for its supervision.
Several Trip Circuit Supervision (TCS) scheme variants are offered. Although there are no dedicated settings for TCS, in the MiCOM P24x / P34x / P443 / P445 / P446 / P54x / P547 / P64x / P746 / P841 the following schemes can be produced using the Programmable Scheme Logic (PSL). A user alarm is used in the PSL to issue an alarm message on the relay front display. If necessary, the user alarm can be re-named using the menu text editor to indicate that there is a fault with the trip circuit.

3.5.1 TCS Scheme 1

3.5.1.1 Scheme Description

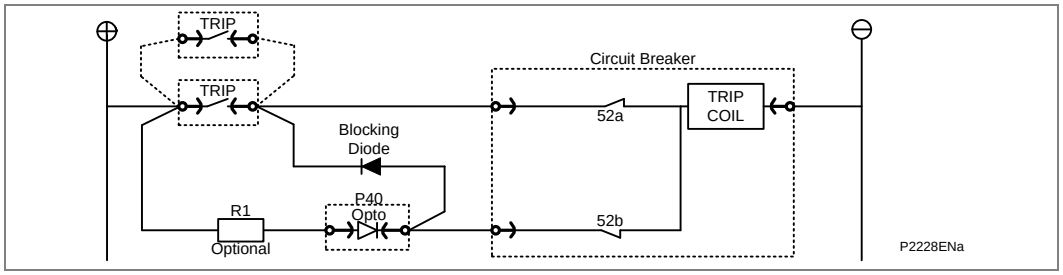


Figure 74 - TCS scheme 1

This scheme provides supervision of the trip coil with the breaker open or closed, however, pre-closing supervision is not provided. This scheme is also incompatible with latched trip contacts, as a latched contact will short out the opto for greater than the recommended DDO timer setting of 400ms. If breaker status monitoring is required a further 1 or 2 opto inputs must be used.

Note	*A 52a CB auxiliary contact follows the CB position and a 52b contact is the opposite.*

When the breaker is closed, supervision current passes through the opto input, blocking diode and trip coil. When the breaker is open current still flows through the opto input and into the trip coil via the 52b auxiliary contact. Hence, no supervision of the trip path is provided whilst the breaker is open. Any fault in the trip path will only be detected on CB closing, after a 400ms delay.
Resistor R1 is an optional resistor that can be fitted to prevent maloperation of the circuit breaker if the opto input is inadvertently shorted, by limiting the current to <60mA. The resistor should not be fitted for auxiliary voltage ranges of 30/34 volts or less, as satisfactory operation can no longer be guaranteed. The table below shows the appropriate resistor value and voltage setting (**Opto Config.** menu) for this scheme. This TCS scheme will function correctly even without resistor R1, since the opto input automatically limits the supervision current to less that 10mA. However, if the opto is accidentally shorted the circuit breaker may trip.

Auxiliary Voltage (Vx)	Resistor R1 (ohms)	Opto Voltage Setting with R1 Fitted
24/27	-	-
30/34	-	-
48/54	1.2k	24/27
110/250	2.5k	48/54
220/250	5.0k	110/125

Note *When R1 is not fitted the opto voltage setting must be set equal to supply voltage of the supervision circuit.*

Table 16 - Auxiliary voltage, Resistor R1 and Opto voltage setting

3.5.2 Scheme 1 PSL

The next figure shows the scheme logic diagram for the TCS scheme 1. Any of the available opto inputs can be used to show whether or not the trip circuit is healthy. The delay on drop off timer operates as soon as the opto is energized, but will take 400ms to drop off/reset in the event of a trip circuit failure. The 400ms delay prevents a false alarm due to voltage dips caused by faults in other circuits or during normal tripping operation when the opto input is shorted by a self-reset trip contact. When the timer is operated the NC (normally closed) output relay opens and the LED and user alarms are reset.

The 50ms delay on pick-up timer prevents false LED and user alarm indications during the relay power up time, following an auxiliary supply interruption.

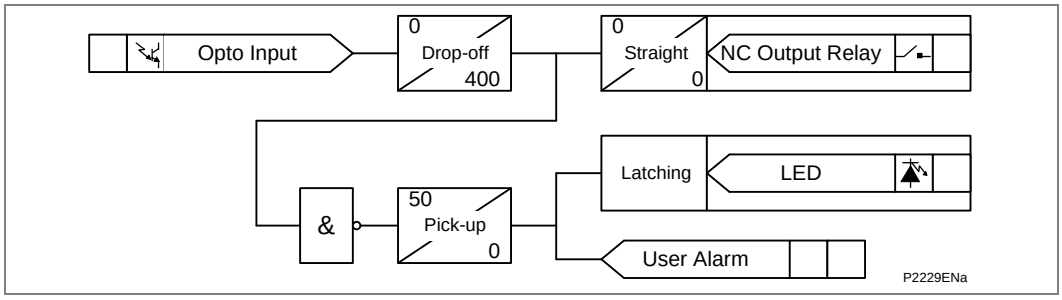


Figure 75 - PSL for TCS schemes 1 and 3

3.5.3 TCS Scheme 2

3.5.3.1 Scheme Description

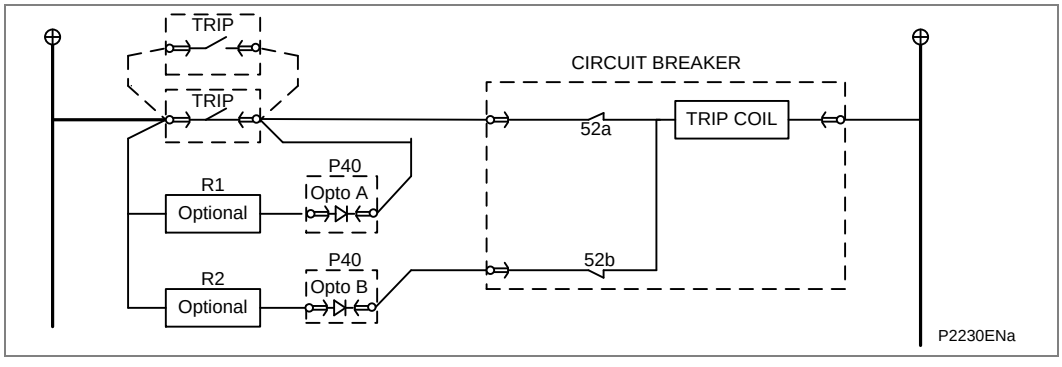


Figure 76 - TCS scheme 2

Much like scheme 1, this scheme provides supervision of the trip coil with the breaker open or closed and also does not provide pre-closing supervision. However, using two opto inputs allows the relay to correctly monitor the circuit breaker status since they are connected in series with the CB auxiliary contacts. This is achieved by assigning Opto A to the 52a contact and Opto B to the 52b contact. Provided the **Circuit Breaker Status** is set to **52a and 52b** (CB CONTROL column) the relay will correctly monitor the status of the breaker. This scheme is also fully compatible with latched contacts as the supervision current will be maintained through the 52b contact when the trip contact is closed.

When the breaker is closed, supervision current passes through opto input A and the trip coil. When the breaker is open current flows through opto input B and the trip coil. As with scheme 1, no supervision of the trip path is provided whilst the breaker is open. Any fault in the trip path will only be detected on CB closing, after a 400 ms delay.

As with scheme 1, optional resistors R1 and R2 can be added to prevent tripping of the CB if either opto is shorted. The resistor values of R1 and R2 are equal and can be set the same as R1 in scheme 1.

3.5.4 Scheme 2 PSL

The PSL for this scheme is practically the same as that of scheme 1. The main difference being that both opto inputs must be off before a trip circuit fail alarm is given.

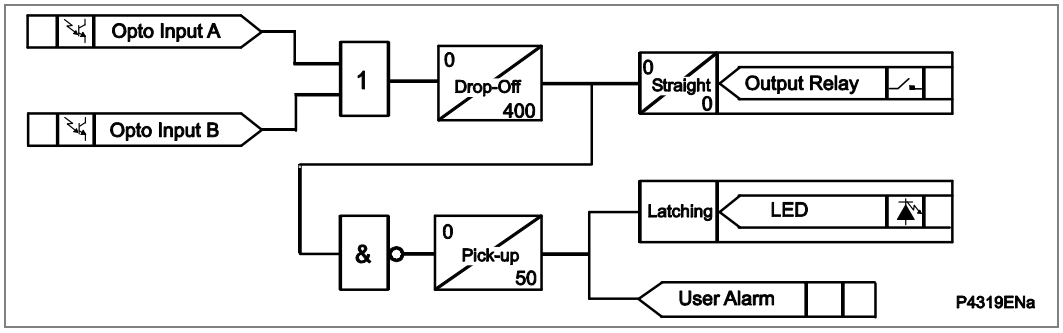


Figure 77 - PSL for TCS scheme 2

3.5.5 TCS Scheme 3

3.5.5.1 Scheme Description

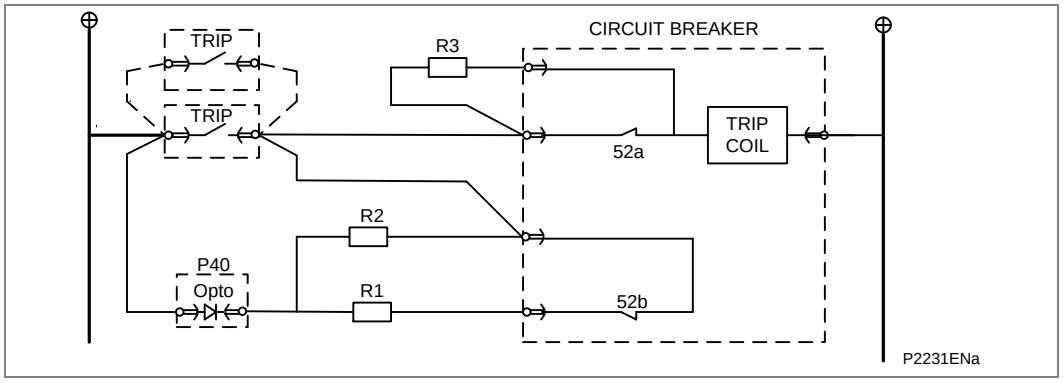


Figure 78 - TCS scheme 3

Scheme 3 is designed to provide supervision of the trip coil with the breaker open or closed, but unlike schemes 1 and 2, it also provides pre-closing supervision. Since only one opto input is used, this scheme is not compatible with latched trip contacts. If circuit breaker status monitoring is required a further 1 or 2 opto inputs must be used.

When the breaker is closed, supervision current passes through the opto input, resistor R2 and the trip coil. When the breaker is open current flows through the opto input, resistors R1 and R2 (in parallel), resistor R3 and the trip coil. Unlike schemes 1 and 2, supervision current is maintained through the trip path with the breaker in either state, thus giving pre-closing supervision.

As with schemes 1 and 2, resistors R1 and R2 are used to prevent false tripping, if the opto-input is accidentally shorted. However, unlike the other two schemes, this scheme is dependent upon the position and value of these resistors. Removing them would result in incomplete trip circuit monitoring. The table below shows the resistor values and voltage settings required for satisfactory operation.

Auxiliary Voltage (Vx)	Resistor R1 & R2 (ohms)	Resistor R3 (ohms)	Opto Voltage Setting
24/27	-	-	-
30/34	-	-	-
48/54	1.2k	0.6k	24/27
110/250	2.5k	1.2k	48/54
220/250	5.0k	2.5k	110/125

Note *Scheme 3 is not compatible with auxiliary supply voltages of 30/34 volts and below.*

Table 17 - Resistor values and voltage settings required

3.5.6 Scheme 3 PSL

The PSL for scheme 3 is identical to that of scheme 1.

3.6 VT Connections

3.6.1 Open Delta (V-Connected) VTs

P64x relays can be used with V-connected VTs by connecting the VT secondaries to:

- C19, C20 and C21 input terminals, with the C22 input left unconnected for P14x, P443, P445, P543, P544 and P841A
- D19, D20 and D21 input terminals, with the D22 input left unconnected for P446, P545, P546, P547 and P841B
- C2, C4 and E2 input terminals, with the Vn input left unconnected for P643. Terminals C1, C3 and E1 must be linked at the relay.
- D2, D4 and F2 input terminals with the Vn input left unconnected for P645. D1, D3 and F1 must be linked at the relay.
- For P642 Open delta VTs are the only connection available

For more details, see the see the *Connection Diagrams* chapter.

This type of VT arrangement cannot pass zero-sequence (residual) voltage to the relay, or provide any phase to neutral voltage quantities. Therefore any protection that is dependent on zero sequence voltage measurements should be disabled. Therefore, residual voltage displacement protection and directional earth fault protection should be disabled.

The accuracy of single-phase voltage measurements can be impaired when using V-connected VTs. The relay attempts to derive the phase to neutral voltages from the phase to phase voltage vectors. If the impedance of the voltage inputs were perfectly matched the phase to neutral voltage measurements would be correct, provided the phase to phase voltage vectors were balanced. However, in practice there are small differences in the impedance of the voltage inputs, which can cause small errors in the phase to neutral voltage measurements.

For P643 and P645, the phase to neutral voltage measurement accuracy can be improved by connecting three well-matched load resistors between the phase voltage inputs (C2, C4, E2 or D2, D4, F2) and neutral (C1,C3,E1 or D1, D3, F1), creating a 'virtual' neutral point. The load resistor values must be chosen so their power consumption is within the limits of the VT. It is recommended that 10kΩ ±1% (6 W) resistors are used for the 110 V (Vn) rated relay, assuming the VT can supply this burden.

3.6.2 VT Single Point Earthing

The MiCOM P64x will function correctly with conventional 3-phase VTs earthed at any one point on the VT secondary circuit. Typical earthing examples being neutral earthing, or B-phase (UK: "**yellow phase**" earthing).

4 CURRENT TRANSFORMER (CT) REQUIREMENTS

4.1 Current Transformer (CT) Theory

The flow current in the primary winding produces an alternating flux in the core and this flux induces an e.m.f. in the secondary winding which results in the flow of secondary current when this winding is connected to an external closed circuit. The magnetic effect of the secondary current is in opposition to that of the primary and the value of the secondary current automatically adjusts itself to such a value, that the resultant magnetic effect of the primary and secondary currents, produces a flux required to induce the e.m.f. necessary to drive the secondary current through the impedance of the secondary. In an ideal transformer, the primary ampere-turns are always exactly equal to the secondary ampere-turns and the secondary current is, therefore, always proportional to the primary current. In an actual Current Transformer (CT), however, this is never the case. All core materials require a certain number of ampere-turns to induce the magnetic flux required to induce the necessary voltage. The most accurate CT is one in which the exciting ampere-turns are least in proportion to the secondary ampere-turns.

In many applications, core saturation will almost inevitably occur during the transient phase of a heavy short circuit. The performance of the CTs during faults is, therefore, an important consideration in providing an effective relaying scheme. In any CT the first consideration is the highest secondary winding voltage possible prior to core saturation.

This may be calculated from:

$$Ek = 4.44 \times B\ A\ f\ N \text{ volts}$$

Where:
Ek = secondary induced volts (rms value, known as the knee-point voltage)
B = flux density in tesla
N = number of secondary turns
f = system frequency in hertz
A = net core cross-sectional area in square meters

This induced voltage causes the maximum current to flow through the external burden while still maintaining a virtually sinusoidal secondary current. Any higher value of primary current demanding further increase in secondary current would, due to core saturation, tend to produce a distorted secondary current.

The circuit voltage required is typically:

$$Es = Is\ (Z_B + Z_S + Z_L)$$

Where:
Is = secondary current of ct in amps (assume nominal value, usually 1 A or 5 A)
Z_B = the connected external burden in ohms
Z_S = the ct secondary winding impedance in ohms
Z_L = the resistance of any associated connecting leads

In any given case, several of these quantities are known or can usually be estimated to predict the performance of the transformers. From the ac magnetization characteristic, commonly plotted in secondary volts versus exciting current, Es can be determined for a minimum exciting current. The equation for Es given above then indicates whether the voltage required is adequate. It may be seen that the secondary burden and the maximum available fault current are two important criteria in determining the performance of a given CT.

The primary current contains two components. These are respectively the secondary current which is transformed in the inverse ratio of the turns ratio and an exciting current, which supplies the eddy and hysteresis losses and magnetizes the core. This latter current flows in the primary winding only and therefore, is the cause of the transformer errors. It is, therefore, not sufficient to assume a value of secondary current and to work backwards to determine the value of primary current by invoking the constant ampere-turns rule, since this approach does not consider the exciting current. From this observation it may be concluded that certain values of secondary current could never be produced whatever the value of primary current and this is the case when the core saturates and a disproportionate amount of primary current is required to magnetize the core.

The amount of exciting current drawn by a CT depends on the core material and the amount of flux which must be developed in the core to satisfy the burden requirements of the CT. The appropriate current may be obtained directly from the exciting characteristic of the transformer since the secondary e.m.f. and therefore the flux developed is proportional to the product of secondary current and burden impedance.

The general shape of the exciting characteristic for a typical grade of Cold Rolled Grain Orientated Silicon Steel (CROSS) core CT is shown in the following diagram. The characteristic is divided into three regions, defined by ankle-point and the knee-point. The working range of a protective CT extends over the full range between the ankle-point and the knee-point and beyond. Protection CTs are required to operate correctly at many times the rated current.

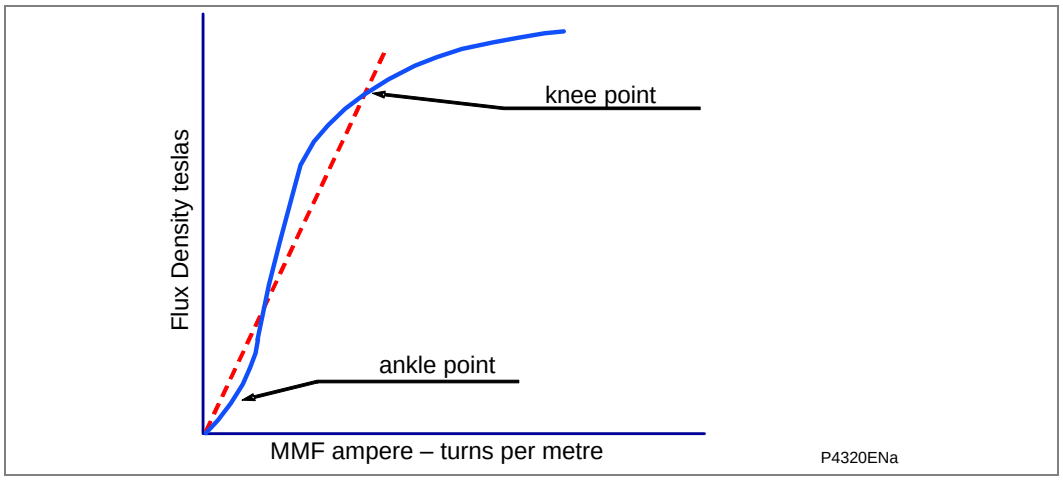


Figure 79 - Exciting characteristic for a CROSS core CT

The CT requirements for each current input will depend on the protection function with which they are related and whether the line CTs are being shared with other current inputs. Where CTs are being shared by multiple current inputs, the knee-point voltage requirements should be calculated for each input and the highest calculated value used.

IEC defines the knee-point of the excitation characteristic as the point at which a 10% increase in secondary voltage produces a 50% increase in exciting current. It may, therefore, be regarded as practical limit beyond which a specified current ratio may be maintained.

The CT magnetization curve, is usually expressed in terms of Kv, (Kv = Es/B), and Ki, (Ki = L/N, where L is the mean magnetic path) which when multiplied by the flux density in teslas and ampere-turns per m respectively gives corresponding volts and amperes.

Caution	**The secondary circuit of a Current Transformer (CT) should never be left open-circuited while primary continues to flow. In these circumstances only the primary winding is effective so the CT behaves as a highly saturated choke (induction) to the flow of primary winding current. Therefore, a peaky and relatively high value of voltage appears at the secondary output of terminals, endangering life, not to mention the possible resulting breakdown of secondary circuit insulation.**

The errors of a CT may be considered as due to the whole of the primary current not being transformed, a component of which being required to excite the core. Alternatively, as shown in the following diagram, we may consider that the whole of the primary current is transformed without loss but that the secondary current is shunted by a parallel circuit. The impedance of this parallel circuit is such that the equivalent of the exciting current flows through it. The circuit shown is the equivalent circuit of the CT. The primary current is assumed to be transformed perfectly, with no ratio or phase single error, to a current IP/N which is often called 'the primary current referred to the secondary'. A part of the current may be considered consumed in exciting the core and this current Ie is called the secondary excitation current. The remainder Is is a true secondary current. It will be evident that the excitation current is a function of the secondary excitation voltage Es and the secondary excitation impedance Ze. It will also be evident that the secondary current is a function of Es and the total impedance in the secondary circuit. This total impedance consists of the effective resistance (and any leakage reactance) of the secondary winding and the impedance of the burden.

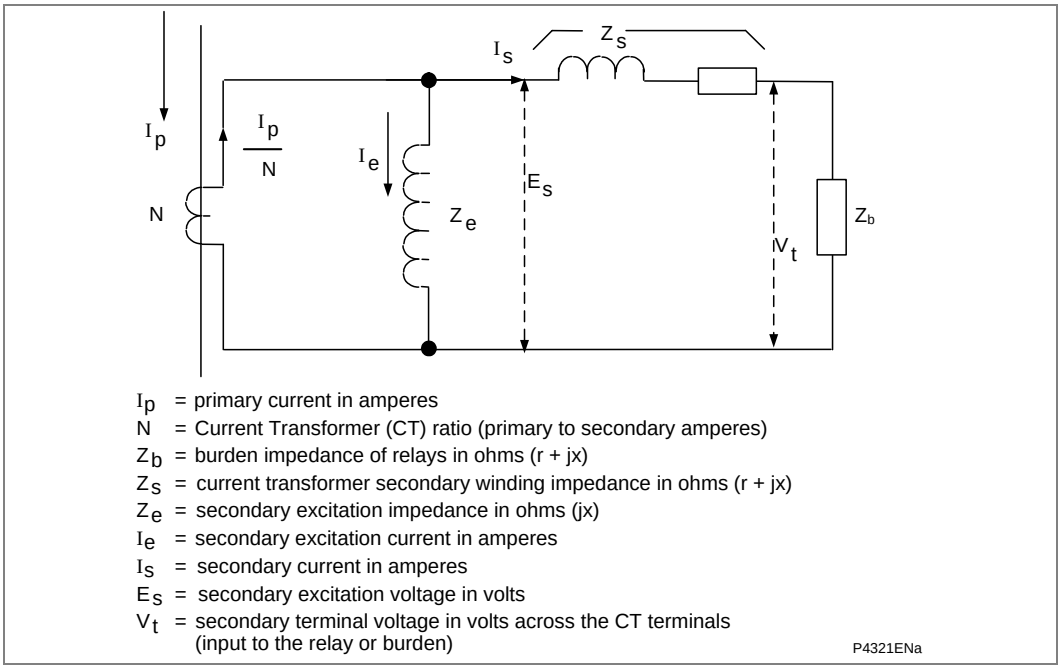


Figure 80 - CT equivalent circuit

4.1.1 Steady CT Saturation

Consider the simplified CT equivalent circuit shown in the following *Simplified CT equivalent circuit* diagram. The excitation branch is represented by a switch that closes when the CT is saturated and opens when the CT is not saturated. Therefore, during saturation no current flows through the CT secondary circuit as it is effectively shorted. It also assumes that the primary load is purely resistive.

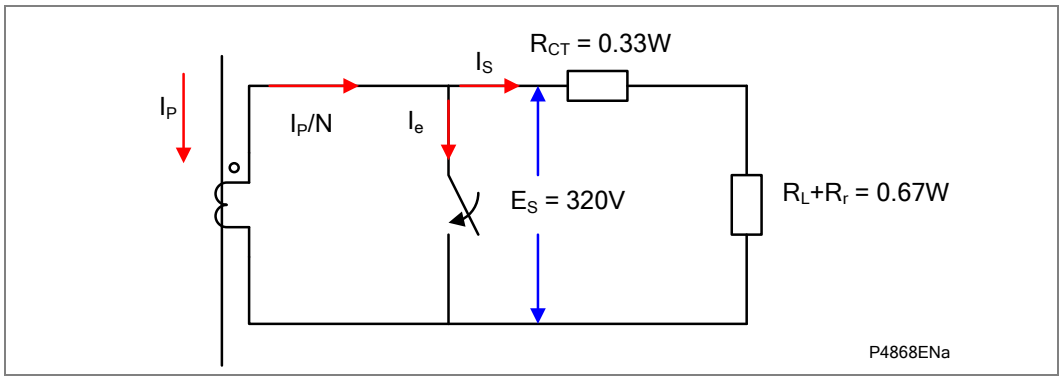


Figure 81 - Simplified CT equivalent circuit

The CT ratio is 800:5, 320 V knee point voltage, 0.33 Ω secondary winding resistance and the secondary winding turns is 160. Consider that the burden (leads and relay) connected to the CT secondary terminals is 0.67 Ω; the total burden is 0.33 Ω + 0.67 Ω = 1 Ω.

Consider that during full load, 5 A flows through the CT secondary circuit. Es is 5 V, therefore the CT operates in the linear region of the magnetizing characteristic shown below.

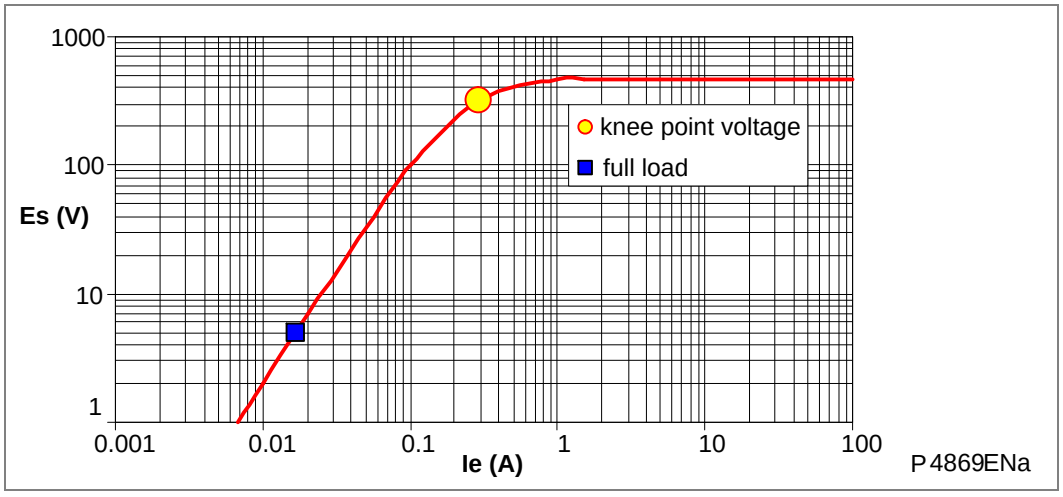


Figure 82 - CT exciting characteristic

The maximum steady state undistorted sinusoidal secondary current that may flow through the CT secondary circuit is Is = V/R = 320/1 = 320A. This corresponds to 320 × 160 = 51.2 kA primary current. 51.2 kA flowing through the CT primary circuit generates the required flux to induced E_S = 320 V in the CT secondary circuit.

The steady state primary current, secondary current, voltage and flux waveforms are as shown in the next two diagrams. Note that the maximum change in flux is 17.86 mWb. The flux is the area below the voltage waveform divided by the secondary turns, i.e.:

$$\phi(t) = \int \frac{Es}{N} dt$$

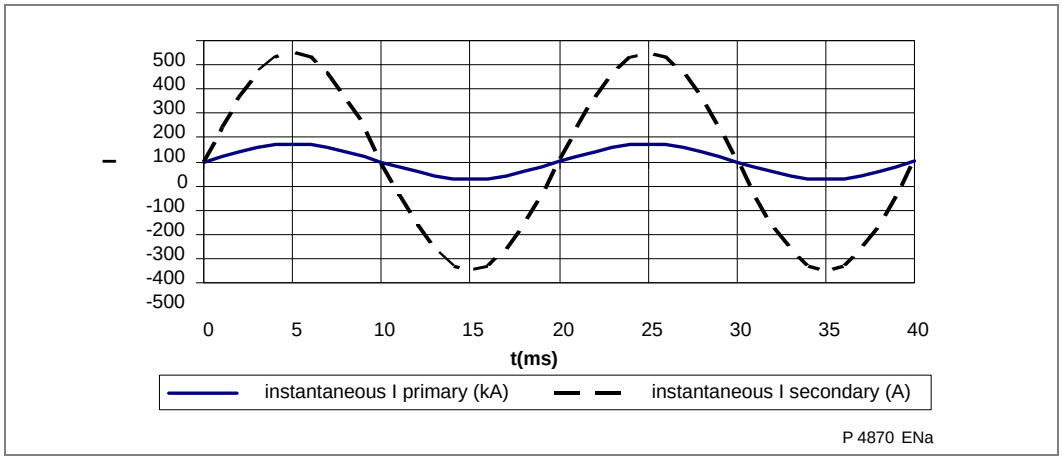


Figure 83 - Primary and secondary current waveforms at the knee point voltage

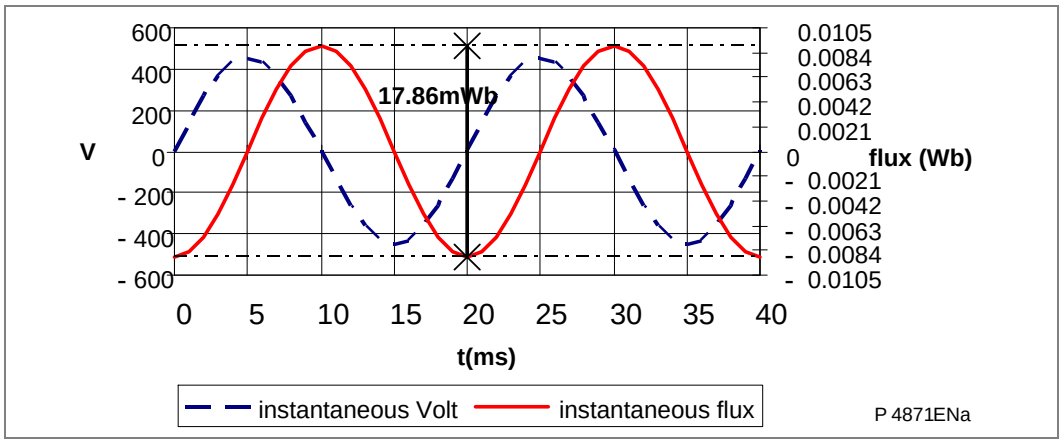


Figure 84 - CT voltage and flux waveforms at the knee point voltage

In this example, the flux must be within -8.93 mWb and 8.93 mWb to avoid saturation. If the primary current is greater than 51.2 kA, then the flux would be outside this range. Increasing the primary current to twice its value considering the simplified CT circuit increases the flux to twice its steady state value. The CT core saturates if the flux ≥ 8.93 mWb or flux ≤ -8.93 mWb. Considering the simplified CT equivalent circuit, during saturation the switch closes, as a result Es and Is collapse to zero where they remain until next primary current zero is reached. This process is repeated each half cycle and results in a pulse secondary current, voltage and flux waveforms as shown in the next two diagrams.

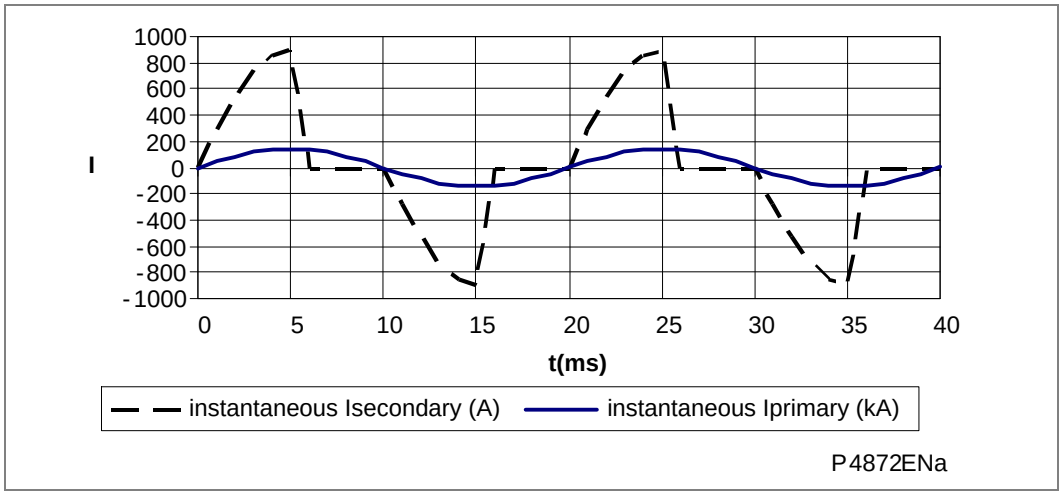


Figure 85 - Primary and secondary current waveforms – I_P = 102.4 kA

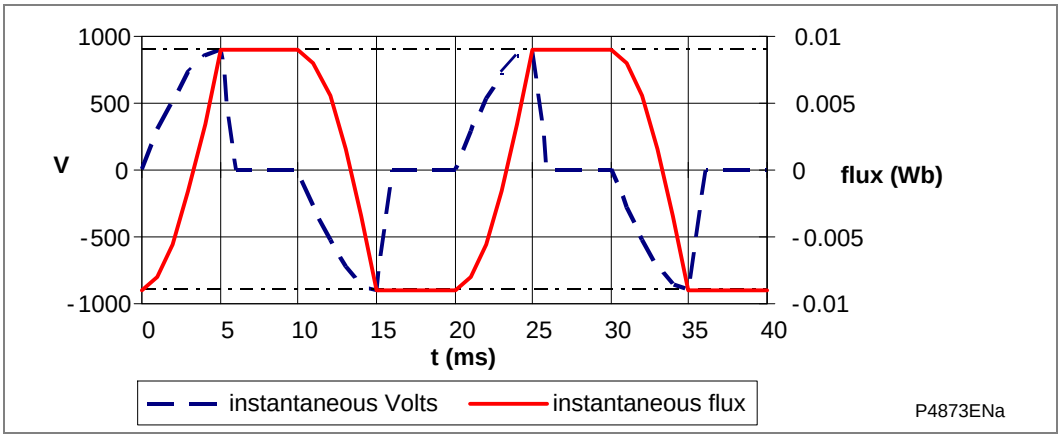


Figure 86 - Voltage and flux waveforms – I_P = 102.4 kA

4.1.2 Transient CT Saturation

Consider a primary system having and equivalent impedance equal to $Z\angle\phi$. V represents the voltage applied to the system and IP is the primary current flowing through the system. The primary current contains an AC and a DC component. The AC component is responsible for steady state CT saturation and the DC component for transient CT saturation.

The DC component is $I_p = -\frac{V_m}{Z} \times \sin(\theta-\phi)\, e^{\frac{-t}{\tau}}$

The AC component is $I_p = \frac{V_m}{Z} \times \sin(\omega t + \theta - \phi)$

$V = V_m \times \sin(\omega t + \theta)$

$$I_p = \frac{V_m}{Z}\left[\sin(\omega t + \theta - \phi) - \sin(\theta - \phi)\, e^{\frac{-t}{\tau}}\right]$$

θ = angle of the voltage waveform at t = 0s

Z = primary system impedance

$$\tau = \frac{L}{R} = \frac{X_L}{2\pi fR}$$

$$\phi = \tan^{-1}\left(\frac{X_L}{R}\right)$$

Consider the same CT used in the *Steady state CT saturation* section.

The relevant formula is shown in the following diagram.

$$I_p = 8000 \times \sqrt{2} \times \left[\sin\left(\omega t - \frac{\pi}{2}\right) + e^{\frac{-t}{0.064}}\right]$$

In this example, X/R is 20 and the maximum DC component is considered.

The maximum DC component occurs when $\sin(\theta-\phi) = \pm 1$

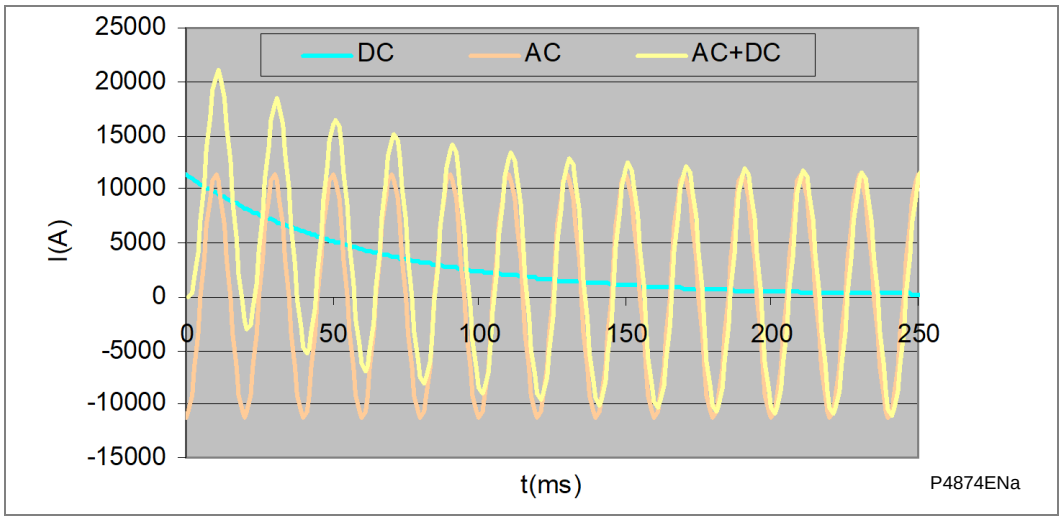


Figure 87 - Primary current – maximum DC offset

Consider that the magnetizing inductance is infinite and the CT ratio is 160; therefore the secondary current is as follows:

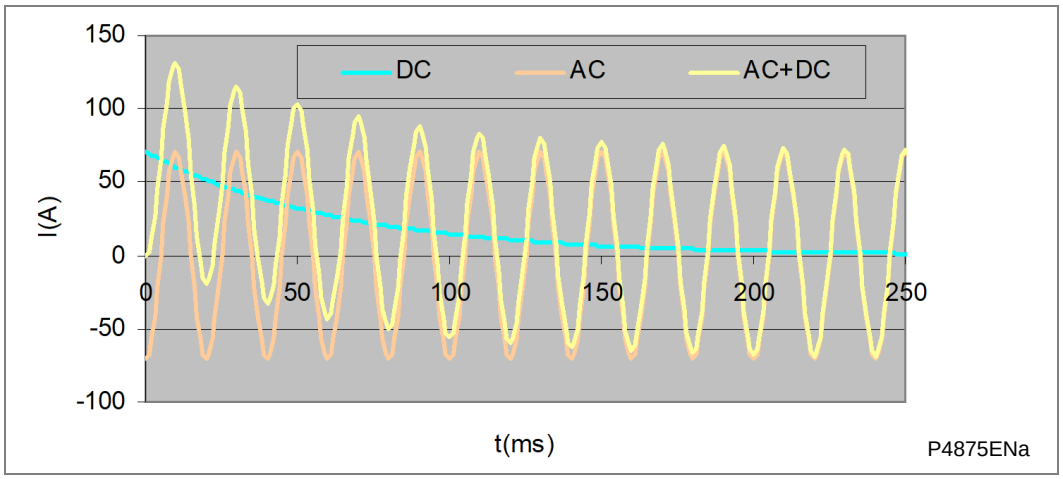


Figure 88 - Secondary current – infinite magnetizing inductance

Consider that the total secondary burden is resistive and equal to 1Ω, the voltage required to drive the secondary current shown in the above diagram is as follows:

$$V = \frac{8000 \times \sqrt{2}}{160} \times R_{burden} \times \left[\sin\left(\omega t - \frac{\pi}{2}\right) + e^{\frac{-t}{0.064}} \right] = 70.7 \left[\sin\left(\omega t - \frac{\pi}{2}\right) + e^{\frac{-t}{0.064}} \right]$$

The total flux is calculated as $\phi(t) = 0.44 \left[\frac{-\cos\left(\omega t - \frac{\pi}{2}\right)}{\omega} - 0.064 \times e^{\frac{-t}{0.064}} \right]$

The flux AC component is $\phi(t) = 0.44 \left[\frac{-\cos\left(\omega t - \frac{\pi}{2}\right)}{\omega} \right]$

The flux DC component is $\phi(t) = 0.44 \left[- 0.064 \times e^{\frac{-t}{0.064}} \right]$

The flux waveforms are shown below. It can be observed the flux required to drive the current DC component is 20 times greater than the flux required to drive the current AC component.

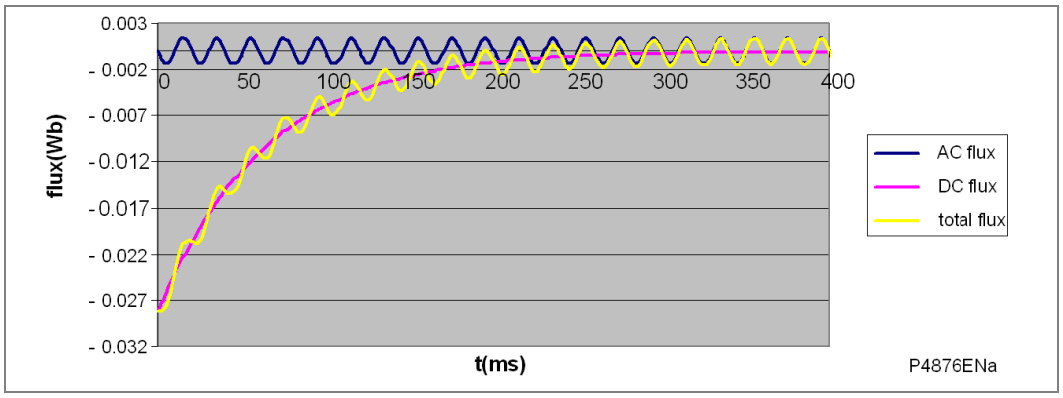


Figure 89 - Flux AC and DC components

The CT described in the *Steady CT Saturation* section the CT will saturate under the flux DC component shown above.

4.1.3 CT Errors

The following table shows the limits of error for protection CTs. At rated frequency and with rated burden connected the current error, phase displacement and composite error shall not exceed the values given in the table. For test purposes, when determining the current error and phase displacement, the burden shall have a power factor of 0.8 inductive except where the burden is less than 5 VA a power factor of 1.0 is permissible.

Limits of error for protection CTS				
Accuracy class	**Current error at rated primary Current (%)-**	**Phase displacement at rated primary current**		**Composite error at rated accuracy**
		Minutes	**Centiradians**	**Limit primary current (%)**
5P	± 1	± 60	± 1.8	5
10P	± 3			10

Table 18 - Limits of error for protection CTS

Considering the excitation impedance (Ze) as a constant, the vectorial relationships between Ip and Is is Ie. Ic constitutes the current error and Iq the component of Ie in quadrature with Is which results in the phase difference. This is shown in this diagram:

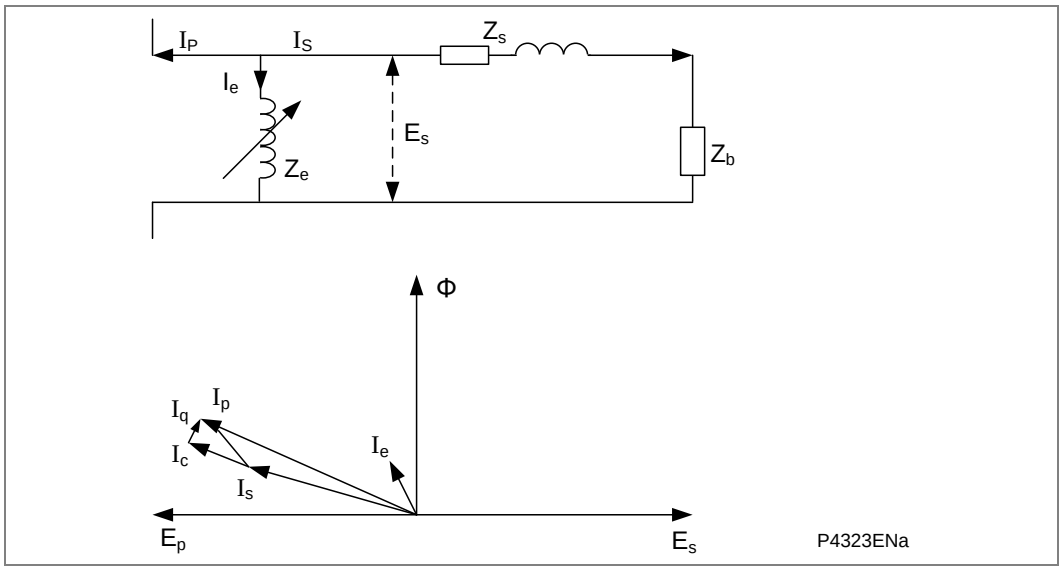


Figure 90 - CT error

If Ze was in fact a constant impedance, the vectorial error Ie of the diagram would be the composite error, but in practice the magnetizing impedance Ze is not constant with the result that the exciting current Ie contains some harmonics of the fundamental frequency which increases its rms value and therefore increases the composite error. This effect is most noticeable in the region approaching saturation of the core when the waveforms of the primary, secondary and exciting currents would be as shown.

Ratio Error (Current Error)

The ratio error is defined as the error in the secondary current due to the incorrect ratio and is expressed as a percentage, by

$[(KnIs – Ip)/Ip] \times 100\%$

Where:

Kn = the nominal ratio (rated primary current/rated secondary current)

Is = is the actual secondary current

Ip = is the actual primary current

The ratio is considered positive when the actual secondary current of the transformer is larger than the rated current

Phase Angle Error

The phase angle error is the angle by which the secondary current vector, when reversed, differs in phase from the primary current. This angle is considered as positive if the reversed secondary current vector leads the primary current.

On very low burden power factors the phase angle error may be negative. Only on rare occasions is it necessary to determine the phase error of a CT used for relaying. These occasions occur when very low circuit settings, 1% to 5% of rated current, are used in relays which are directionalized by voltage transformer inputs. For example, sensitive reverse power relays may need phase error to be taken into account to ensure correct directional operation where very low power factor primary currents are involved. For example, 1% to 3% power when certain types of prime movers are being motored such as steam turbines and hydro sets.

4.1.4 Current Transformer (CT) Ratings

Current Transformer Burden: All CT accuracy considerations require knowledge of the CT burden, which is the load applied to the secondary of the CT and should preferably be expressed in terms of the impedance of the load and its resistance and reactance components. In practice it is usual to quote the relay burdens, in the first place, in terms of V.A. (volt-amperes) and power factor. A burden of 12.5 VA at 5 A would have an ohmic value of $12.5/5^2 = 0.5$ ohm. CT burdens are usually given in preferred values, such as, 2.5, 5, 7.5, 10, 15, 30 VA.

Continuous Rated Current: This is the maximum current the CT can carry continuously. It is usually the rated primary current.

Short Time Rated Current: This is the amount of current which can flow for a given period without any harmful effects. This is usually specified for 0.5, 1, 2 or 3 seconds and with the secondary short circuited.

Rated Secondary Current: This is the maximum continuous current the secondary is rated to carry. It is usually 1 or 5 A.

Accuracy Limit Factor (ALF): A CT is designed to maintain its ratio within specified limits up to a certain value of primary current, expressed as a multiple of its rated primary current. This multiple is termed its rated ALF. In determining the ALF it is necessary to consider the maximum value of primary current up to which the CT is required to maintain its ratio.

CT primary rating is usually chosen to be equal to or greater than the normal full load current of the protected circuit. The total secondary burden of a CT includes the internal impedance of the secondary winding, the impedance of the instruments and relays which are connected to it, and the resistance of the secondary leads.

4.2 Types of Protection Current Transformers (CTs)

Generally, there are three different types of CTs:

- High remanence CTs

  The high remanence type has no given limit for the remanent flux. The CT has a magnetic core without any air gaps and the remanent flux might remain for almost infinite time. The remanent flux can be up to 70-80% of the saturation flux. Typical examples of high remanent type CTs are class P, PX, TPS, TPX according to IEC 60044 and non-gapped class C according to ANSI/IEEE.

- Low remanence CTs

  The low remanence type has a specified limit for the remanent flux. The magnetic core is provided with small air gaps to reduce the remanent flux to a level that does not exceed 10% of the saturation flux. Examples are class TPY according to IEC 60044-6 and class PR according to IEC 60044-1.

- Non remanence CTs

  The non remanence type CT has practically negligible level of remanent flux. The magnetic core has relatively large air gaps to reduce the secondary time constant of the CT (to lower the needed transient factor) which also reduces the remanent flux to practically zero level. An example is class TPZ according to IEC 60044-6.

4.3 Current Transformers (CTs) Standards

4.3.1 IEC 60044-1

Class PX: Usually specified in terms of:

- Rated Burden
- Class (5P or 10P)
- Accuracy Limit Factor (ALF)

Consider the example:

15 VA 10P20

With an external secondary burden of 15 VA the composite error will be 10% or less for primary currents up to 20 times rated current. To convert from VA and ALF into volts, use the expression:

$$V_K = \frac{V_A}{I_N} ALF$$

or when the internal voltage drop in the CT needs to be considered:

$$V_K = (ALF)\left(I_N R_{CT} + \frac{V_A}{I_N}\right)$$

Class PX current transformers are typically used for general applications.

Class PR: A current transformer with less than 10% remanent flux due to small air gaps for which, in some cases, a value of the secondary loop time constant and/or a limiting value of the winding resistance may also be specified.

Class PX: The performance of Class X current transformers of the low (secondary) reactance type shall be specified in terms of each of the following characteristics:

- Rated primary current
- Turns ratio. (The error in turns ratio shall not exceed $\pm$ 0.25%)
- Knee-point voltage
- Exciting current at the knee-point voltage or at a stated percentage of the knee-point voltage.
- Resistance of secondary winding
- Class PX type CTs are used for high impedance circulating current protection and are also suitable for most protection schemes.

4.3.2 IEC 60044-6

This standard specifies the performance of inductive CTs for currents containing exponentially decaying DC components of defined time constant.

Class TPS: Protection current transformers specified in terms of complying with class TPS are generally applied to unit systems where balancing of outputs from each end of the protected plant is vital. This balance, or stability during through fault conditions, is essentially of a transient nature so the extent of the unsaturated (or linear) zones is of paramount importance. It is normal to derive, from heavy current test results, a formula stating the lowest permissible value of Vk if stable operation is to be guaranteed.

The performance of class TPS current transformers of the low (secondary) reactance type is defined by IEC 60044-6 for transient performance. They are specified in terms of each of the following characteristics:

- Rated primary current
- Turns ratio (the error in turns ratio shall not exceed ±0.25%)
- Secondary limiting voltage
- Resistance of secondary winding

Class TPS CTs are typically applied for high impedance circulating current protection.

Class TPX: The basic characteristics for class TPX current transformers are generally similar to those of class TPS current transformers except for the different error limits prescribed and possible influencing effects which may necessitate a physically larger construction. Class TPX CTs have no air gaps in the core and therefore a high remanence factor (70-80% remanent flux). The accuracy limit is defined by the peak instantaneous error during the specified transient duty cycle.

Class TPX CTs are typically used for line protection.

Class TPY: Class TPY CTs have a specified limit for the remanent flux. The magnetic core is provided with small air gaps to reduce the remanent flux to a level that does not exceed 10% of the saturation flux. They have a higher error in current measurement than TPX during unsaturated operation and the accuracy limit is defined by peak instantaneous error during the specified transient duty cycle.

Class TPY CTs are typically used for line protection with auto-reclose.

Class TPZ: For class TPZ CTs the remanent flux is practically negligible due to large air gaps in the core. These air gaps also minimize the influence of the DC component from the primary fault current, but reduce the measuring accuracy in the unsaturated (linear) region of operation. The accuracy limit is defined by peak instantaneous alternating current component error during single energization with maximum DC offset at specified secondary loop time constant.

Class TPZ CTs are typically used for special applications such as differential protection of large generators.

4.3.3 IEEE C57.13-1978

ANSI classifications define minimum steady-state performance of Current Transformers (CTs) at high fault current levels. Performance is described by using a two-term identification system that consists of a letter and a number selected from: (C, T) (10, 20, 50, 100, 200, 400, 800), for example, C800.

The letter describes performance in terms of CT construction. “C” CTs include bushing, window, or bar-type CTs with uniformly distributed windings. “C” CTs do not have a primary winding. The primary conductor passes once through the center of a toroidal core. Since a single primary turn is used and the secondary winding is uniformly distributed, the flux that links the links the primary conductor also links the secondary winding. This type of CT has negligible leakage flux, therefore the leakage reactance is also negligible. As a result, excitation characteristic can be used directly to determine performance. The ratio correction at any current can be calculated adequately if the burden, secondary winding resistance, and the excitation characteristics are known.

Class T current transformers include wound-type CTs. These are usually constructed with more than one primary turn and undistributed windings. Due to the physical space required for insulation and bracing of the primary winding and fringing effects of non-uniformly distributed windings, flux which does not link both primary and secondary windings results. The presence of the leakage flux has a significant effect on current transformer performance. When this flux is appreciable, it is not possible to calculate ratio correction knowing the burden and the excitation characteristic. Hence, ratio correction is determined by test.

The number is the secondary terminal voltage rating. It specifies the secondary voltage that can be delivered by the full winding at 20 times rated secondary current without exceeding 10 percent ratio correction.

As an example, an 800 V rating means that the ratio correction will not exceed 10 percent at any current from 1 to 20 times rated current with a standard 8.0Ω burden. (8.0Ω times 5 A times 20 times rated secondary current equals 800 V.) The ANSI voltage rating applies to the full secondary winding only. If other than the full winding is used, the voltage rating is reduced in proportion to turns used.

4.4 Differential Function

For accuracy, class PX or class 5P Current Transformers (CTs) are strongly recommended.

The CT knee-point voltage requirements are based on these settings for transformer differential protection:

Is1 = 0.2 pu,
K1 = 30%,
Is2 = 1 pu,
K2 = 80%,
Is-HS1 = 10 pu,
Is-HS2 = 32 pu,
Ih(2)%> = 20%,
Cross blocking = enabled,
5th harm blocked = enabled,
Ih(5)%> = 35%,
CTSat and NoGap = enabled or disabled.

A series of internal and external faults were performed to determine the CT requirements for the differential function. These tests were performed under different X/R ratios, CT burdens, fault currents, fault types and point on wave. Heavy internal fault currents can cause serious CT saturation, which lead to long tripping times when the inrush restraint function is in operation. Therefore, CT saturation and NoGap detectors are implemented in the relay to speed up tripping times in such situations. However, a high CT knee point voltage can mitigate saturation to let differential protection trip in time.

Therefore, the CT requirements are quoted in the following two situations:

(1) guarantees 35ms tripping time for an internal fault;

(2) allows tripping time for an internal fault up to 75ms.

(1) The CT requirements are determined either by:

The operating time for internal faults ≤35ms (100%), and relay keeps stable for through faults

CT dimension factor K = 55

Knee point voltage: $V_k = 55 \times I_n \times (R_{CT} + 2R_L + R_r)$

(2) The CT requirements are determined either by:

The operating time for internal faults ≤35ms (85%) and ≤75ms (100%), and relay keeps stable for through fault

CT dimension factor K = 25

Knee point voltage: $V_k = 25 \times I_n \times (R_{CT} + 2R_L + R_r)$

Where:

V_K = Minimum current transformer knee-point voltage

$_n$ = Relay rated current

R_{ct} = Resistance of current transformer secondary winding (Ω)

R_L = Resistance of a single lead from relay to current transformer (Ω)

R_r = Resistance of any other protective relays sharing the current transformer (Ω)

To ensure that through fault stability is achieved the following ratios:

$V_{k\text{-}HV} / R_{tot\text{-}HV} : V_{k\text{-}LV} / R_{tot\text{-}LV}$

$V_{k\text{-}HV} / R_{tot\text{-}HV} : V_{k\text{-}TV} / R_{tot\text{-}TV}$

$V_{k\text{-}LV} / R_{tot\text{-}LV} : V_{k\text{-}TV} / R_{tot\text{-}TV}$

should not exceed a maximum disparity of 4:1. This ensures that during a through fault condition the flux density in the current transformers is not greatly different.

Where:

$V_{k\text{-}HV}$ = Knee point voltage of CT at HV side

$R_{tot\text{-}HV}$ = Total burden connected to CT at HV side
= (R_{CT} + 2R_l + R_r) or (R_{CT} + R_l + R_r)

$V_{k\text{-}LV}$ = Knee point voltage of CT at LV side

$R_{tot\text{-}LV}$ = Total burden connected to CT at LV side
= (R_{CT}+ 2R_l + R_r) or (R_{CT} + R_l + R_r)

$V_{k\text{-}TV}$ = Knee point voltage of CT at TV side

$R_{tot\text{-}TV}$ = Total burden connected to CT at TV side
= (R_{CT}+ 2R_l + R_r) or (R_{CT} + R_l + R_r)

4.4.1 Differential Function - CT Requirements Calculation Examples

All the possible system operating conditions must be analyzed to determine the appropriate CT requirements. The operating conditions of the power system are decided by the Utility practices. For example, the power system may operate under maximum or minimum generation; both conditions must be studied and the condition resulting in the highest knee point voltage considered. The highest knee point voltage is the minimum voltage required to maintain stability during through fault conditions. Consider the system shown in this diagram. The equivalent sources 1 and 2 represent the system under maximum generation. Through faults 1 and 2 are considered to determine the highest knee point voltage. In this example, only 3-phase and single-phase faults have been considered. In real applications, all fault types should be studied to determine the minimum knee point voltage needed to maintain stability during through fault conditions.

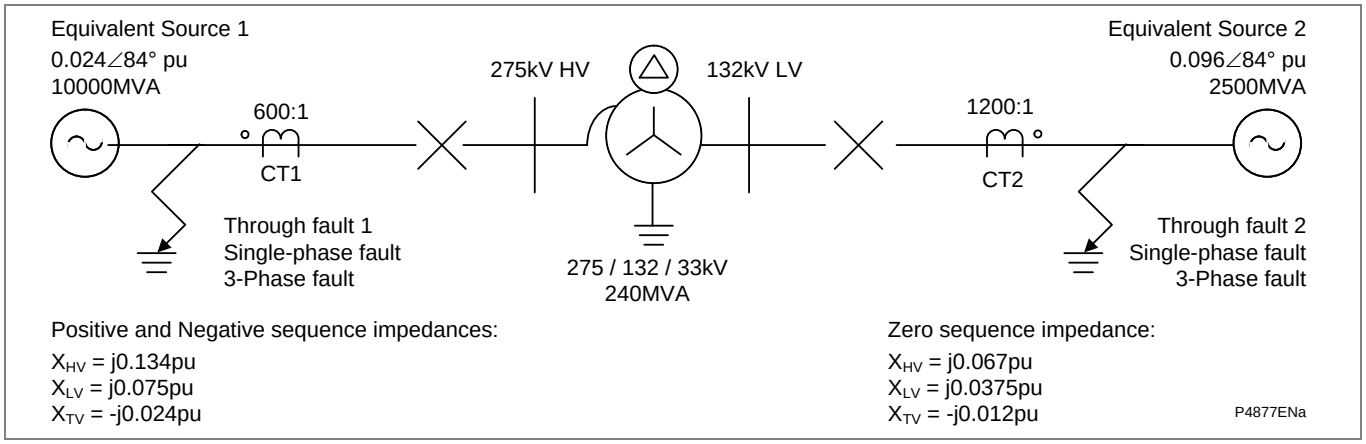


Figure 91 - CT requirements calculation

The following examples are provided:

- 4.4.1.1 - Through Fault 1 – Single Phase Fault:
- 4.4.1.2 - Through Fault 2 – Single Phase Fault:
- 4.4.1.3 - Through Fault 1 – 3-Phase Fault:
- 4.4.1.4 - Through Fault 2 – 3-Phase Fault:
- 4.4.1.5 - Summarized Results

4.4.1.1 Through Fault 1 – Single Phase Fault:

Through Fault 1 is an A phase to ground fault. The sequence network is shown in the following diagram. For a detailed calculation of the currents refer to the *Possible Misindication of the Unfaulted Phases due to Fault Current Distribution* section. The current flowing through CT1 and CT2 has been calculated as well as X/R considering source 2 and the transformer impedance.

The currents flowing through CT1 and CT2 are calculated as follows:

$$\begin{bmatrix} Ia \\ Ib \\ Ic \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix} x \begin{bmatrix} I_0 \\ I_1 \\ I_2 \end{bmatrix}$$

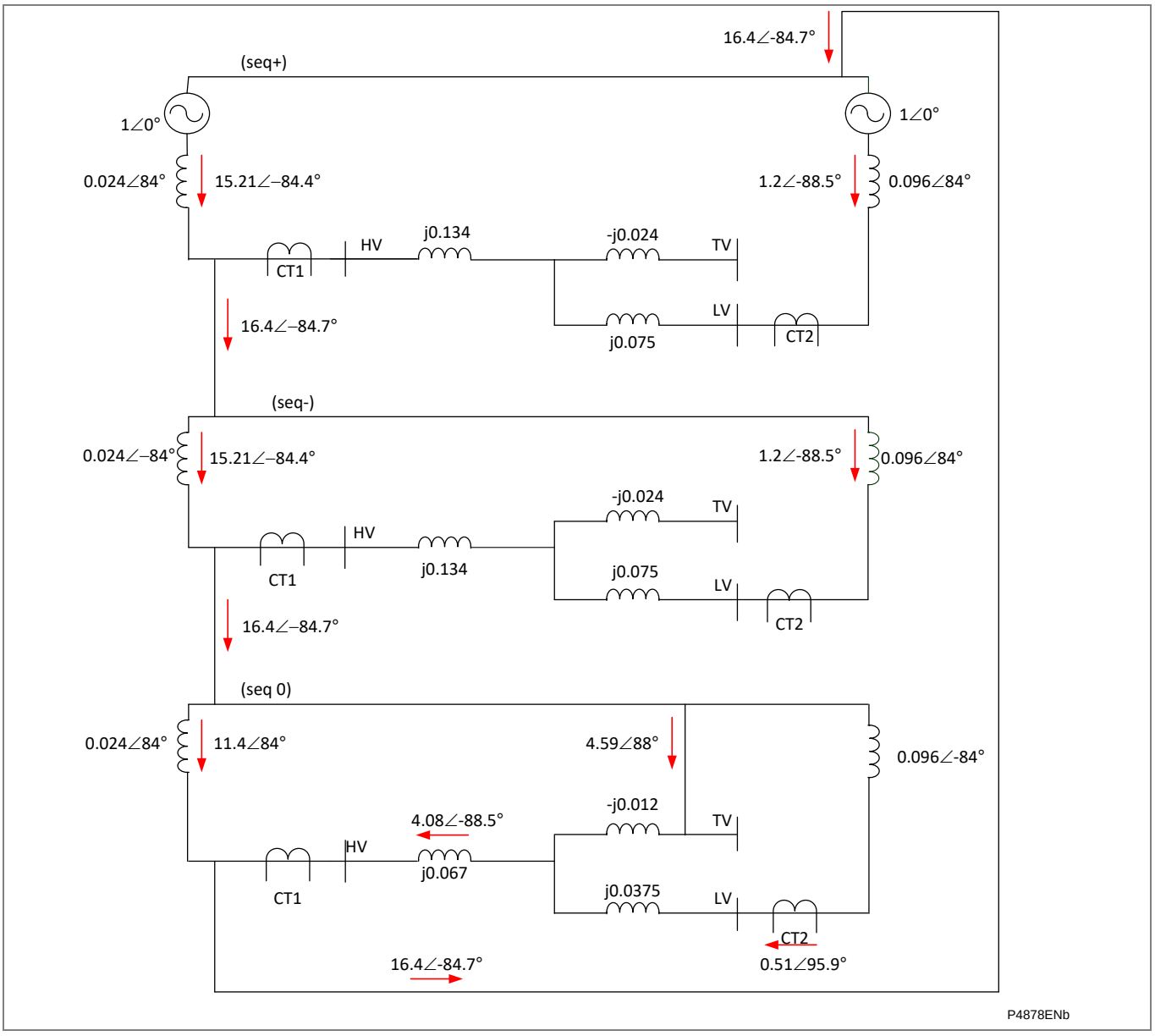


Figure 92 - Sequence network – single phase - through fault 1

Current flowing through CT1:

$I_a = I_0 + I_1 + I_2 = 5.1\angle -88.8° + 1.2\angle -88.5° + 1.2\angle -88.5° = 7.5\angle -88.7°pu$

$$\Rightarrow 7.5 \times \left(\frac{240 \times 10^6}{\sqrt{3} \times 275 \times 10^3}\right) = 3779\ A_{prim}$$

$$\Rightarrow \frac{3779}{600} = 6.3\ A\ sec$$

$I_b = I_0 + a^2 I_1 + a I_2$

$I_b = 5.1\angle -88.8° + 1\angle 240° \times 1.2\angle -88.5° + 1\angle 120° \times 1.2\angle -88.5° = 3.9\angle -88.9°pu$

$I_c = I_0 + a I_1 + a^2 I_2$

$I_c = 5.1\angle -88.8° + 1\angle 120° \times 1.2\angle -88.5° + 1\angle 240° \times 1.2\angle -88.5° = 3.9\angle -88.9°pu$

Current flowing through CT2:

$I_a = I_0 + I_1 + I_2 = 0.51\angle 95.9° + 1.2\angle -88.5° + 1.2\angle -88.5° = 1.89\angle -89.7°pu$

$$\Rightarrow 1.89 \times \left(\frac{240 \times 10^6}{\sqrt{3} \times 132 \times 10^3}\right) = 1984\ A_{prim}$$

$$\Rightarrow \frac{1984}{1200} = 1.65\ A\ sec$$

$I_b = I_0 + a^2 I_1 + a I_2$

$I_b = 0.51\angle 95.9° + 1\angle 240° \times 1.2\angle -88.5° + 1\angle 120° \times 1.2\angle -88.5° = 1.71\angle 92.8°pu$

$I_c = I_0 + a I_1 + a^2 I_2$

$I_c = 0.51\angle 95.9° + 1\angle 120° \times 1.2\angle -88.5° + 1\angle 240° \times 1.2\angle -88.5° = 1.71\angle 92.8°pu$

Equivalent X/R:

The following diagram is the equivalent sequence network of the previous one. The equivalent system responsible for the current flowing through CT1 and CT2 consists of the source and the autotransformer impedance. The equivalent system X/R is determined as follows:

$V_A = V_0 + V_1 + V_2 = 1\angle 0°pu$

$I_a = I_0 + I_1 + I_2 = 5.1\angle -88.8° + 1.2\angle -88.5° + 1.2\angle -88.5° = 7.5\angle -88.7°pu$

$$Z = \frac{V}{I} = \frac{1\angle 0°}{7.2\angle -88.7°} = 0.133\angle 88.7° \Rightarrow \frac{X}{R} = \tan(88.7) = 44$$

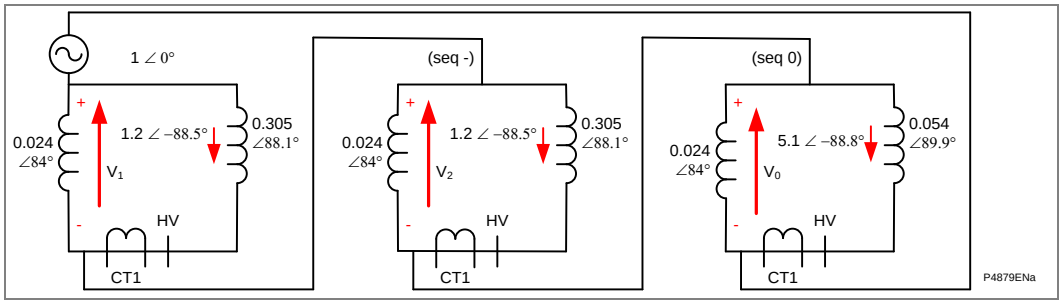


Figure 93 - Sequence network – single phase - through fault 1

4.4.1.2 Through Fault 2 – Single Phase Fault:

Through Fault 2 sequence network is shown in the following diagram. The current flowing through CT1 and CT2 is calculated as well as X/R considering source 1 and the transformer impedance.

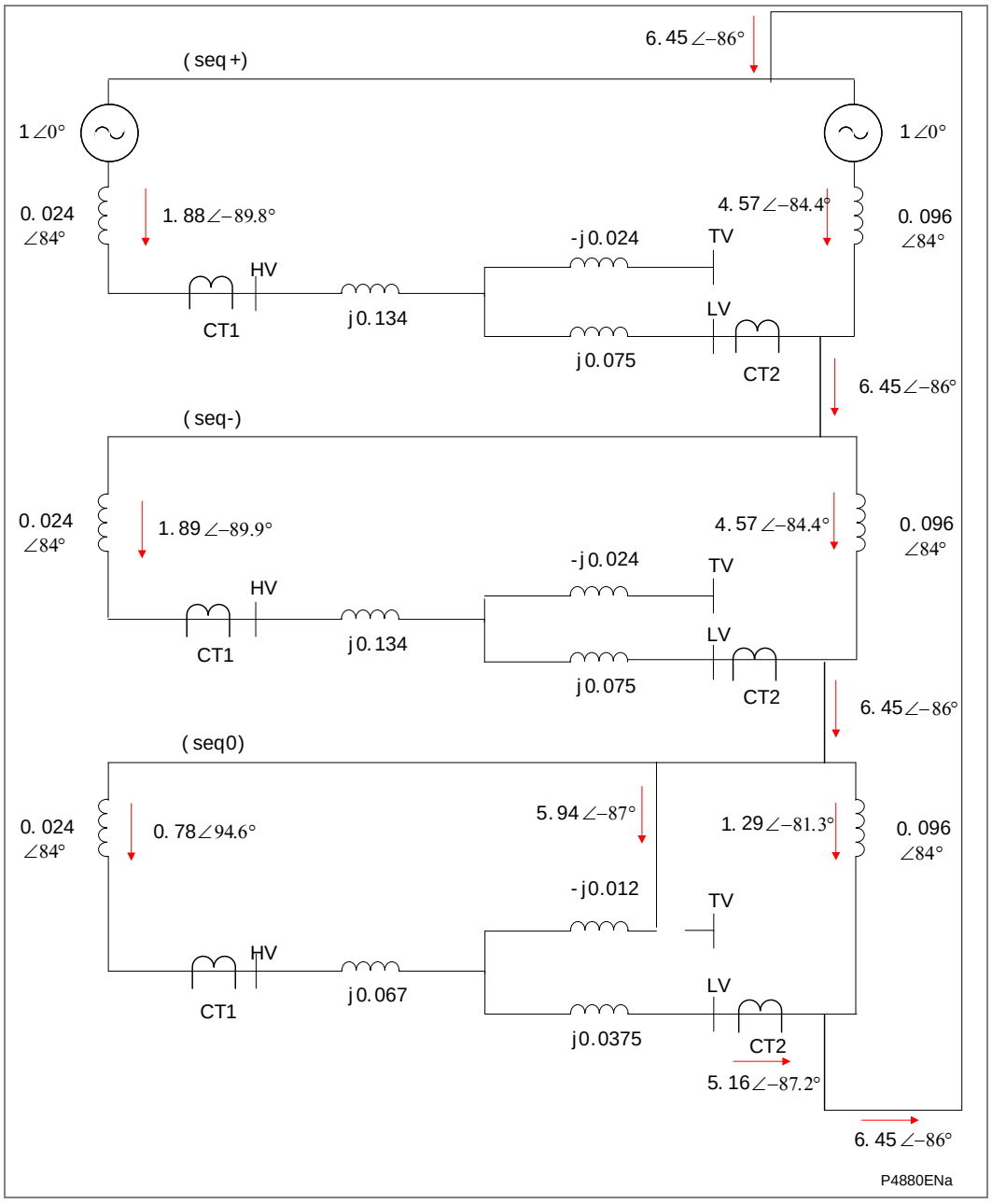


Figure 94 - Sequence network – single phase - through fault 2

The currents flowing through CT1 and CT2 are calculated as follows:

$$\begin{bmatrix} Ia \\ Ib \\ Ic \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix} x \begin{bmatrix} I_0 \\ I_1 \\ I_2 \end{bmatrix}$$

Current flowing through CT1:

$I_a = I_0 + I_1 + I_2 = 0.78\angle 94.6° + 1.88\angle -89.9° + 1.88\angle -89.9° = 2.98\angle -91°pu$

$$\Rightarrow 2.98 \times \left(\frac{240 \times 10^6}{\sqrt{3} \times 275 \times 10^3}\right) = 1502\ A_{prim}$$

$$\Rightarrow \frac{1502}{600} = 2.5A\ sec$$

$I_b = I_0 + a^2 I_1 + aI_2$

$I_b = 0.78\angle 94.6° + 1\angle 240° \times 1.88\angle -89.9° + 1\angle 120° \times 1.88\angle -89.9° = 2.66\angle 91.4°pu$

$I_c = I_0 + aI_1 + a^2 I_2$

$I_c = 0.78\angle 94.6° + 1\angle 120° \times 1.88\angle -89.9° + 1\angle 240° \times 1.88\angle -89.9° = 2.66\angle 91.4°pu$

Current flowing through CT2:

$I_a = I_0 + I_1 + I_2 = 5.16\angle -87.2° + 1.88\angle -89.9° + 1.88\angle -89.9° = 2.66\angle 91.4°pu$

$$\Rightarrow 8.9 \times \left(\frac{240 \times 10^6}{\sqrt{3} \times 132 \times 10^3}\right) = 9343\ A_{prim}$$

$$\Rightarrow \frac{9343}{1200} = 7.8A\ sec$$

$I_b = I_0 + a^2 I_1 + aI_2$

$I_b = 5.16\angle -87.2° + 1\angle 240° \times 1.88\angle -89.9° + 1\angle 120° \times 1.88\angle -89.9° = 3.28\angle -85.7°pu$

$I_c = I_0 + aI_1 + a^2 I_2$

$I_c = 5.16\angle -87.2° + 1\angle 120° \times 1.88\angle -89.9° + 1\angle 240° \times 1.88\angle -89.9° = 3.28\angle 85.7°pu$

Equivalent X/R:

The following diagram is the equivalent sequence network of the previous one. The equivalent system responsible for the current flowing through CT1 and CT2 consists of the source and the autotransformer impedance. The equivalent system X/R is determined as follows:

$V_A = V_0 = V_1 + V_2 = 1\angle 0°pu$

$I_a = I_0 + I_1 + I_2 = 1.88\angle -89.9° + 1.88\angle -89.9° + 5.16\angle -87.2° = 8.92\angle -88.3°pu$

$$Z = \frac{V}{I} = \frac{1\angle 0°}{8.92\angle -88.3°} = 0.112\angle 88.3° \Rightarrow \frac{X}{R} = \tan(88.3) = 34$$

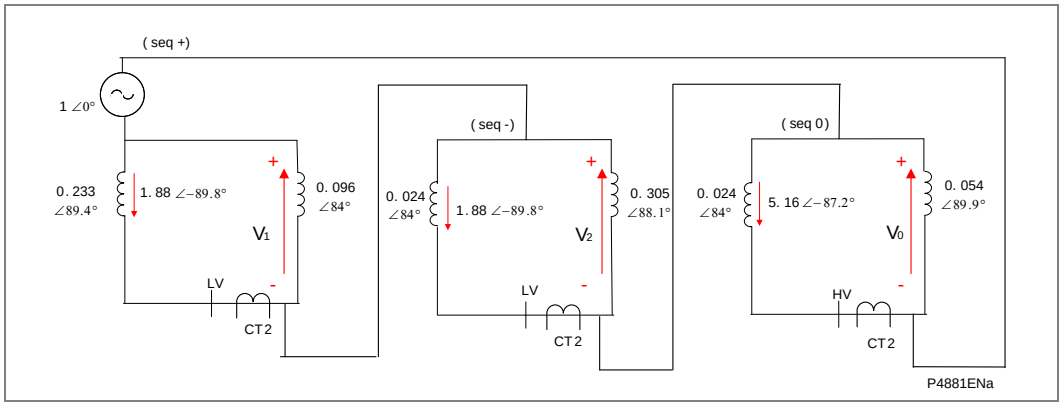


Figure 95 - Sequence network – single phase - through fault 2

4.4.1.3 **Through Fault 1 – 3-Phase Fault:**

The 3-phase through fault 1 sequence network is shown in this diagram. The current flowing through CT1 and CT2 is calculated as well as the X/R considering source 2 and the transformer impedance.

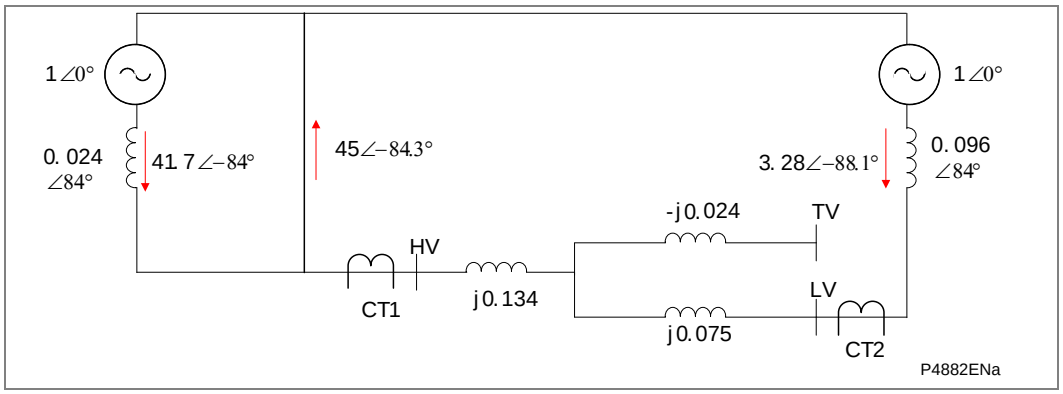


Figure 96 - Sequence network – 3-phase - through fault 1

Current flowing through CT1:

I = 3.28∠-88.1°pu

$$\Rightarrow 3.28 \times \left(\frac{240 \times 10^6}{\sqrt{3} \times 275 \times 10^3}\right) = 1653\ A_{prim}$$

$$\Rightarrow \frac{1653}{600} = 2.75A\ sec$$

Current flowing through CT2:

I = 3.28∠-88.1°pu

$$\Rightarrow 3.28 \times \left(\frac{240 \times 10^6}{\sqrt{3} \times 132 \times 10^3}\right) = 3443\ A_{prim}$$

$$\Rightarrow \frac{3443}{1200} = 2.9A\ sec$$

Equivalent X/R:

The system equivalent X/R is determined as follows:

V = 1∠-88.1°pu

I = 3.28∠-88.1°pu

$$Z = \frac{V}{I} = \frac{1\angle 0°}{3.28\angle -88.1°} = 0.30\angle 88.1° \Rightarrow \frac{X}{R} = \tan(88.1) = 30$$

4.4.1.4

Through Fault 2 – 3-Phase Fault:

The 3-phase through fault 2 sequence network is shown in the following diagram. The current flowing through CT1 and CT2 must be calculated as well as the X/R considering source 1 and the transformer impedance.

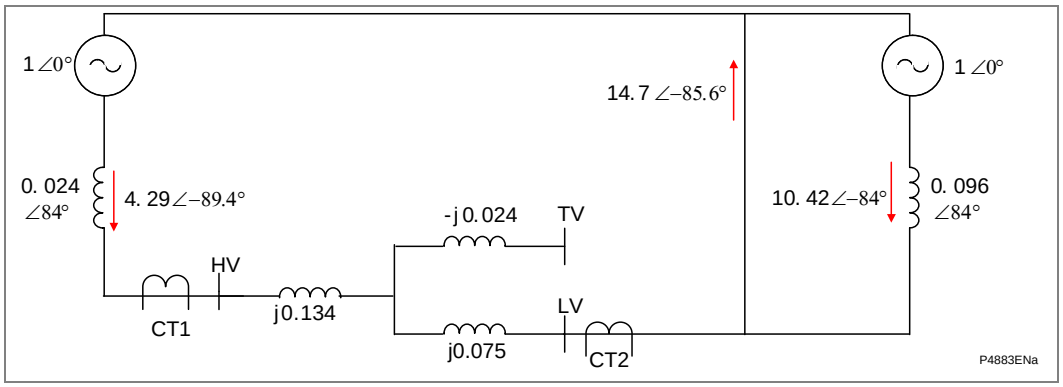


Figure 97 - Sequence network – 3-phase - through fault 2

Current flowing through CT1:

I = 4.29∠-89.4°pu

$$\Rightarrow 4.29 \times \left(\frac{240 \times 10^6}{\sqrt{3} \times 275 \times 10^3}\right) = 2162\ A_{prim}$$

$$\Rightarrow \frac{2162}{600} = 3.6A\ sec$$

Current flowing through CT2:

I = 4.29∠-89.4°pu

$$\Rightarrow 4.29 \times \left(\frac{240 \times 10^6}{\sqrt{3} \times 132 \times 10^3}\right) = 4503\ A_{prim}$$

$$\Rightarrow \frac{4503}{1200} = 3.75A\ sec$$

Equivalent X/R:

The system equivalent X/R is determined as follows:

V = 1∠-0°pu

I = 4.29∠-89.4°pu

$$Z = \frac{V}{I} = \frac{1\angle 0°}{4.29\angle -89.4°} = 0.23\angle 89.4° \Rightarrow \frac{X}{R} = \tan(89.4) = 95$$

4.4.1.5 Summarized Results

The results have been summarized as follows:

	Through Fault 1 Single Phase	Through Fault 2 Single Phase	Through Fault 1 Three Phase	Through Fault 2 Three Phase
X/R	44	34	30	95
CT1	6.3 A sec	2.5 A sec	2.75 A sec	3.6 A sec
CT2	1.65 A sec	7.8 A sec	2.9 A sec	3.75 A sec

Table 19 - Through fault single and three-phase results summary

According to the requirements of fast internal fault clearance, the K factor required is 55 and the CT knee point voltage must comply with $V_K \geq 30 \times I_n \times (R_{CT} + 2R_L + R_r)$ for single phase faults and $V_K \geq 30 \times I_n \times (R_{CT} + R_L + R_r)$ for 3-phase faults.
Consider that $R_L = 2\ \Omega$ and $R_{CT1} = 0.4\ \Omega$ and $R_{CT2} = 0.8\ \Omega$, then the knee point voltages are as follows:

	Through Fault 1 Single Phase	Through Fault 2 Single Phase	Through Fault 1 Three Phase	Through Fault 2 Three Phase
CT1	132 V	132 V	72 V	72 V
CT2	144 V	144 V	84 V	84 V

Table 20 - Through fault single and three-phase results summary

Therefore, CT1 requires a minimum knee point voltage of 132 V and CT2 a minimum knee point voltage of 144 V.

The maximum disparity ratio allowed is 4:1, then $V_{k\text{-}HV} / R_{tot\text{-}HV} : V_{k\text{-}LV} / R_{tot\text{-}LV}$ should not exceed 4:1. If CT1 and CT2 have 132 V and 144 V knee point voltages respectively, then the disparity ratio is 1:1.

4.5 Low Impedance Restricted Earth Fault (REF)

For accuracy, Class PX or Class 5P CTs should be used for low impedance Restricted Earth Fault (REF) applications.

The CT requirements for low impedance REF protection are generally lower than those for differential protection. As the line CTs for low impedance REF protection are the same as those used for differential protection the differential CT requirements cover both differential and low impedance REF applications.

The CT knee-point voltage requirements are based on the following settings for transformer REF protection; IS1 = 0.09In, IS2 = 0.9In, K1 = 0%, K2 = 150%.

A series of internal and external faults were performed to determine the CT requirements for the REF function. These tests were performed under different X/R ratios, CT burdens, fault currents, fault types and point on wave.

The K dimensioning factor for the REF function is smaller than that for the transformer differential protection. Since the highest K factor must be considered, the CT requirements for transformer differential must be considered.

4.5.1 Single Breaker Application

According to the CT requirements test results, to achieve *through fault stability* the K dimensioning factor must comply with these expressions:

System conditions: $2I_n < I_F \leq 64I_n$

$5 \leq X/R \leq 120$

Knee point voltage: $V_K \geq K \times In \times (R_{CT} + 2R_L + R_r)$

K (CT dimensioning factor): $K = 12$

Where:

V_K	=	Minimum Current Transformer (CT) knee-point voltage
K	=	CT dimensioning factor
R_{ct}	=	Resistance of CT secondary winding (Ω)
R_L	=	Resistance of a single lead from relay to CT (Ω)
R_r	=	Resistance of any other protective relays sharing the CT (Ω)
I_n	=	CT secondary nominal current (either 1A or 5)
I_F	=	Maximum external single phase fault

To ensure that the quoted operating times and through fault stability limits are met the following ratios should not exceed a maximum disparity ratio:

$V_{k\text{-}HV} / R_{tot\text{-}HV} : V_{k\text{-}TN1} / R_{tot\text{-}TN1}$

$V_{k\text{-}LV} / R_{tot\text{-}LV} : V_{k\text{-}TN2} / R_{tot\text{-}TN2}$

$V_{k\text{-}TV} / R_{tot\text{-}TV} : V_{k\text{-}TN3} / R_{tot\text{-}TN3}$

In this application, the maximum disparity ratio is 7:1.

This ensures that during a through fault condition the flux density in the current transformers is not greatly different.

Where:

$V_{k\text{-}HV}$ = Knee point voltage of CT at HV side

$R_{tot\text{-}HV}$ = Total burden connected to CT at HV side = $(R_{CT} + 2R_l + R_r)$

$V_{k\text{-}LV}$ = Knee point voltage of CT at LV side

$R_{tot\text{-}LV}$ = Total burden connected to CT at LV side = $(R_{CT} + 2R_l + R_r)$

$V_{k\text{-}TV}$ = Knee point voltage of CT at TV side

$R_{tot\text{-}TV}$ = Total burden connected to CT at TV side = $(R_{CT} + 2R_l + R_r)$

$V_{k\text{-}TN1}$ = Knee point voltage of TN1 CT

$R_{tot\text{-}TN1}$ = Total burden connected to TN1 CT = $(R_{CT} + 2R_l + R_r)$

$V_{k\text{-}TN2}$ = Knee point voltage of TN2 CT

$R_{tot\text{-}TN2}$ = Total burden connected to TN2 CT = $(R_{CT} + 2R_l + R_r)$

$V_{k\text{-}TN3}$ = Knee point voltage of TN3 CT

$R_{tot\text{-}TN3}$ = Total burden connected to TN3 CT = $(R_{CT} + 2R_l + R_r)$

4.5.2 One and a Half Breaker Application and Autotransformer Application

According to the CT requirements test results, to achieve *through fault stability* the K dimensioning factor must comply with these expressions:

System conditions: $5I_n < I_F \leq 64I_n$

$5 \leq X/R \leq 120$

Knee point voltage: $V_K \geq K \times In \times (R_{CT} + 2R_L + R_r)$

K (CT dimensioning factor): $K = 27$

Where:

V_K = Minimum Current Transformer (CT) knee-point voltage
K = CT dimensioning factor
R_{ct} = Resistance of CT secondary winding (Ω)
R_L = Resistance of a single lead from relay to CT (Ω)
R_r = Resistance of any other protective relays sharing the CT (Ω)
I_n = CT secondary nominal current (either 1A or 5)
I_F = Maximum external single phase fault

To ensure that the quoted operating times and through fault stability limits are met the following ratios should not exceed a maximum disparity ratio:

$V_{k\text{-}HV} / R_{tot\text{-}HV} : V_{k\text{-}TN1} / R_{tot\text{-}TN1}$

$V_{k\text{-}LV} / R_{tot\text{-}LV} : V_{k\text{-}TN2} / R_{tot\text{-}TN2}$

$V_{k\text{-}TV} / R_{tot\text{-}TV} : V_{k\text{-}TN3} / R_{tot\text{-}TN3}$

In this application, the maximum disparity ratio is 4:1.

This ensures that during a through fault condition the flux density in the current transformers is not greatly different.

Where:

$V_{k\text{-}HV}$ = Knee point voltage of CT at HV side
$R_{tot\text{-}HV}$ = Total burden connected to CT at HV side = $(R_{CT} + 2R_l + R_r)$
$V_{k\text{-}LV}$ = Knee point voltage of CT at LV side
$R_{tot\text{-}LV}$ = Total burden connected to CT at LV side = $(R_{CT} + 2R_l + R_r)$
$V_{k\text{-}TV}$ = Knee point voltage of CT at TV side
$R_{tot\text{-}TV}$ = Total burden connected to CT at TV side = $(R_{CT} + 2R_l + R_r)$

4.6 High Impedance Restricted Earth Fault (REF)

In a High Impedance Restricted Earth Fault (REF) scheme, the general stability voltage requirement is described by:

$V_s \geq K \times I_F (2R_L + R_{CT})$

The required stability voltage setting (V_S) is expressed in terms of an external fault (I_F), burden ($2R_L + R_{CT}$) and a stability factor (K).

A $V_K/V_S = 4$ is recommended as the average operating time is 38 ms and K is 1 approximately.

4.7 Short-Interconnector Application

For accuracy, class PX or class 5P current transformers (CTs) are strongly recommended.

The current transformer knee-point voltage requirements are based on the following settings for short-interconnector protection; IS1 = 1.2 pu, IS2 = 0.4 pu, K1 = 20%, K2 = 80%,
Is-HS1 = 10 pu, HS2 Status = disabled, 2nd harm blocked = disabled,
5th harm blocked = disabled. The matching factors are 1.0 and the zero sequence filters are disabled.

A series of internal and external faults were performed to determine the CT requirements for short-interconnector protection applications. These tests were performed under different X/R ratios, CT burdens, fault currents, fault types and point on wave.

According to the CT requirements test results, to achieve *through fault stability* the K dimensioning factor must comply with these expressions:

System conditions: $5I_n < I_F \leq 64I_n$

$5 \leq X/R \leq 120$

Knee point voltage: $V_K \geq K \times In \times (R_{CT} + 2R_L + R_r)$

K (CT dimensioning factor): $K = 28$

Where:

V_K	=	Minimum Current Transformer (CT) knee-point voltage
K	=	CT dimensioning factor
R_{ct}	=	Resistance of CT secondary winding (Ω)
R_L	=	Resistance of a single lead from relay to CT (Ω)
R_r	=	Resistance of any other protective relays sharing the CT (Ω)
I_n	=	CT secondary nominal current (either 1A or 5)
I_F	=	Maximum external single phase fault

To ensure that the quoted operating times and through fault stability limits are met the following ratios should not exceed a maximum disparity ratio:

$V_{k\text{-}HV} / R_{tot\text{-}HV} : V_{k\text{-}LV} / R_{tot\text{-}LV}$

$V_{k\text{-}HV} / R_{tot\text{-}HV} : V_{k\text{-}TV} / R_{tot\text{-}TV}$

$V_{k\text{-}LV} / R_{tot\text{-}LV} : V_{k\text{-}TV} / R_{tot\text{-}TV}$

In this application, the maximum disparity ratio is 8:1.

This ensures that during a through fault condition the flux density in the current transformers is not greatly different.

Where:
$V_{k\text{-}HV}$ = Knee point voltage of CT at HV side
$R_{tot\text{-}HV}$ = Total burden connected to CT at HV side = ($R_{CT} + 2R_l + R_r$)
$V_{k\text{-}LV}$ = Knee point voltage of CT at LV side
$R_{tot\text{-}LV}$ = Total burden connected to CT at LV side = ($R_{CT}+ 2R_l + R_r$)
$V_{k\text{-}TV}$ = Knee point voltage of CT at TV side
$R_{tot\text{-}TV}$ = Total burden connected to CT at TV side = ($R_{CT}+ 2R_l + R_r$)

4.8 Converting IEC185 CT Standard Protection Classification to Knee-Point Voltage

The suitability of an IEC standard protection class Current Transformer (CT) can be checked against the kneepoint voltage requirements specified previously.

If, for example, the available CTs have a 15 VA 5P 10 designation, then an estimated kneepoint voltage can be obtained as follows:

$$V_k = \frac{VA \times ALF}{In} + A_{LF} \times I_n \times R_{ct}$$

Where:

V_k	=	Required kneepoint voltage
VA	=	Current transformer rated burden (VA)
ALF	=	Accuracy limit factor
I_n	=	Current transformer secondary rated current (A)
R_{ct}	=	Resistance of current transformer secondary winding (Ω)

If Rct is not available, then the second term in the above equation can be ignored.
Example: 400/5A, 15VA 5P 10, Rct = 0.2Ω

$$V_k = \frac{15 \times 10}{5} + 10 \times 5 \times 0.2 \quad = 40 \text{ V}$$

4.9 Converting IEC185 CT Standard Protection Classification to ANSI/IEEE Standard Voltage

MiCOM Px40 series protection is compatible with ANSI/IEEE current transformers as specified in the IEEE C57.13 standard. The applicable class for protection is class "C", which specifies a non air-gapped core. The CT design is identical to IEC class P / PX, or British Standard class X, but the rating is specified differently.

The ANSI/IEEE “C” Class standard voltage rating required will be lower than an IEC knee point voltage. This is because the ANSI/IEEE voltage rating is defined in terms of useful output voltage at the terminals of the CT, whereas the IEC knee point voltage includes the voltage drop across the internal resistance of the CT secondary winding added to the useful output. The IEC/BS knee point is also typically 5% higher than the ANSI/IEEE knee point. Therefore:

$V_c = [V_k - \text{Internal voltage drop}] / 1.05$
$= [V_k - (In . RCT . ALF)] / 1.05$

Where:

Vc	=	“C” Class standard voltage rating
Vk	=	IEC Knee point voltage required
In	=	CT rated current = 5 A in USA
RCT	=	CT secondary winding resistance (for 5 A CTs, the typical resistance is 0.002 ohms/secondary turn)
ALF	=	The CT accuracy limit factor, the rated dynamic current output of a "C" class CT (Kssc) is always 20 x In

The IEC accuracy limit factor is identical to the 20 times secondary current ANSI/IEEE rating. Therefore:

$V_c = [V_k - (100 . R_{CT})] / 1.05$

5 AUXILIARY SUPPLY FUSE RATING

In the Safety Information part of this manual, the maximum allowable fuse rating of 16A is quoted. To allow time grading with fuses upstream, a lower fuselink current rating is often preferable. Use of standard ratings of between 6A and 16A is recommended. Low voltage fuselinks, rated at 250V minimum and compliant with IEC60269-2 general application type gG are acceptable, with high rupturing capacity. This gives equivalent characteristics to HRC "red spot" fuses type NIT/TIA often specified historically.

The table below recommends advisory limits on relays connected per fused spur. This applies to MiCOM Px40 series devices with hardware suffix C and higher, as these have inrush current limitation on switch-on, to conserve the fuse-link.

Maximum Number of MiCOM Px40 Relays Recommended Per Fuse				
Battery Nominal Voltage	**6A**	**10A Fuse**	**15 or 16A Fuse**	**Fuse Rating > 16A**
24 to 54V	2	4	6	Not permitted
60 to 125V	4	8	12	Not permitted
138 to 250V	6	10	16	Not permitted
Alternatively, Miniature Circuit Breakers (MCBs) may be used to protect the auxiliary supply circuits.				

Table 21 - Maximum number of MiCOM Px40 relays recommended per fuse

USING THE PSL EDITOR

CHAPTER 7

Date:	08/2017	
Products covered by this chapter:	This chapter covers the specific versions of the MiCOM products listed below. This includes ***only*** the following combinations of Software Version and Hardware Suffix.	
Hardware Suffix:	All MiCOM Px4x products	
Software Version:	All MiCOM Px4x products	
Connection Diagrams:	P14x (P141, P142, P143 & P145): 10P141xx (xx = 01 to 02) 10P142xx (xx = 01 to 05) 10P143xx (xx = 01 to 11) 10P145xx (xx = 01 to 11) P24x (P241, P242 & P243): 10P241xx (xx = 01 to 02) 10P242xx (xx = 01) 10P243xx (xx = 01) P341: 10P341xx (xx = 01 to 12) P34x (P342, P343, P344, P345 & P391): 10P342xx (xx = 01 to 17) 10P343xx (xx = 01 to 19) 10P344xx (xx = 01 to 12) 10P345xx (xx = 01 to 07) 10P391xx (xx = 01 to 02) P445: 10P445xx (xx = 01 to 04) P44x: 10P44101 (SH 1 & 2) 10P44201 (SH 1 & 2) 10P44202 (SH 1) 10P44203 (SH 1 & 2) 10P44401 (SH 1) 10P44402 (SH 1) 10P44403 (SH 1 & 2) 10P44404 (SH 1) 10P44405 (SH 1) 10P44407 (SH 1 & 2) P44y (P443 & P446): 10P44303 (SH 01 and 03) 10P44304 (SH 01 and 03) 10P44305 (SH 01 and 03) 10P44306 (SH 01 and 03) 10P44600 10P44601 (SH 1 to 2) 10P44602 (SH 1 to 2) 10P44603 (SH 1 to 2)	P54x (P543, P544, P545 & P546): 10P54302 (SH 1 to 2) 10P54303 (SH 1 to 2) 10P54400 10P54404 (SH 1 to 2) 10P54405 (SH 1 to 2) 10P54502 (SH 1 to 2) 10P54503 (SH 1 to 2) 10P54600 10P54604 (SH 1 to 2) 10P54605 (SH 1 to 2) 10P54606 (SH 1 to 2) P547: 10P54702xx (xx = 01 to 02) 10P54703xx (xx = 01 to 02) 10P54704xx (xx = 01 to 02) 10P54705xx (xx = 01 to 02) P64x (P642, P643 & P645): 10P642xx (xx = 01 to 10) 10P643xx (xx = 01 to 06) 10P645xx (xx = 01 to 09) P74x: 10P740xx (xx = 01 to 07) P746: 10P746xx (xx = 00 to 21) P841: 10P84100 10P84101 (SH 1 to 2) 10P84102 (SH 1 to 2) 10P84103 (SH 1 to 2) 10P84104 (SH 1 to 2) 10P84105 (SH 1 to 2) P849: 10P849xx (xx = 01 to 06)

CONTENTS

FIGURES

Page (SE) 7-

TABLES

Notes:

1 OVERVIEW

The purpose of the Programmable Scheme Logic (PSL) is to allow the relay user to configure an individual protection scheme to suit their own particular application. This is achieved through the use of programmable logic gates and delay timers.
The input to the PSL is any combination of the status of opto inputs. It is also used to assign the mapping of functions to the opto inputs and output contacts, the outputs of the protection elements, e.g. protection starts and trips, and the outputs of the fixed protection scheme logic. The fixed scheme logic provides the relay's standard protection schemes.
The PSL itself consists of software logic gates and timers. The logic gates can be programmed to perform a range of different logic functions and can accept any number of inputs. The timers are used either to create a programmable delay, and/or to condition the logic outputs, e.g. to create a pulse of fixed duration on the output regardless of the length of the pulse on the input. The outputs of the PSL are the LEDs on the front panel of the relay and the output contacts at the rear.
The execution of the PSL logic is event driven; the logic is processed whenever any of its inputs change, for example as a result of a change in one of the digital input signals or a trip output from a protection element. Also, only the part of the PSL logic that is affected by the particular input change that has occurred is processed. This reduces the amount of processing time that is used by the PSL; even with large, complex PSL schemes the relay trip time will not lengthen.
This system provides flexibility for the user to create their own scheme logic design. However, it also means that the PSL can be configured into a very complex system; hence setting of the PSL is implemented through the PC support package Easergy Studio.

Note	*MiCOM S1 Studio has been renamed as Easergy Studio.*

2 EASERGY STUDIO PSL EDITOR

Note	*MiCOM S1 Studio has been renamed as Easergy Studio.*

The PSL Editor can be used inside Easergy Studio or directly.
This chapter assumes that you are using the PSL Editor from within Easergy Studio.
If you use it from Easergy Studio, the Studio software will be locked whilst you are using the PSL editor software. The Studio software will be unlocked when you close the PSL Editor software.
The Easergy Studio product is updated periodically. These updates provide support for new features (such as allowing you to manage new MiCOM products, as well as using new software releases and hardware suffixes). The updates may also include fixes.
Accordingly, we strongly advise customers to use the latest Schneider Electric version of Easergy Studio.
If you need more information regarding bug fixes, please contact your **Schneider Electric** local support.

2.1 How to Obtain Easergy Studio Software

Easergy Studio is available from the Schneider Electric website:

- www.schneider-electric.com

2.2 To Start Easergy Studio

To Start the Easergy Studio software, click the **Start** > **All apps** > **Schneider Electric** > **Easergy Studio** menu option.

2.3 To Open a Pre-Existing System

Within Easergy Studio, click the **File** + **Open System** menu option.
Navigate to where the scheme is stored, then double-click to open the scheme.

2.4 To Start the PSL Editor

The PSL editor lets you connect to any MiCOM device front port, retrieve and edit its PSL files and send the modified file back to a suitable MiCOM device.
Px30 and Px40 products are edited using different versions of the PSL Editor. There is one link to the Px30 editor and one link to the Px40 editor.
To start the PSL editor for Px40 products:

Highlight the PSL file you wish to edit, and then either:

Double-click the highlighted PSL file,

Click the open icon or

In the Easergy Studio main menu, select Tools > PSL PSL editor (Px40) menu.

The PSL Editor will then start, and show you the relevant PSL Diagram(s) for the file you have opened. An example of such a PSL diagram is shown in the *Example of a PSL editor module* diagram.

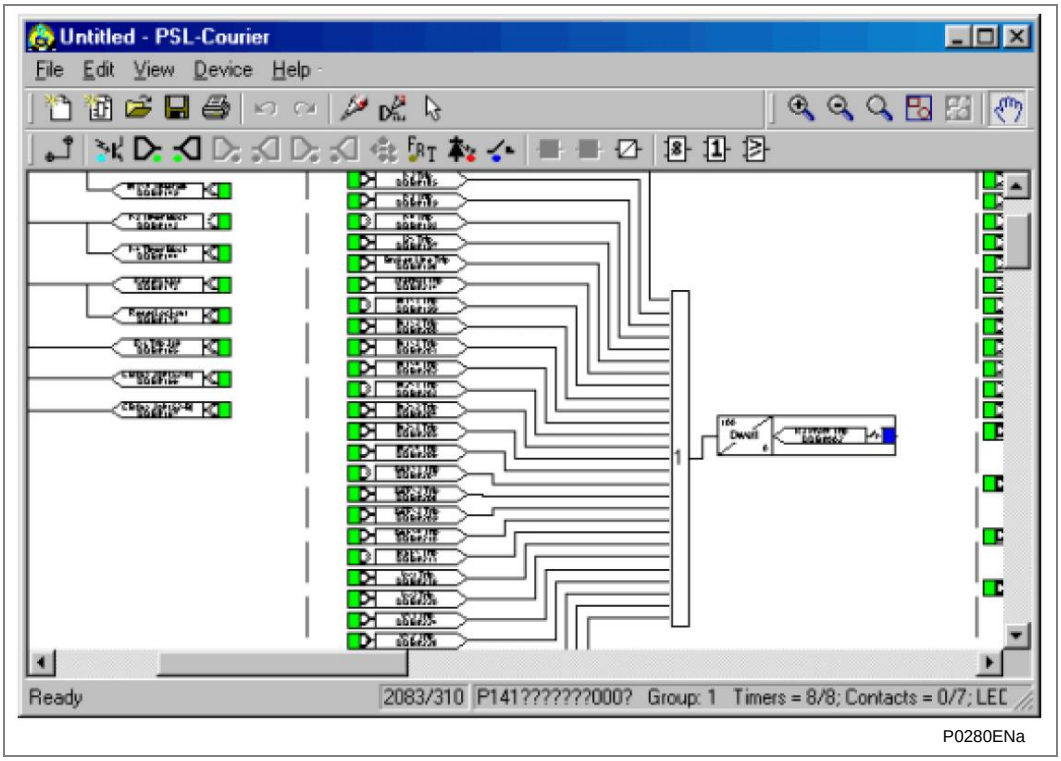


Figure 1 - Example of a PSL editor module

2.5 How to use MiCOM PSL Editor

The MiCOM PSL editor lets you:

- Start a new PSL diagram
- Extract a PSL file from a MiCOM Px40 IED
- Open a diagram from a PSL file
- Add logic components to a PSL file
- Move components in a PSL file
- Edit link of a PSL file
- Add link to a PSL file
- Highlight path in a PSL file
- Use a conditioner output to control logic
- Download PSL file to a MiCOM Px40 IED
- Print PSL files

For a detailed discussion on how to use these functions, please refer to the Easergy Studio online help.

2.6 Warnings

Before the scheme is sent to the relay checks are done. Various warning messages may be displayed as a result of these checks.
The Editor first reads in the model number of the connected relay, then compares it with the stored model number. A "wildcard" comparison is used. If a model mismatch occurs, a warning is generated before sending starts. Both the stored model number and the number read from the relay are displayed with the warning. However, the user must decide if the settings to be sent are compatible with the relay that is connected. Ignoring the warning could lead to undesired behavior of the relay.
If there are any potential problems of an obvious nature then a list will be generated. The types of potential problems that the program attempts to detect are:

- One or more gates, LED signals, contact signals, and/or timers have their outputs linked directly back to their inputs. An erroneous link of this sort could lock up the relay, or cause other more subtle problems to arise.
- Inputs to Trigger (ITT) exceeds the number of inputs. If a programmable gate has its ITT value set to greater than the number of actual inputs; the gate can never activate. There is no lower ITT value check. A 0-value does not generate a warning.
- Too many gates. There is a theoretical upper limit of 256 gates in a scheme, but the practical limit is determined by the complexity of the logic. In practice the scheme would have to be very complex, and this error is unlikely to occur.
- Too many links. There is no fixed upper limit to the number of links in a scheme. However, as with the maximum number of gates, the practical limit is determined by the complexity of the logic. In practice the scheme would have to be very complex, and this error is unlikely to occur.

3 TOOLBAR AND COMMANDS

There are a number of toolbars available for easy navigation and editing of PSL.

3.1 Standard Tools

For file management and printing.

	Blank Scheme	Create a blank scheme based on a relay model.
	Default Configuration	Create a default scheme based on a relay model.
	Open	Open an existing diagram.
	Save	Save the active diagram.
	Print	Display the Windows Print dialog, enabling you to print the current diagram.
	Undo	Undo the last action.
	Redo	Redo the previously undone action.
	Redraw	Redraw the diagram.
	No of DDBs	Display the DDB numbers of the links.
	Calculate CRC	Calculate unique number based on both the function and layout of the logic.
	Compare Files	Compare current file with another stored on disk.
	Select	Enable the select function. While this button is active, the mouse pointer is displayed as an arrow. This is the default mouse pointer. It is sometimes referred to as the selection pointer.

Point to a component and click the left mouse button to select it. Several components may be selected by clicking the left mouse button on the diagram and dragging the pointer to create a rectangular selection area.

3.2 Alignment Tools

To align logic elements horizontally or vertically into groups.

	Align Top	Align all selected components so the top of each is level with the others.
	Align Middle	Align all selected components so the middle of each is level with the others.
	Align Bottom	Align all selected components so the bottom of each is level with the others.
	Align Left	Align all selected components so the leftmost point of each is level with the others.
	Align Centre	Align all selected components so the centre of each is level with the others.
	Align Right	Align all selected components so the rightmost point of each is level with the others.

3.3 Drawing Tools

To add text comments and other annotations, for easier reading of PSL schemes.

	Rectangle	When selected, move the mouse pointer to where you want one of the corners to be hold down the left mouse button and move it to where you want the diagonally opposite corner to be. Release the button. To draw a square hold down the SHIFT key to ensure height and width remain the same.
	Ellipse	When selected, move the mouse pointer to where you want one of the corners to be hold down the left mouse button and move until the ellipse is the size you want it to be. Release the button. To draw a circle hold down the SHIFT key to ensure height and width remain the same.
	Line	When selected, move the mouse pointer to where you want the line to start, hold down left mouse, move to the position of the end of the line and release button. To draw horizontal or vertical lines only hold down the SHIFT key.
	Polyline	When selected, move the mouse pointer to where you want the polyline to start and click the left mouse button. Now move to the next point on the line and click the left button. Double click to indicate the final point in the polyline.
	Curve	When selected, move the mouse pointer to where you want the polycurve to start and click the left mouse button. Each time you click the button after this a line will be drawn, each line bisects its associated curve. Double click to end. The straight lines will disappear leaving the polycurve. Note: whilst drawing the lines associated with the polycurve, a curve will not be displayed until either three lines in succession have been drawn or the polycurve line is complete.
	Text	When selected, move the mouse pointer to where you want the text to begin and click the left mouse button. To change the font, size or colour, or text attributes select Properties from the right mouse button menu.
	Image	When selected, the Open dialog is displayed, enabling you to select a bitmap or icon file. Click Open, position the mouse pointer where you want the image to be and click the left mouse button.

3.4 Nudge Tools

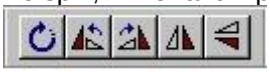
To move logic elements.

The nudge tool buttons enable you to shift a selected component a single unit in the selected direction, or five pixels if the SHIFT key is held down.
As well as using the tool buttons, single unit nudge actions on the selected components can be achieved using the arrow keys on the keyboard.

	Nudge Up	Shift the selected component(s) upwards by one unit. Holding down the SHIFT key while clicking on this button will shift the component five units upwards.
	Nudge Down	Shift the selected component(s) downwards by one unit. Holding down the SHIFT key while clicking on this button will shift the component five units downwards.
	Nudge Left	Shift the selected component(s) to the left by one unit. Holding down the SHIFT key while clicking on this button will shift the component five units to the left.
	Nudge Right	Shift the selected component(s) to the right by one unit. Holding down the SHIFT key while clicking on this button will shift the component five units to the right.

3.5 Rotation Tools

To spin, mirror and flip.



	Free Rotate	Enable the rotation function. While rotation is active components may be rotated as required. Press the ESC key or click on the diagram to disable the function.
	Rotate Left	Rotate the selected component 90 degrees to the left.
	Rotate Right	Rotate the selected component 90 degrees to the right.
	Flip Horizontal	Flip the component horizontally.
	Flip Vertical	Flip the component vertically.

3.6 Structure Tools

To change the stacking order of logic components.

	Bring to Front	Bring the selected components in front of all other components.
	Send to Back	Bring the selected components behind all other components.
	Bring Forward	Bring the selected component forward one layer.
	Send Backward	Send the selected component backwards one layer.

3.7 Zoom and Pan Tools

For scaling the displayed screen size, viewing the entire PSL, or zooming to a selection.

	Zoom In	Increases the Zoom magnification by 25%.
	Zoom Out	Decreases the Zoom magnification by 25%.
	Zoom	Enable the zoom function. While this button is active, the mouse pointer is displayed as a magnifying glass. Right-clicking will zoom out and left-clicking will zoom in. Press the ESC key to return to the selection pointer. Click and drag to zoom in to an area.
	Zoom to Fit	Display at the highest magnification that will show all the diagram's components.
	Zoom to Selection	Display at the highest magnification that will show the selected component(s).
	Pan	Enable the pan function. While this button is active, the mouse pointer is displayed as a hand. Hold down the left mouse button and drag the pointer across the diagram to pan. Press the ESC key to return to the selection pointer.

3.8 Logic Symbols

This toolbar provides icons to place each type of logic element into the scheme diagram. Not all elements are available in all devices. Icons will only be displayed for those elements available in the selected device. Depending on the device, the toolbar may not include Function key or coloured LED conditioner/signal or Contact conditioner or SR Gate icons.

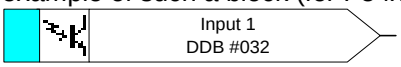
P2718ENa

Link Create a link between two logic symbols.	
Opto Signal Create an opto signal.	
Input Signal Create an input signal.	
Output Signal Create an output signal.	
GOOSE In Create an input signal to logic to receive a UCA2.0 or IEC 61850 GOOSE message transmitted from another IED.	
GOOSE Out Create an output signal from logic to transmit a UCA2.0 or IEC 61850 GOOSE message to another IED.	
Control In Create an input signal to logic that can be operated from an external command.	
Integral Intertripping In/InterMiCOM In Create an input signal to logic to receive a MiCOM command transmitted from another IED. InterMiCOM is not available for all products.	
Integral Intertripping Out/InterMiCOM OutCreate an output signal from logic to transmit a MiCOM command to another IED. InterMiCOM is not available for all products.	

Function Key Create a function key input signal.	
Trigger Signal Create a fault record trigger.	
LED Signal Create an LED input signal that repeats the status of the LED. The icon colour shows whether the product uses mono-colour or tri-color LEDs.	
Contact Signal Create a contact signal.	
LED Conditioner Create a LED conditioner. The icon colour shows whether the product uses mono-colour or tri-color LEDs.	
Contact Conditioner Create a contact conditioner. Contact conditioning is not available for all products.	
Timer Create a timer.	
AND Gate Create an AND Gate.	
OR Gate Create an OR Gate.	
Programmable Gate Create a programmable gate.	
SR gate Create an SR gate.	

4 PSL LOGIC SIGNALS PROPERTIES

The logic signal toolbar is used for the selection of logic signals.
This allows you to link signals together to program the PSL. A number of different properties are associated with each signal. In the following sections, these are characterized by the use of an icon from the toolbar; together with a signal name and a DDB number. The name and DDB number are shown in a pointed rectangular block, which includes a colour code, the icon, the name, DDB No and a directional pointer. One example of such a block (for P54x for Opto Signal 1 DDB No #032) is shown below:



More examples of these are shown in the following properties sections.

Important	**The DDB Numbers vary according to the particular product and the particular name, so that Opto Signal 1 may not be DDB No #032 for all products. The various names and DDB numbers illustrated below are provided as an example.** **You need to look up the DDB numbers for the signal and the specific MiCOM product you are working on in the relevant DDB table for your chosen product.** **Available functions will depend on model/firmware version.**

4.1 Signal Properties Menu

The logic signal toolbar is used for the selection of logic signals. To use this:

- Use the logic toolbar to select logic signals.
  This is enabled by default but to hide or show it, select **View** > **Logic Toolbar**.
- Zoom in or out of a logic diagram using the toolbar icon or select **View** > **Zoom Percent**.
- Right-click any logic signal and a context-sensitive menu appears.
- Certain logic elements show the **Properties…** option. Select this and a **Component Properties** window appears. The Component Properties window and the signals listed vary depending on the logic symbol selected.

The following subsections describe each of the available logic symbols.

4.2 Link Properties

Links form the logical link between the output of a signal, gate or condition and the input to any element.
Any link that is connected to the input of a gate can be inverted. Right-click the input and select **Properties…**. The **Link Properties** window appears.

Figure 2 - Link properties

4.2.1 Rules for Linking Symbols

An inverted link is shown with a small circle on the input to a gate. A link must be connected to the input of a gate to be inverted.
Links can only be started from the output of a signal, gate, or conditioner, and can only be ended at an input to any element.

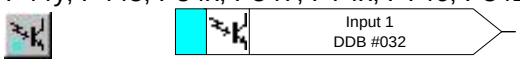
Signals can only be an input or an output. To follow the convention for gates and conditioners, input signals are connected from the left and output signals to the right. The Editor automatically enforces this convention.
A link is refused for the following reasons:

- An attempt to connect to a signal that is already driven. The reason for the refusal may not be obvious because the signal symbol may appear elsewhere in the diagram.

  Right-click the link and select Highlight to find the other signal. Click anywhere on the diagram to disable the highlight.
- An attempt is made to repeat a link between two symbols. The reason for the refusal may not be obvious because the existing link may be represented elsewhere in the diagram.

4.3 Opto Signal Properties

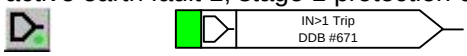
Each opto input can be selected and used for programming in PSL. Activation of the opto input drives an associated DDB signal.
For example, activating opto Input L1 asserts DDB 032 in the PSL for the P14x, P34x, P44y, P445, P54x, P547, P74x, P746, P841, P849 products.



DDB Nos	*"Input 1 DDB #064" applies to: P24x, P64x.* *"Opto Label DDB #064" applies to: P44x.*

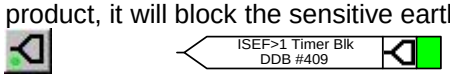
4.4 Input Signal Properties

Relay logic functions provide logic output signals that can be used for programming in PSL. Depending on the relay functionality, operation of an active relay function drives an associated DDB signal in PSL.
For example, DDB 671 is asserted in the PSL for the P44y, P547 & P841 product if the active earth fault 1, stage 1 protection operate/trip.



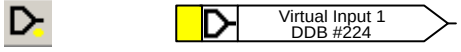
4.5 Output Signal Properties

Relay logic functions provide logic input signals that can be used for programming in PSL. Depending on the relay functionality, activation of the output signal will drive an associated DDB signal in PSL and cause an associated response to the relay function.
For example, if DDB 409 is asserted in the PSL for the P44y, P54x, P547 and P841 product, it will block the sensitive earth function stage 1 timer.



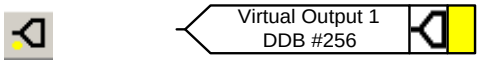
4.6 GOOSE Input Signal Properties

The PSL interfaces with the GOOSE Scheme Logic using virtual inputs. The Virtual Inputs can be used in much the same way as the Opto Input signals.
The logic that drives each of the Virtual Inputs is contained within the relay's GOOSE Scheme Logic file. It is possible to map any number of bit-pairs, from any enrolled device, using logic gates onto a Virtual Input (see Easergy Studio (MiCOM S1 Studio) User Manual for more details). The number of available GOOSE virtual inputs is shown in the *Programmable Logic* chapter.
For example DDB 224 will be asserted in PSL for the P44y, P54x, P547 & P841 product should virtual input 1 operate.



4.7 GOOSE Output Signal Properties

The PSL interfaces with the GOOSE Scheme Logic using 32 virtual outputs. Virtual outputs can be mapped to bit-pairs for transmitting to any enrolled devices.
For example if DDB 256 is asserted in PSL for the P44y, P54x, P547 and P841 product, Virtual Output 32 and its associated mappings will operate.

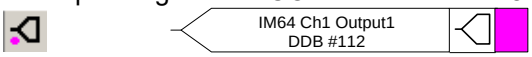


4.8 Control In Signal Properties

There are 32 control inputs which can be activated via the relay menu, 'hotkeys' or via rear communications. Depending on the programmed setting i.e. latched or pulsed, an associated DDB signal will be activated in PSL when a control input is operated
For example, when operated control input 1 will assert DDB 192 in the PSL for the P44y, P54x, P547 and P841 products.

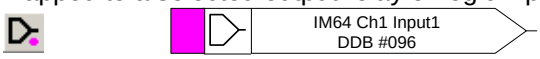
4.9 InterMiCOM Output Commands Properties

There are 16 InterMiCOM outputs that could be selected and use for teleprotection, remote commands, etc. "InterMiCOM Out" is a send command to a remote end that could be mapped to any logic output or opto input. This will be transmitted to the remote end as corresponding "InterMiCOM In" command for the P14x, P44y, P445 & P54x products.



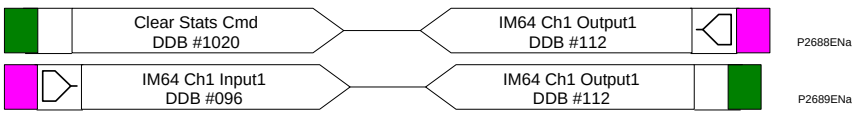
4.10 InterMiCOM Input Commands Properties

There are 16 InterMiCOM inputs that could be selected and use for teleprotection, remote commands, etc. "InterMiCOM In" is a received signal from remote end that could be mapped to a selected output relay or logic input.



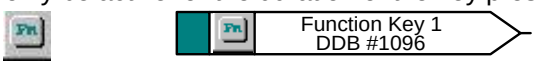
Example:

Relay End A	At end A, InterMiCOM Output 1 is mapped to the command indication "Clear Statistics" (issued at end A).
Relay End B	At end B, InterMiCOM Input 1 is mapped to the command "Clear Statistics". Upon receive of IM64 1 from relay at end A, the relay at end B will reset its statistics.



4.11 Function Key Properties

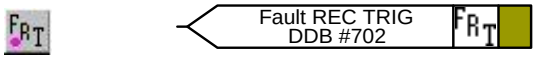
Each function key can be selected and used for programming in PSL. Activation of the function key will drive an associated DDB signal and the DDB signal will remain active depending on the programmed setting i.e. toggled or normal. Toggled mode means the DDB signal will remain latched or unlatched on key press and normal means the DDB will only be active for the duration of the key press.



For example, operate function key 1 to assert DDB 1096 in the PSL for the P44y, P54x, P547 or P841 products.

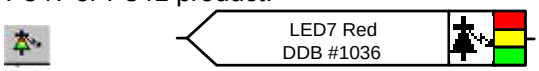
4.12 Fault Recorder Trigger Properties

The fault recording facility can be activated by driving the fault recorder trigger DDB signal.
For example assert DDB 702 to activate the fault recording in the PSL for the P44y, P54x, P547 or P841 product.



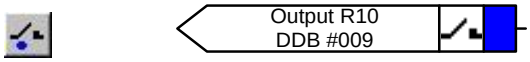
4.13 LED Signal Properties

All programmable LEDs will drive associated DDB signal when the LED is activated.
For example DDB 1036 will be asserted when LED 7 is activated for the P44y, P54x, P547 or P841 product.



4.14 Contact Signal Properties

All relay output contacts will drive associated DDB signal when the output contact is activated.
For example, DDB 009 will be asserted when output R10 is activated for all products.



4.15 LED Conditioner Properties

1. Select the **LED name** from the list (only shown when inserting a new symbol).
2. Configure the LED output to be Red, Yellow or Green.

   Configure a Green LED by driving the Green DDB input.
   Configure a RED LED by driving the RED DDB input.
   Configure a Yellow LED by driving the RED and GREEN DDB inputs simultaneously.

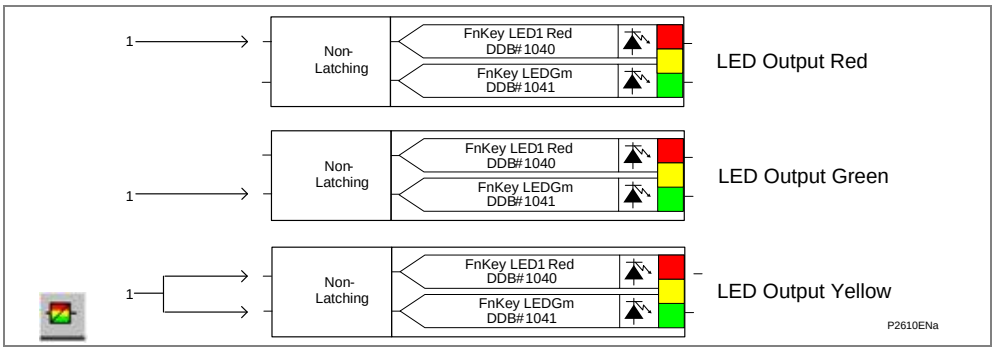


Figure 3 - Red, green and yellow LED outputs

3. Configure the LED output to be latching or non-latching.

DDB #642 and DDB #643 applies to these products: P14x, P44x, P74x, P746 and P849.
DDB #1040 and DDB #1041 applies to these products: P24x, P34x, P44y, P54x, P547, P64x and P841.

4.16 Contact Conditioner Properties

Each contact can be conditioned with an associated timer that can be selected for pick up, drop off, dwell, pulse, pick-up/drop-off, straight-through, or latching operation. **Straight-through** means it is not conditioned in any way whereas **Latching** is used to create a sealed-in or lockout type function.

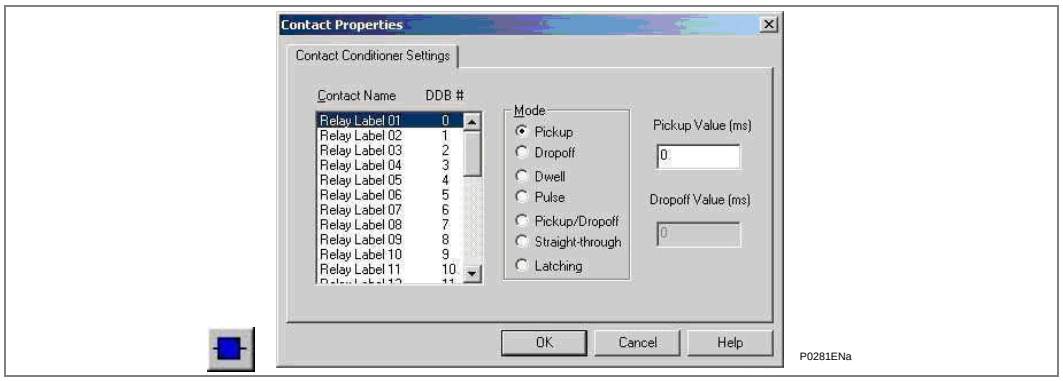


Figure 4 - Contact conditioner settings

1. Select the contact **name** from the **Contact Name** list (only shown when inserting a new symbol).
2. Choose the conditioner type required in the **Mode** tick list.
3. Set the **Pick-up** Time (in milliseconds), if required.
4. Set the **Drop-off** Time (in milliseconds), if required.

4.17 Timer Properties

Each timer can be selected for pick up, drop off, dwell, pulse or pick-up/drop-off operation.

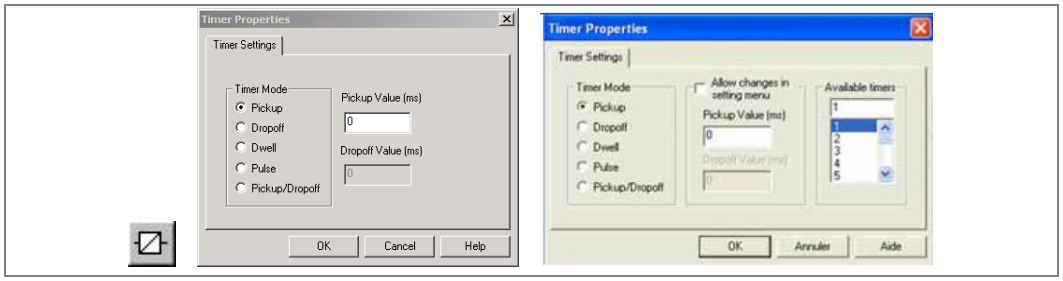


Figure 5 - Timer settings

1. Choose the operation mode from the **Timer Mode** tick list.
2. Set the Pick-up Time (in milliseconds), if required.
3. Set the Drop-off Time (in milliseconds), if required.

4.18 Gate Properties

A Gate may be an AND, OR, or programmable gate.

	An **AND** gate requires that all inputs are TRUE for the output to be TRUE.
	An **OR** gate requires that one or more input is TRUE for the output to be TRUE.
	A **Programmable** gate requires that the number of inputs that are TRUE is equal to or greater than its 'Inputs to Trigger' setting for the output to be TRUE.

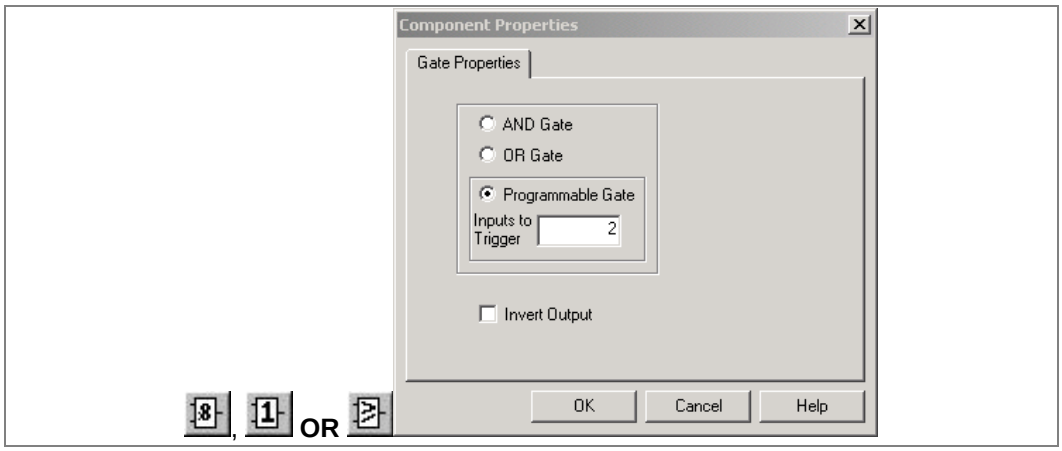


Figure 6 - Gate properties

1. Select the Gate type AND, OR, or Programmable.
2. Set the number of inputs to trigger when Programmable is selected.
3. Select if the output of the gate should be inverted using the Invert Output check box. An inverted output is indicated with a "bubble" on the gate output.

4.19 SR Programmable Gate Properties

For many products a number of programmable SR Latches are added. They are configured by an appropriate version of PSL Editor (S1v2.14 version 5.0.0 or greater) where an SRQ icon features on the toolbar.
Each SR latch has a Q output. The Q output may be inverted in the PSL Editor under the SR Latch component properties window. The SR Latches may be configured as Standard (no input dominant), Set Dominant or Reset Dominant in the PSL Editor under the SR Latch component properties window. The truth table for the SR Latches is given below.
A **Programmable** SR gate can be selected to operate with these latch properties:

S input	R input	O - Standard	O – Set input dominant	O – Reset input dominant
0	0	0	0	0
0	1	0	0	0
1	0	1	1	1
1	1	0	1	0

Table 1 - SR programmable gate properties

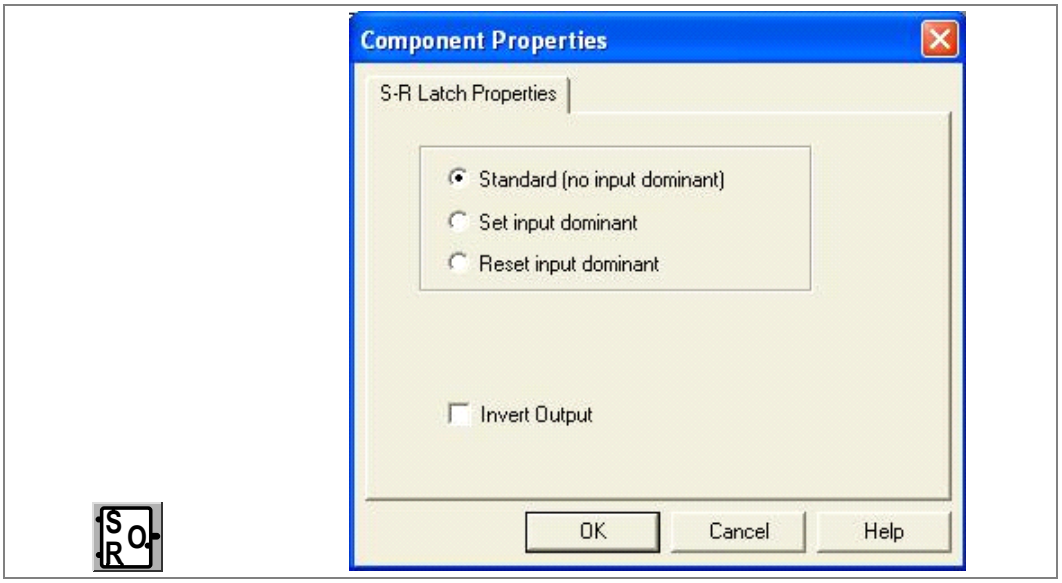


Figure 7 - SR latch component properties

Select if the output of the gate should be inverted using the Invert Output check box. An inverted output is indicated with a "bubble" on the gate output.

4.20 PSL Signal Grouping Modes

PSL Signal Grouping Nodes

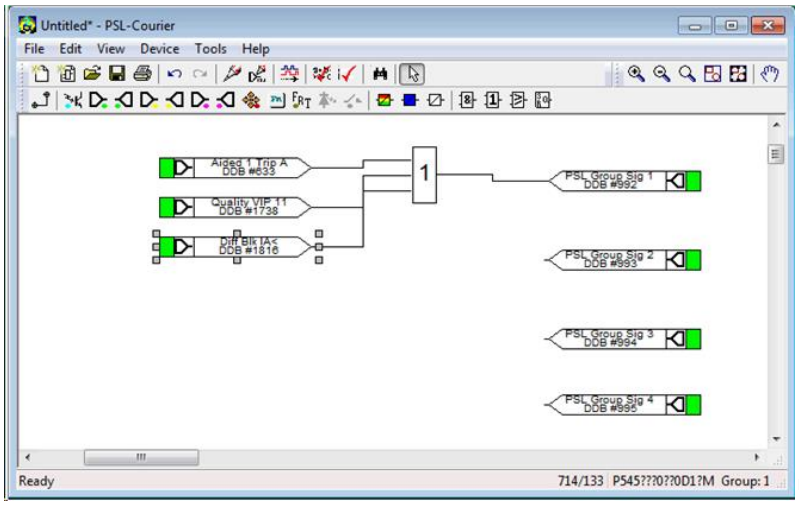
For Software Version D1a and later, these DDB “Group” Nodes can be mapped to individual or multiple DDBs in the PSL:
PSL Group Sig 1
PSL Group Sig 2
PSL Group Sig 3
PSL Group Sig 4
There are now four additional ***DDB Group Sig x*** Nodes that can be mapped to individual or multiple DDBs in the PSL. These can then be set to trigger the DR via the DISTURBANCE RECORD menu.

These "Nodes" are general and can also be used to group signals together in the PSL for any other reason. These four nodes are available in each of the four PSL setting groups.

Number	PSL Group Sig
992	PSL Group Sig 1
993	PSL Group Sig 2
994	PSL Group Sig 3
995	PSL Group Sig 4

1. For a control input, the DR can be triggered directly by triggering directly from the Individual Control Input (e.g. Low to High (L to H) change)
2. For an input that cannot be triggered directly, or where any one of a number of DDBs are required to trigger a DR, map the DDBs to the new PSL Group sig n and then trigger the DR on this.

e.g. in the PSL:

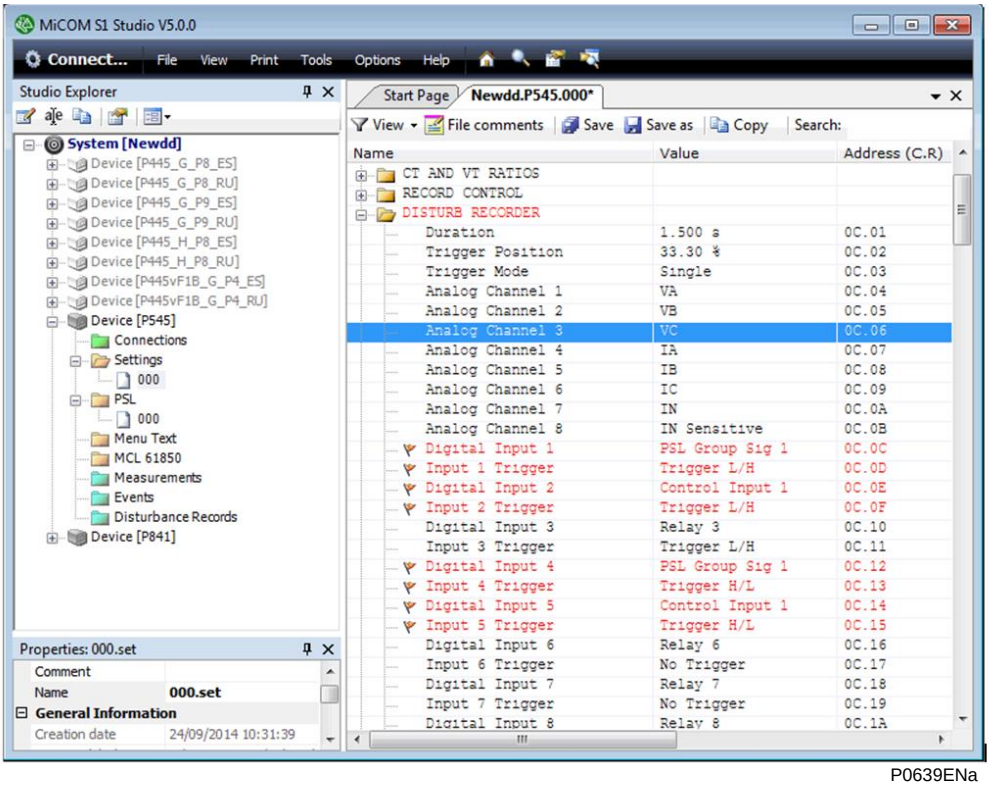


P0638ENa

Figure 8 - PSL diagram

In the DR Settings:

- Digital Input 1 is triggered by the PSL Group Sig 1 (L to H)
- Digital Input 2 is triggered by Control Input 1 (L to H)



P0639ENa

Figure 9 – Easergy Studio (MiCOM S1 Studio) Disturb Recorder table diagram

If triggering on both edges is required map another DR channel to the H/L as well

Digital Input 4 is triggered by the PSL Group Sig 1 (H to L)

Digital Input 5 is triggered by Control Input 1 (H to L)

5 SPECIFIC TASKS

Note	*MiCOM S1 Studio has been renamed as Easergy Studio.*

5.1 DR Digital Input Label Operation (P44y, P54x, P445 & P841 only)

The digital input labels can be modified via the MiCOM Px40 user interface or Easergy Studio (MiCOM S1 Studio). The following example is using S1 Studio Version 5.0.0. The digital input labels are available in the “DR CHAN LABELS” folder in the settings file as shown below:

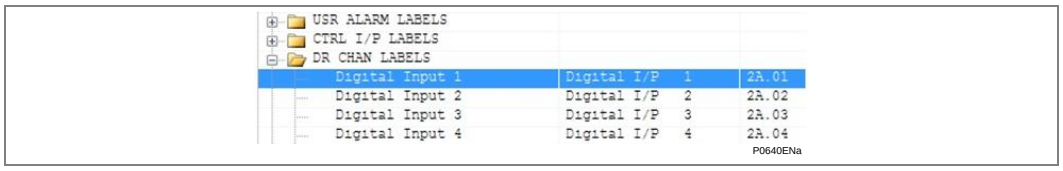


Figure 10 - DR Chan Labels tree

Easergy Studio (MiCOM S1 Studio) removes leading spaces from the value field so making the ‘D’ look as if it’s the 1st character in the label. The default values above in fact have a leading space which is used to switch off the use of the label as show below in the change settings view.

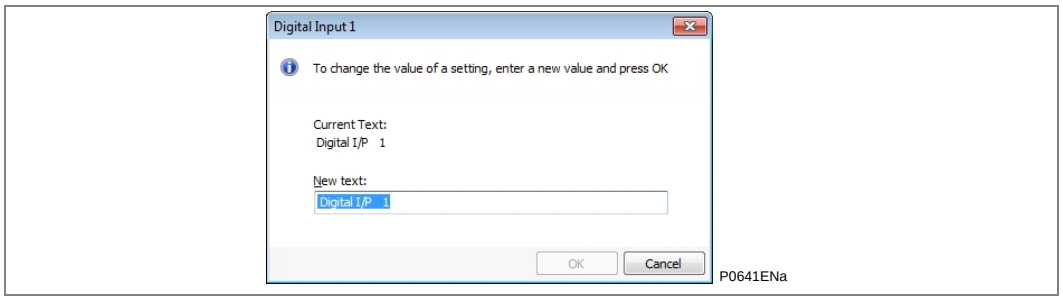


Figure 11 - Digital Input 1 dialog box

Pressing OK will save the setting and return to the settings page as follows:

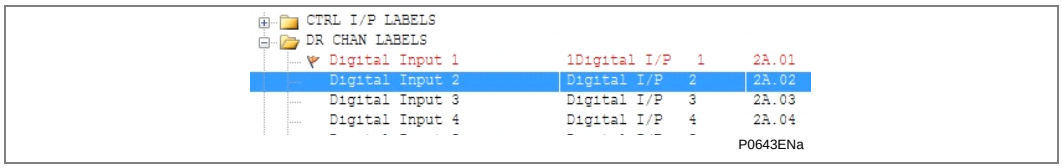


Figure 12 - DR Chan Labels tree

Digital Input 1 label will now be used in the Disturbance Record when the settings file is downloaded to the relay.

5.2 Virtual Input Label Operation

The Virtual Input labels can be modified via the MiCOM Px40 user interface or Easergy Studio.

The default labels are available in the “VIR I/P LABELS” (or “VIRT I/P LABELS”) folder in the settings file as shown below:

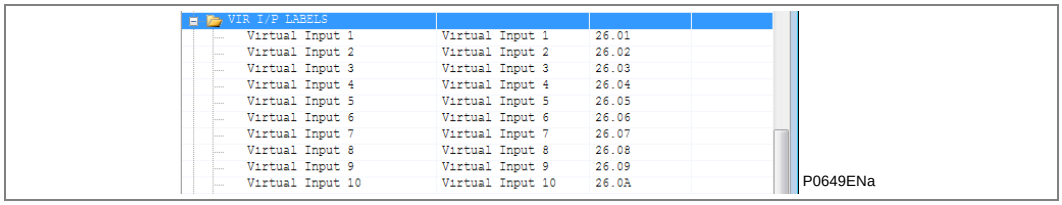


Figure 13 - Easergy Studio VIR I/P Labels Tree

The default “Virtual Input” labels can be changed to customer requirements. For example, to change default text from “Virtual Input 1” to “Customer Func 1” open the ***Virtual Input 1*** box, and change “Virtual Input 1” in the ***New Text:*** box to “Customer Func 1”:

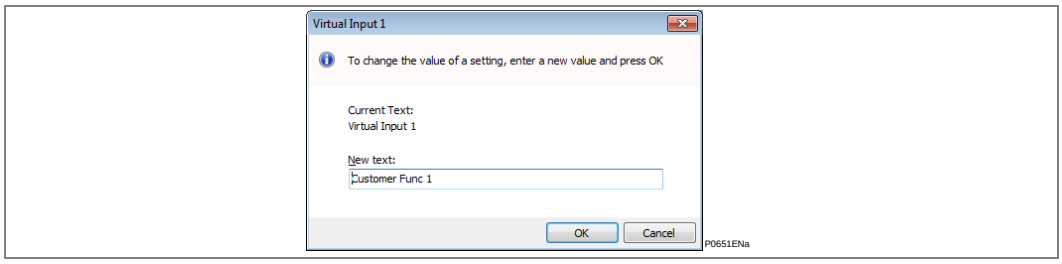


Figure 14 - Virtual Input 1 dialog box

Pressing OK will save the setting and return to the settings page as follows:

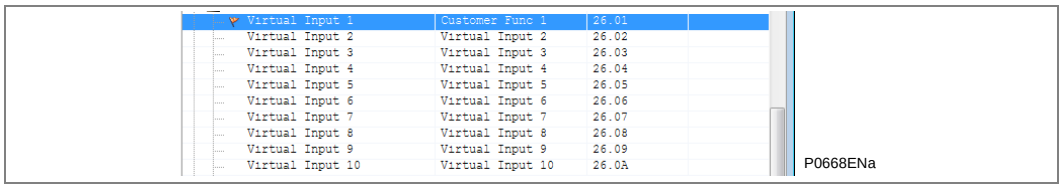


Figure 15 - Easergy Studio VIR I/P Labels Tree

The above “Customer Func 1” label text will now be used in place of “Virtual Input 1” in the Disturbance / Event Records after the settings file is downloaded to the relay.

5.3 Virtual Output Label Operation

The Virtual Output labels can be modified via the relay user interface or Easergy Studio.

The virtual Output labels are available in the “VIR O/P LABELS” ” (or “VIRT O/P LABELS”) folder in the settings file as shown below:

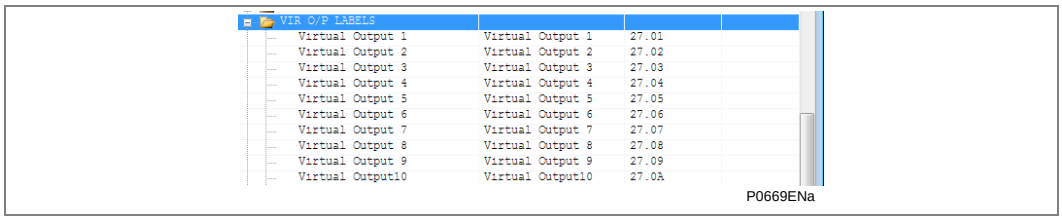


Figure 16 - Easergy Studio VIR O/P Labels Tree

The default “Virtual Output Labels” can be changed to suit the customer requirements. The process is identical to the previously described procedure for the Virtual Input Labels.

5.4 SR/MR User Alarm Label Operation

The SR/MR User Alarm input labels can be modified via the MiCOM Px40 user interface or Easergy Studio.

The default labels are available in the “USR ALARM LABELS” folder in the settings file as shown below:

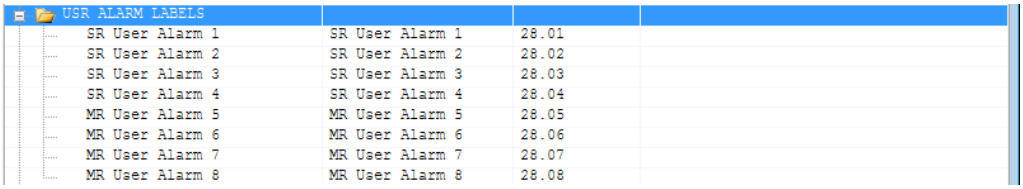


Figure 17 - Easergy Studio USR Labels Tree

The default “SR User Alarm” and “MR User Alarm” labels can be changed to suit the customer requirements. For example, to change default text from “SR User Alarm 1” to “Customer Alarm 1” open the ***SR User Alarm 1*** dialog box and change “SR User Alarm 1” in the ***New Text:*** Text box to be “Customer Alarm 1”.

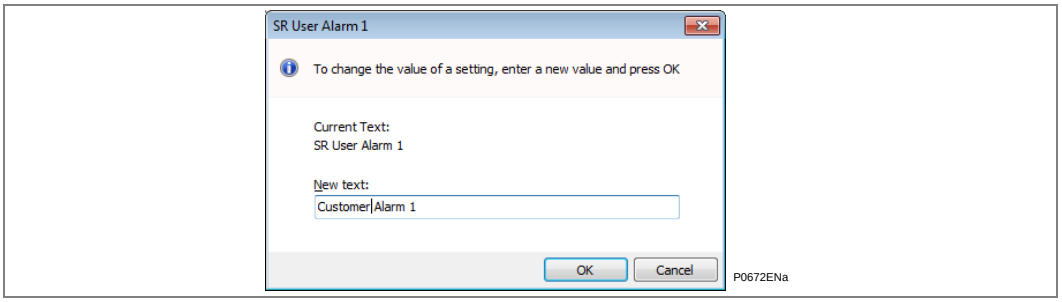


Figure 18 – User Alarm dialog box

Pressing OK will save the setting and return to the settings page as follows:

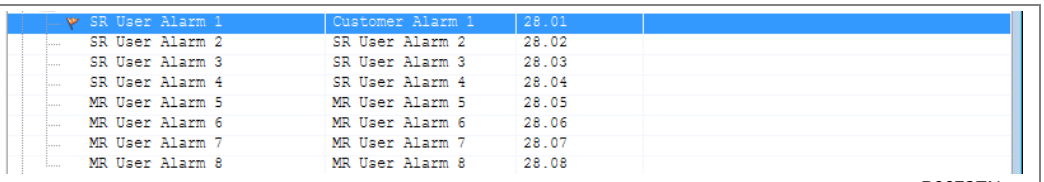


Figure 19 - Virtual Input 1 settings

The above “Customer Alarm 1” label text will now be used in place of “SR User Alarm 1” in the Disturbance / Event Records after the settings file is downloaded to the relay.

5.5 Settable Control Input Operation (P14x, P44y, P54x, P445 & P841 only)

The settings should be applied to all relays in the current differential protection scheme. As from Software Versions C1/D1/F1/G4/H4/J4, there are now 32 Standard Control Inputs and 16 additional Settable Control Inputs available. These are settable via the "CONTROL INPUTS" folder and are located after the standard "Control Input" labels in the relevant settings file.

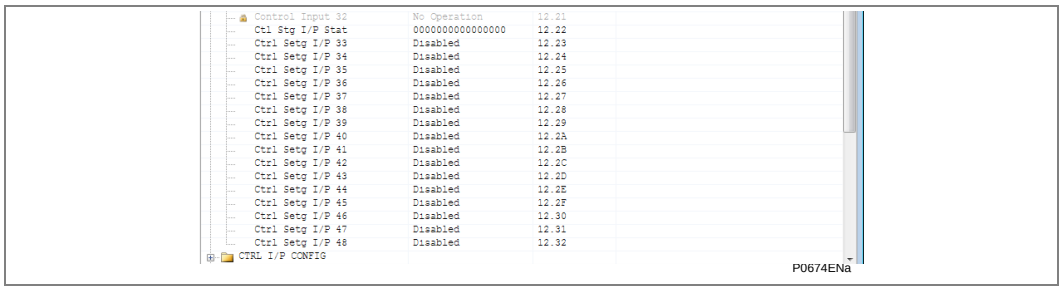


Figure 20 - Easergy Studio Control Inputs tree

Each Settable control Input "Ctrl Setg I/P xx" can be controlled using Enable / Disable settings. To change from (the default) Disabled to Enabled, open the ***Ctrl Setg I/P xx*** dialog box, then change Disabled to Enabled in the ***New Setting*** drop-down list box:

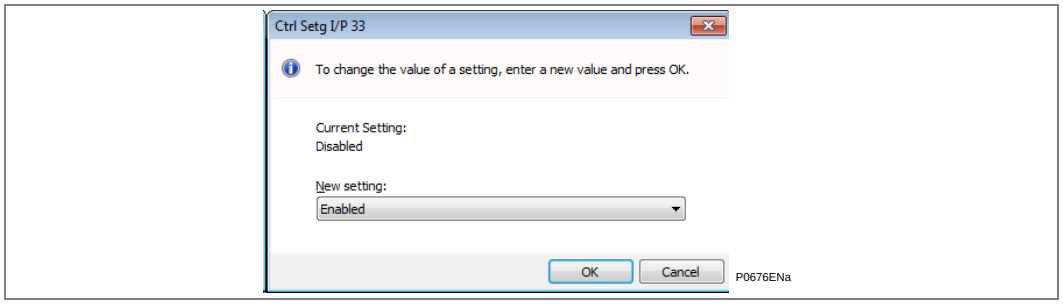


Figure 21 – Ctrl Setg I/P 33 dialog box

Pressing OK will save the setting and return to the settings page as follows:

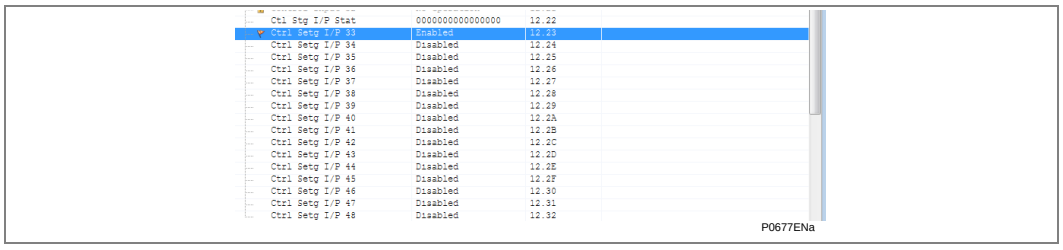


Figure 22 - Easergy Studio Control Inputs (Ctl Setg I/P 33) tree

The setting "Ctl Stg I/P Stat" can be used to control multiple "Ctrl Setg I/P" at the same time, e.g. clear Ctrl Setg I/P 33 and set Ctrl Setg I/P 34 to 38, but please note that the status will not be reflected in the individual inputs settings or vice versa.
This cell may be hidden in the Easergy Studio files.

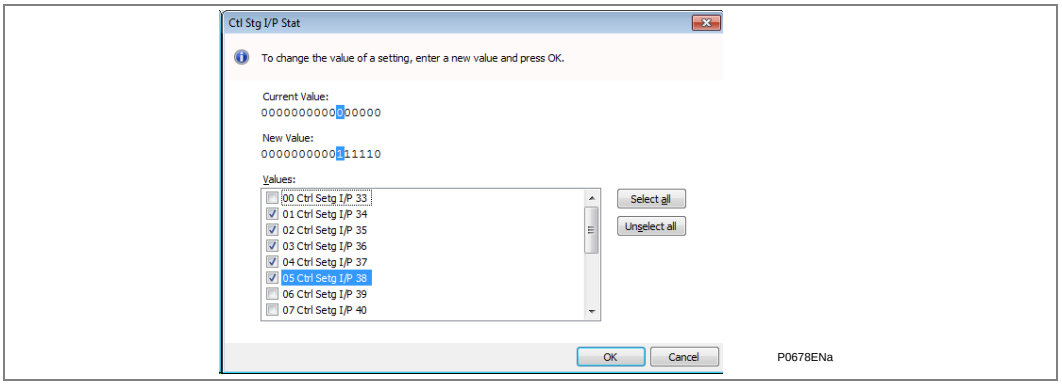


Figure 23 – Ctrl Stg I/P Stat dialog box

5.6 Settable Control Setg I/P Label Operation (P14x, P44y, P54x, P445 & P841 only)

The default labels are available in the “CTRL I/P LABELS” folder and are located after the standard “Control Input” labels in the settings file as shown below:

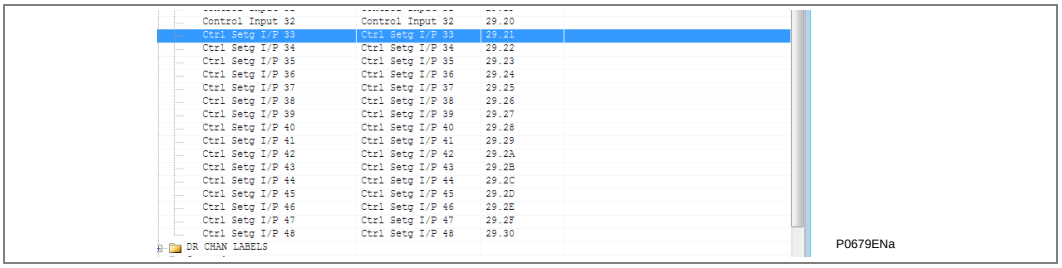


Figure 24 - Easergy Studio Control I/P Labels (Ctl Setg I/P 33) tree

The default “Ctrl Setg I/P” labels can be changed to suit the customer requirements using the same procedure as for the standard “Control Inputs”. For example to change the default text from “Ctrl Setg I/P 33” to “Custom Ctrl Sg 1” open the ***Ctrl Setg I/P 33*** dialog box, then change “Ctrl Setg I/P 33” in the ***New Text:*** box to be “Custom Ctrl Sg 1”.

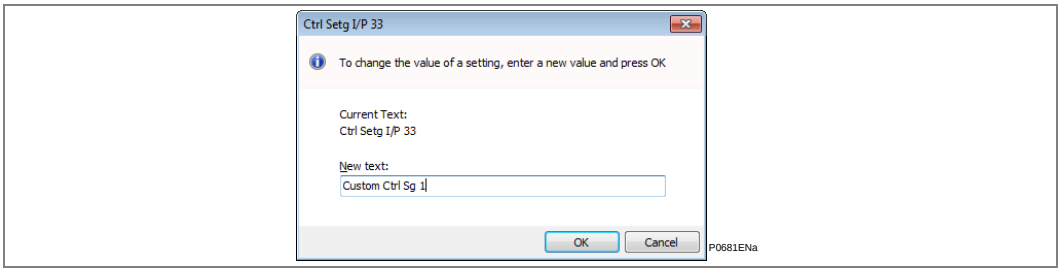


Figure 25 – Ctrl Setg I/P 33 dialog box

Pressing OK will save the setting and return to the settings page as follows:

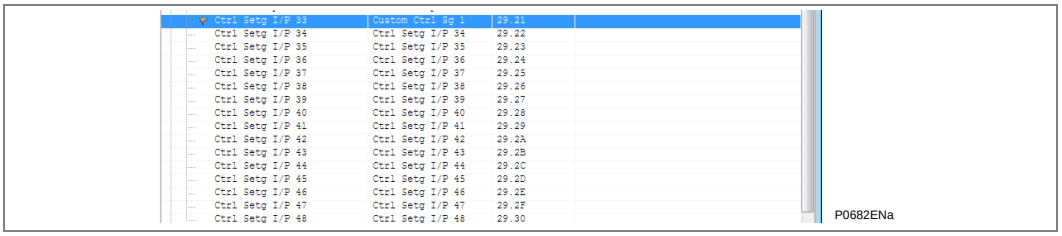


Figure 26 - Easergy Studio Control I/P Labels (Ctl Setg I/P 33) tree

The above “Custom Ctrl Sg 1” label text will now be used in place of “Ctrl Setg I/P 33” in the Disturbance / Event Records after the settings file is downloaded to the relay.

6 MAKING A RECORD OF MICOM PX40 DEVICE SETTINGS

6.1 Using Easergy Studio to Manage Device Settings

An engineer often needs to create a record of what settings have been applied to a device. In the past, they could have used paper printouts of all the available settings, and mark up the ones they had used. Keeping such a paper-based Settings Records could be time-consuming and prone to error (e.g. due to being settings written down incorrectly). The Easergy Studio software lets you read from or write to MiCOM devices.

- **Extract** lets you download all the settings from a MiCOM Px40 device. A summary is given in the ***Extract Settings from a MiCOM Px40 Device*** section.
- **Send** lets you send the settings you currently have open in Easergy Studio. A summary is given in the ***Send Settings to a MiCOM Px40 Device*** section.

In most cases, it will be quicker and less error prone to extract settings electronically and store them in a settings file on a memory stick. In this way, there will be a digital record which is certain to be accurate. It is also possible to archive these settings files in a repository; so they can be used again or adapted for another use.

Full details of how to do this is provided in the Easergy Studio help.

A quick summary of the main steps is here. In each case, you need to make sure that:

- Your computer includes the Easergy Studio software.
- Your computer and the MiCOM device are powered on.
- You have used a suitable cable to connect your computer to the MiCOM device (Front Port, Rear Port, Ethernet port or Modem as available).

6.2 Extract Settings from a MiCOM Px40 Device

Full details of how to do this is provided in the Easergy Studio help.

As a quick guide, you need to do the following:

1. In Easergy Studio, click the Quick Connect… button.
2. Select the relevant Device Type in the Quick Connect dialog box.
3. Click the relevant port in the Port Selection dialog box.
4. Enter the relevant connection parameters in the Connection Parameters dialog box and click the Finish button
5. Studio will try to communicate with the Px40 device. It will display a connected message if the connection attempt is successful.
6. The device will appear in the Studio Explorer pane on the top-left hand side of the interface.
7. Click the + button to expand the options for the device, then click on the Settings folder.
8. Right-click on Settings and select the Extract Settings link to read the settings on the device and store them on your computer or a memory stick attached to your computer.
9. After retrieving the settings file, close the dialog box by clicking the Close button.

6.3 Send Settings to a MiCOM Px40 Device

Full details of how to do this is provided in the Easergy Studio help.
As a quick guide, you need to do the following:

1. In Easergy Studio, click the Quick Connect… button.
2. Select the relevant Device Type in the Quick Connect dialog box.
3. Click the relevant port in the Port Selection dialog box.
4. Enter the relevant connection parameters in the Connection Parameters dialog box and click the Finish button
5. Studio will try to communicate with the Px40 device. It will display a connected message if the connection attempt is successful.
6. The device will appear in the Studio Explorer pane on the top-left hand side of the interface.
7. Click the + button to expand the options for the device, then click on the Settings link.
8. Right-click on the device name and select the Send link.

Note	*When you send settings to a MiCOM Px40 device, the data is stored in a temporary location at first. This temporary data is tested to make sure it is complete. If the temporary data is complete, it will be programmed into the MiCOM Px40 device. This avoids the risk of a device being programmed with incomplete or corrupt settings.*

9. In the Send To dialog box, select the settings file(s) you wish to send, then click the Send button.
10. Close the Send To dialog box by clicking the Close button.

PROGRAMMABLE LOGIC

CHAPTER 8

Date:	07/2018
Products covered by this chapter:	This chapter covers the specific versions of the MiCOM products listed below. This includes ***only*** the following combinations of Software Version and Hardware Suffix.
Hardware Suffix:	L (P642) M (P643/P645)
Software Version:	B4 - P64x (P642, P643 & P645)
Connection Diagrams:	10P642xx (xx = 01 to 10) 10P643xx (xx = 01 to 06) 10P645xx (xx = 01 to 09)

CONTENTS

FIGURES

TABLES

Notes:

1 OVERVIEW

The purpose of the Programmable Scheme Logic (PSL) is to allow the user to configure an individual protection scheme to suit their own particular application. This is achieved through the use of programmable logic gates and delay timers.

The input to the PSL is any combination of the status of opto inputs. It is also used to assign the mapping of functions to the opto inputs and output contacts, the outputs of the protection elements, e.g. protection starts and trips, and the outputs of the fixed protection scheme logic. The fixed scheme logic provides the relay's standard protection schemes.

The PSL itself consists of software logic gates and timers. The logic gates can be programmed to perform a range of different logic functions and can accept any number of inputs. The timers are used either to create a programmable delay, and/or to condition the logic outputs, e.g. to create a pulse of fixed duration on the output regardless of the length of the pulse on the input. The outputs of the PSL are the LEDs on the front panel of the relay and the output contacts at the rear.

The execution of the PSL logic is event driven; the logic is processed whenever any of its inputs change, for example as a result of a change in one of the digital input signals. Also, only the part of the PSL logic that is affected by the particular input change that has occurred is processed. This reduces the amount of processing time that is used by the PSL. This means that even with large, complex PSL schemes the device trip time will not lengthen.

This system provides flexibility for the user to create their own scheme logic design. It also means that the PSL can be configured into a very complex system, hence setting of the PSL is implemented through the PC support package MiCOM S1 Studio.

How to edit the PSL schemes is described in the "Using the PSL Editor" chapter.

This chapter contains details of the logic nodes which are specific to this product, together with any PSL diagrams which we have published for this product.

2 DESCRIPTION OF LOGIC NODES

The following table shows the available DDB Numbers, a Description of what they are and which product (or products) they apply to. If a DDB Number is not shown, it is not used in this range of products.

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
0	SW	DDB_OUTPUT_RELAY_1	Output Relay 1	see 4B01	Yes	Yes	Yes
1	SW	DDB_OUTPUT_RELAY_2	Output Relay 2	see 4B02	Yes	Yes	Yes
2	SW	DDB_OUTPUT_RELAY_3	Output Relay 3	see 4B03	Yes	Yes	Yes
3	SW	DDB_OUTPUT_RELAY_4	Output Relay 4	see 4B04	Yes	Yes	Yes
4	SW	DDB_OUTPUT_RELAY_5	Output Relay 5	see 4B05	Yes	Yes	Yes
5	SW	DDB_OUTPUT_RELAY_6	Output Relay 6	see 4B06	Yes	Yes	Yes
6	SW	DDB_OUTPUT_RELAY_7	Output Relay 7	see 4B07	Yes	Yes	Yes
7	SW	DDB_OUTPUT_RELAY_8	Output Relay 8	see 4B08	Yes	Yes	Yes
8	SW	DDB_OUTPUT_RELAY_9	Output Relay 9	see 4B09	Yes	Yes	Yes
9	SW	DDB_OUTPUT_RELAY_10	Output Relay 10	see 4B0A	Yes	Yes	Yes
10	SW	DDB_OUTPUT_RELAY_11	Output Relay 11	see 4B0B	Yes	Yes	Yes
11	SW	DDB_OUTPUT_RELAY_12	Output Relay 12	see 4B0C	Yes	Yes	Yes
12	SW	DDB_OUTPUT_RELAY_13	Output Relay 13	see 4B0D		Yes	Yes
13	SW	DDB_OUTPUT_RELAY_14	Output Relay 14	see 4B0E		Yes	Yes
14	SW	DDB_OUTPUT_RELAY_15	Output Relay 15	see 4B0F		Yes	Yes
15	SW	DDB_OUTPUT_RELAY_16	Output Relay 16	see 4B10		Yes	Yes
16	SW	DDB_OUTPUT_RELAY_17	Output Relay 17	see 4B11		Yes	Yes
17	SW	DDB_OUTPUT_RELAY_18	Output Relay 18	see 4B12		Yes	Yes
18	SW	DDB_OUTPUT_RELAY_19	Output Relay 19	see 4B13		Yes	Yes
19	SW	DDB_OUTPUT_RELAY_20	Output Relay 20	see 4B14		Yes	Yes
20	SW	DDB_OUTPUT_RELAY_21	Output Relay 21	see 4B15		Yes	Yes
21	SW	DDB_OUTPUT_RELAY_22	Output Relay 22	see 4B16		Yes	Yes
22	SW	DDB_OUTPUT_RELAY_23	Output Relay 23	see 4B17		Yes	Yes
23	SW	DDB_OUTPUT_RELAY_24	Output Relay 24	see 4B18		Yes	Yes
24	SW	DDB_OUTPUT_RELAY_25	Output Relay 25	see 4B19			
25	SW	DDB_OUTPUT_RELAY_26	Output Relay 26	see 4B1A			
26	SW	DDB_OUTPUT_RELAY_27	Output Relay 27	see 4B1B			
27	SW	DDB_OUTPUT_RELAY_28	Output Relay 28	see 4B1C			
28	SW	DDB_OUTPUT_RELAY_29	Output Relay 29	see 4B1D			
29	SW	DDB_OUTPUT_RELAY_30	Output Relay 30	see 4B1E			
30	SW	DDB_OUTPUT_RELAY_31	Output Relay 31	see 4B1F			
31	SW	DDB_OUTPUT_RELAY_32	Output Relay 32	see 4B20			
32	SW	DDB_UNUSED	DDB_UNUSED				
33	SW	DDB_UNUSED	DDB_UNUSED				
34	SW	DDB_UNUSED	DDB_UNUSED				
35	SW	DDB_UNUSED	DDB_UNUSED				
36	SW	DDB_UNUSED	DDB_UNUSED				
37	SW	DDB_UNUSED	DDB_UNUSED				
38	SW	DDB_UNUSED	DDB_UNUSED				
39	SW	DDB_UNUSED	DDB_UNUSED				

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
40	SW	DDB_UNUSED	DDB_UNUSED				
41	SW	DDB_UNUSED	DDB_UNUSED				
42	SW	DDB_UNUSED	DDB_UNUSED				
43	SW	DDB_UNUSED	DDB_UNUSED				
44	SW	DDB_UNUSED	DDB_UNUSED				
45	SW	DDB_UNUSED	DDB_UNUSED				
46	SW	DDB_UNUSED	DDB_UNUSED				
47	SW	DDB_UNUSED	DDB_UNUSED				
48	SW	DDB_UNUSED	DDB_UNUSED				
49	SW	DDB_UNUSED	DDB_UNUSED				
50	SW	DDB_UNUSED	DDB_UNUSED				
51	SW	DDB_UNUSED	DDB_UNUSED				
52	SW	DDB_UNUSED	DDB_UNUSED				
53	SW	DDB_UNUSED	DDB_UNUSED				
54	SW	DDB_UNUSED	DDB_UNUSED				
55	SW	DDB_UNUSED	DDB_UNUSED				
56	SW	DDB_UNUSED	DDB_UNUSED				
57	SW	DDB_UNUSED	DDB_UNUSED				
58	SW	DDB_UNUSED	DDB_UNUSED				
59	SW	DDB_UNUSED	DDB_UNUSED				
60	SW	DDB_UNUSED	DDB_UNUSED				
61	SW	DDB_UNUSED	DDB_UNUSED				
62	SW	DDB_UNUSED	DDB_UNUSED				
63	SW	DDB_UNUSED	DDB_UNUSED				
64	SW	DDB_OPTO_ISOLATOR_1	Opto Isolator Input 1	see 4A01	Yes	Yes	Yes
65	SW	DDB_OPTO_ISOLATOR_2	Opto Isolator Input 2	see 4A02	Yes	Yes	Yes
66	SW	DDB_OPTO_ISOLATOR_3	Opto Isolator Input 3	see 4A03	Yes	Yes	Yes
67	SW	DDB_OPTO_ISOLATOR_4	Opto Isolator Input 4	see 4A04	Yes	Yes	Yes
68	SW	DDB_OPTO_ISOLATOR_5	Opto Isolator Input 5	see 4A05	Yes	Yes	Yes
69	SW	DDB_OPTO_ISOLATOR_6	Opto Isolator Input 6	see 4A06	Yes	Yes	Yes
70	SW	DDB_OPTO_ISOLATOR_7	Opto Isolator Input 7	see 4A07	Yes	Yes	Yes
71	SW	DDB_OPTO_ISOLATOR_8	Opto Isolator Input 8	see 4A08	Yes	Yes	Yes
72	SW	DDB_OPTO_ISOLATOR_9	Opto Isolator Input 9	see 4A09	Yes	Yes	Yes
73	SW	DDB_OPTO_ISOLATOR_10	Opto Isolator Input 10	see 4A0A	Yes	Yes	Yes
74	SW	DDB_OPTO_ISOLATOR_11	Opto Isolator Input 11	see 4A0B	Yes	Yes	Yes
75	SW	DDB_OPTO_ISOLATOR_12	Opto Isolator Input 12	see 4A0C	Yes	Yes	Yes
76	SW	DDB_OPTO_ISOLATOR_13	Opto Isolator Input 13	see 4A0D		Yes	Yes
77	SW	DDB_OPTO_ISOLATOR_14	Opto Isolator Input 14	see 4A0E		Yes	Yes
78	SW	DDB_OPTO_ISOLATOR_15	Opto Isolator Input 15	see 4A0F		Yes	Yes
79	SW	DDB_OPTO_ISOLATOR_16	Opto Isolator Input 16	see 4A10		Yes	Yes
80	SW	DDB_OPTO_ISOLATOR_17	Opto Isolator Input 17	see 4A11		Yes	Yes
81	SW	DDB_OPTO_ISOLATOR_18	Opto Isolator Input 18	see 4A12		Yes	Yes
82	SW	DDB_OPTO_ISOLATOR_19	Opto Isolator Input 19	see 4A13		Yes	Yes
83	SW	DDB_OPTO_ISOLATOR_20	Opto Isolator Input 20	see 4A14		Yes	Yes

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
84	SW	DDB_OPTO_ISOLATOR_21	Opto Isolator Input 21	see 4A15		Yes	Yes
85	SW	DDB_OPTO_ISOLATOR_22	Opto Isolator Input 22	see 4A16		Yes	Yes
86	SW	DDB_OPTO_ISOLATOR_23	Opto Isolator Input 23	see 4A17		Yes	Yes
87	SW	DDB_OPTO_ISOLATOR_24	Opto Isolator Input 24	see 4A18		Yes	Yes
88	SW	DDB_OPTO_ISOLATOR_25	Opto Isolator Input 25	see 4A19			
89	SW	DDB_OPTO_ISOLATOR_26	Opto Isolator Input 26	see 4A1A			
90	SW	DDB_OPTO_ISOLATOR_27	Opto Isolator Input 27	see 4A1B			
91	SW	DDB_OPTO_ISOLATOR_28	Opto Isolator Input 28	see 4A1C			
92	SW	DDB_OPTO_ISOLATOR_29	Opto Isolator Input 29	see 4A1D			
93	SW	DDB_OPTO_ISOLATOR_30	Opto Isolator Input 30	see 4A1E			
94	SW	DDB_OPTO_ISOLATOR_31	Opto Isolator Input 31	see 4A1F			
95	SW	DDB_OPTO_ISOLATOR_32	Opto Isolator Input 32	see 4A20			
96	SW	DDB_OPTO_ISOLATOR_33	Opto Isolator Input 33	see 4A21			
97	SW	DDB_OPTO_ISOLATOR_34	Opto Isolator Input 34	see 4A22			
98	SW	DDB_OPTO_ISOLATOR_35	Opto Isolator Input 35	see 4A23			
99	SW	DDB_OPTO_ISOLATOR_36	Opto Isolator Input 36	see 4A24			
100	SW	DDB_OPTO_ISOLATOR_37	Opto Isolator Input 37	see 4A25			
101	SW	DDB_OPTO_ISOLATOR_38	Opto Isolator Input 38	see 4A26			
102	SW	DDB_OPTO_ISOLATOR_39	Opto Isolator Input 39	see 4A27			
103	SW	DDB_OPTO_ISOLATOR_40	Opto Isolator Input 40	see 4A28			
104	SW	DDB_UNUSED	DDB_UNUSED				
105	SW	DDB_UNUSED	DDB_UNUSED				
106	SW	DDB_UNUSED	DDB_UNUSED				
107	SW	DDB_UNUSED	DDB_UNUSED				
108	SW	DDB_UNUSED	DDB_UNUSED				
109	SW	DDB_UNUSED	DDB_UNUSED				
110	SW	DDB_UNUSED	DDB_UNUSED				
111	SW	DDB_UNUSED	DDB_UNUSED				
112	SW	DDB_UNUSED	DDB_UNUSED				
113	SW	DDB_UNUSED	DDB_UNUSED				
114	SW	DDB_UNUSED	DDB_UNUSED				
115	SW	DDB_UNUSED	DDB_UNUSED				
116	SW	DDB_UNUSED	DDB_UNUSED				
117	SW	DDB_UNUSED	DDB_UNUSED				
118	SW	DDB_UNUSED	DDB_UNUSED				
119	SW	DDB_UNUSED	DDB_UNUSED				
120	SW	DDB_UNUSED	DDB_UNUSED				
121	SW	DDB_UNUSED	DDB_UNUSED				
122	SW	DDB_UNUSED	DDB_UNUSED				
123	SW	DDB_UNUSED	DDB_UNUSED				
124	SW	DDB_UNUSED	DDB_UNUSED				
125	SW	DDB_UNUSED	DDB_UNUSED				
126	SW	DDB_UNUSED	DDB_UNUSED				
127	SW	DDB_UNUSED	DDB_UNUSED				

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
128	PSL	DDB_OUTPUT_CON_1	Relay Conditioner 1	Relay Cond 1	Yes	Yes	Yes
129	PSL	DDB_OUTPUT_CON_2	Relay Conditioner 2	Relay Cond 2	Yes	Yes	Yes
130	PSL	DDB_OUTPUT_CON_3	Relay Conditioner 3	Relay Cond 3	Yes	Yes	Yes
131	PSL	DDB_OUTPUT_CON_4	Relay Conditioner 4	Relay Cond 4	Yes	Yes	Yes
132	PSL	DDB_OUTPUT_CON_5	Relay Conditioner 5	Relay Cond 5	Yes	Yes	Yes
133	PSL	DDB_OUTPUT_CON_6	Relay Conditioner 6	Relay Cond 6	Yes	Yes	Yes
134	PSL	DDB_OUTPUT_CON_7	Relay Conditioner 7	Relay Cond 7	Yes	Yes	Yes
135	PSL	DDB_OUTPUT_CON_8	Relay Conditioner 8	Relay Cond 8	Yes	Yes	Yes
136	PSL	DDB_OUTPUT_CON_9	Relay Conditioner 9	Relay Cond 9	Yes	Yes	Yes
137	PSL	DDB_OUTPUT_CON_10	Relay Conditioner 10	Relay Cond 10	Yes	Yes	Yes
138	PSL	DDB_OUTPUT_CON_11	Relay Conditioner 11	Relay Cond 11	Yes	Yes	Yes
139	PSL	DDB_OUTPUT_CON_12	Relay Conditioner 12	Relay Cond 12	Yes	Yes	Yes
140	PSL	DDB_OUTPUT_CON_13	Relay Conditioner 13	Relay Cond 13		Yes	Yes
141	PSL	DDB_OUTPUT_CON_14	Relay Conditioner 14	Relay Cond 14		Yes	Yes
142	PSL	DDB_OUTPUT_CON_15	Relay Conditioner 15	Relay Cond 15		Yes	Yes
143	PSL	DDB_OUTPUT_CON_16	Relay Conditioner 16	Relay Cond 16		Yes	Yes
144	PSL	DDB_OUTPUT_CON_17	Relay Conditioner 17	Relay Cond 17		Yes	Yes
145	PSL	DDB_OUTPUT_CON_18	Relay Conditioner 18	Relay Cond 18		Yes	Yes
146	PSL	DDB_OUTPUT_CON_19	Relay Conditioner 19	Relay Cond 19		Yes	Yes
147	PSL	DDB_OUTPUT_CON_20	Relay Conditioner 20	Relay Cond 20		Yes	Yes
148	PSL	DDB_OUTPUT_CON_21	Relay Conditioner 21	Relay Cond 21		Yes	Yes
149	PSL	DDB_OUTPUT_CON_22	Relay Conditioner 22	Relay Cond 22		Yes	Yes
150	PSL	DDB_OUTPUT_CON_23	Relay Conditioner 23	Relay Cond 23		Yes	Yes
151	PSL	DDB_OUTPUT_CON_24	Relay Conditioner 24	Relay Cond 24		Yes	Yes
152	PSL	DDB_OUTPUT_CON_25	Relay Conditioner 25	Relay Cond 25		Yes	Yes
153	PSL	DDB_OUTPUT_CON_26	Relay Conditioner 26	Relay Cond 26		Yes	Yes
154	PSL	DDB_OUTPUT_CON_27	Relay Conditioner 27	Relay Cond 27		Yes	Yes
155	PSL	DDB_OUTPUT_CON_28	Relay Conditioner 28	Relay Cond 28		Yes	Yes
156	PSL	DDB_OUTPUT_CON_29	Relay Conditioner 29	Relay Cond 29			Yes
157	PSL	DDB_OUTPUT_CON_30	Relay Conditioner 30	Relay Cond 30			Yes
158	PSL	DDB_OUTPUT_CON_31	Relay Conditioner 31	Relay Cond 31			Yes
159	PSL	DDB_OUTPUT_CON_32	Relay Conditioner 32	Relay Cond 32			Yes
160	SW	DDB_UNUSED					
161	SW	DDB_UNUSED					
162	SW	DDB_UNUSED			Yes		
163	SW	DDB_UNUSED			Yes	Yes	
164	SW	DDB_UNUSED			Yes	Yes	
165	SW	DDB_UNUSED			Yes	Yes	
166	SW	DDB_UNUSED			Yes	Yes	
167	SW	DDB_UNUSED			Yes	Yes	
168	SW	DDB_UNUSED	DDB_UNUSED				
169	SW	DDB_UNUSED	DDB_UNUSED				
170	SW	DDB_UNUSED	DDB_UNUSED				
171	SW	DDB_UNUSED	DDB_UNUSED				

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
172	SW	DDB_UNUSED	DDB_UNUSED				
173	SW	DDB_UNUSED	DDB_UNUSED				
174	SW	DDB_UNUSED	DDB_UNUSED				
175	SW	DDB_UNUSED	DDB_UNUSED				
176	SW	DDB_UNUSED	DDB_UNUSED				
177	SW	DDB_UNUSED	DDB_UNUSED				
178	SW	DDB_UNUSED	DDB_UNUSED				
179	SW	DDB_UNUSED	DDB_UNUSED				
180	SW	DDB_UNUSED	DDB_UNUSED				
181	SW	DDB_UNUSED	DDB_UNUSED				
182	SW	DDB_UNUSED	DDB_UNUSED				
183	SW	DDB_UNUSED	DDB_UNUSED				
184	SW	DDB_UNUSED	DDB_UNUSED				
185	SW	DDB_UNUSED	DDB_UNUSED				
186	SW	DDB_UNUSED	DDB_UNUSED				
187	SW	DDB_UNUSED	DDB_UNUSED				
188	SW	DDB_UNUSED	DDB_UNUSED				
189	SW	DDB_UNUSED	DDB_UNUSED				
190	SW	DDB_UNUSED	DDB_UNUSED				
191	SW	DDB_UNUSED	DDB_UNUSED				
192	SW	DDB_OUTPUT_TRI_LED_1_RED	Tri-LED - 1 - Red	LED1 Red		Yes	Yes
193	SW	DDB_OUTPUT_TRI_LED_1_GRN	Tri-LED - 1 - Green	LED1 Grn		Yes	Yes
194	SW	DDB_OUTPUT_TRI_LED_2_RED	Tri-LED - 2 - Red	LED2 Red		Yes	Yes
195	SW	DDB_OUTPUT_TRI_LED_2_GRN	Tri-LED - 2 - Green	LED2 Grn		Yes	Yes
196	SW	DDB_OUTPUT_TRI_LED_3_RED	Tri-LED - 3 - Red	LED3 Red		Yes	Yes
197	SW	DDB_OUTPUT_TRI_LED_3_GRN	Tri-LED - 3 - Green	LED3 Grn		Yes	Yes
198	SW	DDB_OUTPUT_TRI_LED_4_RED	Tri-LED - 4 - Red	LED4 Red		Yes	Yes
199	SW	DDB_OUTPUT_TRI_LED_4_GRN	Tri-LED - 4 - Green	LED4 Grn		Yes	Yes
200	SW	DDB_OUTPUT_TRI_LED_5_RED	Tri-LED - 5 - Red	LED5 Red		Yes	Yes
201	SW	DDB_OUTPUT_TRI_LED_5_GRN	Tri-LED - 5 - Green	LED5 Grn		Yes	Yes
202	SW	DDB_OUTPUT_TRI_LED_6_RED	Tri-LED - 6 - Red	LED6 Red		Yes	Yes
203	SW	DDB_OUTPUT_TRI_LED_6_GRN	Tri-LED - 6 - Green	LED6 Grn		Yes	Yes
204	SW	DDB_OUTPUT_TRI_LED_7_RED	Tri-LED - 7 - Red	LED7 Red		Yes	Yes
205	SW	DDB_OUTPUT_TRI_LED_7_GRN	Tri-LED - 7 - Green	LED7 Grn		Yes	Yes
206	SW	DDB_OUTPUT_TRI_LED_8_RED	Tri-LED - 8 - Red	LED8 Red		Yes	Yes
207	SW	DDB_OUTPUT_TRI_LED_8_GRN	Tri-LED - 8 - Green	LED8 Grn		Yes	Yes
208	SW	DDB_OUTPUT_TRI_LED_9_RED	Tri-LED - 9 - Red	FnKey LED1 Red		Yes	Yes
209	SW	DDB_OUTPUT_TRI_LED_9_GRN	Tri-LED - 9 - Green	FnKey LED1 Grn		Yes	Yes
210	SW	DDB_OUTPUT_TRI_LED_10_RED	Tri-LED - 10 - Red	FnKey LED2 Red		Yes	Yes
211	SW	DDB_OUTPUT_TRI_LED_10_GRN	Tri-LED - 10 - Green	FnKey LED2 Grn		Yes	Yes
212	SW	DDB_OUTPUT_TRI_LED_11_RED	Tri-LED - 11 - Red	FnKey LED3 Red		Yes	Yes
213	SW	DDB_OUTPUT_TRI_LED_11_GRN	Tri-LED - 11 - Green	FnKey LED3 Grn		Yes	Yes
214	SW	DDB_OUTPUT_TRI_LED_12_RED	Tri-LED - 12 - Red	FnKey LED4 Red		Yes	Yes
215	SW	DDB_OUTPUT_TRI_LED_12_GRN	Tri-LED - 12 - Green	FnKey LED4 Grn		Yes	Yes

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
216	SW	DDB_OUTPUT_TRI_LED_13_RED	Tri-LED - 13 - Red	FnKey LED5 Red		Yes	Yes
217	SW	DDB_OUTPUT_TRI_LED_13_GRN	Tri-LED - 13 - Green	FnKey LED5 Grn		Yes	Yes
218	SW	DDB_OUTPUT_TRI_LED_14_RED	Tri-LED - 14 - Red	FnKey LED6 Red		Yes	Yes
219	SW	DDB_OUTPUT_TRI_LED_14_GRN	Tri-LED - 14 - Green	FnKey LED6 Grn		Yes	Yes
220	SW	DDB_OUTPUT_TRI_LED_15_RED	Tri-LED - 15 - Red	FnKey LED7 Red		Yes	Yes
221	SW	DDB_OUTPUT_TRI_LED_15_GRN	Tri-LED - 15 - Green	FnKey LED7 Grn		Yes	Yes
222	SW	DDB_OUTPUT_TRI_LED_16_RED	Tri-LED - 16 - Red	FnKey LED8 Red		Yes	Yes
223	SW	DDB_OUTPUT_TRI_LED_16_GRN	Tri-LED - 16 - Green	FnKey LED8 Grn		Yes	Yes
224	SW	DDB_OUTPUT_TRI_LED_17_RED	Tri-LED - 17 - Red	FnKey LED9 Red		Yes	Yes
225	SW	DDB_OUTPUT_TRI_LED_17_GRN	Tri-LED - 17 - Green	FnKey LED9 Grn		Yes	Yes
226	SW	DDB_OUTPUT_TRI_LED_18_RED	Tri-LED - 18 - Red	FnKey LED10 Red		Yes	Yes
227	SW	DDB_OUTPUT_TRI_LED_18_GRN	Tri-LED - 18 - Green	FnKey LED10 Grn		Yes	Yes
228	SW	DDB_UNUSED	DDB_UNUSED				
229	SW	DDB_UNUSED	DDB_UNUSED				
230	SW	DDB_UNUSED	DDB_UNUSED				
231	SW	DDB_UNUSED	DDB_UNUSED				
232	SW	DDB_UNUSED	DDB_UNUSED				
233	SW	DDB_UNUSED	DDB_UNUSED				
234	SW	DDB_UNUSED	DDB_UNUSED				
235	SW	DDB_UNUSED	DDB_UNUSED				
236	SW	DDB_UNUSED	DDB_UNUSED				
237	SW	DDB_UNUSED	DDB_UNUSED				
238	SW	DDB_UNUSED	DDB_UNUSED				
239	SW	DDB_UNUSED	DDB_UNUSED				
240	SW	DDB_UNUSED	DDB_UNUSED				
241	SW	DDB_UNUSED	DDB_UNUSED				
242	SW	DDB_UNUSED	DDB_UNUSED				
243	SW	DDB_UNUSED	DDB_UNUSED				
244	SW	DDB_UNUSED	DDB_UNUSED				
245	SW	DDB_UNUSED	DDB_UNUSED				
246	SW	DDB_UNUSED	DDB_UNUSED				
247	SW	DDB_UNUSED	DDB_UNUSED				
248	SW	DDB_UNUSED	DDB_UNUSED				
249	SW	DDB_UNUSED	DDB_UNUSED				
250	SW	DDB_UNUSED	DDB_UNUSED				
251	SW	DDB_UNUSED	DDB_UNUSED				
252	SW	DDB_UNUSED	DDB_UNUSED				
253	SW	DDB_UNUSED	DDB_UNUSED				
254	SW	DDB_UNUSED	DDB_UNUSED				
255	SW	DDB_UNUSED	DDB_UNUSED				
256	PSL	DDB_TRI_LED_RED_CON_1	Tri-LED Conditioner - 1 - Red	LED1 Con R		Yes	Yes
257	PSL	DDB_TRI_LED_GRN_CON_1	Tri-LED Conditioner- 1 - Green	LED1 Con G		Yes	Yes
258	PSL	DDB_TRI_LED_RED_CON_2	Tri-LED Conditioner - 2 - Red	LED2 Con R		Yes	Yes
259	PSL	DDB_TRI_LED_GRN_CON_2	Tri-LED Conditioner - 2 - Green	LED2 Con G		Yes	Yes

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
260	PSL	DDB_TRI_LED_RED_CON_3	Tri-LED Conditioner - 3 - Red	LED3 Con R		Yes	Yes
261	PSL	DDB_TRI_LED_GRN_CON_3	Tri-LED Conditioner - 3 - Green	LED3 Con G		Yes	Yes
262	PSL	DDB_TRI_LED_RED_CON_4	Tri-LED Conditioner - 4 - Red	LED4 Con R		Yes	Yes
263	PSL	DDB_TRI_LED_GRN_CON_4	Tri-LED Conditioner - 4 - Green	LED4 Con G		Yes	Yes
264	PSL	DDB_TRI_LED_RED_CON_5	Tri-LED Conditioner - 5 - Red	LED5 Con R		Yes	Yes
265	PSL	DDB_TRI_LED_GRN_CON_5	Tri-LED Conditioner - 5 - Green	LED5 Con G		Yes	Yes
266	PSL	DDB_TRI_LED_RED_CON_6	Tri-LED Conditioner - 6 - Red	LED6 Con R		Yes	Yes
267	PSL	DDB_TRI_LED_GRN_CON_6	Tri-LED Conditioner - 6 - Green	LED6 Con G		Yes	Yes
268	PSL	DDB_TRI_LED_RED_CON_7	Tri-LED Conditioner - 7 - Red	LED7 Con R		Yes	Yes
269	PSL	DDB_TRI_LED_GRN_CON_7	Tri-LED Conditioner - 7 - Green	LED7 Con G		Yes	Yes
270	PSL	DDB_TRI_LED_RED_CON_8	Tri-LED Conditioner - 8 - Red	LED8 Con R		Yes	Yes
271	PSL	DDB_TRI_LED_GRN_CON_8	Tri-LED Conditioner - 8 - Green	LED8 Con G		Yes	Yes
272	PSL	DDB_TRI_LED_RED_CON_9	Tri-LED Conditioner - 9 - Red	FnKey LED1 ConR		Yes	Yes
273	PSL	DDB_TRI_LED_GRN_CON_9	Tri-LED Conditioner - 9 - Green	FnKey LED1 ConG		Yes	Yes
274	PSL	DDB_TRI_LED_RED_CON_10	Tri-LED Conditioner - 10 - Red	FnKey LED2 ConR		Yes	Yes
275	PSL	DDB_TRI_LED_GRN_CON_10	Tri-LED Conditioner - 10 - Green	FnKey LED2 ConG		Yes	Yes
276	PSL	DDB_TRI_LED_RED_CON_11	Tri-LED Conditioner - 11 - Red	FnKey LED3 ConR		Yes	Yes
277	PSL	DDB_TRI_LED_GRN_CON_11	Tri-LED Conditioner - 11 - Green	FnKey LED3 ConG		Yes	Yes
278	PSL	DDB_TRI_LED_RED_CON_12	Tri-LED Conditioner - 12 - Red	FnKey LED4 ConR		Yes	Yes
279	PSL	DDB_TRI_LED_GRN_CON_12	Tri-LED Conditioner - 12 - Green	FnKey LED4 ConG		Yes	Yes
280	PSL	DDB_TRI_LED_RED_CON_13	Tri-LED Conditioner - 13 - Red	FnKey LED5 ConR		Yes	Yes
281	PSL	DDB_TRI_LED_GRN_CON_13	Tri-LED Conditioner - 13 - Green	FnKey LED5 ConG		Yes	Yes
282	PSL	DDB_TRI_LED_RED_CON_14	Tri-LED Conditioner - 14 - Red	FnKey LED6 ConR		Yes	Yes
283	PSL	DDB_TRI_LED_GRN_CON_14	Tri-LED Conditioner - 14 - Green	FnKey LED6 ConG		Yes	Yes
284	PSL	DDB_TRI_LED_RED_CON_15	Tri-LED Conditioner - 15 - Red	FnKey LED7 ConR		Yes	Yes
285	PSL	DDB_TRI_LED_GRN_CON_15	Tri-LED Conditioner - 15 - Green	FnKey LED7 ConG		Yes	Yes
286	PSL	DDB_TRI_LED_RED_CON_16	Tri-LED Conditioner - 16 - Red	FnKey LED8 ConR		Yes	Yes
287	PSL	DDB_TRI_LED_GRN_CON_16	Tri-LED Conditioner - 16 - Green	FnKey LED8 ConG		Yes	Yes
288	PSL	DDB_TRI_LED_RED_CON_17	Tri-LED Conditioner - 17 - Red	FnKey LED9 ConR		Yes	Yes
289	PSL	DDB_TRI_LED_GRN_CON_17	Tri-LED Conditioner - 17 - Green	FnKey LED9 ConG		Yes	Yes
290	PSL	DDB_TRI_LED_RED_CON_18	Tri-LED Conditioner - 18 - Red	FnKey LED10 ConR		Yes	Yes
291	PSL	DDB_TRI_LED_GRN_CON_18	Tri-LED Conditioner - 18 - Green	FnKey LED10 ConG		Yes	Yes
292	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
293	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
294	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
295	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
296	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
297	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
298	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
299	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
300	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
301	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
302	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
303	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
304	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
305	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
306	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
307	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
308	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
309	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
310	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
311	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
312	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
313	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
314	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
315	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
316	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
317	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
318	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
319	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
320	SW	DDB_OUTPUT_LED_1	LED 1	LED 1	Yes		
321	SW	DDB_OUTPUT_LED_2	LED 2	LED 2	Yes		
322	SW	DDB_OUTPUT_LED_3	LED 3	LED 3	Yes		
323	SW	DDB_OUTPUT_LED_4	LED 4	LED 4	Yes		
324	SW	DDB_OUTPUT_LED_5	LED 5	LED 5	Yes		
325	SW	DDB_OUTPUT_LED_6	LED 6	LED 6	Yes		
326	SW	DDB_OUTPUT_LED_7	LED 7	LED 7	Yes		
327	SW	DDB_OUTPUT_LED_8	LED 8	LED 8	Yes		
328	PSL	DDB_LED_CON_1	LED Conditioner IN 1	LED Cond IN 1	Yes		
329	PSL	DDB_LED_CON_2	LED Conditioner IN 2	LED Cond IN 2	Yes		
330	PSL	DDB_LED_CON_3	LED Conditioner IN 3	LED Cond IN 3	Yes		
331	PSL	DDB_LED_CON_4	LED Conditioner IN 4	LED Cond IN 4	Yes		
332	PSL	DDB_LED_CON_5	LED Conditioner IN 5	LED Cond IN 5	Yes		
333	PSL	DDB_LED_CON_6	LED Conditioner IN 6	LED Cond IN 6	Yes		
334	PSL	DDB_LED_CON_7	LED Conditioner IN 7	LED Cond IN 7	Yes		
335	PSL	DDB_LED_CON_8	LED Conditioner IN 8	LED Cond IN 8	Yes		
336	SW	DDB_DST_STATUS	If this location DST is in effect now	DST status	Yes	Yes	Yes
337	SW	DDB_UNUSED	DDB_UNUSED				
338	SW	DDB_UNUSED	DDB_UNUSED				
339	SW	DDB_UNUSED	DDB_UNUSED				
340	SW	DDB_UNUSED	DDB_UNUSED				
341	SW	DDB_UNUSED	DDB_UNUSED				
342	SW	DDB_UNUSED	DDB_UNUSED				
343	SW	DDB_UNUSED	DDB_UNUSED				
344	SW	DDB_UNUSED	DDB_UNUSED				
345	SW	DDB_UNUSED	DDB_UNUSED				
346	SW	DDB_UNUSED	DDB_UNUSED				
347	SW	DDB_UNUSED	DDB_UNUSED				

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
348	SW	DDB_UNUSED	DDB_UNUSED				
349	SW	DDB_UNUSED	DDB_UNUSED				
350	SW	DDB_UNUSED	DDB_UNUSED				
351	SW	DDB_UNUSED	DDB_UNUSED				
352	SW	DDB_FN_KEY_1	Function Key 1	Function Key 1		Yes	Yes
353	SW	DDB_FN_KEY_2	Function Key 2	Function Key 2		Yes	Yes
354	SW	DDB_FN_KEY_3	Function Key 3	Function Key 3		Yes	Yes
355	SW	DDB_FN_KEY_4	Function Key 4	Function Key 4		Yes	Yes
356	SW	DDB_FN_KEY_5	Function Key 5	Function Key 5		Yes	Yes
357	SW	DDB_FN_KEY_6	Function Key 6	Function Key 6		Yes	Yes
358	SW	DDB_FN_KEY_7	Function Key 7	Function Key 7		Yes	Yes
359	SW	DDB_FN_KEY_8	Function Key 8	Function Key 8		Yes	Yes
360	SW	DDB_FN_KEY_9	Function Key 9	Function Key 9		Yes	Yes
361	SW	DDB_FN_KEY_10	Function Key 10	Function Key 10		Yes	Yes
362	SW	DDB_UNUSED	DDB_UNUSED				
363	SW	DDB_UNUSED	DDB_UNUSED				
364	SW	DDB_UNUSED	DDB_UNUSED				
365	SW	DDB_UNUSED	DDB_UNUSED				
366	SW	DDB_UNUSED	DDB_UNUSED				
367	SW	DDB_UNUSED	DDB_UNUSED				
368	SW	DDB_UNUSED	DDB_UNUSED				
369	SW	DDB_UNUSED	DDB_UNUSED				
370	SW	DDB_UNUSED	DDB_UNUSED				
371	SW	DDB_UNUSED	DDB_UNUSED				
372	SW	DDB_UNUSED	DDB_UNUSED				
373	SW	DDB_UNUSED	DDB_UNUSED				
374	SW	DDB_UNUSED	DDB_UNUSED				
375	SW	DDB_UNUSED	DDB_UNUSED				
376	SW	DDB_UNUSED	DDB_UNUSED				
377	SW	DDB_UNUSED	DDB_UNUSED				
378	SW	DDB_UNUSED	DDB_UNUSED				
379	SW	DDB_UNUSED	DDB_UNUSED				
380	SW	DDB_UNUSED	DDB_UNUSED				
381	SW	DDB_UNUSED	DDB_UNUSED				
382	SW	DDB_UNUSED	DDB_UNUSED				
383	SW	DDB_UNUSED	DDB_UNUSED				
384	SW	DDB_TIMEROUT_1	Auxiliary Timer out 1	Timer out 1	Yes	Yes	Yes
385	SW	DDB_TIMEROUT_2	Auxiliary Timer out 2	Timer out 2	Yes	Yes	Yes
386	SW	DDB_TIMEROUT_3	Auxiliary Timer out 3	Timer out 3	Yes	Yes	Yes
387	SW	DDB_TIMEROUT_4	Auxiliary Timer out 4	Timer out 4	Yes	Yes	Yes
388	SW	DDB_TIMEROUT_5	Auxiliary Timer out 5	Timer out 5	Yes	Yes	Yes
389	SW	DDB_TIMEROUT_6	Auxiliary Timer out 6	Timer out 6	Yes	Yes	Yes
390	SW	DDB_TIMEROUT_7	Auxiliary Timer out 7	Timer out 7	Yes	Yes	Yes
391	SW	DDB_TIMEROUT_8	Auxiliary Timer out 8	Timer out 8	Yes	Yes	Yes

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
392	SW	DDB_TIMEROUT_9	Auxiliary Timer out 9	Timer out 9	Yes	Yes	Yes
393	SW	DDB_TIMEROUT_10	Auxiliary Timer out 10	Timer out 10	Yes	Yes	Yes
394	SW	DDB_TIMEROUT_11	Auxiliary Timer out 11	Timer out 11	Yes	Yes	Yes
395	SW	DDB_TIMEROUT_12	Auxiliary Timer out 12	Timer out 12	Yes	Yes	Yes
396	SW	DDB_TIMEROUT_13	Auxiliary Timer out 13	Timer out 13	Yes	Yes	Yes
397	SW	DDB_TIMEROUT_14	Auxiliary Timer out 14	Timer out 14	Yes	Yes	Yes
398	SW	DDB_TIMEROUT_15	Auxiliary Timer out 15	Timer out 15	Yes	Yes	Yes
399	SW	DDB_TIMEROUT_16	Auxiliary Timer out 16	Timer out 16	Yes	Yes	Yes
400	SW	DDB_UNUSED	DDB_UNUSED				
401	SW	DDB_UNUSED	DDB_UNUSED				
402	SW	DDB_UNUSED	DDB_UNUSED				
403	SW	DDB_UNUSED	DDB_UNUSED				
404	SW	DDB_UNUSED	DDB_UNUSED				
405	SW	DDB_UNUSED	DDB_UNUSED				
406	SW	DDB_UNUSED	DDB_UNUSED				
407	SW	DDB_UNUSED	DDB_UNUSED				
408	SW	DDB_UNUSED	DDB_UNUSED				
409	SW	DDB_UNUSED	DDB_UNUSED				
410	SW	DDB_UNUSED	DDB_UNUSED				
411	SW	DDB_UNUSED	DDB_UNUSED				
412	SW	DDB_UNUSED	DDB_UNUSED				
413	SW	DDB_UNUSED	DDB_UNUSED				
414	SW	DDB_UNUSED	DDB_UNUSED				
415	SW	DDB_UNUSED	DDB_UNUSED				
416	PSL	DDB_TIMERIN_1	Auxiliary Timer in 1	Timer in 1	Yes	Yes	Yes
417	PSL	DDB_TIMERIN_2	Auxiliary Timer in 2	Timer in 2	Yes	Yes	Yes
418	PSL	DDB_TIMERIN_3	Auxiliary Timer in 3	Timer in 3	Yes	Yes	Yes
419	PSL	DDB_TIMERIN_4	Auxiliary Timer in 4	Timer in 4	Yes	Yes	Yes
420	PSL	DDB_TIMERIN_5	Auxiliary Timer in 5	Timer in 5	Yes	Yes	Yes
421	PSL	DDB_TIMERIN_6	Auxiliary Timer in 6	Timer in 6	Yes	Yes	Yes
422	PSL	DDB_TIMERIN_7	Auxiliary Timer in 7	Timer in 7	Yes	Yes	Yes
423	PSL	DDB_TIMERIN_8	Auxiliary Timer in 8	Timer in 8	Yes	Yes	Yes
424	PSL	DDB_TIMERIN_9	Auxiliary Timer in 9	Timer in 9	Yes	Yes	Yes
425	PSL	DDB_TIMERIN_10	Auxiliary Timer in 10	Timer in 10	Yes	Yes	Yes
426	PSL	DDB_TIMERIN_11	Auxiliary Timer in 11	Timer in 11	Yes	Yes	Yes
427	PSL	DDB_TIMERIN_12	Auxiliary Timer in 12	Timer in 12	Yes	Yes	Yes
428	PSL	DDB_TIMERIN_13	Auxiliary Timer in 13	Timer in 13	Yes	Yes	Yes
429	PSL	DDB_TIMERIN_14	Auxiliary Timer in 14	Timer in 14	Yes	Yes	Yes
430	PSL	DDB_TIMERIN_15	Auxiliary Timer in 15	Timer in 15	Yes	Yes	Yes
431	PSL	DDB_TIMERIN_16	Auxiliary Timer in 16	Timer in 16	Yes	Yes	Yes
432	SW	DDB_UNUSED	DDB_UNUSED				
433	SW	DDB_UNUSED	DDB_UNUSED				
434	SW	DDB_UNUSED	DDB_UNUSED				
435	SW	DDB_UNUSED	DDB_UNUSED				

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
436	SW	DDB_UNUSED	DDB_UNUSED				
437	SW	DDB_UNUSED	DDB_UNUSED				
438	SW	DDB_UNUSED	DDB_UNUSED				
439	SW	DDB_UNUSED	DDB_UNUSED				
440	SW	DDB_UNUSED	DDB_UNUSED				
441	SW	DDB_UNUSED	DDB_UNUSED				
442	SW	DDB_UNUSED	DDB_UNUSED				
443	SW	DDB_UNUSED	DDB_UNUSED				
444	SW	DDB_UNUSED	DDB_UNUSED				
445	SW	DDB_UNUSED	DDB_UNUSED				
446	SW	DDB_UNUSED	DDB_UNUSED				
447	SW	DDB_UNUSED	DDB_UNUSED				
448	SW	DDB_UNUSED	DDB ALARMS				
449	SW	DDB_UNUSED	DDB_UNUSED				
450	SW	DDB_ILLEGAL_OPTO_SETTINGS_GROUP	Setting Group selection by DDB inputs invalid	SG-DDB Invalid	Yes	Yes	Yes
451	SW	DDB_CB_STATUS_ALARM	CB Status Alarm	CB Status Alarm	Yes	Yes	Yes
451	FL	DDB_CB_STATUS_ALARM	CB Status Alarm	CB Status Alarm			
452	FL	DDB_RTD_ALARM	RTD Thermal Alarm	RTD Thermal Alm	Yes	Yes	Yes
453	SW	DDB_RTD_OPEN_CCT	RTD Open Circuit Failure	RTD Open Cct	Yes	Yes	Yes
454	SW	DDB_RTD_SHORT_CCT	RTD Short Circuit Failure	RTD short Cct	Yes	Yes	Yes
455	SW	DDB_RTD_DATA_ERROR	RTD Data Inconsistency Error	RTD Data Error	Yes	Yes	Yes
456	SW	DDB_RTD_BOARD_FAILURE	RTD Board Failure	RTD Board Fail	Yes	Yes	Yes
457	SW	DDB_CL_INPUT_1_ALARM	Current Loop Input 1 Alarm	CL Input 1 Alarm	Yes	Yes	Yes
458	SW	DDB_CL_INPUT_2_ALARM	Current Loop Input 2 Alarm	CL Input 2 Alarm	Yes	Yes	Yes
459	SW	DDB_CL_INPUT_3_ALARM	Current Loop Input 3 Alarm	CL Input 3 Alarm	Yes	Yes	Yes
460	SW	DDB_CL_INPUT_4_ALARM	Current Loop Input 4 Alarm	CL Input 4 Alarm	Yes	Yes	Yes
461	SW	DDB_CLI_1_UNDERCURRENT_ALARM	Current Loop Input 1 Undercurrent Fail Alarm	CLI1 I< Fail Alm	Yes	Yes	Yes
462	SW	DDB_CLI_2_UNDERCURRENT_ALARM	Current Loop Input 2 Undercurrent Fail Alarm	CLI2 I< Fail Alm	Yes	Yes	Yes
463	SW	DDB_CLI_3_UNDERCURRENT_ALARM	Current Loop Input 3 Undercurrent Fail Alarm	CLI3 I< Fail Alm	Yes	Yes	Yes
464	SW	DDB_CLI_4_UNDERCURRENT_ALARM	Current Loop Input 4 Undercurrent Fail Alarm	CLI4 I< Fail Alm	Yes	Yes	Yes
465	SW	DDB_OOS_ALARM	OOS ALARM	Prot'n Disabled	Yes	Yes	Yes
466	FL	DDB_FREQ_ALARM	Frequency out of range	F out of range	Yes	Yes	Yes
467	SW	DDB_CIR_FLT_Z1_ALM	Circuilty Fault Z1 Alm	Cct Fail Z1 Alm			
468	SW	DDB_CIR_FLT_Z2_ALM	Circuilty Fault Z2 Alm	Cct Fail Z2 Alm			
469	SW	DDB_CIR_FLT_CZ_ALM	Circuilty Fault CZ Alm	Cct Fail CZ Alm			
470	SW	DDB_CLIO_CARD_INPUT_FAIL	CL Card I/P Fail	CL Card I/P Fail	Yes	Yes	Yes
471	SW	DDB_CLIO_CARD_OUTPUT_FAIL	CL Card O/P Fail	CL Card O/P Fail	Yes	Yes	Yes
472	SW	DDB_VCO_1_CONFIG_ALARM	The configuration of VCO terminal input don't match to the location of main VT	VCO>1 Config err	Yes	Yes	Yes

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
473	SW	DDB_VCO_2_CONFIG_ALARM	The configuration of VCO terminal input don't match to the location of main VT	VCO>2 Config err	Yes	Yes	Yes
474	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
475	SW	DDB_CTS_INDICATION	CTS Fail Alarm	CTS Fail Alarm	Yes	Yes	Yes
476	SW	DDB_CIRCUITRY_FLT_ALM	Circuity FLT Alm	Circuity FLT Alm	Yes	Yes	Yes
477	SW	DDB_VTS_INDICATION	VTS VT Fail Alarm	VT Fail Alarm	Yes	Yes	Yes
478	SW	DDB_TOL_PRETRIP_ALARM	Thermal Pretrp Alarm	Therm Pretrp Alm	Yes	Yes	Yes
479	SW	DDB_FAA_ALARM	FAA alarm	FAA alarm	Yes	Yes	Yes
480	SW	DDB_LOL_ALARM	LOL alarm	LOL alarm	Yes	Yes	Yes
481	SW	DDB_BREAKER_FAIL_ALARM	Breaker Fail Alarm	Breaker Fail	Yes	Yes	Yes
482	SW	DDB_CT_MISMATCH_ALARM	Ct para mismatch	Ct para mismatch	Yes	Yes	Yes
483	SW	DDB_CT_REPEATED_SELECTED_ALARM	CT being repeated selected between windings	CT Selection Alm	Yes	Yes	Yes
484	SW	DDB_SINGLEPHASE_CT_ALARM	Single Phase CT not being only used by High Impedance REF	SinglePha CT Alm	Yes	Yes	Yes
485	SW	DDB_INSUFF_NO_OF_CT	Unsufficient number of CTs	insuff No. of CT		Yes	Yes
486	SW	DDB_DISC_CT_INVALID	Invalid disconnected CT status	Disc CT invalid		Yes	Yes
487	SW	DDB_HV_SCALING_FACTOR_ALARM	HV LowZ REF scaling factor out of range	HV-LZREF sf OOR	Yes	Yes	Yes
488	SW	DDB_LV_SCALING_FACTOR_ALARM	LV LowZ REF scaling factor out of range	LV-LZREF sf OOR	Yes	Yes	Yes
489	SW	DDB_TV_SCALING_FACTOR_ALARM	TV LowZ REF scaling factor out of range	TV-LZREF sf OOR		Yes	Yes
490	SW	DDB_AUTO_SCALING_FACTOR_ALARM	Auto LowZ REF scaling factor out of range	AutoLZREF sf OOR	Yes	Yes	Yes
491	SW	DDB_CB_FAIL_ALM_T9	CB Fail Alarm T9	CB Fail Alm T9			
491	SW	DDB_CB_FAIL_ALM_T10	CB Fail Alarm T10	CB Fail Alm T10			
492	SW	DDB_CB_FAIL_ALM_T11	CB Fail Alarm T11	CB Fail Alm T11			
493	SW	DDB_CB_FAIL_ALM_T12	CB Fail Alarm T12	CB Fail Alm T12			
494	SW	DDB_CB_FAIL_ALM_T13	CB Fail Alarm T13	CB Fail Alm T13			
495	SW	DDB_CB_FAIL_ALM_T14	CB Fail Alarm T14	CB Fail Alm T14			
496	SW	DDB_CB_FAIL_ALM_T15	CB Fail Alarm T15	CB Fail Alm T15			
497	SW	DDB_CB_FAIL_ALM_T16	CB Fail Alarm T16	CB Fail Alm T16			
498	SW	DDB_CB_FAIL_ALM_T17	CB Fail Alarm T17	CB Fail Alm T17			
499	SW	DDB_CB_FAIL_ALM_T18	CB Fail Alarm T18	CB Fail Alm T18			
500	SW	DDB_CB_FAIL_BUS_CB	CB Fail Alarm Bus CB	CB Fail Alarm Bus CB			
501	SW	DDB_VPERHZ_ALARM_1	W1 V/Hz> Alarm	W1 V/Hz> Alarm		Yes	Yes
502	SW	DDB_VPERHZ_PRETRP_ALARM_1	W1 V/Hz> PrTrp Alm	W1 V/Hz> PrTrp		Yes	Yes
503	SW	DDB_VPERHZ_ALARM_2	W2 V/Hz> Alarm	W2 V/Hz> Alarm	Yes	Yes	Yes
504	SW	DDB_VPERHZ_PRETRP_ALARM_2	W2 V/Hz> PrTrp Alm	W2 V/Hz> PrTrp	Yes	Yes	Yes
505	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
506	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
507	SW	DDB_FREQ_PROT_ALM	Frequency Protection Alarm	Freq Prot Alm	Yes	Yes	Yes
508	SW	DDB_THROUGH_FAULT_ALARM	Through fault Alarm	Through flt Alm	Yes	Yes	Yes

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
509	SW	DDB_Z1_INTEST_ALARM	Z1 in Test Mode Alarm	Z1 in Test Mode Alarm			
510	SW	DDB_Z2_INTEST_ALARM	Z2 in Test Mode Alarm	Z2 in Test Mode Alarm			
511	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
512	SW	DDB_BATTERY_FAIL_ALARM	Battery Fail alarm indication	Battery Fail	Yes	Yes	Yes
513	SW	DDB_FIELD_VOLTS_FAIL	Field Voltage Failure	Field Volts Fail	Yes	Yes	Yes
514	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
515	SW	DDB_GOOSE_MISSING_IED_ALARM	Enrolled GOOSE IED absent alarm indication	GOOSE IED Absent	Yes	Yes	Yes
516	SW	DDB_ECARD_NOT_FITTED_ALARM	Network Interface Card not fitted/failed alarm	NIC Not Fitted	Yes	Yes	Yes
517	SW	DDB_NIC_NOT_RESPONDING_ALARM	Network Interface Card not responding alarm	NIC No Response	Yes	Yes	Yes
518	SW	DDB_NIC_FATAL_ERROR_ALARM	Network Interface Card fatal error alarm indication	NIC Fatal Error	Yes	Yes	Yes
519	SW	DDB_NIC_SOFTWARE_RELOAD_ALARM	Network Interface Card software reload alarm	NIC Soft. Reload	Yes	Yes	Yes
520	SW	DDB_MU_OOS_ALARM	MU OOS Alarm	MU OOS Alarm	Yes	Yes	Yes
521	SW	DDB_INVALID_SV_CONFIG_ALARM	Invalid IEC 61850 Configuration Alarm for PB	Invalid SV conf.	Yes	Yes	Yes
522	SW	DDB_SV_ABSENCE_ALARM	SV Absence Alm	SV Absence Alm			
523	SW	DDB_SW_MISMATCH_ALARM	Main card/NIC software mismatch alarm indication	NIC SW Mis-Match	Yes	Yes	Yes
524	SW	DDB_IP_ADDRESS_CONFLICT_ALARM	IP address conflict alarm indication	IP Addr Conflict	Yes	Yes	Yes
525	SW	DDB_UNUSED	DDB_UNUSED				
526	SW	DDB_UNUSED	DDB_UNUSED				
527	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
528	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
529	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
530	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
531	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
532	SW	DDB_UNUSED	DDB_UNUSED				
533	SW	DDB_INVALID_DNPOE_IP_ALARM	Invalid DNPoE IP Configuration Alarm	Invalid DNPoE IP	Yes	Yes	Yes
534	SW	DDB_INVALID_CONFIG_ALARM	Invalid IEC 61850 Configuration Alarm	Invalid Config.	Yes	Yes	Yes
535	SW	DDB_TEST_MODE_ALARM	Test Mode Activated Alarm	Test Mode Alm	Yes	Yes	Yes
536	SW	DDB_CONT_BLK_ALARM	Contacts Blocked Alarm	Contacts Blk Alm	Yes	Yes	Yes
537	SW	DDB_HW_MISMATCH_ALARM	Main card/Ethernet card hw option mismatch Alarm	NIC HW Mis-Match	Yes	Yes	Yes
538	SW	DDB_IEC61850_VER_MISMATCH_ALARM	Main card/Ethernet card IEC61850 ver mismatch Alarm	NIC Ed Mis-Match	Yes	Yes	Yes
539	SW	DDB_ACEPT_SIMULATED_ALM	IEC 61850 accept simulation signal alarm	Sim.Signal Alm	Yes	Yes	Yes
540	SW	DDB_SV_SMPSYNCH_ALARM	SV SmpSynch alarm	SV SmpSynch Alm	Yes	Yes	Yes
541	SW	DDB_SV_TEST_ALARM	SV Test alarm	SV Test Alm	Yes	Yes	Yes

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
542	SW	DDB_SV_INVALID_ALARM	SV Invalid alarm	SV Invalid Alm	Yes	Yes	Yes
543	SW	DDB_SV_QUESTIONABLE_ALARM	SV Questionable alarm	SV Quest Alm	Yes	Yes	Yes
544	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
545	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
546	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
547	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
548	PSL	DDB_INHIBIT_BUSDIFF_Z1	Block Z1 Diff	Block Z1 Diff	Yes	Yes	Yes
549	PSL	DDB_INHIBIT_BUSDIFF_Z2	Block Z2 Diff	Block Z2 Diff	Yes	Yes	Yes
550	PSL	DDB_INHIBIT_BUSDIFF_CZ	Block CZ Diff	Block CZ Diff	Yes	Yes	Yes
551	PSL	DDB_BLK_TRANS_DIFF	Block Transformer Differential protection	Block Transdiff	Yes	Yes	Yes
552	SW	DDB_2ND_HAR_BLKA	2nd Harmonic A	I(2)/I(1)> A	Yes	Yes	Yes
553	SW	DDB_2ND_HAR_BLKB	2nd Harmonic B	I(2)/I(1)> B	Yes	Yes	Yes
554	SW	DDB_2ND_HAR_BLKC	2nd Harmonic C	I(2)/I(1)> C	Yes	Yes	Yes
555	SW	DDB_5TH_HAR_BLKA	5th Har Blk A	5th Har Blk A	Yes	Yes	Yes
556	SW	DDB_5TH_HAR_BLKB	5th Har Blk B	5th Har Blk B	Yes	Yes	Yes
557	SW	DDB_5TH_HAR_BLKC	5th Har Blk C	5th Har Blk C	Yes	Yes	Yes
558	SW	DDB_DEADBUS_ZONE1_DETECTED	Dead Bus Zone 1Detected	Dead Bus Zone 1			
559	SW	DDB_DEADBUS_ZONE2_DETECTED	Dead Bus Zone 2Detected	Dead Bus Zone 2			
560	SW	DDB_VT_CHECK_ALLOW_ZONE1	VT Check Allow Z1 Trip	VT Check Allow Z1 Trip	Yes	Yes	Yes
561	SW	DDB_VT_CHECK_ALLOW_ZONE2	VT Check Allow Z2 Trip	VT Check Allow Z2 Trip	Yes	Yes	Yes
562	PSL	DDB_PUV_1_TIMER_BLOCK	Block Phase Under Voltage Stage 1 time delay	V<1 Timer Block	Yes	Yes	Yes
563	PSL	DDB_PUV_2_TIMER_BLOCK	Block Phase Under Voltage Stage 2 time delay	V<2 Timer Block	Yes	Yes	Yes
564	PSL	DDB_POV_1_TIMER_BLOCK	Block Phase Over Voltage Stage 1 time delay	V>1 Timer Block	Yes	Yes	Yes
565	PSL	DDB_POV_2_TIMER_BLOCK	Block Phase Over Voltage Stage 2 time delay	V>2 Timer Block	Yes	Yes	Yes
566	PSL	DDB_RESOV_1_TIMER_BLOCK	Block Residual Over Voltage Stage 1 time delay	VN>1 Timer Blk	Yes	Yes	Yes
567	PSL	DDB_RESOV_2_TIMER_BLOCK	Block Residual Over Voltage Stage 2 time delay	VN>2 Timer Blk	Yes	Yes	Yes
568	SW	DDB_UNUSED					
569	SW	DDB_UNUSED					
570	SW	DDB_UNUSED					
571	PSL	DDB_INHIBIT_CTS	Inhibit CTS	Inhibit CTS	Yes	Yes	Yes
572	SW	DDB_CTS_BLK	CTS BLK	CTS BLK	Yes	Yes	Yes
573	SW	DDB_CTS_CT1	CTS CT1	CTS CT1	Yes	Yes	Yes
574	SW	DDB_CTS_CT2	CTS CT2	CTS CT2	Yes	Yes	Yes
575	SW	DDB_CTS_CT3	CTS CT3	CTS CT3		Yes	Yes
576	SW	DDB_CTS_CT4	CTS CT4	CTS CT4			Yes
577	SW	DDB_CTS_CT5	CTS CT5	CTS CT5			Yes
578	SW	DDB_CTS_CT1_IND	CT1 fail indication	CT1 Fail	Yes	Yes	Yes

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
579	SW	DDB_CTS_CT2_IND	CT2 fail indication	CT2 Fail	Yes	Yes	Yes
580	SW	DDB_CTS_CT3_IND	CT3 fail indication	CT3 Fail		Yes	Yes
581	SW	DDB_CTS_CT4_IND	CT4 fail indication	CT4 Fail			Yes
582	SW	DDB_CTS_CT5_IND	CT5 fail indication	CT5 Fail			Yes
583	SW	DDB_CTS_TERMINAL_4	CTS T4	CTS T4			
584	SW	DDB_CTS_TERMINAL_5	CTS T5	CTS T5			
585	SW	DDB_CTS_TERMINAL_6	CTS T6	CTS T6			
586	SW	DDB_LOGIC_0	Logic 0 for use in PSL (Never changes state!)	Logic 0 Ref.	Yes	Yes	Yes
587	SW	DDB_IRIGB_SIGNAL_VALID	IRIG-B Status Signal Valid	IRIG-B Valid	Yes	Yes	Yes
588	PSL	DDB_BLK_TOL	Blk TOL	Blk TOL	Yes	Yes	Yes
589	SW	DDB_CTS_HV	CTS HV	CTS HV	Yes	Yes	Yes
590	SW	DDB_CTS_LV	CTS LV	CTS LV	Yes	Yes	Yes
591	SW	DDB_CTS_TV	CTS TV	CTS TV	Yes	Yes	Yes
592	PSL	DDB_INHIBIT_VTS	Inhibit VTS	Inhibit VTS	Yes	Yes	Yes
593	SW	DDB_VTS_BLK_Z1	VTS Block Z1	VTS Block	Yes	Yes	Yes
594	PSL	DDB_BLK_REF_HV	Blk REF HV	Blk REF HV	Yes	Yes	Yes
595	PSL	DDB_BLK_REF_LV	Blk REF LV	Blk REF LV	Yes	Yes	Yes
596	PSL	DDB_BLK_REF_TV	Blk REF TV	Blk REF TV		Yes	Yes
597	PSL	DDB_BLK_REF_AUTO	Blk REF Auto	Blk REF Auto	Yes	Yes	Yes
598	PSL	DDB_POC1_STAGE1_TIMER_BLOCK	Overcurrent 1 I>1 Timer Block	POC 1 I>1 TBlk	Yes	Yes	Yes
598	PSL	DDB_T1_POC_1_TIMER_BLOCK	T1 I>1 Timer Block	T1 I>1 Timer Blk			
599	PSL	DDB_POC1_STAGE2_TIMER_BLOCK	Overcurrent 1 I>2 Timer Block	POC 1 I>2 TBlk	Yes	Yes	Yes
599	PSL	DDB_T1_POC_2_TIMER_BLOCK	T1 I>2 Timer Block	T1 I>2 Timer Blk			
600	PSL	DDB_POC1_STAGE3_TIMER_BLOCK	Overcurrent 1 I>3 Timer Block	POC 1 I>3 TBlk	Yes	Yes	Yes
600	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
601	PSL	DDB_POC1_STAGE4_TIMER_BLOCK	Overcurrent 1 I>4 Timer Block	POC 1 I>4 TBlk	Yes	Yes	Yes
601	PSL	DDB_T2_POC_1_TIMER_BLOCK	T2 I>1 Timer Block	T2 I>1 Timer Blk			
602	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
602	PSL	DDB_T2_POC_2_TIMER_BLOCK	T2 I>2 Timer Block	T2 I>2 Timer Blk			
603	PSL	DDB_POC2_STAGE1_TIMER_BLOCK	Overcurrent 2 I>1 Timer Block	POC 2 I>1 TBlk	Yes	Yes	Yes
603	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
604	PSL	DDB_POC2_STAGE2_TIMER_BLOCK	Overcurrent 2 I>2 Timer Block	POC 2 I>2 TBlk	Yes	Yes	Yes
604	PSL	DDB_T3_POC_1_TIMER_BLOCK	T3 I>1 Timer Block	T3 I>1 Timer Blk			
605	PSL	DDB_POC2_STAGE3_TIMER_BLOCK	Overcurrent 2 I>3 Timer Block	POC 2 I>3 TBlk	Yes	Yes	Yes
605	PSL	DDB_T3_POC_2_TIMER_BLOCK	T3 I>2 Timer Block	T3 I>2 Timer Blk			
606	PSL	DDB_POC2_STAGE4_TIMER_BLOCK	Overcurrent 2 I>4 Timer Block	POC 2 I>4 TBlk	Yes	Yes	Yes
606	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
607	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
607	PSL	DDB_T4_POC_1_TIMER_BLOCK	T4 I>1 Timer Block	T4 I>1 Timer Blk			
608	PSL	DDB_POC3_STAGE1_TIMER_BLOCK	Overcurrent 3 I>1 Timer Block	POC 3 I>1 TBlk		Yes	Yes
608	PSL	DDB_T4_POC_2_TIMER_BLOCK	T4 I>2 Timer Block	T4 I>2 Timer Blk			
609	PSL	DDB_POC3_STAGE2_TIMER_BLOCK	Overcurrent 3 I>2 Timer Block	POC 3 I>2 TBlk		Yes	Yes
609	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
610	PSL	DDB_POC3_STAGE3_TIMER_BLOCK	Overcurrent 3 I>3 Timer Block	POC 3 I>3 TBlk		Yes	Yes
610	PSL	DDB_T5_POC_1_TIMER_BLOCK	T5 I>1 Timer Block	T5 I>1 Timer Blk			
611	PSL	DDB_POC3_STAGE4_TIMER_BLOCK	Overcurrent 3 I>4 Timer Block	POC 3 I>4 TBlk		Yes	Yes
611	PSL	DDB_T5_POC_2_TIMER_BLOCK	T5 I>2 Timer Block	T5 I>2 Timer Blk			
612	PSL	DDB_T1_TBF1_TIMER_BLOCK	CB1 CBF1 Timer Block	CBF1 Timer1 Blk	Yes	Yes	Yes
613	PSL	DDB_T1_TBF2_TIMER_BLOCK	CB1 CBF2 Timer Block	CBF1 Timer2 Blk	Yes	Yes	Yes
614	PSL	DDB_T2_TBF1_TIMER_BLOCK	CB2 CBF1 Timer Block	CBF2 Timer1 Blk	Yes	Yes	Yes
615	PSL	DDB_T2_TBF2_TIMER_BLOCK	CB2 CBF2 Timer Block	CBF2 Timer2 Blk	Yes	Yes	Yes
616	PSL	DDB_T3_TBF1_TIMER_BLOCK	CB3 CBF1 Timer Block	CBF3 Timer1 Blk		Yes	Yes
617	PSL	DDB_T3_TBF2_TIMER_BLOCK	CB3 CBF2 Timer Block	CBF3 Timer2 Blk		Yes	Yes
618	PSL	DDB_T4_TBF1_TIMER_BLOCK	CB4 CBF1 Timer Block	CBF4 Timer1 Blk			Yes
619	PSL	DDB_T4_TBF2_TIMER_BLOCK	CB4 CBF2 Timer Block	CBF4 Timer2 Blk			Yes
620	PSL	DDB_T5_TBF1_TIMER_BLOCK	CB5 CBF1 Timer Block	CBF5 Timer1 Blk			Yes
621	PSL	DDB_T5_TBF2_TIMER_BLOCK	CB5 CBF2 Timer Block	CBF5 Timer2 Blk			Yes
622	PSL	DDB_T11_POC_1_TIMER_BLOCK	T11 I>1 Timer Block	T11 I>1 TimerBlk			
623	PSL	DDB_T11_POC_2_TIMER_BLOCK	T11 I>2 Timer Block	T11 I>2 TimerBlk			
624	PSL	DDB_T12_POC_1_TIMER_BLOCK	T12 I>1 Timer Block	T12 I>1 TimerBlk			
625	PSL	DDB_T12_POC_2_TIMER_BLOCK	T12 I>2 Timer Block	T12 I>2 TimerBlk			
626	PSL	DDB_T13_POC_1_TIMER_BLOCK	T13 I>1 Timer Block	T13 I>1 TimerBlk			
627	PSL	DDB_T13_POC_2_TIMER_BLOCK	T13 I>2 Timer Block	T13 I>2 TimerBlk			
628	PSL	DDB_T14_POC_1_TIMER_BLOCK	T14 I>1 Timer Block	T14 I>1 TimerBlk			
629	PSL	DDB_T14_POC_2_TIMER_BLOCK	T14 I>2 Timer Block	T14 I>2 TimerBlk			
630	PSL	DDB_T15_POC_1_TIMER_BLOCK	T15 I>1 Timer Block	T15 I>1 TimerBlk			
631	PSL	DDB_T15_POC_2_TIMER_BLOCK	T15 I>2 Timer Block	T15 I>2 TimerBlk			
632	PSL	DDB_T16_POC_1_TIMER_BLOCK	T16 I>1 Timer Block	T16 I>1 TimerBlk			
633	PSL	DDB_T16_POC_2_TIMER_BLOCK	T16 I>2 Timer Block	T16 I>2 TimerBlk			
634	PSL	DDB_T17_POC_1_TIMER_BLOCK	T17 I>1 Timer Block	T17 I>1 TimerBlk			
635	PSL	DDB_T17_POC_2_TIMER_BLOCK	T17 I>2 Timer Block	T17 I>2 TimerBlk			
636	PSL	DDB_T18_POC_1_TIMER_BLOCK	T18 I>1 Timer Block	T18 I>1 TimerBlk			
637	PSL	DDB_T18_POC_2_TIMER_BLOCK	T18 I>2 Timer Block	T18 I>2 TimerBlk			
638	PSL	DDB_UFREQ_1_TIMER_BLOCK	F<1 Timer Block	F<1 Bloc.tempo.	Yes	Yes	Yes
639	PSL	DDB_UFREQ_2_TIMER_BLOCK	F<2 Timer Block	F<2 Bloc.tempo.	Yes	Yes	Yes
640	PSL	DDB_UFREQ_3_TIMER_BLOCK	F<3 Timer Block	F<3 Bloc.tempo.	Yes	Yes	Yes
641	PSL	DDB_UFREQ_4_TIMER_BLOCK	F<4 Timer Block	F<4 Bloc.tempo.	Yes	Yes	Yes
642	PSL	DDB_OFREQ_1_TIMER_BLOCK	F>1 Timer Block	F>1 Bloc.tempo.	Yes	Yes	Yes

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
643	PSL	DDB_OFREQ_2_TIMER_BLOCK	F>2 Timer Block	F>2 Bloc.tempo.	Yes	Yes	Yes
644	PSL	DDB_STUB_BUS_HV_ENABLED	HV StubBus Enabled	HV StubBus En		Yes	Yes
645	PSL	DDB_STUB_BUS_LV_ENABLED	LV StubBus Enabled	LV StubBus En		Yes	Yes
646	PSL	DDB_STUB_BUS_TV_ENABLED	TV StubBus Enabled	TV StubBus En			Yes
647	PSL	DDB_STUB_BUS_HV_ACTIVED	HV StubBus Actived	HV StubBus Act	Yes	Yes	Yes
648	PSL	DDB_STUB_BUS_LV_ACTIVED	LV StubBus Actived	LV StubBus Act	Yes	Yes	Yes
649	PSL	DDB_STUB_BUS_TV_ACTIVED	TV StubBus Actived	TV StubBus Act	Yes	Yes	Yes
650	PSL	DDB_FREQ_STOP_TRACK	Stop Freq Track	Stop Freq Track	Yes	Yes	Yes
651	PSL	DDB_EF1_STAGE1_TIMER_BLOCK	Earth Fault 1 IN>1 TimeBlk	EF 1 IN>1 TBlk	Yes	Yes	Yes
651	PSL	DDB_T1_EF_1_TIMER_BLOCK	T1 IN>1 TimeBlk	T1 IN>1 TimeBlk			
652	PSL	DDB_EF1_STAGE2_TIMER_BLOCK	Earth Fault 1 IN>2 TimeBlk	EF 1 IN>2 TBlk	Yes	Yes	Yes
652	PSL	DDB_T1_EF_2_TIMER_BLOCK	T1 IN>2 TimeBlk	T1 IN>2 TimeBlk			
653	PSL	DDB_EF1_STAGE3_TIMER_BLOCK	Earth Fault 1 IN>3 TimeBlk	EF 1 IN>3 TBlk	Yes	Yes	Yes
653	PSL	DDB_T2_EF_1_TIMER_BLOCK	T2 IN>1 TimeBlk	T2 IN>1 TimeBlk			
654	PSL	DDB_EF1_STAGE4_TIMER_BLOCK	Earth Fault 1 IN>4 TimeBlk	EF 1 IN>4 TBlk	Yes	Yes	Yes
654	PSL	DDB_T2_EF_2_TIMER_BLOCK	T2 IN>2 TimeBlk	T2 IN>2 TimeBlk			
655	PSL	DDB_EF2_STAGE1_TIMER_BLOCK	Earth Fault 2 IN>1 TimeBlk	EF 2 IN>1 TBlk	Yes	Yes	Yes
655	PSL	DDB_T3_EF_1_TIMER_BLOCK	T3 IN>1 TimeBlk	T3 IN>1 TimeBlk			
656	PSL	DDB_EF2_STAGE2_TIMER_BLOCK	Earth Fault 2 IN>2 TimeBlk	EF 2 IN>2 TBlk	Yes	Yes	Yes
656	PSL	DDB_T3_EF_2_TIMER_BLOCK	T3 IN>2 TimeBlk	T3 IN>2 TimeBlk			
657	PSL	DDB_EF2_STAGE3_TIMER_BLOCK	Earth Fault 2 IN>3 TimeBlk	EF 2 IN>3 TBlk	Yes	Yes	Yes
657	PSL	DDB_T4_EF_1_TIMER_BLOCK	T4 IN>1 TimeBlk	T4 IN>1 TimeBlk			
658	PSL	DDB_EF2_STAGE4_TIMER_BLOCK	Earth Fault 2 IN>4 TimeBlk	EF 2 IN>4 TBlk	Yes	Yes	Yes
658	PSL	DDB_T4_EF_2_TIMER_BLOCK	T4 IN>2 TimeBlk	T4 IN>2 TimeBlk			
659	PSL	DDB_EF3_STAGE1_TIMER_BLOCK	Earth Fault 3 IN>1 TimeBlk	EF 3 IN>1 TBlk		Yes	Yes
659	PSL	DDB_T5_EF_1_TIMER_BLOCK	T5 IN>1 TimeBlk	T5 IN>1 TimeBlk			
660	PSL	DDB_EF3_STAGE2_TIMER_BLOCK	Earth Fault 3 IN>2 TimeBlk	EF 3 IN>2 TBlk		Yes	Yes
660	PSL	DDB_T5_EF_2_TIMER_BLOCK	T5 IN>2 TimeBlk	T5 IN>2 TimeBlk			
661	PSL	DDB_EF3_STAGE3_TIMER_BLOCK	Earth Fault 3 IN>3 TimeBlk	EF 3 IN>3 TBlk		Yes	Yes
661	PSL	DDB_T6_EF_1_TIMER_BLOCK	T6 IN>1 TimeBlk	T6 IN>1 TimeBlk			
662	PSL	DDB_EF3_STAGE4_TIMER_BLOCK	Earth Fault 3 IN>4 TimeBlk	EF 3 IN>4 TBlk		Yes	Yes
662	PSL	DDB_T6_EF_2_TIMER_BLOCK	T6 IN>2 TimeBlk	T6 IN>2 TimeBlk			
663	PSL	DDB_NPSOV_1_ACCELERATE	Accelerate NPS Over Voltage Stage 1 Start		Yes	Yes	Yes
664	SW	DDB_VCO_1_PH_AB_START	VCO>1 voltage on Line A-B under threshold	VCO VAB<1 Start	Yes	Yes	Yes
665	SW	DDB_VCO_1_PH_BC_START	VCO>1 voltage on Line B-C under threshold	VCO VBC<1 Start	Yes	Yes	Yes
666	SW	DDB_VCO_1_PH_CA_START	VCO>1 voltage on Line C-A under threshold	VCO VCA<1 Start	Yes	Yes	Yes
667	SW	DDB_VCO_2_PH_AB_START	VCO>2 voltage on Line A-B under threshold	VCO VAB<2 Start	Yes	Yes	Yes
668	SW	DDB_VCO_2_PH_BC_START	VCO>2 voltage on Line B-C under threshold	VCO VBC<2 Start	Yes	Yes	Yes
669	SW	DDB_VCO_2_PH_CA_START	VCO>2 voltage on Line C-A under threshold	VCO VCA<2 Start	Yes	Yes	Yes

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
670	PSL	DDB_VCO_1_TIMER_BLOCK	VCO>1 Timer Block	VCO>1 TimeBlk	Yes	Yes	Yes
671	PSL	DDB_VCO_2_TIMER_BLOCK	VCO>2 Timer Block	VCO>2 TimeBlk	Yes	Yes	Yes
672	PSL	DDB_GOOSEOUT_1	Virtual Output 01	Virtual Output01	Yes	Yes	Yes
673	PSL	DDB_GOOSEOUT_2	Virtual Output 02	Virtual Output02	Yes	Yes	Yes
674	PSL	DDB_GOOSEOUT_3	Virtual Output 03	Virtual Output03	Yes	Yes	Yes
675	PSL	DDB_GOOSEOUT_4	Virtual Output 04	Virtual Output04	Yes	Yes	Yes
676	PSL	DDB_GOOSEOUT_5	Virtual Output 05	Virtual Output05	Yes	Yes	Yes
677	PSL	DDB_GOOSEOUT_6	Virtual Output 06	Virtual Output06	Yes	Yes	Yes
678	PSL	DDB_GOOSEOUT_7	Virtual Output 07	Virtual Output07	Yes	Yes	Yes
679	PSL	DDB_GOOSEOUT_8	Virtual Output 08	Virtual Output08	Yes	Yes	Yes
680	PSL	DDB_GOOSEOUT_9	Virtual Output 09	Virtual Output09	Yes	Yes	Yes
681	PSL	DDB_GOOSEOUT_10	Virtual Output 10	Virtual Output10	Yes	Yes	Yes
682	PSL	DDB_GOOSEOUT_11	Virtual Output 11	Virtual Output11	Yes	Yes	Yes
683	PSL	DDB_GOOSEOUT_12	Virtual Output 12	Virtual Output12	Yes	Yes	Yes
684	PSL	DDB_GOOSEOUT_13	Virtual Output 13	Virtual Output13	Yes	Yes	Yes
685	PSL	DDB_GOOSEOUT_14	Virtual Output 14	Virtual Output14	Yes	Yes	Yes
686	PSL	DDB_GOOSEOUT_15	Virtual Output 15	Virtual Output15	Yes	Yes	Yes
687	PSL	DDB_GOOSEOUT_16	Virtual Output 16	Virtual Output16	Yes	Yes	Yes
688	PSL	DDB_GOOSEOUT_17	Virtual Output 17	Virtual Output17	Yes	Yes	Yes
689	PSL	DDB_GOOSEOUT_18	Virtual Output 18	Virtual Output18	Yes	Yes	Yes
690	PSL	DDB_GOOSEOUT_19	Virtual Output 19	Virtual Output19	Yes	Yes	Yes
691	PSL	DDB_GOOSEOUT_20	Virtual Output 20	Virtual Output20	Yes	Yes	Yes
692	PSL	DDB_GOOSEOUT_21	Virtual Output 21	Virtual Output21	Yes	Yes	Yes
693	PSL	DDB_GOOSEOUT_22	Virtual Output 22	Virtual Output22	Yes	Yes	Yes
694	PSL	DDB_GOOSEOUT_23	Virtual Output 23	Virtual Output23	Yes	Yes	Yes
695	PSL	DDB_GOOSEOUT_24	Virtual Output 24	Virtual Output24	Yes	Yes	Yes
696	PSL	DDB_GOOSEOUT_25	Virtual Output 25	Virtual Output25	Yes	Yes	Yes
697	PSL	DDB_GOOSEOUT_26	Virtual Output 26	Virtual Output26	Yes	Yes	Yes
698	PSL	DDB_GOOSEOUT_27	Virtual Output 27	Virtual Output27	Yes	Yes	Yes
699	PSL	DDB_GOOSEOUT_28	Virtual Output 28	Virtual Output28	Yes	Yes	Yes
700	PSL	DDB_GOOSEOUT_29	Virtual Output 29	Virtual Output29	Yes	Yes	Yes
701	PSL	DDB_GOOSEOUT_30	Virtual Output 30	Virtual Output30	Yes	Yes	Yes
702	PSL	DDB_GOOSEOUT_31	Virtual Output 31	Virtual Output31	Yes	Yes	Yes
703	PSL	DDB_GOOSEOUT_32	Virtual Output 32	Virtual Output32	Yes	Yes	Yes
704	SW	DDB_CT1_EXCLUDED	Exclude CT1 from the relay	CT1 Excluded		Yes	Yes
705	SW	DDB_CT2_EXCLUDED	Exclude CT2 from the relay	CT2 Excluded		Yes	Yes
706	SW	DDB_CT3_EXCLUDED	Exclude CT3 from the relay	CT3 Excluded		Yes	Yes
707	SW	DDB_CT4_EXCLUDED	Exclude CT4 from the relay	CT4 Excluded			Yes
708	SW	DDB_CT5_EXCLUDED	Exclude CT5 from the relay	CT5 Excluded	Yes	Yes	Yes
709	PSL	DDB_CM_SELECTOR_1X	Cooling Mode Select 1X	CM Select 1X	Yes	Yes	Yes
710	PSL	DDB_CM_SELECTOR_X1	Cooling Mode Selext X1	CM Select X1	Yes	Yes	Yes
711	PSL	DDB_SET_Z2_TEST_MODE	Enable Z2 Test Mode	Set Z2 Test Mode	Yes	Yes	Yes
712	PSL	DDB_INHIBIT_VPERHZ_1	BLK W1 VPERHZ>1	BLK W1 VPERHZ>1		Yes	Yes
713	PSL	DDB_INHIBIT_VPERHZ_2	BLK W2 VPERHZ>1	BLK W2 VPERHZ>1	Yes	Yes	Yes

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
714	PSL	DDB_CL_INPUT_1_BLOCK	Block Current Loop Input 1 protection	CL Input 1 Blk	Yes	Yes	Yes
715	PSL	DDB_CL_INPUT_2_BLOCK	Block Current Loop Input 2 protection	CL Input 2 Blk	Yes	Yes	Yes
716	PSL	DDB_CL_INPUT_3_BLOCK	Block Current Loop Input 3 protection	CL Input 3 Blk	Yes	Yes	Yes
717	PSL	DDB_CL_INPUT_4_BLOCK	Block Current Loop Input 4 protection	CL Input 4 Blk	Yes	Yes	Yes
718	PSL	DDB_CB1_AUX_3PH_ALARM	CB1 Alarm	CB1 Alarm	Yes	Yes	Yes
719	PSL	DDB_CB1_AUX_3PH_CLOSED	CB1 Closed	CB1 Closed	Yes	Yes	Yes
720	PSL	DDB_CB2_AUX_3PH_ALARM	CB2 Alarm	CB2 Alarm	Yes	Yes	Yes
721	PSL	DDB_CB2_AUX_3PH_CLOSED	CB2 Closed	CB2 Closed	Yes	Yes	Yes
722	PSL	DDB_CB3_AUX_3PH_ALARM	CB3 Alarm	CB3 Alarm		Yes	Yes
723	PSL	DDB_CB3_AUX_3PH_CLOSED	CB3 Closed	CB3 Closed		Yes	Yes
724	PSL	DDB_CB4_AUX_3PH_ALARM	CB4 Alarm	CB4 Alarm			Yes
725	PSL	DDB_CB4_AUX_3PH_CLOSED	CB4 Closed	CB4 Closed			Yes
726	PSL	DDB_CB5_AUX_3PH_ALARM	CB5 Alarm	CB5 Alarm			Yes
727	PSL	DDB_CB5_AUX_3PH_CLOSED	CB5 Closed	CB5 Closed			Yes
728	PSL	DDB_CB6_AUX_3PH_ALARM	CB6 Alarm	CB6 Alarm			
729	PSL	DDB_CB6_AUX_3PH_CLOSED	CB6 Closed	CB6 Closed			
730	PSL	DDB_CB7_AUX_3PH_ALARM	CB7 Alarm	CB7 Alarm			
731	PSL	DDB_CB7_AUX_3PH_CLOSED	CB7 Closed	CB7 Closed			
732	PSL	DDB_CB8_AUX_3PH_ALARM	CB8 Alarm	CB8 Alarm			
733	PSL	DDB_CB8_AUX_3PH_CLOSED	CB8 Closed	CB8 Closed			
734	PSL	DDB_CB9_AUX_3PH_ALARM	CB9 Alarm	CB9 Alarm			
735	PSL	DDB_CB9_AUX_3PH_CLOSED	CB9 Closed	CB9 Closed			
736	PSL	DDB_CT_EXCLUSION_ENABLED	CT Exclusion Enabled	CT Exclu Ena		Yes	Yes
737	PSL	DDB_CT1_EXCLUSION_ENABLED	CT1 Exclusion Enabled	CT1 Exclu Ena		Yes	Yes
738	PSL	DDB_CT2_EXCLUSION_ENABLED	CT2 Exclusion Enabled	CT2 Exclu Ena		Yes	Yes
739	PSL	DDB_CT3_EXCLUSION_ENABLED	CT3 Exclusion Enabled	CT3 Exclu Ena		Yes	Yes
740	PSL	DDB_CT4_EXCLUSION_ENABLED	CT4 Exclusion Enabled	CT4 Exclu Ena			Yes
741	PSL	DDB_CT5_EXCLUSION_ENABLED	CT5 Exclusion Enabled	CT5 Exclu Ena			Yes
742	SW	DDB_CT_SATURATION_A	CT Saturation Flag of Phase A	CT Saturation A	Yes	Yes	Yes
743	SW	DDB_CT_SATURATION_B	CT Saturation Flag of Phase B	CT Saturation B	Yes	Yes	Yes
744	SW	DDB_CT_SATURATION_C	CT Saturation Flag of Phase C	CT Saturation C	Yes	Yes	Yes
745	SW	DDB_MAX_OVER_A	maximum value of phase A is more than positive limitation	MAX_OVER_A	Yes	Yes	Yes
746	SW	DDB_MAX_OVER_B	maximum value of phase B is more than positive limitation	MAX_OVER_B	Yes	Yes	Yes
747	SW	DDB_MAX_OVER_C	maximum value of phase C is more than positive limitation	MAX_OVER_C	Yes	Yes	Yes
748	SW	DDB_MIN_UNDER_A	minimum value of phase A is less than negative limitation	MIN_UNDER_A	Yes	Yes	Yes
749	SW	DDB_MIN_UNDER_B	minimum value of phase B is less than negative limitation	MIN_UNDER_B	Yes	Yes	Yes
750	SW	DDB_MIN_UNDER_C	minimum value of phase C is less than negative limitation	MIN_UNDER_C	Yes	Yes	Yes
751	SW	DDB_SEG_VALID_A	the width of detected segment of phase A is valid	SEG_VALID_A	Yes	Yes	Yes

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
752	SW	DDB_SEG_VALID_B	the width of detected segment of phase B is valid	SEG_VALID_B	Yes	Yes	Yes
753	SW	DDB_SEG_VALID_C	the width of detected segment of phase C is valid	SEG_VALID_C	Yes	Yes	Yes
754	SW	DDB_1_MAX_DEL3_A	the maximum 3rd difference of 1st half locates at the first 3 points	1_MAX_DEL3_A	Yes	Yes	Yes
755	SW	DDB_1_MAX_DEL3_B	the maximum 3rd difference of 1st half locates at the first 3 points	1_MAX_DEL3_B	Yes	Yes	Yes
756	SW	DDB_1_MAX_DEL3_C	the maximum 3rd difference of 1st half locates at the first 3 points	1_MAX_DEL3_C	Yes	Yes	Yes
757	SW	DDB_MAX_DEL1_A	the maximum 1st difference locates at the first 3 points	MAX_DEL1_A	Yes	Yes	Yes
758	SW	DDB_MAX_DEL1_B	the maximum 1st difference locates at the first 3 points	MAX_DEL1_B	Yes	Yes	Yes
759	SW	DDB_MAX_DEL1_C	the maximum 1st difference locates at the first 3 points	MAX_DEL1_C	Yes	Yes	Yes
760	SW	DDB_MAX_DEL3_OVER_THRES_A	maximum 3rd difference exceeds threshold	DEL3 > Thres A	Yes	Yes	Yes
761	SW	DDB_MAX_DEL3_OVER_THRES_B	maximum 3rd difference exceeds threshold	DEL3 > Thres B	Yes	Yes	Yes
762	SW	DDB_MAX_DEL3_OVER_THRES_C	maximum 3rd difference exceeds threshold	DEL3 > Thres C	Yes	Yes	Yes
763	SW	DDB_1_OVER_2K_MAXDEL3_A	the 1st of maximum 3rd difference is greater than k times of 2nd one	1>2K DEL3 A	Yes	Yes	Yes
764	SW	DDB_1_OVER_2K_MAXDEL3_B	the 1st of maximum 3rd difference is greater than k times of 2nd one	1>2K DEL3 B	Yes	Yes	Yes
765	SW	DDB_1_OVER_2K_MAXDEL3_C	the 1st of maximum 3rd difference is greater than k times of 2nd one	1>2K DEL3 C	Yes	Yes	Yes
766	SW	DDB_UNUSED	DDB_UNUSED				
767	SW	DDB_UNUSED	DDB_UNUSED				
768	PSL	DDB_USER_ALARM_1	User Alarm 1	User Alarm 1	Yes	Yes	Yes
769	PSL	DDB_USER_ALARM_2	User Alarm 2	User Alarm 2	Yes	Yes	Yes
770	PSL	DDB_USER_ALARM_3	User Alarm 3	User Alarm 3	Yes	Yes	Yes
771	PSL	DDB_USER_ALARM_4	User Alarm 4	User Alarm 4	Yes	Yes	Yes
772	PSL	DDB_USER_ALARM_5	User Alarm 5	User Alarm 5	Yes	Yes	Yes
773	PSL	DDB_USER_ALARM_6	User Alarm 6	User Alarm 6	Yes	Yes	Yes
774	PSL	DDB_USER_ALARM_7	User Alarm 7	User Alarm 7	Yes	Yes	Yes
775	PSL	DDB_USER_ALARM_8	User Alarm 8	User Alarm 8	Yes	Yes	Yes
776	PSL	DDB_USER_ALARM_9	User Alarm 9	User Alarm 9	Yes	Yes	Yes
777	PSL	DDB_USER_ALARM_10	User Alarm 10	User Alarm 10	Yes	Yes	Yes
778	PSL	DDB_USER_ALARM_11	User Alarm 11	User Alarm 11	Yes	Yes	Yes
779	PSL	DDB_USER_ALARM_12	User Alarm 12	User Alarm 12	Yes	Yes	Yes
780	PSL	DDB_USER_ALARM_13	User Alarm 13	User Alarm 13	Yes	Yes	Yes
781	PSL	DDB_USER_ALARM_14	User Alarm 14	User Alarm 14	Yes	Yes	Yes
782	PSL	DDB_USER_ALARM_15	User Alarm 15	User Alarm 15	Yes	Yes	Yes
783	PSL	DDB_USER_ALARM_16	User Alarm 16	User Alarm 16	Yes	Yes	Yes
784	PSL	DDB_USER_ALARM_17	User Alarm 17	User Alarm 17	Yes	Yes	Yes
785	PSL	DDB_USER_ALARM_18	User Alarm 18	User Alarm 18	Yes	Yes	Yes

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
786	PSL	DDB_USER_ALARM_19	User Alarm 19	User Alarm 19	Yes	Yes	Yes
787	PSL	DDB_USER_ALARM_20	User Alarm 20	User Alarm 20	Yes	Yes	Yes
788	PSL	DDB_USER_ALARM_21	User Alarm 21	User Alarm 21	Yes	Yes	Yes
789	PSL	DDB_USER_ALARM_22	User Alarm 22	User Alarm 22	Yes	Yes	Yes
790	PSL	DDB_USER_ALARM_23	User Alarm 23	User Alarm 23	Yes	Yes	Yes
791	PSL	DDB_USER_ALARM_24	User Alarm 24	User Alarm 24	Yes	Yes	Yes
792	PSL	DDB_USER_ALARM_25	User Alarm 25	User Alarm 25	Yes	Yes	Yes
793	PSL	DDB_USER_ALARM_26	User Alarm 26	User Alarm 26	Yes	Yes	Yes
794	PSL	DDB_USER_ALARM_27	User Alarm 27	User Alarm 27	Yes	Yes	Yes
795	PSL	DDB_USER_ALARM_28	User Alarm 28	User Alarm 28	Yes	Yes	Yes
796	PSL	DDB_USER_ALARM_29	User Alarm 29	User Alarm 29	Yes	Yes	Yes
797	PSL	DDB_USER_ALARM_30	User Alarm 30	User Alarm 30	Yes	Yes	Yes
798	PSL	DDB_USER_ALARM_31	User Alarm 31	User Alarm 31	Yes	Yes	Yes
799	PSL	DDB_USER_ALARM_32	User Alarm 32	User Alarm 32	Yes	Yes	Yes
800	FL	DDB_USER_ALARM_INPUT_1	User Alarm in 1	User Alarm in 1	Yes	Yes	Yes
801	FL	DDB_USER_ALARM_INPUT_2	User Alarm in 2	User Alarm in 2	Yes	Yes	Yes
802	FL	DDB_USER_ALARM_INPUT_3	User Alarm in 3	User Alarm in 3	Yes	Yes	Yes
803	FL	DDB_USER_ALARM_INPUT_4	User Alarm in 4	User Alarm in 4	Yes	Yes	Yes
804	FL	DDB_USER_ALARM_INPUT_5	User Alarm in 5	User Alarm in 5	Yes	Yes	Yes
805	FL	DDB_USER_ALARM_INPUT_6	User Alarm in 6	User Alarm in 6	Yes	Yes	Yes
806	FL	DDB_USER_ALARM_INPUT_7	User Alarm in 7	User Alarm in 7	Yes	Yes	Yes
807	FL	DDB_USER_ALARM_INPUT_8	User Alarm in 8	User Alarm in 8	Yes	Yes	Yes
808	FL	DDB_USER_ALARM_INPUT_9	User Alarm in 9	User Alarm in 9	Yes	Yes	Yes
809	FL	DDB_USER_ALARM_INPUT_10	User Alarm in 10	User Alarm in 10	Yes	Yes	Yes
810	FL	DDB_USER_ALARM_INPUT_11	User Alarm in 11	User Alarm in 11	Yes	Yes	Yes
811	FL	DDB_USER_ALARM_INPUT_12	User Alarm in 12	User Alarm in 12	Yes	Yes	Yes
812	FL	DDB_USER_ALARM_INPUT_13	User Alarm in 13	User Alarm in 13	Yes	Yes	Yes
813	FL	DDB_USER_ALARM_INPUT_14	User Alarm in 14	User Alarm in 14	Yes	Yes	Yes
814	FL	DDB_USER_ALARM_INPUT_15	User Alarm in 15	User Alarm in 15	Yes	Yes	Yes
815	FL	DDB_USER_ALARM_INPUT_16	User Alarm in 16	User Alarm in 16	Yes	Yes	Yes
816	FL	DDB_USER_ALARM_INPUT_17	User Alarm in 17	User Alarm in 17	Yes	Yes	Yes
817	FL	DDB_USER_ALARM_INPUT_18	User Alarm in 18	User Alarm in 18	Yes	Yes	Yes
818	FL	DDB_USER_ALARM_INPUT_19	User Alarm in 19	User Alarm in 19	Yes	Yes	Yes
819	FL	DDB_USER_ALARM_INPUT_20	User Alarm in 20	User Alarm in 20	Yes	Yes	Yes
820	FL	DDB_USER_ALARM_INPUT_21	User Alarm in 21	User Alarm in 21	Yes	Yes	Yes
821	FL	DDB_USER_ALARM_INPUT_22	User Alarm in 22	User Alarm in 22	Yes	Yes	Yes
822	FL	DDB_USER_ALARM_INPUT_23	User Alarm in 23	User Alarm in 23	Yes	Yes	Yes
823	FL	DDB_USER_ALARM_INPUT_24	User Alarm in 24	User Alarm in 24	Yes	Yes	Yes
824	FL	DDB_USER_ALARM_INPUT_25	User Alarm in 25	User Alarm in 25	Yes	Yes	Yes
825	FL	DDB_USER_ALARM_INPUT_26	User Alarm in 26	User Alarm in 26	Yes	Yes	Yes
826	FL	DDB_USER_ALARM_INPUT_27	User Alarm in 27	User Alarm in 27	Yes	Yes	Yes
827	FL	DDB_USER_ALARM_INPUT_28	User Alarm in 28	User Alarm in 28	Yes	Yes	Yes
828	FL	DDB_USER_ALARM_INPUT_29	User Alarm in 29	User Alarm in 29	Yes	Yes	Yes
829	FL	DDB_USER_ALARM_INPUT_30	User Alarm in 30	User Alarm in 30	Yes	Yes	Yes

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
830	FL	DDB_USER_ALARM_INPUT_31	User Alarm in 31	User Alarm in 31	Yes	Yes	Yes
831	FL	DDB_USER_ALARM_INPUT_32	User Alarm in 32	User Alarm in 32	Yes	Yes	Yes
832	PSL	DDB_RP1_READ_ONLY	Remote Read Only 1 DDB	RP1 Read Only	Yes	Yes	Yes
833	PSL	DDB_RP2_READ_ONLY	Remote Read Only 2 DDB	RP2 Read Only	Yes	Yes	Yes
834	PSL	DDB_NIC_READ_ONLY	Remote Read Only NIC DDB	NIC Read Only	Yes	Yes	Yes
835	PSL	DDB_MONITOR_BLOCKING	Monitor Block	103 MonitorBlock	Yes	Yes	Yes
836	PSL	DDB_COMMAND_BLOCKING	Command Block	103 CommandBlock	Yes	Yes	Yes
837	SW	DDB_UNUSED	DDB_UNUSED				
838	PSL	DDB_UNUSED_DR	Unused	Unused	Yes	Yes	Yes
839	SW	DDB_DIFF_EXTERNAL_FAULT_A	transformer Diff check zone		Yes	Yes	Yes
840	SW	DDB_DIFF_EXTERNAL_FAULT_B	transformer Diff check zone		Yes	Yes	Yes
841	SW	DDB_DIFF_EXTERNAL_FAULT_C	transformer Diff check zone		Yes	Yes	Yes
842	SW	DDB_CIR_FLT_C_CZ	CZ Phase C Circuity Flt	CZ Phase C Circuity Flt			
843	SW	DDB_CIR_FLT_Z1	Z1 Circuity Flt	Z1 Circuity Flt	Yes	Yes	Yes
844	SW	DDB_CIR_FLT_Z2	Z2 Circuity Flt	Z2 Circuity Flt	Yes	Yes	Yes
845	SW	DDB_CIR_FLT_A	Phase A Circuity Flt	Phase A Circuity Flt	Yes	Yes	Yes
846	SW	DDB_CIR_FLT_B	Phase B Circuity Flt	Phase B Circuity Flt	Yes	Yes	Yes
847	SW	DDB_CIR_FLT_C	Phase C Circuity Flt	Phase C Circuity Flt	Yes	Yes	Yes
848	SW	DDB_CIR_FLT_CZ	CZ Circuity Flt	CZ Circuity Flt	Yes	Yes	Yes
849	PSL	DDB_INHIBIT_NPSOC1	Inhibit Negative Sequence overcurrent 1	Inhibit NPSOC 1	Yes	Yes	Yes
850	PSL	DDB_NPSOC1_STAGE1_TIMER_BLOCK	Negative Sequence Overcurrent 1 I2>1 Timer Block	NOC 1 I2>1 TBlk	Yes	Yes	Yes
851	PSL	DDB_NPSOC1_STAGE2_TIMER_BLOCK	Negative Sequence Overcurrent 1 I2>2 Timer Block	NOC 1 I2>2 TBlk	Yes	Yes	Yes
852	PSL	DDB_NPSOC1_STAGE3_TIMER_BLOCK	Negative Sequence Overcurrent 1 I2>3 Timer Block	NOC 1 I2>3 TBlk	Yes	Yes	Yes
853	PSL	DDB_NPSOC1_STAGE4_TIMER_BLOCK	Negative Sequence Overcurrent 1 I2>4 Timer Block	NOC 1 I2>4 TBlk	Yes	Yes	Yes
854	PSL	DDB_INHIBIT_NPSOC2	Inhibit Negative Sequence overcurrent 2	Inhibit NPSOC 2	Yes	Yes	Yes
855	PSL	DDB_NPSOC2_STAGE1_TIMER_BLOCK	Negative Sequence Overcurrent 2 I2>1 Timer Block	NOC 2 I2>1 TBlk	Yes	Yes	Yes
856	PSL	DDB_NPSOC2_STAGE2_TIMER_BLOCK	Negative Sequence Overcurrent 2 I2>2 Timer Block	NOC 2 I2>2 TBlk	Yes	Yes	Yes
857	PSL	DDB_NPSOC2_STAGE3_TIMER_BLOCK	Negative Sequence Overcurrent 2 I2>3 Timer Block	NOC 2 I2>3 TBlk	Yes	Yes	Yes
858	PSL	DDB_NPSOC2_STAGE4_TIMER_BLOCK	Negative Sequence Overcurrent 2 I2>4 Timer Block	NOC 2 I2>4 TBlk	Yes	Yes	Yes
859	PSL	DDB_INHIBIT_NPSOC3	Inhibit Negative Sequence overcurrent 3	Inhibit NPSOC 3		Yes	Yes
860	PSL	DDB_NPSOC3_STAGE1_TIMER_BLOCK	Negative Sequence Overcurrent 3 I2>1 Timer Block	NOC 3 I2>1 TBlk		Yes	Yes
861	PSL	DDB_NPSOC3_STAGE2_TIMER_BLOCK	Negative Sequence Overcurrent 3 I2>2 Timer Block	NOC 3 I2>2 TBlk		Yes	Yes
862	PSL	DDB_NPSOC3_STAGE3_TIMER_BLOCK	Negative Sequence Overcurrent 3 I2>3 Timer Block	NOC 3 I2>3 TBlk		Yes	Yes

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
863	PSL	DDB_NPSOC3_STAGE4_TIMER_BLOCK	Negative Sequence Overcurrent 3 I2>4 Timer Block	NOC 3 I2>4 TBlk		Yes	Yes
864	SW	DDB_MONITOR_PORT_1	Monitor Port 1	Commissioning Test	Yes	Yes	Yes
865	SW	DDB_MONITOR_PORT_2	Monitor Port 2	Commissioning Test	Yes	Yes	Yes
866	SW	DDB_MONITOR_PORT_3	Monitor Port 3	Commissioning Test	Yes	Yes	Yes
867	SW	DDB_MONITOR_PORT_4	Monitor Port 4	Commissioning Test	Yes	Yes	Yes
868	SW	DDB_MONITOR_PORT_5	Monitor Port 5	Commissioning Test	Yes	Yes	Yes
869	SW	DDB_MONITOR_PORT_6	Monitor Port 6	Commissioning Test	Yes	Yes	Yes
870	SW	DDB_MONITOR_PORT_7	Monitor Port 7	Commissioning Test	Yes	Yes	Yes
871	SW	DDB_MONITOR_PORT_8	Monitor Port 8	Commissioning Test	Yes	Yes	Yes
872	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
873	PSL	DDB_UNUSED	DDB_UNUSED	DDB_UNUSED			
874	PSL	DDB_VTS_MCB_OPTO	MCB/VTS opto	MCB/VTS	Yes	Yes	Yes
875	PSL	DDB_UNUSED	DDB_UNUSED	DDB_UNUSED			
876	PSL	DDB_RESET_RELAYS_LEDS	Reset Latched Relays & LED's	Reset Relays/LED	Yes	Yes	Yes
877	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
878	PSL	DDB_TFR_DE_ENERGISED	Transformer De-energised Status	TFR De-energised	Yes	Yes	Yes
879	PSL	DDB_CS103_BLOCK	IEC60870-5-103 Monitor Blocking	Monitor Blocked	Yes	Yes	Yes
880	PSL	DDB_CS103_CMD_BLOCK	IEC60870-5-103 Command Blocking	Command Blocked	Yes	Yes	Yes
881	PSL	DDB_TIME_SYNCH	Time synchronise to nearest minute on 0-1 change	Time Synch	Yes	Yes	Yes
882	PSL	DDB_TEST_MODE	Initiate Test Mode	Test Mode	Yes	Yes	Yes
883	PSL	DDB_FAULT_RECORDER_START	Fault Record Trigger Input	Fault REC TRIG	Yes	Yes	Yes
884	PSL	DDB_SG_SELECTOR_X1	Setting Group Selector x1 (bit 0)	SG Select x1	Yes	Yes	Yes
885	PSL	DDB_SG_SELECTOR_1X	Setting Group Selector 1x (bit 1)	SG Select 1x	Yes	Yes	Yes
886	PSL	DDB_ANY_TRIP	Any Trip	Any Trip	Yes	Yes	Yes
886	FL	DDB_ANY_TRIP	Any Trip	Any Trip			
887	PSL	DDB_RESET_LOL	Rest Lost of life	Reset LOL	Yes	Yes	Yes
888	PSL	DDB_RESET_THERMAL	Rest Thermal Overload	Reset Thermal	Yes	Yes	Yes
889	PSL	DDB_RESET_VPERHZ_1	W1 Rest V/Hz	W1 Reset V/Hz	Yes	Yes	Yes
890	PSL	DDB_RESET_VPERHZ_2	W2 Rest V/Hz	W2 Reset V/Hz	Yes	Yes	Yes
891	FL	DDB_TRIP_INITIAL	Trip Initial (same as Any trip)	Trip Initial	Yes	Yes	Yes
892	PSL	DDB_RESET_CIR_FLT	Reset Circuitry fault	Reset CcT Fail	Yes	Yes	Yes
893	FL	DDB_FAULT_A	Phase A Fault	Phase A Fault	Yes	Yes	Yes
894	FL	DDB_FAULT_B	Phase B Fault	Phase B Fault	Yes	Yes	Yes
895	FL	DDB_FAULT_C	Phase C Fault	Phase C Fault	Yes	Yes	Yes
896	FL	DDB_FAULT_N	Earth Fault	Fault N	Yes	Yes	Yes
897	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
898	SW	DDB_Z2_BUS_CB_TRIP	Z2 BusCB Trip	Z2 BusCB Trp			
899	SW	DDB_IDIFF_TRIPA	Idiff Trip A	Idiff Trip A	Yes	Yes	Yes
900	SW	DDB_IDIFF_TRIPB	Idiff Trip B	Idiff Trip B	Yes	Yes	Yes
901	SW	DDB_IDIFF_TRIPC	Idiff Trip C	Idiff Trip C	Yes	Yes	Yes
902	SW	DDB_IDIFF_TRIP	Idiff Trip	Idiff Trip	Yes	Yes	Yes
903	SW	DDB_IDIFF_HS1_TRIPA	Idiff HS1 Trip A	Idiff HS1 Trip A	Yes	Yes	Yes

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
903	SW	DDB_BUS_IDIFF_TRIPA_Z1	Z1 Diff Phase A Trip	Z1 Diff Phase A Trip			
904	SW	DDB_IDIFF_HS1_TRIPB	Idiff HS1 Trip B	Idiff HS1 Trip B	Yes	Yes	Yes
904	SW	DDB_BUS_IDIFF_TRIPB_Z1	Z1 Diff Phase B Trip	Z1 Diff Phase B Trip			
905	SW	DDB_IDIFF_HS1_TRIPC	Idiff HS1 Trip C	Idiff HS1 Trip C	Yes	Yes	Yes
905	SW	DDB_BUS_IDIFF_TRIPC_Z1	Z1 Diff Phase C Trip	Z1 Diff Phase C Trip			
906	SW	DDB_IDIFF_HS2_TRIPA	Idiff HS2 Trip A	Idiff HS2 Trip A	Yes	Yes	Yes
906	SW	DDB_BUS_IDIFF_TRIPA_Z2	Z2 Diff Phase A Trip	Z2 Diff Phase A Trip			
907	SW	DDB_IDIFF_HS2_TRIPB	Idiff HS2 Trip B	Idiff HS2 Trip B	Yes	Yes	Yes
907	SW	DDB_BUS_IDIFF_TRIPB_Z2	Z2 Diff Phase B Trip	Z2 Diff Phase B Trip			
908	SW	DDB_IDIFF_HS2_TRIPC	Idiff HS2 Trip C	Idiff HS2 Trip C	Yes	Yes	Yes
908	SW	DDB_BUS_IDIFF_TRIPC_Z2	Z2 Diff Phase C Trip	Z2 Diff Phase C Trip			
909	SW	DDB_IDIFF_BIAS_TRIPA	Id Bias Trip A	Id Bias Trip A	Yes	Yes	Yes
909	SW	DDB_Z1_BUS_CB_TRIP	Z1 BusCB Trip	Z1 BusCB Trp			
910	SW	DDB_IDIFF_BIAS_TRIPB	Id Bias Trip B	Id Bias Trip B	Yes	Yes	Yes
911	SW	DDB_IDIFF_BIAS_TRIPC	Id Bias Trip C	Id Bias Trip C	Yes	Yes	Yes
912	SW	DDB_NO_GAP_A	No Gap in the last cycle of phase A	No Gap A	Yes	Yes	Yes
913	SW	DDB_NO_GAP_B	No Gap in the last cycle of phase B	No Gap B	Yes	Yes	Yes
914	SW	DDB_NO_GAP_C	No Gap in the last cycle of phase C	No Gap C	Yes	Yes	Yes
915	SW	DDB_BUS_ZONE_TRIP_T1	Zone Trip T1 by Diff Trip or CBF Back Zone Trip or External Zone Trip	Zone Trip T1 by Diff Trip or CBF Back Zone Trip or External Zone Trip			
916	SW	DDB_BUS_ZONE_TRIP_T2	Zone Trip T2 by Diff Trip or CBF Back Zone Trip or External Zone Trip	Zone Trip T2 by Diff Trip or CBF Back Zone Trip or External Zone Trip			
917	SW	DDB_BUS_ZONE_TRIP_T3	Zone Trip T3 by Diff Trip or CBF Back Zone Trip or External Zone Trip	Zone Trip T3 by Diff Trip or CBF Back Zone Trip or External Zone Trip			
918	SW	DDB_BUS_ZONE_TRIP_T4	Zone Trip T4 by Diff Trip or CBF Back Zone Trip or External Zone Trip	Zone Trip T4 by Diff Trip or CBF Back Zone Trip or External Zone Trip			
919	SW	DDB_BUS_ZONE_TRIP_T5	Zone Trip T5 by Diff Trip or CBF Back Zone Trip or External Zone Trip	Zone Trip T5 by Diff Trip or CBF Back Zone Trip or External Zone Trip			
920	SW	DDB_BUS_ZONE_TRIP_T6	Zone Trip T6 by Diff Trip or CBF Back Zone Trip or External Zone Trip	Zone Trip T6 by Diff Trip or CBF Back Zone Trip or External Zone Trip			
921	SW	DDB_BUS_ZONE_TRIP_T7	Zone Trip T7 by Diff Trip or CBF Back Zone Trip or External Zone Trip	Zone Trip T7 by Diff Trip or CBF Back Zone Trip or External Zone Trip			
922	SW	DDB_BUS_ZONE_TRIP_T8	Zone Trip T8 by Diff Trip or CBF Back Zone Trip or External Zone Trip	Zone Trip T8 by Diff Trip or CBF Back Zone Trip or External Zone Trip			

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
923	SW	DDB_BUS_ZONE_TRIP_T9	Zone Trip T9 by Diff Trip or CBF Back Zone Trip or External Zone Trip	Zone Trip T9 by Diff Trip or CBF Back Zone Trip or External Zone Trip			
924	SW	DDB_BUS_ZONE_TRIP_T10	Zone Trip T10 by Diff Trip or CBF Back Zone Trip or External Zone Trip	Zone Trip T10 by Diff Trip or CBF Back Zone Trip or External Zone Trip			
925	SW	DDB_BUS_ZONE_TRIP_T11	Zone Trip T11 by Diff Trip or CBF Back Zone Trip or External Zone Trip	Zone Trip T11 by Diff Trip or CBF Back Zone Trip or External Zone Trip			
926	SW	DDB_BUS_ZONE_TRIP_T12	Zone Trip T12 by Diff Trip or CBF Back Zone Trip or External Zone Trip	Zone Trip T12 by Diff Trip or CBF Back Zone Trip or External Zone Trip			
927	SW	DDB_BUS_ZONE_TRIP_T13	Zone Trip T13 by Diff Trip or CBF Back Zone Trip or External Zone Trip	Zone Trip T13 by Diff Trip or CBF Back Zone Trip or External Zone Trip			
928	SW	DDB_BUS_ZONE_TRIP_T14	Zone Trip T14 by Diff Trip or CBF Back Zone Trip or External Zone Trip	Zone Trip T14 by Diff Trip or CBF Back Zone Trip or External Zone Trip			
929	SW	DDB_BUS_ZONE_TRIP_T15	Zone Trip T15 by Diff Trip or CBF Back Zone Trip or External Zone Trip	Zone Trip T15 by Diff Trip or CBF Back Zone Trip or External Zone Trip			
930	SW	DDB_BUS_ZONE_TRIP_T16	Zone Trip T16 by Diff Trip or CBF Back Zone Trip or External Zone Trip	Zone Trip T16 by Diff Trip or CBF Back Zone Trip or External Zone Trip			
931	SW	DDB_BUS_ZONE_TRIP_T17	Zone Trip T17 by Diff Trip or CBF Back Zone Trip or External Zone Trip	Zone Trip T17 by Diff Trip or CBF Back Zone Trip or External Zone Trip			
932	SW	DDB_BUS_ZONE_TRIP_T18	Zone Trip T18 by Diff Trip or CBF Back Zone Trip or External Zone Trip	Zone Trip T18 by Diff Trip or CBF Back Zone Trip or External Zone Trip			
933	SW	DDB_DZ1_OC_3PH_TRIP	T1 DeadZone Trip	T1 DeadZone Trip			
934	SW	DDB_DZ2_OC_3PH_TRIP	T2 DeadZone Trip	T2 DeadZone Trip			
935	SW	DDB_DZ3_OC_3PH_TRIP	T3 DeadZone Trip	T3 DeadZone Trip			
936	SW	DDB_DZ4_OC_3PH_TRIP	T4 DeadZone Trip	T4 DeadZone Trip			
937	SW	DDB_DZ5_OC_3PH_TRIP	T5 DeadZone Trip	T5 DeadZone Trip			
938	SW	DDB_DZ6_OC_3PH_TRIP	T6 DeadZone Trip	T6 DeadZone Trip			
939	SW	DDB_DZ7_OC_3PH_TRIP	T7 DeadZone Trip	T7 DeadZone Trip			
940	SW	DDB_DZ8_OC_3PH_TRIP	T8 DeadZone Trip	T8 DeadZone Trip			
941	SW	DDB_DZ9_OC_3PH_TRIP	T9 DeadZone Trip	T9 DeadZone Trip			
942	SW	DDB_DZ10_OC_3PH_TRIP	T10 DeadZone Trip	T10 DeadZone Trip			
943	SW	DDB_DZ11_OC_3PH_TRIP	T11 DeadZone Trip	T11 DeadZone Trip			
944	SW	DDB_DZ12_OC_3PH_TRIP	T12 DeadZone Trip	T12 DeadZone Trip			
945	SW	DDB_DZ13_OC_3PH_TRIP	T13 DeadZone Trip	T13 DeadZone Trip			

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
946	SW	DDB_DZ14_OC_3PH_TRIP	T14 DeadZone Trip	T14 DeadZone Trip			
947	SW	DDB_DZ15_OC_3PH_TRIP	T15 DeadZone Trip	T15 DeadZone Trip			
948	SW	DDB_DZ16_OC_3PH_TRIP	T16 DeadZone Trip	T16 DeadZone Trip			
949	SW	DDB_DZ17_OC_3PH_TRIP	T17 DeadZone Trip	T17 DeadZone Trip			
950	SW	DDB_REF_TRIP_HV	REF Trip HV	REF Trip HV	Yes	Yes	Yes
951	SW	DDB_REF_TRIP_LV	REF Trip LV	REF Trip LV	Yes	Yes	Yes
952	SW	DDB_REF_TRIP_TV	REF Trip TV	REF Trip TV		Yes	Yes
953	SW	DDB_REF_TRIP_AUTO	REF Trip Auto	REF Trip Auto	Yes	Yes	Yes
954	SW	DDB_HOT_SPOT_1_TRIP	Hot Spot T>1 Trip	Hot Spot >1 Trip	Yes	Yes	Yes
955	SW	DDB_HOT_SPOT_2_TRIP	Hot Spot T>2 Trip	Hot Spot >2 Trip	Yes	Yes	Yes
956	SW	DDB_HOT_SPOT_3_TRIP	Hot Spot T>3 Trip	Hot Spot >3 Trip	Yes	Yes	Yes
957	SW	DDB_TOP_OIL_1_TRIP	Top Oil T>1 Trip	Top Oil >1 Trip	Yes	Yes	Yes
958	SW	DDB_TOP_OIL_2_TRIP	Top Oil T>2 Trip	Top Oil >2 Trip	Yes	Yes	Yes
959	SW	DDB_TOP_OIL_3_TRIP	Top Oil T>3 Trip	Top Oil >3 Trip	Yes	Yes	Yes
960	SW	DDB_POC1_STAGE1_3PH_TRIP	Phase Overcurrent 1 I>1 Trip	POC 1 I>1 Trip	Yes	Yes	Yes
961	SW	DDB_POC1_STAGE1_PH_A_TRIP	Phase Overcurrent 1 I>1 Trip A	POC 1 I>1 Trip A	Yes	Yes	Yes
962	SW	DDB_POC1_STAGE1_PH_B_TRIP	Phase Overcurrent 1 I>1 Trip B	POC 1 I>1 Trip B	Yes	Yes	Yes
963	SW	DDB_POC1_STAGE1_PH_C_TRIP	Phase Overcurrent 1 I>1 Trip C	POC 1 I>1 Trip C	Yes	Yes	Yes
964	SW	DDB_POC1_STAGE2_3PH_TRIP	Phase Overcurrent 1 I>2 Trip	POC 1 I>2 Trip	Yes	Yes	Yes
965	SW	DDB_POC1_STAGE2_PH_A_TRIP	Phase Overcurrent 1 I>2 Trip A	POC 1 I>2 Trip A	Yes	Yes	Yes
966	SW	DDB_POC1_STAGE2_PH_B_TRIP	Phase Overcurrent 1 I>2 Trip B	POC 1 I>2 Trip B	Yes	Yes	Yes
967	SW	DDB_POC1_STAGE2_PH_C_TRIP	Phase Overcurrent 1 I>2 Trip C	POC 1 I>2 Trip C	Yes	Yes	Yes
968	SW	DDB_POC1_STAGE3_3PH_TRIP	Phase Overcurrent 1 I>3 Trip	POC 1 I>3 Trip	Yes	Yes	Yes
969	SW	DDB_POC1_STAGE3_PH_A_TRIP	Phase Overcurrent 1 I>3 Trip A	POC 1 I>3 Trip A	Yes	Yes	Yes
970	SW	DDB_POC1_STAGE3_PH_B_TRIP	Phase Overcurrent 1 I>3 Trip B	POC 1 I>3 Trip B	Yes	Yes	Yes
971	SW	DDB_POC1_STAGE3_PH_C_TRIP	Phase Overcurrent 1 I>3 Trip C	POC 1 I>3 Trip C	Yes	Yes	Yes
972	SW	DDB_POC1_STAGE4_3PH_TRIP	Phase Overcurrent 1 I>4 Trip	POC 1 I>4 Trip	Yes	Yes	Yes
973	SW	DDB_POC1_STAGE4_PH_A_TRIP	Phase Overcurrent 1 I>4 Trip A	POC 1 I>4 Trip A	Yes	Yes	Yes
974	SW	DDB_POC1_STAGE4_PH_B_TRIP	Phase Overcurrent 1 I>4 Trip B	POC 1 I>4 Trip B	Yes	Yes	Yes
975	SW	DDB_POC1_STAGE4_PH_C_TRIP	Phase Overcurrent 1 I>4 Trip C	POC 1 I>4 Trip C	Yes	Yes	Yes
976	SW	DDB_POC2_STAGE1_3PH_TRIP	Phase Overcurrent 2 I>1 Trip	POC 2 I>1 Trip	Yes	Yes	Yes
977	SW	DDB_POC2_STAGE1_PH_A_TRIP	Phase Overcurrent 2 I>1 Trip A	POC 2 I>1 Trip A	Yes	Yes	Yes
978	SW	DDB_POC2_STAGE1_PH_B_TRIP	Phase Overcurrent 2 I>1 Trip B	POC 2 I>1 Trip B	Yes	Yes	Yes
979	SW	DDB_POC2_STAGE1_PH_C_TRIP	Phase Overcurrent 2 I>1 Trip C	POC 2 I>1 Trip C	Yes	Yes	Yes
980	SW	DDB_POC2_STAGE2_3PH_TRIP	Phase Overcurrent 2 I>2 Trip	POC 2 I>2 Trip	Yes	Yes	Yes
981	SW	DDB_POC2_STAGE2_PH_A_TRIP	Phase Overcurrent 2 I>2 Trip A	POC 2 I>2 Trip A	Yes	Yes	Yes
982	SW	DDB_POC2_STAGE2_PH_B_TRIP	Phase Overcurrent 2 I>2 Trip B	POC 2 I>2 Trip B	Yes	Yes	Yes
983	SW	DDB_POC2_STAGE2_PH_C_TRIP	Phase Overcurrent 2 I>2 Trip C	POC 2 I>2 Trip C	Yes	Yes	Yes
984	SW	DDB_POC2_STAGE3_3PH_TRIP	Phase Overcurrent 2 I>3 Trip	POC 2 I>3 Trip	Yes	Yes	Yes
985	SW	DDB_POC2_STAGE3_PH_A_TRIP	Phase Overcurrent 2 I>3 Trip A	POC 2 I>3 Trip A	Yes	Yes	Yes
986	SW	DDB_POC2_STAGE3_PH_B_TRIP	Phase Overcurrent 2 I>3 Trip B	POC 2 I>3 Trip B	Yes	Yes	Yes
987	SW	DDB_POC2_STAGE3_PH_C_TRIP	Phase Overcurrent 2 I>3 Trip C	POC 2 I>3 Trip C	Yes	Yes	Yes
988	SW	DDB_POC2_STAGE4_3PH_TRIP	Phase Overcurrent 2 I>4 Trip	POC 2 I>4 Trip	Yes	Yes	Yes
989	SW	DDB_POC2_STAGE4_PH_A_TRIP	Phase Overcurrent 2 I>4 Trip A	POC 2 I>4 Trip A	Yes	Yes	Yes

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
990	SW	DDB_POC2_STAGE4_PH_B_TRIP	Phase Overcurrent 2 I>4 Trip B	POC 2 I>4 Trip B	Yes	Yes	Yes
991	SW	DDB_POC2_STAGE4_PH_C_TRIP	Phase Overcurrent 2 I>4 Trip C	POC 2 I>4 Trip C	Yes	Yes	Yes
992	SW	DDB_POC3_STAGE1_3PH_TRIP	Phase Overcurrent 3 I>1 Trip	POC 3 I>1 Trip		Yes	Yes
993	SW	DDB_POC3_STAGE1_PH_A_TRIP	Phase Overcurrent 3 I>1 Trip A	POC 3 I>1 Trip A		Yes	Yes
994	SW	DDB_POC3_STAGE1_PH_B_TRIP	Phase Overcurrent 3 I>1 Trip B	POC 3 I>1 Trip B		Yes	Yes
995	SW	DDB_POC3_STAGE1_PH_C_TRIP	Phase Overcurrent 3 I>1 Trip C	POC 3 I>1 Trip C		Yes	Yes
996	SW	DDB_POC3_STAGE2_3PH_TRIP	Phase Overcurrent 3 I>2 Trip	POC 3 I>2 Trip		Yes	Yes
997	SW	DDB_POC3_STAGE2_PH_A_TRIP	Phase Overcurrent 3 I>2 Trip A	POC 3 I>2 Trip A		Yes	Yes
998	SW	DDB_POC3_STAGE2_PH_B_TRIP	Phase Overcurrent 3 I>2 Trip B	POC 3 I>2 Trip B		Yes	Yes
999	SW	DDB_POC3_STAGE2_PH_C_TRIP	Phase Overcurrent 3 I>2 Trip C	POC 3 I>2 Trip C		Yes	Yes
1000	SW	DDB_POC3_STAGE3_3PH_TRIP	Phase Overcurrent 3 I>3 Trip	POC 3 I>3 Trip		Yes	Yes
1001	SW	DDB_POC3_STAGE3_PH_A_TRIP	Phase Overcurrent 3 I>3 Trip A	POC 3 I>3 Trip A		Yes	Yes
1002	SW	DDB_POC3_STAGE3_PH_B_TRIP	Phase Overcurrent 3 I>3 Trip B	POC 3 I>3 Trip B		Yes	Yes
1003	SW	DDB_POC3_STAGE3_PH_C_TRIP	Phase Overcurrent 3 I>3 Trip C	POC 3 I>3 Trip C		Yes	Yes
1004	SW	DDB_POC3_STAGE4_3PH_TRIP	Phase Overcurrent 3 I>4 Trip	POC 3 I>4 Trip		Yes	Yes
1005	SW	DDB_POC3_STAGE4_PH_A_TRIP	Phase Overcurrent 3 I>4 Trip A	POC 3 I>4 Trip A		Yes	Yes
1006	SW	DDB_POC3_STAGE4_PH_B_TRIP	Phase Overcurrent 3 I>4 Trip B	POC 3 I>4 Trip B		Yes	Yes
1007	SW	DDB_POC3_STAGE4_PH_C_TRIP	Phase Overcurrent 3 I>4 Trip C	POC 3 I>4 Trip C		Yes	Yes
1008	SW	DDB_VCO_1_3PH_TRIP	VCO>1 Trip	VCO>1 Trip	Yes	Yes	Yes
1009	SW	DDB_VCO_1_PH_A_TRIP	VCO>1 Trip A	VCO>1 Trip A	Yes	Yes	Yes
1010	SW	DDB_VCO_1_PH_B_TRIP	VCO>1 Trip B	VCO>1 Trip B	Yes	Yes	Yes
1011	SW	DDB_VCO_1_PH_C_TRIP	VCO>1 Trip C	VCO>1 Trip C	Yes	Yes	Yes
1012	SW	DDB_VCO_2_3PH_TRIP	VCO>2 Trip	VCO>2 Trip	Yes	Yes	Yes
1013	SW	DDB_VCO_2_PH_A_TRIP	VCO>2 Trip A	VCO>2 Trip A	Yes	Yes	Yes
1014	SW	DDB_VCO_2_PH_B_TRIP	VCO>2 Trip B	VCO>2 Trip B	Yes	Yes	Yes
1015	SW	DDB_VCO_2_PH_C_TRIP	VCO>2 Trip C	VCO>2 Trip C	Yes	Yes	Yes
1016	SW	DDB_T5_POC_1_3PH_TRIP	T5 I>1 Trip	T5 I>1 Trip			
1017	SW	DDB_T5_POC_2_3PH_TRIP	T5 I>2 Trip	T5 I>2 Trip			
1018	SW	DDB_T6_POC_1_3PH_TRIP	T6 I>1 Trip	T6 I>1 Trip			
1019	SW	DDB_T6_POC_2_3PH_TRIP	T6 I>2 Trip	T6 I>2 Trip			
1020	SW	DDB_T7_POC_1_3PH_TRIP	T7 I>1 Trip	T7 I>1 Trip			
1021	SW	DDB_T7_POC_2_3PH_TRIP	T7 I>2 Trip	T7 I>2 Trip			
1022	SW	DDB_T8_POC_1_3PH_TRIP	T8 I>1 Trip	T8 I>1 Trip			
1023	SW	DDB_T8_POC_2_3PH_TRIP	T8 I>2 Trip	T8 I>2 Trip			
1024	SW	DDB_T9_POC_1_3PH_TRIP	T9 I>1 Trip	T9 I>1 Trip			
1025	SW	DDB_T9_POC_2_3PH_TRIP	T9 I>2 Trip	T9 I>2 Trip			
1026	SW	DDB_T10_POC_1_3PH_TRIP	T10 I>1 Trip	T10 I>1 Trip			
1027	SW	DDB_T10_POC_2_3PH_TRIP	T10 I>2 Trip	T10 I>2 Trip			
1028	SW	DDB_T11_POC_1_3PH_TRIP	T11 I>1 Trip	T11 I>1 Trip			
1029	SW	DDB_T11_POC_2_3PH_TRIP	T11 I>2 Trip	T11 I>2 Trip			
1030	SW	DDB_T12_POC_1_3PH_TRIP	T12 I>1 Trip	T12 I>1 Trip			
1031	SW	DDB_T12_POC_2_3PH_TRIP	T12 I>2 Trip	T12 I>2 Trip			
1032	SW	DDB_T13_POC_1_3PH_TRIP	T13 I>1 Trip	T13 I>1 Trip			
1033	SW	DDB_T13_POC_2_3PH_TRIP	T13 I>2 Trip	T13 I>2 Trip			

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
1034	SW	DDB_T14_POC_1_3PH_TRIP	T14 I>1 Trip	T14 I>1 Trip			
1035	SW	DDB_T14_POC_2_3PH_TRIP	T14 I>2 Trip	T14 I>2 Trip			
1036	SW	DDB_T15_POC_1_3PH_TRIP	T15 I>1 Trip	T15 I>1 Trip			
1037	SW	DDB_T15_POC_2_3PH_TRIP	T15 I>2 Trip	T15 I>2 Trip			
1038	SW	DDB_T16_POC_1_3PH_TRIP	T16 I>1 Trip	T16 I>1 Trip			
1039	SW	DDB_T16_POC_2_3PH_TRIP	T16 I>2 Trip	T16 I>2 Trip			
1040	SW	DDB_T17_POC_1_3PH_TRIP	T17 I>1 Trip	T17 I>1 Trip			
1041	SW	DDB_T17_POC_2_3PH_TRIP	T17 I>2 Trip	T17 I>2 Trip			
1042	SW	DDB_T18_POC_1_3PH_TRIP	T18 I>1 Trip	T18 I>1 Trip			
1043	SW	DDB_T18_POC_2_3PH_TRIP	T18 I>2 Trip	T18 I>2 Trip			
1044	SW	DDB_EF1_STAGE1_TRIP	Earth Fault 1 IN>1 Trip	EF 1 IN>1 Trip	Yes	Yes	Yes
1044	SW	DDB_T1_EF_1_TRIP	T1 IN>1 Trip	T1 IN>1 Trip			
1045	SW	DDB_EF1_STAGE2_TRIP	Earth Fault 1 IN>2 Trip	EF 1 IN>2 Trip	Yes	Yes	Yes
1045	SW	DDB_T1_EF_2_TRIP	T1 IN>2 Trip	T1 IN>2 Trip			
1046	SW	DDB_EF1_STAGE3_TRIP	Earth Fault 1 IN>3 Trip	EF 1 IN>3 Trip	Yes	Yes	Yes
1046	SW	DDB_T2_EF_1_TRIP	T2 IN>1 Trip	T2 IN>1 Trip			
1047	SW	DDB_EF1_STAGE4_TRIP	Earth Fault 1 IN>4 Trip	EF 1 IN>4 Trip	Yes	Yes	Yes
1047	SW	DDB_T2_EF_2_TRIP	T2 IN>2 Trip	T2 IN>2 Trip			
1048	SW	DDB_EF2_STAGE1_TRIP	Earth Fault 2 IN>1 Trip	EF 2 IN>1 Trip	Yes	Yes	Yes
1048	SW	DDB_T3_EF_1_TRIP	T3 IN>1 Trip	T3 IN>1 Trip			
1049	SW	DDB_EF2_STAGE2_TRIP	Earth Fault 2 IN>2 Trip	EF 2 IN>2 Trip	Yes	Yes	Yes
1049	SW	DDB_T3_EF_2_TRIP	T3 IN>2 Trip	T3 IN>2 Trip			
1050	SW	DDB_EF2_STAGE3_TRIP	Earth Fault 2 IN>3 Trip	EF 2 IN>3 Trip	Yes	Yes	Yes
1050	SW	DDB_T4_EF_1_TRIP	T4 IN>1 Trip	T4 IN>1 Trip			
1051	SW	DDB_EF2_STAGE4_TRIP	Earth Fault 2 IN>4 Trip	EF 2 IN>4 Trip	Yes	Yes	Yes
1051	SW	DDB_T4_EF_2_TRIP	T4 IN>2 Trip	T4 IN>2 Trip			
1052	SW	DDB_EF3_STAGE1_TRIP	Earth Fault 3 IN>1 Trip	EF 3 IN>1 Trip		Yes	Yes
1052	SW	DDB_T5_EF_1_TRIP	T5 IN>1 Trip	T5 IN>1 Trip			
1053	SW	DDB_EF3_STAGE2_TRIP	Earth Fault 3 IN>2 Trip	EF 3 IN>2 Trip		Yes	Yes
1053	SW	DDB_T5_EF_2_TRIP	T5 IN>2 Trip	T5 IN>2 Trip			
1054	SW	DDB_EF3_STAGE3_TRIP	Earth Fault 3 IN>3 Trip	EF 3 IN>3 Trip		Yes	Yes
1054	SW	DDB_T6_EF_1_TRIP	T6 IN>1 Trip	T6 IN>1 Trip			
1055	SW	DDB_EF3_STAGE4_TRIP	Earth Fault 3 IN>4 Trip	EF 3 IN>4 Trip		Yes	Yes
1055	SW	DDB_T6_EF_2_TRIP	T6 IN>2 Trip	T6 IN>2 Trip			
1056	SW	DDB_VIP_QUALITY_1	GOOSE Virtual input 1 Quality bit	Quality VIP 1	Yes	Yes	Yes
1057	SW	DDB_VIP_QUALITY_2	GOOSE Virtual input 2 Quality bit	Quality VIP 2	Yes	Yes	Yes
1058	SW	DDB_VIP_QUALITY_3	GOOSE Virtual input 3 Quality bit	Quality VIP 3	Yes	Yes	Yes
1059	SW	DDB_VIP_QUALITY_4	GOOSE Virtual input 4 Quality bit	Quality VIP 4	Yes	Yes	Yes
1060	SW	DDB_VIP_QUALITY_5	GOOSE Virtual input 5 Quality bit	Quality VIP 5	Yes	Yes	Yes
1061	SW	DDB_VIP_QUALITY_6	GOOSE Virtual input 6 Quality bit	Quality VIP 6	Yes	Yes	Yes
1062	SW	DDB_VIP_QUALITY_7	GOOSE Virtual input 7 Quality bit	Quality VIP 7	Yes	Yes	Yes
1063	SW	DDB_VIP_QUALITY_8	GOOSE Virtual input 8 Quality bit	Quality VIP 8	Yes	Yes	Yes
1064	SW	DDB_VIP_QUALITY_9	GOOSE Virtual input 9 Quality bit	Quality VIP 9	Yes	Yes	Yes
1065	SW	DDB_VIP_QUALITY_10	GOOSE Virtual input 10 Quality bit	Quality VIP 10	Yes	Yes	Yes

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
1066	SW	DDB_VIP_QUALITY_11	GOOSE Virtual input 11 Quality bit	Quality VIP 11	Yes	Yes	Yes
1067	SW	DDB_VIP_QUALITY_12	GOOSE Virtual input 12 Quality bit	Quality VIP 12	Yes	Yes	Yes
1068	SW	DDB_VIP_QUALITY_13	GOOSE Virtual input 13 Quality bit	Quality VIP 13	Yes	Yes	Yes
1069	SW	DDB_VIP_QUALITY_14	GOOSE Virtual input 14 Quality bit	Quality VIP 14	Yes	Yes	Yes
1070	SW	DDB_VIP_QUALITY_15	GOOSE Virtual input 15 Quality bit	Quality VIP 15	Yes	Yes	Yes
1071	SW	DDB_VIP_QUALITY_16	GOOSE Virtual input 16 Quality bit	Quality VIP 16	Yes	Yes	Yes
1072	SW	DDB_VIP_QUALITY_17	GOOSE Virtual input 17 Quality bit	Quality VIP 17	Yes	Yes	Yes
1073	SW	DDB_VIP_QUALITY_18	GOOSE Virtual input 18 Quality bit	Quality VIP 18	Yes	Yes	Yes
1074	SW	DDB_VIP_QUALITY_19	GOOSE Virtual input 19 Quality bit	Quality VIP 19	Yes	Yes	Yes
1075	SW	DDB_VIP_QUALITY_20	GOOSE Virtual input 20 Quality bit	Quality VIP 20	Yes	Yes	Yes
1076	SW	DDB_VIP_QUALITY_21	GOOSE Virtual input 21 Quality bit	Quality VIP 21	Yes	Yes	Yes
1077	SW	DDB_VIP_QUALITY_22	GOOSE Virtual input 22 Quality bit	Quality VIP 22	Yes	Yes	Yes
1078	SW	DDB_VIP_QUALITY_23	GOOSE Virtual input 23 Quality bit	Quality VIP 23	Yes	Yes	Yes
1079	SW	DDB_VIP_QUALITY_24	GOOSE Virtual input 24 Quality bit	Quality VIP 24	Yes	Yes	Yes
1080	SW	DDB_VIP_QUALITY_25	GOOSE Virtual input 25 Quality bit	Quality VIP 25	Yes	Yes	Yes
1081	SW	DDB_VIP_QUALITY_26	GOOSE Virtual input 26 Quality bit	Quality VIP 26	Yes	Yes	Yes
1082	SW	DDB_VIP_QUALITY_27	GOOSE Virtual input 27 Quality bit	Quality VIP 27	Yes	Yes	Yes
1083	SW	DDB_VIP_QUALITY_28	GOOSE Virtual input 28 Quality bit	Quality VIP 28	Yes	Yes	Yes
1084	SW	DDB_VIP_QUALITY_29	GOOSE Virtual input 29 Quality bit	Quality VIP 29	Yes	Yes	Yes
1085	SW	DDB_VIP_QUALITY_30	GOOSE Virtual input 30 Quality bit	Quality VIP 30	Yes	Yes	Yes
1086	SW	DDB_VIP_QUALITY_31	GOOSE Virtual input 31 Quality bit	Quality VIP 31	Yes	Yes	Yes
1087	SW	DDB_VIP_QUALITY_32	GOOSE Virtual input 32 Quality bit	Quality VIP 32	Yes	Yes	Yes
1088	SW	DDB_VIP_QUALITY_33	GOOSE Virtual input 33 Quality bit	Quality VIP 33	Yes	Yes	Yes
1089	SW	DDB_VIP_QUALITY_34	GOOSE Virtual input 34 Quality bit	Quality VIP 34	Yes	Yes	Yes
1090	SW	DDB_VIP_QUALITY_35	GOOSE Virtual input 35 Quality bit	Quality VIP 35	Yes	Yes	Yes
1091	SW	DDB_VIP_QUALITY_36	GOOSE Virtual input 36 Quality bit	Quality VIP 36	Yes	Yes	Yes
1092	SW	DDB_VIP_QUALITY_37	GOOSE Virtual input 37 Quality bit	Quality VIP 37	Yes	Yes	Yes
1093	SW	DDB_VIP_QUALITY_38	GOOSE Virtual input 38 Quality bit	Quality VIP 38	Yes	Yes	Yes
1094	SW	DDB_VIP_QUALITY_39	GOOSE Virtual input 39 Quality bit	Quality VIP 39	Yes	Yes	Yes
1095	SW	DDB_VIP_QUALITY_40	GOOSE Virtual input 40 Quality bit	Quality VIP 40	Yes	Yes	Yes
1096	SW	DDB_VIP_QUALITY_41	GOOSE Virtual input 41 Quality bit	Quality VIP 41	Yes	Yes	Yes
1097	SW	DDB_VIP_QUALITY_42	GOOSE Virtual input 42 Quality bit	Quality VIP 42	Yes	Yes	Yes
1098	SW	DDB_VIP_QUALITY_43	GOOSE Virtual input 43 Quality bit	Quality VIP 43	Yes	Yes	Yes
1099	SW	DDB_VIP_QUALITY_44	GOOSE Virtual input 44 Quality bit	Quality VIP 44	Yes	Yes	Yes
1100	SW	DDB_VIP_QUALITY_45	GOOSE Virtual input 45 Quality bit	Quality VIP 45	Yes	Yes	Yes
1101	SW	DDB_VIP_QUALITY_46	GOOSE Virtual input 46 Quality bit	Quality VIP 46	Yes	Yes	Yes
1102	SW	DDB_VIP_QUALITY_47	GOOSE Virtual input 47 Quality bit	Quality VIP 47	Yes	Yes	Yes
1103	SW	DDB_VIP_QUALITY_48	GOOSE Virtual input 48 Quality bit	Quality VIP 48	Yes	Yes	Yes
1104	SW	DDB_VIP_QUALITY_49	GOOSE Virtual input 49 Quality bit	Quality VIP 49	Yes	Yes	Yes
1105	SW	DDB_VIP_QUALITY_50	GOOSE Virtual input 50 Quality bit	Quality VIP 50	Yes	Yes	Yes
1106	SW	DDB_VIP_QUALITY_51	GOOSE Virtual input 51 Quality bit	Quality VIP 51	Yes	Yes	Yes
1107	SW	DDB_VIP_QUALITY_52	GOOSE Virtual input 52 Quality bit	Quality VIP 52	Yes	Yes	Yes
1108	SW	DDB_VIP_QUALITY_53	GOOSE Virtual input 53 Quality bit	Quality VIP 53	Yes	Yes	Yes
1109	SW	DDB_VIP_QUALITY_54	GOOSE Virtual input 54 Quality bit	Quality VIP 54	Yes	Yes	Yes

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
1110	SW	DDB_VIP_QUALITY_55	GOOSE Virtual input 55 Quality bit	Quality VIP 55	Yes	Yes	Yes
1111	SW	DDB_VIP_QUALITY_56	GOOSE Virtual input 56 Quality bit	Quality VIP 56	Yes	Yes	Yes
1112	SW	DDB_VIP_QUALITY_57	GOOSE Virtual input 57 Quality bit	Quality VIP 57	Yes	Yes	Yes
1113	SW	DDB_VIP_QUALITY_58	GOOSE Virtual input 58 Quality bit	Quality VIP 58	Yes	Yes	Yes
1114	SW	DDB_VIP_QUALITY_59	GOOSE Virtual input 59 Quality bit	Quality VIP 59	Yes	Yes	Yes
1115	SW	DDB_VIP_QUALITY_60	GOOSE Virtual input 60 Quality bit	Quality VIP 60	Yes	Yes	Yes
1116	SW	DDB_VIP_QUALITY_61	GOOSE Virtual input 61 Quality bit	Quality VIP 61	Yes	Yes	Yes
1117	SW	DDB_VIP_QUALITY_62	GOOSE Virtual input 62 Quality bit	Quality VIP 62	Yes	Yes	Yes
1118	SW	DDB_VIP_QUALITY_63	GOOSE Virtual input 63 Quality bit	Quality VIP 63	Yes	Yes	Yes
1119	SW	DDB_VIP_QUALITY_64	GOOSE Virtual input 64 Quality bit	Quality VIP 64	Yes	Yes	Yes
1120	SW	DDB_VIP_PUB_PRES_1	GOOSE Virtual input 1 publisher bit	PubPres VIP 1	Yes	Yes	Yes
1121	SW	DDB_VIP_PUB_PRES_2	GOOSE Virtual input 2 publisher bit	PubPres VIP 2	Yes	Yes	Yes
1122	SW	DDB_VIP_PUB_PRES_3	GOOSE Virtual input 3 publisher bit	PubPres VIP 3	Yes	Yes	Yes
1123	SW	DDB_VIP_PUB_PRES_4	GOOSE Virtual input 4 publisher bit	PubPres VIP 4	Yes	Yes	Yes
1124	SW	DDB_VIP_PUB_PRES_5	GOOSE Virtual input 5 publisher bit	PubPres VIP 5	Yes	Yes	Yes
1125	SW	DDB_VIP_PUB_PRES_6	GOOSE Virtual input 6 publisher bit	PubPres VIP 6	Yes	Yes	Yes
1126	SW	DDB_VIP_PUB_PRES_7	GOOSE Virtual input 7 publisher bit	PubPres VIP 7	Yes	Yes	Yes
1127	SW	DDB_VIP_PUB_PRES_8	GOOSE Virtual input 8 publisher bit	PubPres VIP 8	Yes	Yes	Yes
1128	SW	DDB_VIP_PUB_PRES_9	GOOSE Virtual input 9 publisher bit	PubPres VIP 9	Yes	Yes	Yes
1129	SW	DDB_VIP_PUB_PRES_10	GOOSE Virtual input 10 publisher bit	PubPres VIP 10	Yes	Yes	Yes
1130	SW	DDB_VIP_PUB_PRES_11	GOOSE Virtual input 11 publisher bit	PubPres VIP 11	Yes	Yes	Yes
1131	SW	DDB_VIP_PUB_PRES_12	GOOSE Virtual input 12 publisher bit	PubPres VIP 12	Yes	Yes	Yes
1132	SW	DDB_VIP_PUB_PRES_13	GOOSE Virtual input 13 publisher bit	PubPres VIP 13	Yes	Yes	Yes
1133	SW	DDB_VIP_PUB_PRES_14	GOOSE Virtual input 14 publisher bit	PubPres VIP 14	Yes	Yes	Yes
1134	SW	DDB_VIP_PUB_PRES_15	GOOSE Virtual input 15 publisher bit	PubPres VIP 15	Yes	Yes	Yes
1135	SW	DDB_VIP_PUB_PRES_16	GOOSE Virtual input 16 publisher bit	PubPres VIP 16	Yes	Yes	Yes
1136	SW	DDB_VIP_PUB_PRES_17	GOOSE Virtual input 17 publisher bit	PubPres VIP 17	Yes	Yes	Yes
1137	SW	DDB_VIP_PUB_PRES_18	GOOSE Virtual input 18 publisher bit	PubPres VIP 18	Yes	Yes	Yes
1138	SW	DDB_VIP_PUB_PRES_19	GOOSE Virtual input 19 publisher bit	PubPres VIP 19	Yes	Yes	Yes
1139	SW	DDB_VIP_PUB_PRES_20	GOOSE Virtual input 20 publisher bit	PubPres VIP 20	Yes	Yes	Yes
1140	SW	DDB_VIP_PUB_PRES_21	GOOSE Virtual input 21 publisher bit	PubPres VIP 21	Yes	Yes	Yes
1141	SW	DDB_VIP_PUB_PRES_22	GOOSE Virtual input 22 publisher bit	PubPres VIP 22	Yes	Yes	Yes
1142	SW	DDB_VIP_PUB_PRES_23	GOOSE Virtual input 23 publisher bit	PubPres VIP 23	Yes	Yes	Yes
1143	SW	DDB_VIP_PUB_PRES_24	GOOSE Virtual input 24 publisher bit	PubPres VIP 24	Yes	Yes	Yes
1144	SW	DDB_VIP_PUB_PRES_25	GOOSE Virtual input 25 publisher bit	PubPres VIP 25	Yes	Yes	Yes
1145	SW	DDB_VIP_PUB_PRES_26	GOOSE Virtual input 26 publisher bit	PubPres VIP 26	Yes	Yes	Yes
1146	SW	DDB_VIP_PUB_PRES_27	GOOSE Virtual input 27 publisher bit	PubPres VIP 27	Yes	Yes	Yes
1147	SW	DDB_VIP_PUB_PRES_28	GOOSE Virtual input 28 publisher bit	PubPres VIP 28	Yes	Yes	Yes
1148	SW	DDB_VIP_PUB_PRES_29	GOOSE Virtual input 29 publisher bit	PubPres VIP 29	Yes	Yes	Yes
1149	SW	DDB_VIP_PUB_PRES_30	GOOSE Virtual input 30 publisher bit	PubPres VIP 30	Yes	Yes	Yes
1150	SW	DDB_VIP_PUB_PRES_31	GOOSE Virtual input 31 publisher bit	PubPres VIP 31	Yes	Yes	Yes
1151	SW	DDB_VIP_PUB_PRES_32	GOOSE Virtual input 32 publisher bit	PubPres VIP 32	Yes	Yes	Yes
1152	SW	DDB_VIP_PUB_PRES_33	GOOSE Virtual input 33 publisher bit	PubPres VIP 33	Yes	Yes	Yes
1153	SW	DDB_VIP_PUB_PRES_34	GOOSE Virtual input 34 publisher bit	PubPres VIP 34	Yes	Yes	Yes

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
1154	SW	DDB_VIP_PUB_PRES_35	GOOSE Virtual input 35 publisher bit	PubPres VIP 35	Yes	Yes	Yes
1155	SW	DDB_VIP_PUB_PRES_36	GOOSE Virtual input 36 publisher bit	PubPres VIP 36	Yes	Yes	Yes
1156	SW	DDB_VIP_PUB_PRES_37	GOOSE Virtual input 37 publisher bit	PubPres VIP 37	Yes	Yes	Yes
1157	SW	DDB_VIP_PUB_PRES_38	GOOSE Virtual input 38 publisher bit	PubPres VIP 38	Yes	Yes	Yes
1158	SW	DDB_VIP_PUB_PRES_39	GOOSE Virtual input 39 publisher bit	PubPres VIP 39	Yes	Yes	Yes
1159	SW	DDB_VIP_PUB_PRES_40	GOOSE Virtual input 40 publisher bit	PubPres VIP 40	Yes	Yes	Yes
1160	SW	DDB_VIP_PUB_PRES_41	GOOSE Virtual input 41 publisher bit	PubPres VIP 41	Yes	Yes	Yes
1161	SW	DDB_VIP_PUB_PRES_42	GOOSE Virtual input 42 publisher bit	PubPres VIP 42	Yes	Yes	Yes
1162	SW	DDB_VIP_PUB_PRES_43	GOOSE Virtual input 43 publisher bit	PubPres VIP 43	Yes	Yes	Yes
1163	SW	DDB_VIP_PUB_PRES_44	GOOSE Virtual input 44 publisher bit	PubPres VIP 44	Yes	Yes	Yes
1164	SW	DDB_VIP_PUB_PRES_45	GOOSE Virtual input 45 publisher bit	PubPres VIP 45	Yes	Yes	Yes
1165	SW	DDB_VIP_PUB_PRES_46	GOOSE Virtual input 46 publisher bit	PubPres VIP 46	Yes	Yes	Yes
1166	SW	DDB_VIP_PUB_PRES_47	GOOSE Virtual input 47 publisher bit	PubPres VIP 47	Yes	Yes	Yes
1167	SW	DDB_VIP_PUB_PRES_48	GOOSE Virtual input 48 publisher bit	PubPres VIP 48	Yes	Yes	Yes
1168	SW	DDB_VIP_PUB_PRES_49	GOOSE Virtual input 49 publisher bit	PubPres VIP 49	Yes	Yes	Yes
1169	SW	DDB_VIP_PUB_PRES_50	GOOSE Virtual input 50 publisher bit	PubPres VIP 50	Yes	Yes	Yes
1170	SW	DDB_VIP_PUB_PRES_51	GOOSE Virtual input 51 publisher bit	PubPres VIP 51	Yes	Yes	Yes
1171	SW	DDB_VIP_PUB_PRES_52	GOOSE Virtual input 52 publisher bit	PubPres VIP 52	Yes	Yes	Yes
1172	SW	DDB_VIP_PUB_PRES_53	GOOSE Virtual input 53 publisher bit	PubPres VIP 53	Yes	Yes	Yes
1173	SW	DDB_VIP_PUB_PRES_54	GOOSE Virtual input 54 publisher bit	PubPres VIP 54	Yes	Yes	Yes
1174	SW	DDB_VIP_PUB_PRES_55	GOOSE Virtual input 55 publisher bit	PubPres VIP 55	Yes	Yes	Yes
1175	SW	DDB_VIP_PUB_PRES_56	GOOSE Virtual input 56 publisher bit	PubPres VIP 56	Yes	Yes	Yes
1176	SW	DDB_VIP_PUB_PRES_57	GOOSE Virtual input 57 publisher bit	PubPres VIP 57	Yes	Yes	Yes
1177	SW	DDB_VIP_PUB_PRES_58	GOOSE Virtual input 58 publisher bit	PubPres VIP 58	Yes	Yes	Yes
1178	SW	DDB_VIP_PUB_PRES_59	GOOSE Virtual input 59 publisher bit	PubPres VIP 59	Yes	Yes	Yes
1179	SW	DDB_VIP_PUB_PRES_60	GOOSE Virtual input 60 publisher bit	PubPres VIP 60	Yes	Yes	Yes
1180	SW	DDB_VIP_PUB_PRES_61	GOOSE Virtual input 61 publisher bit	PubPres VIP 61	Yes	Yes	Yes
1181	SW	DDB_VIP_PUB_PRES_62	GOOSE Virtual input 62 publisher bit	PubPres VIP 62	Yes	Yes	Yes
1182	SW	DDB_VIP_PUB_PRES_63	GOOSE Virtual input 63 publisher bit	PubPres VIP 63	Yes	Yes	Yes
1183	SW	DDB_VIP_PUB_PRES_64	GOOSE Virtual input 64 publisher bit	PubPres VIP 64	Yes	Yes	Yes
1184	SW	DDB_UNUSED	DDB_UNUSED				
1185	SW	DDB_UNUSED	DDB_UNUSED				
1186	SW	DDB_UNUSED	DDB_UNUSED				
1187	SW	DDB_UNUSED	DDB_UNUSED				
1188	SW	DDB_RTD_1_TRIP	RTD 1 Trip	RTD 1 Trip	Yes	Yes	Yes
1189	SW	DDB_RTD_2_TRIP	RTD 2 Trip	RTD 2 Trip	Yes	Yes	Yes
1190	SW	DDB_RTD_3_TRIP	RTD 3 Trip	RTD 3 Trip	Yes	Yes	Yes
1191	SW	DDB_RTD_4_TRIP	RTD 4 Trip	RTD 4 Trip	Yes	Yes	Yes
1192	SW	DDB_RTD_5_TRIP	RTD 5 Trip	RTD 5 Trip	Yes	Yes	Yes
1193	SW	DDB_RTD_6_TRIP	RTD 6 Trip	RTD 6 Trip	Yes	Yes	Yes
1194	SW	DDB_RTD_7_TRIP	RTD 7 Trip	RTD 7 Trip	Yes	Yes	Yes
1195	SW	DDB_RTD_8_TRIP	RTD 8 Trip	RTD 8 Trip	Yes	Yes	Yes
1196	SW	DDB_RTD_9_TRIP	RTD 9 Trip	RTD 9 Trip	Yes	Yes	Yes
1197	SW	DDB_RTD_10_TRIP	RTD 10 Trip	RTD 10 Trip	Yes	Yes	Yes

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
1198	FL	DDB_ANY_RTD_TRIP	Any RTD Trip	Any RTD Trip	Yes	Yes	Yes
1199	SW	DDB_CL_INPUT_1_TRIP	Current Loop Input 1 Trip	CL Input 1 Trip	Yes	Yes	Yes
1200	SW	DDB_CL_INPUT_2_TRIP	Current Loop Input 2 Trip	CL Input 2 Trip	Yes	Yes	Yes
1201	SW	DDB_CL_INPUT_3_TRIP	Current Loop Input 3 Trip	CL Input 3 Trip	Yes	Yes	Yes
1202	SW	DDB_CL_INPUT_4_TRIP	Current Loop Input 4 Trip	CL Input 4 Trip	Yes	Yes	Yes
1203	SW	DDB_PUV_1_PH_A_TRIP	1st Stage Phase U/V Trip A/AB	V<1 Trip A/AB		Yes	Yes
1204	SW	DDB_PUV_1_PH_B_TRIP	1st Stage Phase U/V Trip B/BC	V<1 Trip B/BC		Yes	Yes
1205	SW	DDB_PUV_1_PH_C_TRIP	1st Stage Phase U/V Trip C/CA	V<1 Trip C/CA		Yes	Yes
1206	SW	DDB_PUV_2_PH_A_TRIP	2nd Stage Phase U/V Trip A/AB	V<2 Trip A/AB		Yes	Yes
1207	SW	DDB_PUV_2_PH_B_TRIP	2nd Stage Phase U/V Trip B/BC	V<2 Trip B/BC		Yes	Yes
1208	SW	DDB_PUV_2_PH_C_TRIP	2nd Stage Phase U/V Trip C/CA	V<2 Trip C/CA		Yes	Yes
1209	SW	DDB_POV_1_PH_A_TRIP	1st Stage Phase O/V Trip A/AB	V>1 Trip A/AB		Yes	Yes
1210	SW	DDB_POV_1_PH_B_TRIP	1st Stage Phase O/V Trip B/BC	V>1 Trip B/BC		Yes	Yes
1211	SW	DDB_POV_1_PH_C_TRIP	1st Stage Phase O/V Trip C/CA	V>1 Trip C/CA		Yes	Yes
1212	SW	DDB_POV_2_PH_A_TRIP	2nd Stage Phase O/V Trip A/AB	V>2 Trip A/AB		Yes	Yes
1213	SW	DDB_POV_2_PH_B_TRIP	2nd Stage Phase O/V Trip B/BC	V>2 Trip B/BC		Yes	Yes
1214	SW	DDB_POV_2_PH_C_TRIP	2nd Stage Phase O/V Trip C/CA	V>2 Trip C/CA		Yes	Yes
1215	SW	DDB_NPSOV_1_TRIP	Negative Sequence Over Voltage Trip	V2> Trip	Yes	Yes	Yes
1216	SW	DDB_NPSOC1_STAGE1_TRIP	Negative Sequence Overcurrent 1 I2>1 Trip	NPOC1 I2>1 Trip	Yes	Yes	Yes
1217	SW	DDB_NPSOC1_STAGE2_TRIP	Negative Sequence Overcurrent 1 I2>2 Trip	NPOC1 I2>2 Trip	Yes	Yes	Yes
1218	SW	DDB_NPSOC1_STAGE3_TRIP	Negative Sequence Overcurrent 1 I2>3 Trip	NPOC1 I2>3 Trip	Yes	Yes	Yes
1219	SW	DDB_NPSOC1_STAGE4_TRIP	Negative Sequence Overcurrent 1 I2>4 Trip	NPOC1 I2>4 Trip	Yes	Yes	Yes
1220	SW	DDB_NPSOC2_STAGE1_TRIP	Negative Sequence Overcurrent 2 I2>1 Trip	NPOC2 I2>1 Trip	Yes	Yes	Yes
1221	SW	DDB_NPSOC2_STAGE2_TRIP	Negative Sequence Overcurrent 2 I2>2 Trip	NPOC2 I2>2 Trip	Yes	Yes	Yes
1222	SW	DDB_NPSOC2_STAGE3_TRIP	Negative Sequence Overcurrent 2 I2>3 Trip	NPOC2 I2>3 Trip	Yes	Yes	Yes
1223	SW	DDB_NPSOC2_STAGE4_TRIP	Negative Sequence Overcurrent 2 I2>4 Trip	NPOC2 I2>4 Trip	Yes	Yes	Yes
1224	SW	DDB_NPSOC3_STAGE1_TRIP	Negative Sequence Overcurrent 3 I2>1 Trip	NPOC3 I2>1 Trip		Yes	Yes
1225	SW	DDB_NPSOC3_STAGE2_TRIP	Negative Sequence Overcurrent 3 I2>2 Trip	NPOC3 I2>2 Trip		Yes	Yes
1226	SW	DDB_NPSOC3_STAGE3_TRIP	Negative Sequence Overcurrent 3 I2>3 Trip	NPOC3 I2>3 Trip		Yes	Yes
1227	SW	DDB_NPSOC3_STAGE4_TRIP	Negative Sequence Overcurrent 3 I2>4 Trip	NPOC3 I2>4 Trip		Yes	Yes
1228	SW	DDB_OFREQ_1_TRIP	Over Frequency Stage 1 Trip	F>1 Trip	Yes	Yes	Yes
1229	SW	DDB_OFREQ_2_TRIP	Over Frequency Stage 2 Trip	F>2 Trip	Yes	Yes	Yes
1230	SW	DDB_UFREQ_1_TRIP	Under Frequency Stage 1 Trip	F<1 Trip	Yes	Yes	Yes
1231	SW	DDB_UFREQ_2_TRIP	Under Frequency Stage 2 Trip	F<2 Trip	Yes	Yes	Yes
1232	SW	DDB_UFREQ_3_TRIP	Under Frequency Stage 3 Trip	F<3 Trip	Yes	Yes	Yes

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
1233	SW	DDB_UFREQ_4_TRIP	Under Frequency Stage 4 Trip	F<4 Trip	Yes	Yes	Yes
1234	SW	DDB_PUV_1_3PH_TRIP	1st Stage Phase U/V Trip 3ph	V<1 Trip		Yes	Yes
1235	SW	DDB_PUV_2_3PH_TRIP	2nd Stage Phase U/V Trip 3ph	V<2 Trip		Yes	Yes
1236	SW	DDB_POV_1_3PH_TRIP	1st Stage Phase O/V Trip 3ph	V>1 Trip		Yes	Yes
1237	SW	DDB_POV_2_3PH_TRIP	2nd Stage Phase O/V Trip 3ph	V>2 Trip		Yes	Yes
1238	SW	DDB_RESOV_1_TRIP	1st Stage Residual O/V Trip	VN>1 Trip		Yes	Yes
1239	SW	DDB_RESOV_2_TRIP	2nd Stage Residual O/V Trip	VN>2 Trip		Yes	Yes
1240	SW	DDB_VPERHZ_1_TRIP_1	W1 V/Hz>1 Trip	W1 V/Hz>1 Trip		Yes	Yes
1241	SW	DDB_VPERHZ_2_TRIP_1	W1 V/Hz>2 Trip	W1 V/Hz>2 Trip		Yes	Yes
1242	SW	DDB_VPERHZ_3_TRIP_1	W1 V/Hz>3 Trip	W1 V/Hz>3 Trip		Yes	Yes
1243	SW	DDB_VPERHZ_4_TRIP_1	W1 V/Hz>4 Trip	W1 V/Hz>4 Trip		Yes	Yes
1244	SW	DDB_VPERHZ_1_TRIP_2	W2 V/Hz>1 Trip	W2 V/Hz>1 Trip	Yes	Yes	Yes
1245	SW	DDB_VPERHZ_2_TRIP_2	W2 V/Hz>2 Trip	W2 V/Hz>2 Trip	Yes	Yes	Yes
1246	SW	DDB_VPERHZ_3_TRIP_2	W2 V/Hz>3 Trip	W2 V/Hz>3 Trip	Yes	Yes	Yes
1247	SW	DDB_VPERHZ_4_TRIP_2	W2 V/Hz>4 Trip	W2 V/Hz>4 Trip	Yes	Yes	Yes
1248	SW	DDB_UI_LOGGEDIN	User logged into UI	Logged into UI	Yes	Yes	Yes
1249	SW	DDB_FCUR_LOGGEDIN	User logged into front port courier	Logged into FP	Yes	Yes	Yes
1250	SW	DDB_RP1_LOGGEDIN	User logged into Rear Port1 courier	Logged into RP1	Yes	Yes	Yes
1251	SW	DDB_RP2_LOGGEDIN	User logged into Rear Port2 courier	Logged into RP2	Yes	Yes	Yes
1252	SW	DDB_TNL_LOGGEDIN	User logged into turnneled courier	Logged into TNL	Yes	Yes	Yes
1253	SW	DDB_CPR_LOGGEDIN	User logged into co-processor courier	Logged into CPR	Yes	Yes	Yes
1254	SW	DDB_UNUSED	DDB_UNUSED				
1255	SW	DDB_UNUSED	DDB_UNUSED				
1256	SW	DDB_UNUSED	DDB_UNUSED				
1257	PSL	DDB_EXT_3PH_TRIP1	External CB1 Trip	Extern CB1 Trip	Yes	Yes	Yes
1258	PSL	DDB_EXT_3PH_TRIP2	External CB2 Trip	Extern CB2 Trip	Yes	Yes	Yes
1259	PSL	DDB_EXT_3PH_TRIP3	External CB3 Trip	Extern CB3 Trip	Yes	Yes	Yes
1260	PSL	DDB_EXT_3PH_TRIP4	External CB4 Trip	Extern CB4 Trip	Yes	Yes	Yes
1261	PSL	DDB_EXT_3PH_TRIP5	External CB5 Trip	Extern CB5 Trip	Yes	Yes	Yes
1262	PSL	DDB_INT_CBF_INIT_T1	Internal signal init CBF T1	Int CBF Init T1	Yes	Yes	Yes
1263	PSL	DDB_INT_CBF_INIT_T2	Internal signal init CBF T2	Int CBF Init T2	Yes	Yes	Yes
1264	PSL	DDB_INT_CBF_INIT_T3	Internal signal init CBF T3	Int CBF Init T3	Yes	Yes	Yes
1265	PSL	DDB_INT_CBF_INIT_T4	Internal signal init CBF T4	Int CBF Init T4	Yes	Yes	Yes
1266	PSL	DDB_INT_CBF_INIT_T5	Internal signal init CBF T5	Int CBF Init T5	Yes	Yes	Yes
1267	PSL	DDB_CHAN_ALT	Alternate other analogue channels	Channel Alt	Yes	Yes	Yes
1268	PSL	DDB_PB_LINK_1_FAIL	Process Bus Network Interface link 1 fail indication	PB Link 1 Fail	Yes	Yes	Yes
1269	PSL	DDB_PB_LINK_2_FAIL	Process Bus Network Interface link 2 fail indication	PB Link 2 Fail	Yes	Yes	Yes
1270	PSL	DDB_PB_LINK_3_FAIL	Process Bus Network Interface link 3 fail indication	PB Link 3 Fail	Yes	Yes	Yes
1271	PSL	DDB_MU1_ABSENCE	DDB_MU1_ABSENCE	MU1 Absence	Yes	Yes	Yes
1272	PSL	DDB_MU2_ABSENCE	DDB_MU2_ABSENCE	MU2 Absence	Yes	Yes	Yes
1273	PSL	DDB_MU3_ABSENCE	DDB_MU3_ABSENCE	MU3 Absence	Yes	Yes	Yes
1274	PSL	DDB_MU4_ABSENCE	DDB_MU4_ABSENCE	MU4 Absence	Yes	Yes	Yes

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
1275	PSL	DDB_MU5_ABSENCE	DDB_MU5_ABSENCE	MU5 Absence	Yes	Yes	Yes
1276	PSL	DDB_MU6_ABSENCE	DDB_MU6_ABSENCE	MU6 Absence	Yes	Yes	Yes
1277	PSL	DDB_MU7_ABSENCE	DDB_MU7_ABSENCE	MU7 Absence	Yes	Yes	Yes
1278	PSL	DDB_MU8_ABSENCE	DDB_MU8_ABSENCE	MU8 Absence	Yes	Yes	Yes
1279	PSL	DDB_MAIN_VT_INHIBIT	Main VT Inhibit	Main VT Inhibit		Yes	Yes
1280	SW	DDB_AUX_VT_INHIBIT	AUX VT Inhibit	Aux VT Inhibit	Yes	Yes	Yes
1281	SW	DDB_CT_T1_INHIBIT	CT1 Inhibit	Phs CT1 Inhibit	Yes	Yes	Yes
1282	SW	DDB_CT_T2_INHIBIT	CT2 Inhibit	Phs CT2 Inhibit	Yes	Yes	Yes
1283	SW	DDB_CT_T3_INHIBIT	CT3 Inhibit	Phs CT3 Inhibit		Yes	Yes
1284	SW	DDB_CT_T4_INHIBIT	CT4 Inhibit	Phs CT4 Inhibit			Yes
1285	SW	DDB_CT_T5_INHIBIT	CT5 Inhibit	Phs CT5 Inhibit			Yes
1286	SW	DDB_TN1_INHIBIT	TN1 Inhibit	IN T1 Inhibit	Yes	Yes	Yes
1287	SW	DDB_TN2_INHIBIT	TN2 Inhibit	IN T2 Inhibit	Yes	Yes	Yes
1288	SW	DDB_TN3_INHIBIT	TN3 Inhibit	IN T3 Inhibit		Yes	Yes
1289	SW	DDB_MAIN_VT_SYNC_ALM	Main VT Synch alarm	Main VT Sync Alm		Yes	Yes
1290	SW	DDB_AUX_VT_SYNC_ALM	AUX VT Synch alarm	Aux VT Sync Alm	Yes	Yes	Yes
1291	SW	DDB_CT_T1_SYNC_ALM	CT1 Synch alarm	Phs CT1 Sync Alm	Yes	Yes	Yes
1292	SW	DDB_CT_T2_SYNC_ALM	CT2 Synch alarm	Phs CT2 Sync Alm	Yes	Yes	Yes
1293	SW	DDB_CT_T3_SYNC_ALM	CT3 Synch alarm	Phs CT3 Sync Alm		Yes	Yes
1294	SW	DDB_CT_T4_SYNC_ALM	CT4 Synch alarm	Phs CT4 Sync Alm			Yes
1295	SW	DDB_CT_T5_SYNC_ALM	CT5 Synch alarm	Phs CT5 Sync Alm			Yes
1296	SW	DDB_TN1_SYNC_ALM	TN1 Synch alarm	IN T1 Sync Alm	Yes	Yes	Yes
1297	SW	DDB_TN2_SYNC_ALM	TN2 Synch alarm	IN T2 Sync Alm	Yes	Yes	Yes
1298	SW	DDB_TN3_SYNC_ALM	TN3 Synch alarm	IN T3 Sync Alm		Yes	Yes
1299	SW	DDB_UNUSED	DDB_UNUSED				
1300	SW	DDB_UNUSED	DDB_UNUSED				
1301	SW	DDB_UNUSED	DDB_UNUSED				
1302	SW	DDB_UNUSED	DDB_UNUSED				
1303	SW	DDB_UNUSED	DDB_UNUSED				
1304	PSL	DDB_INT_CBF_INIT_T15	Internal signal init CBF T15	Int CBF Init T15	Yes	Yes	Yes
1305	PSL	DDB_INT_CBF_INIT_T16	Internal signal init CBF T16	Int CBF Init T16	Yes	Yes	Yes
1306	PSL	DDB_INT_CBF_INIT_T17	Internal signal init CBF T17	Int CBF Init T17	Yes	Yes	Yes
1307	PSL	DDB_INT_CBF_INIT_T18	Internal signal init CBF T18	Int CBF Init T18	Yes	Yes	Yes
1308	PSL	DDB_INT_CBF_INIT_BUS_CB	Internal signal init CBF Bus CB	IntCBFInit BusCB	Yes	Yes	Yes
1309	SW	DDB_UNUSED					
1310	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
1311	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
1312	FL	DDB_ANY_START	Any Start	Any Start	Yes	Yes	Yes
1313	SW	DDB_IDIFF_BIAS_STARTA	Diff Phase A Start	Id Bias Start A	Yes	Yes	Yes
1314	SW	DDB_IDIFF_BIAS_STARTB	Diff Phase B Start	Id Bias Start B	Yes	Yes	Yes
1315	SW	DDB_IDIFF_BIAS_STARTC	Diff Phase C Start	Id Bias Start C	Yes	Yes	Yes
1316	SW	DDB_UNUSED	DDB_UNUSED				
1317	SW	DDB_UNUSED	DDB_UNUSED				
1318	SW	DDB_UNUSED	DDB_UNUSED				

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
1319	SW	DDB_UNUSED	DDB_UNUSED				
1320	SW	DDB_UNUSED	DDB_UNUSED				
1321	SW	DDB_UNUSED	DDB_UNUSED				
1322	SW	DDB_DZ7_OC_3PH_START	T7 DeadZone Over Current Start	T7 DeadZone Over Current Start			
1323	SW	DDB_DZ8_OC_3PH_START	T8 DeadZone Over Current Start	T8 DeadZone Over Current Start			
1324	SW	DDB_DZ9_OC_3PH_START	T9 DeadZone Over Current Start	T9 DeadZone Over Current Start			
1325	SW	DDB_DZ10_OC_3PH_START	T10 DeadZone Over Current Start	T10 DeadZone Over Current Start			
1326	SW	DDB_DZ11_OC_3PH_START	T11 DeadZone Over Current Start	T11 DeadZone Over Current Start			
1327	SW	DDB_DZ12_OC_3PH_START	T12 DeadZone Over Current Start	T12 DeadZone Over Current Start			
1328	SW	DDB_DZ13_OC_3PH_START	T13 DeadZone Over Current Start	T13 DeadZone Over Current Start			
1329	SW	DDB_DZ14_OC_3PH_START	T14 DeadZone Over Current Start	T14 DeadZone Over Current Start			
1330	SW	DDB_DZ15_OC_3PH_START	T15 DeadZone Over Current Start	T15 DeadZone Over Current Start			
1331	SW	DDB_DZ16_OC_3PH_START	T16 DeadZone Over Current Start	T16 DeadZone Over Current Start			
1332	SW	DDB_DZ17_OC_3PH_START	T17 DeadZone Over Current Start	T17 DeadZone Over Current Start			
1333	SW	DDB_DZ18_OC_3PH_START	T18 DeadZone Over Current Start	T18 DeadZone Over Current Start			
1334	SW	DDB_HOT_SPOT_1_START	Hot Spot>1 Start	Hot Spot>1 Start	Yes	Yes	Yes
1335	SW	DDB_HOT_SPOT_2_START	Hot Spot>2 Start	Hot Spot>2 Start	Yes	Yes	Yes
1336	SW	DDB_HOT_SPOT_3_START	Hot Spot>3 Start	Hot Spot>3 Start	Yes	Yes	Yes
1337	SW	DDB_TOP_OIL_1_START	Top Oil >1 start	Top Oil >1 start	Yes	Yes	Yes
1338	SW	DDB_TOP_OIL_2_START	Top Oil >2 start	Top Oil >2 start	Yes	Yes	Yes
1339	SW	DDB_TOP_OIL_3_START	Top Oil >3 start	Top Oil >3 start	Yes	Yes	Yes
1340	SW	DDB_POC1_STAGE1_3PH_START	Phase Overcurrent 1 I>1 Start	POC1 I>1 Start	Yes	Yes	Yes
1341	SW	DDB_POC1_STAGE1_PH_A_START	Phase Overcurrent 1 I>1 Start A	POC1 I>1 Start A	Yes	Yes	Yes
1342	SW	DDB_POC1_STAGE1_PH_B_START	Phase Overcurrent 1 I>1 Start B	POC1 I>1 Start B	Yes	Yes	Yes
1343	SW	DDB_POC1_STAGE1_PH_C_START	Phase Overcurrent 1 I>1 Start C	POC1 I>1 Start C	Yes	Yes	Yes
1344	SW	DDB_POC1_STAGE2_3PH_START	Phase Overcurrent 1 I>2 Start	POC1 I>2 Start	Yes	Yes	Yes
1345	SW	DDB_POC1_STAGE2_PH_A_START	Phase Overcurrent 1 I>2 Start A	POC1 I>2 Start A	Yes	Yes	Yes
1346	SW	DDB_POC1_STAGE2_PH_B_START	Phase Overcurrent 1 I>2 Start B	POC1 I>2 Start B	Yes	Yes	Yes
1347	SW	DDB_POC1_STAGE2_PH_C_START	Phase Overcurrent 1 I>2 Start C	POC1 I>2 Start C	Yes	Yes	Yes
1348	SW	DDB_POC1_STAGE3_3PH_START	Phase Overcurrent 1 I>3 Start	POC1 I>3 Start	Yes	Yes	Yes
1349	SW	DDB_POC1_STAGE3_PH_A_START	Phase Overcurrent 1 I>3 Start A	POC1 I>3 Start A	Yes	Yes	Yes
1350	SW	DDB_POC1_STAGE3_PH_B_START	Phase Overcurrent 1 I>3 Start B	POC1 I>3 Start B	Yes	Yes	Yes
1351	SW	DDB_POC1_STAGE3_PH_C_START	Phase Overcurrent 1 I>3 Start C	POC1 I>3 Start C	Yes	Yes	Yes
1352	SW	DDB_POC1_STAGE4_3PH_START	Phase Overcurrent 1 I>4 Start	POC1 I>4 Start	Yes	Yes	Yes
1353	SW	DDB_POC1_STAGE4_PH_A_START	Phase Overcurrent 1 I>4 Start A	POC1 I>4 Start A	Yes	Yes	Yes

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
1354	SW	DDB_POC1_STAGE4_PH_B_START	Phase Overcurrent 1 I>4 Start B	POC1 I>4 Start B	Yes	Yes	Yes
1355	SW	DDB_POC1_STAGE4_PH_C_START	Phase Overcurrent 1 I>4 Start C	POC1 I>4 Start C	Yes	Yes	Yes
1356	SW	DDB_POC2_STAGE1_3PH_START	Phase Overcurrent 2 I>1 Start	POC2 I>1 Start	Yes	Yes	Yes
1357	SW	DDB_POC2_STAGE1_PH_A_START	Phase Overcurrent 2 I>1 Start A	POC2 I>1 Start A	Yes	Yes	Yes
1358	SW	DDB_POC2_STAGE1_PH_B_START	Phase Overcurrent 2 I>1 Start B	POC2 I>1 Start B	Yes	Yes	Yes
1359	SW	DDB_POC2_STAGE1_PH_C_START	Phase Overcurrent 2 I>1 Start C	POC2 I>1 Start C	Yes	Yes	Yes
1360	SW	DDB_POC2_STAGE2_3PH_START	Phase Overcurrent 2 I>2 Start	POC2 I>2 Start	Yes	Yes	Yes
1361	SW	DDB_POC2_STAGE2_PH_A_START	Phase Overcurrent 2 I>2 Start A	POC2 I>2 Start A	Yes	Yes	Yes
1362	SW	DDB_POC2_STAGE2_PH_B_START	Phase Overcurrent 2 I>2 Start B	POC2 I>2 Start B	Yes	Yes	Yes
1363	SW	DDB_POC2_STAGE2_PH_C_START	Phase Overcurrent 2 I>2 Start C	POC2 I>2 Start C	Yes	Yes	Yes
1364	SW	DDB_POC2_STAGE3_3PH_START	Phase Overcurrent 2 I>3 Start	POC2 I>3 Start	Yes	Yes	Yes
1365	SW	DDB_POC2_STAGE3_PH_A_START	Phase Overcurrent 2 I>3 Start A	POC2 I>3 Start A	Yes	Yes	Yes
1366	SW	DDB_POC2_STAGE3_PH_B_START	Phase Overcurrent 2 I>3 Start B	POC2 I>3 Start B	Yes	Yes	Yes
1367	SW	DDB_POC2_STAGE3_PH_C_START	Phase Overcurrent 2 I>3 Start C	POC2 I>3 Start C	Yes	Yes	Yes
1368	SW	DDB_POC2_STAGE4_3PH_START	Phase Overcurrent 2 I>4 Start	POC2 I>4 Start	Yes	Yes	Yes
1369	SW	DDB_POC2_STAGE4_PH_A_START	Phase Overcurrent 2 I>4 Start A	POC2 I>4 Start A	Yes	Yes	Yes
1370	SW	DDB_POC2_STAGE4_PH_B_START	Phase Overcurrent 2 I>4 Start B	POC2 I>4 Start B	Yes	Yes	Yes
1371	SW	DDB_POC2_STAGE4_PH_C_START	Phase Overcurrent 2 I>4 Start C	POC2 I>4 Start C	Yes	Yes	Yes
1372	SW	DDB_POC3_STAGE1_3PH_START	Phase Overcurrent 3 I>1 Start	POC3 I>1 Start		Yes	Yes
1373	SW	DDB_POC3_STAGE1_PH_A_START	Phase Overcurrent 3 I>1 Start A	POC3 I>1 Start A		Yes	Yes
1374	SW	DDB_POC3_STAGE1_PH_B_START	Phase Overcurrent 3 I>1 Start B	POC3 I>1 Start B		Yes	Yes
1375	SW	DDB_POC3_STAGE1_PH_C_START	Phase Overcurrent 3 I>1 Start C	POC3 I>1 Start C		Yes	Yes
1376	SW	DDB_POC3_STAGE2_3PH_START	Phase Overcurrent 3 I>2 Start	POC3 I>2 Start		Yes	Yes
1377	SW	DDB_POC3_STAGE2_PH_A_START	Phase Overcurrent 3 I>2 Start A	POC3 I>2 Start A		Yes	Yes
1378	SW	DDB_POC3_STAGE2_PH_B_START	Phase Overcurrent 3 I>2 Start B	POC3 I>2 Start B		Yes	Yes
1379	SW	DDB_POC3_STAGE2_PH_C_START	Phase Overcurrent 3 I>2 Start C	POC3 I>2 Start C		Yes	Yes
1380	SW	DDB_POC3_STAGE3_3PH_START	Phase Overcurrent 3 I>3 Start	POC3 I>3 Start		Yes	Yes
1381	SW	DDB_POC3_STAGE3_PH_A_START	Phase Overcurrent 3 I>3 Start A	POC3 I>3 Start A		Yes	Yes
1382	SW	DDB_POC3_STAGE3_PH_B_START	Phase Overcurrent 3 I>3 Start B	POC3 I>3 Start B		Yes	Yes
1383	SW	DDB_POC3_STAGE3_PH_C_START	Phase Overcurrent 3 I>3 Start C	POC3 I>3 Start C		Yes	Yes
1384	SW	DDB_POC3_STAGE4_3PH_START	Phase Overcurrent 3 I>4 Start	POC3 I>4 Start		Yes	Yes
1385	SW	DDB_POC3_STAGE4_PH_A_START	Phase Overcurrent 3 I>4 Start A	POC3 I>4 Start A		Yes	Yes
1386	SW	DDB_POC3_STAGE4_PH_B_START	Phase Overcurrent 3 I>4 Start B	POC3 I>4 Start B		Yes	Yes
1387	SW	DDB_POC3_STAGE4_PH_C_START	Phase Overcurrent 3 I>4 Start C	POC3 I>4 Start C		Yes	Yes
1388	SW	DDB_VCO_1_3PH_START	VCO>1 Start	VCO>1 Start	Yes	Yes	Yes
1389	SW	DDB_VCO_1_PH_A_START	VCO>1 Start A	VCO>1 Start A	Yes	Yes	Yes
1390	SW	DDB_VCO_1_PH_B_START	VCO>1 Start B	VCO>1 Start B	Yes	Yes	Yes
1391	SW	DDB_VCO_1_PH_C_START	VCO>1 Start C	VCO>1 Start C	Yes	Yes	Yes
1392	SW	DDB_VCO_2_3PH_START	VCO>2 Start	VCO>2 Start	Yes	Yes	Yes
1393	SW	DDB_VCO_2_PH_A_START	VCO>2 Start A	VCO>2 Start A	Yes	Yes	Yes
1394	SW	DDB_VCO_2_PH_B_START	VCO>2 Start B	VCO>2 Start B	Yes	Yes	Yes
1395	SW	DDB_VCO_2_PH_C_START	VCO>2 Start C	VCO>2 Start C	Yes	Yes	Yes
1396	SW	DDB_T8_POC_1_3PH_START	T8 I>1 Start	T8 I>1 Start			
1397	SW	DDB_T8_POC_1_PH_A_START	T8 I>1 Start A	T8 I>1 Start A			

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
1398	SW	DDB_T8_POC_1_PH_B_START	T8 I>1 Start B	T8 I>1 Start B			
1399	SW	DDB_T8_POC_1_PH_C_START	T8 I>1 Start C	T8 I>1 Start C			
1400	SW	DDB_T8_POC_2_3PH_START	T8 I>2 Start	T8 I>2 Start			
1401	SW	DDB_T8_POC_2_PH_A_START	T8 I>2 Start A	T8 I>2 Start A			
1402	SW	DDB_T8_POC_2_PH_B_START	T8 I>2 Start B	T8 I>2 Start B			
1403	SW	DDB_T8_POC_2_PH_C_START	T8 I>2 Start C	T8 I>2 Start C			
1404	SW	DDB_T9_POC_1_3PH_START	T9 I>1 Start	T9 I>1 Start			
1405	SW	DDB_T9_POC_1_PH_A_START	T9 I>1 Start A	T9 I>1 Start A			
1406	SW	DDB_T9_POC_1_PH_B_START	T9 I>1 Start B	T9 I>1 Start B			
1407	SW	DDB_T9_POC_1_PH_C_START	T9 I>1 Start C	T9 I>1 Start C			
1408	SW	DDB_T9_POC_2_3PH_START	T9 I>2 Start	T9 I>2 Start			
1409	SW	DDB_T9_POC_2_PH_A_START	T9 I>2 Start A	T9 I>2 Start A			
1410	SW	DDB_T9_POC_2_PH_B_START	T9 I>2 Start B	T9 I>2 Start B			
1411	SW	DDB_T9_POC_2_PH_C_START	T9 I>2 Start C	T9 I>2 Start C			
1412	SW	DDB_T10_POC_1_3PH_START	T10 I>1 Start	T10 I>1 Start			
1413	SW	DDB_T10_POC_1_PH_A_START	T10 I>1 Start A	T10 I>1 Start A			
1414	SW	DDB_T10_POC_1_PH_B_START	T10 I>1 Start B	T10 I>1 Start B			
1415	SW	DDB_T10_POC_1_PH_C_START	T10 I>1 Start C	T10 I>1 Start C			
1416	SW	DDB_T10_POC_2_3PH_START	T10 I>2 Start	T10 I>2 Start			
1417	SW	DDB_T10_POC_2_PH_A_START	T10 I>2 Start A	T10 I>2 Start A			
1418	SW	DDB_T10_POC_2_PH_B_START	T10 I>2 Start B	T10 I>2 Start B			
1419	SW	DDB_T10_POC_2_PH_C_START	T10 I>2 Start C	T10 I>2 Start C			
1420	SW	DDB_T11_POC_1_3PH_START	T11 I>1 Start	T11 I>1 Start			
1421	SW	DDB_T11_POC_1_PH_A_START	T11 I>1 Start A	T11 I>1 Start A			
1422	SW	DDB_T11_POC_1_PH_B_START	T11 I>1 Start B	T11 I>1 Start B			
1423	SW	DDB_T11_POC_1_PH_C_START	T11 I>1 Start C	T11 I>1 Start C			
1424	SW	DDB_T11_POC_2_3PH_START	T11 I>2 Start	T11 I>2 Start			
1425	SW	DDB_T11_POC_2_PH_A_START	T11 I>2 Start A	T11 I>2 Start A			
1426	SW	DDB_T11_POC_2_PH_B_START	T11 I>2 Start B	T11 I>2 Start B			
1427	SW	DDB_T11_POC_2_PH_C_START	T11 I>2 Start C	T11 I>2 Start C			
1428	SW	DDB_T12_POC_1_3PH_START	T12 I>1 Start	T12 I>1 Start			
1429	SW	DDB_T12_POC_1_PH_A_START	T12 I>1 Start A	T12 I>1 Start A			
1430	SW	DDB_T12_POC_1_PH_B_START	T12 I>1 Start B	T12 I>1 Start B			
1431	SW	DDB_T12_POC_1_PH_C_START	T12 I>1 Start C	T12 I>1 Start C			
1432	SW	DDB_T12_POC_2_3PH_START	T12 I>2 Start	T12 I>2 Start			
1433	SW	DDB_T12_POC_2_PH_A_START	T12 I>2 Start A	T12 I>2 Start A			
1434	SW	DDB_T12_POC_2_PH_B_START	T12 I>2 Start B	T12 I>2 Start B			
1435	SW	DDB_T12_POC_2_PH_C_START	T12 I>2 Start C	T12 I>2 Start C			
1436	SW	DDB_T13_POC_1_3PH_START	T13 I>1 Start	T13 I>1 Start			
1437	SW	DDB_T13_POC_1_PH_A_START	T13 I>1 Start A	T13 I>1 Start A			
1438	SW	DDB_T13_POC_1_PH_B_START	T13 I>1 Start B	T13 I>1 Start B			
1439	SW	DDB_T13_POC_1_PH_C_START	T13 I>1 Start C	T13 I>1 Start C			
1440	SW	DDB_T13_POC_2_3PH_START	T13 I>2 Start	T13 I>2 Start			
1441	SW	DDB_T13_POC_2_PH_A_START	T13 I>2 Start A	T13 I>2 Start A			

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
1442	SW	DDB_T13_POC_2_PH_B_START	T13 I>2 Start B	T13 I>2 Start B			
1443	SW	DDB_T13_POC_2_PH_C_START	T13 I>2 Start C	T13 I>2 Start C			
1444	SW	DDB_T14_POC_1_3PH_START	T14 I>1 Start	T14 I>1 Start			
1445	SW	DDB_T14_POC_1_PH_A_START	T14 I>1 Start A	T14 I>1 Start A			
1446	SW	DDB_T14_POC_1_PH_B_START	T14 I>1 Start B	T14 I>1 Start B			
1447	SW	DDB_T14_POC_1_PH_C_START	T14 I>1 Start C	T14 I>1 Start C			
1448	SW	DDB_T14_POC_2_3PH_START	T14 I>2 Start	T14 I>2 Start			
1449	SW	DDB_T14_POC_2_PH_A_START	T14 I>2 Start A	T14 I>2 Start A			
1450	SW	DDB_T14_POC_2_PH_B_START	T14 I>2 Start B	T14 I>2 Start B			
1451	SW	DDB_T14_POC_2_PH_C_START	T14 I>2 Start C	T14 I>2 Start C			
1452	SW	DDB_T15_POC_1_3PH_START	T15 I>1 Start	T15 I>1 Start			
1453	SW	DDB_T15_POC_1_PH_A_START	T15 I>1 Start A	T15 I>1 Start A			
1454	SW	DDB_T15_POC_1_PH_B_START	T15 I>1 Start B	T15 I>1 Start B			
1455	SW	DDB_T15_POC_1_PH_C_START	T15 I>1 Start C	T15 I>1 Start C			
1456	SW	DDB_T15_POC_2_3PH_START	T15 I>2 Start	T15 I>2 Start			
1457	SW	DDB_T15_POC_2_PH_A_START	T15 I>2 Start A	T15 I>2 Start A			
1458	SW	DDB_T15_POC_2_PH_B_START	T15 I>2 Start B	T15 I>2 Start B			
1459	SW	DDB_T15_POC_2_PH_C_START	T15 I>2 Start C	T15 I>2 Start C			
1460	SW	DDB_T16_POC_1_3PH_START	T16 I>1 Start	T16 I>1 Start			
1461	SW	DDB_T16_POC_1_PH_A_START	T16 I>1 Start A	T16 I>1 Start A			
1462	SW	DDB_T16_POC_1_PH_B_START	T16 I>1 Start B	T16 I>1 Start B			
1463	SW	DDB_T16_POC_1_PH_C_START	T16 I>1 Start C	T16 I>1 Start C			
1464	SW	DDB_T16_POC_2_3PH_START	T16 I>2 Start	T16 I>2 Start			
1465	SW	DDB_T16_POC_2_PH_A_START	T16 I>2 Start A	T16 I>2 Start A			
1466	SW	DDB_T16_POC_2_PH_B_START	T16 I>2 Start B	T16 I>2 Start B			
1467	SW	DDB_T16_POC_2_PH_C_START	T16 I>2 Start C	T16 I>2 Start C			
1468	SW	DDB_T17_POC_1_3PH_START	T17 I>1 Start	T17 I>1 Start			
1469	SW	DDB_T17_POC_1_PH_A_START	T17 I>1 Start A	T17 I>1 Start A			
1470	SW	DDB_T17_POC_1_PH_B_START	T17 I>1 Start B	T17 I>1 Start B			
1471	SW	DDB_T17_POC_1_PH_C_START	T17 I>1 Start C	T17 I>1 Start C			
1472	SW	DDB_T17_POC_2_3PH_START	T17 I>2 Start	T17 I>2 Start			
1473	SW	DDB_T17_POC_2_PH_A_START	T17 I>2 Start A	T17 I>2 Start A			
1474	SW	DDB_T17_POC_2_PH_B_START	T17 I>2 Start B	T17 I>2 Start B			
1475	SW	DDB_T17_POC_2_PH_C_START	T17 I>2 Start C	T17 I>2 Start C			
1476	SW	DDB_T18_POC_1_3PH_START	T18 I>1 Start	T18 I>1 Start			
1477	SW	DDB_T18_POC_1_PH_A_START	T18 I>1 Start A	T18 I>1 Start A			
1478	SW	DDB_T18_POC_1_PH_B_START	T18 I>1 Start B	T18 I>1 Start B			
1479	SW	DDB_T18_POC_1_PH_C_START	T18 I>1 Start C	T18 I>1 Start C			
1480	SW	DDB_T18_POC_2_3PH_START	T18 I>2 Start	T18 I>2 Start			
1481	SW	DDB_T18_POC_2_PH_A_START	T18 I>2 Start A	T18 I>2 Start A			
1482	SW	DDB_T18_POC_2_PH_B_START	T18 I>2 Start B	T18 I>2 Start B			
1483	SW	DDB_T18_POC_2_PH_C_START	T18 I>2 Start C	T18 I>2 Start C			
1484	SW	DDB_EF1_STAGE1_START	Earth Fault 1 IN>1 Start	EF 1 IN>1 Start	Yes	Yes	Yes
1485	SW	DDB_EF1_STAGE2_START	Earth Fault 1 IN>2 Start	EF 1 IN>2 Start	Yes	Yes	Yes

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
1486	SW	DDB_EF1_STAGE3_START	Earth Fault 1 IN>3 Start	EF 1 IN>3 Start	Yes	Yes	Yes
1487	SW	DDB_EF1_STAGE4_START	Earth Fault 1 IN>4 Start	EF 1 IN>4 Start	Yes	Yes	Yes
1488	SW	DDB_EF2_STAGE1_START	Earth Fault 2 IN>1 Start	EF 2 IN>1 Start	Yes	Yes	Yes
1489	SW	DDB_EF2_STAGE2_START	Earth Fault 2 IN>2 Start	EF 2 IN>2 Start	Yes	Yes	Yes
1490	SW	DDB_EF2_STAGE3_START	Earth Fault 2 IN>3 Start	EF 2 IN>3 Start	Yes	Yes	Yes
1491	SW	DDB_EF2_STAGE4_START	Earth Fault 2 IN>4 Start	EF 2 IN>4 Start	Yes	Yes	Yes
1492	SW	DDB_EF3_STAGE1_START	Earth Fault 3 IN>1 Start	EF 3 IN>1 Start		Yes	Yes
1493	SW	DDB_EF3_STAGE2_START	Earth Fault 3 IN>2 Start	EF 3 IN>2 Start		Yes	Yes
1494	SW	DDB_EF3_STAGE3_START	Earth Fault 3 IN>3 Start	EF 3 IN>3 Start		Yes	Yes
1495	SW	DDB_EF3_STAGE4_START	Earth Fault 3 IN>4 Start	EF 3 IN>4 Start		Yes	Yes
1496	SW	DDB_T1_EF_1_START	T1 IN>1 Start	T1 IN>1 Start			
1497	SW	DDB_T1_EF_2_START	T1 IN>2 Start	T1 IN>2 Start			
1498	SW	DDB_T2_EF_1_START	T2 IN>1 Start	T2 IN>1 Start			
1499	SW	DDB_T2_EF_2_START	T2 IN>2 Start	T2 IN>2 Start			
1500	SW	DDB_T3_EF_1_START	T3 IN>1 Start	T3 IN>1 Start			
1501	SW	DDB_T3_EF_2_START	T3 IN>2 Start	T3 IN>2 Start			
1502	SW	DDB_T4_EF_1_START	T4 IN>1 Start	T4 IN>1 Start			
1503	SW	DDB_T4_EF_2_START	T4 IN>2 Start	T4 IN>2 Start			
1504	SW	DDB_T5_EF_1_START	T5 IN>1 Start	T5 IN>1 Start			
1505	SW	DDB_T5_EF_2_START	T5 IN>2 Start	T5 IN>2 Start			
1506	SW	DDB_T6_EF_1_START	T6 IN>1 Start	T6 IN>1 Start			
1507	SW	DDB_T6_EF_2_START	T6 IN>2 Start	T6 IN>2 Start			
1508	FL	DDB_ANY_DIFF_START	Any Diff Start	Any Diff Start	Yes	Yes	Yes
1509	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
1510	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
1511	SW	DDB_REF_START_HV	REF HV Start	REF HV Start	Yes	Yes	Yes
1512	SW	DDB_REF_START_LV	REF LV Start	REF LV Start	Yes	Yes	Yes
1513	SW	DDB_REF_START_TV	REF TV Start	REF TV Start		Yes	Yes
1514	SW	DDB_REF_START_AUTO	REF Auto Start	REF Auto Start	Yes	Yes	Yes
1515	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
1516	SW	DDB_BUS_IDIFF_STARTA_Z1	Idiff Z1 StartA	Idiff Z1 StartA			
1517	SW	DDB_BUS_IDIFF_STARTB_Z1	Idiff Z1 StartB	Idiff Z1 StartB			
1518	SW	DDB_BUS_IDIFF_STARTC_Z1	Idiff Z1 StartC	Idiff Z1 StartC			
1519	SW	DDB_BUS_IDIFF_STARTA_Z2	Idiff Z2 StartA	Idiff Z2 StartA			
1520	SW	DDB_BUS_IDIFF_STARTB_Z2	Idiff Z2 StartB	Idiff Z2 StartB			
1521	SW	DDB_BUS_IDIFF_STARTC_Z2	Idiff Z2 StartC	Idiff Z2 StartC			
1522	SW	DDB_BUS_IDIFF_START_Z1	Z1 Diff Start	Z1 Diff Start	Yes	Yes	Yes
1523	SW	DDB_BUS_IDIFF_START_Z2	Z2 Diff Start	Z2 Diff Start	Yes	Yes	Yes
1524	SW	DDB_BUS_IDIFF_STARTA_CZ	CZ Phase A Diff Start	CZ Phase A Diff Start	Yes	Yes	Yes
1525	SW	DDB_BUS_IDIFF_STARTB_CZ	CZ Phase B Diff Start	CZ Phase B Diff Start	Yes	Yes	Yes
1526	SW	DDB_BUS_IDIFF_STARTC_CZ	CZ Phase C Diff Start	CZ Phase C Diff Start	Yes	Yes	Yes
1527	SW	DDB_BUS_IDIFF_START_CZ	CZ Diff Start	CZ Diff Start	Yes	Yes	Yes

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
1528	SW	DDB_CB1_3PH_RETRIP	CB1 ReTrip 3ph	CB1 ReTrip 3ph	Yes	Yes	Yes
1528	SW	DDB_CBF_RETRIP_T1	CBF Retrip T1	CBF Retrip T1			
1529	SW	DDB_CB1_3PH_BKTRIP	CB1 BkTrip 3ph	CB1 BkTrip 3ph	Yes	Yes	Yes
1529	SW	DDB_CBF_RETRIP_T2	CBF Retrip T2	CBF Retrip T2			
1530	SW	DDB_CB2_3PH_RETRIP	CB2 ReTrip 3ph	CB2 ReTrip 3ph	Yes	Yes	Yes
1530	SW	DDB_CBF_RETRIP_T3	CBF Retrip T3	CBF Retrip T3			
1531	SW	DDB_CB2_3PH_BKTRIP	CB2 BkTrip 3ph	CB2 BkTrip 3ph	Yes	Yes	Yes
1531	SW	DDB_CBF_RETRIP_T4	CBF Retrip T4	CBF Retrip T4			
1532	SW	DDB_CB3_3PH_RETRIP	CB3 ReTrip 3ph	CB3 ReTrip 3ph		Yes	Yes
1532	SW	DDB_CBF_RETRIP_T5	CBF Retrip T5	CBF Retrip T5			
1533	SW	DDB_CB3_3PH_BKTRIP	CB3 BkTrip 3ph	CB3 BkTrip 3ph		Yes	Yes
1533	SW	DDB_CBF_RETRIP_T6	CBF Retrip T6	CBF Retrip T6			
1534	SW	DDB_CB4_3PH_RETRIP	CB4 ReTrip 3ph	CB4 ReTrip 3ph			Yes
1534	SW	DDB_CBF_RETRIP_T7	CBF Retrip T7	CBF Retrip T7			
1535	SW	DDB_CB4_3PH_BKTRIP	CB4 BkTrip 3ph	CB4 BkTrip 3ph			Yes
1535	SW	DDB_CBF_RETRIP_T8	CBF Retrip T8	CBF Retrip T8			
1536	SW	DDB_CB5_3PH_RETRIP	CB5 ReTrip 3ph	CB5 ReTrip 3ph			Yes
1536	SW	DDB_CBF_RETRIP_T9	CBF Retrip T9	CBF Retrip T9			
1537	SW	DDB_CB5_3PH_BKTRIP	CB5 BkTrip 3ph	CB5 BkTrip 3ph			Yes
1537	SW	DDB_CBF_RETRIP_T10	CBF Retrip T10	CBF Retrip T10			
1538	SW	DDB_CBF_RETRIP_T11	CBF Retrip T11	CBF Retrip T11			
1539	SW	DDB_CBF_RETRIP_T12	CBF Retrip T12	CBF Retrip T12			
1540	SW	DDB_CBF_RETRIP_T13	CBF Retrip T13	CBF Retrip T13			
1541	SW	DDB_CBF_RETRIP_T14	CBF Retrip T14	CBF Retrip T14			
1542	SW	DDB_CBF_RETRIP_T15	CBF Retrip T15	CBF Retrip T15			
1543	SW	DDB_CBF_RETRIP_T16	CBF Retrip T16	CBF Retrip T16			
1544	SW	DDB_CBF_RETRIP_T17	CBF Retrip T17	CBF Retrip T17			
1545	SW	DDB_CBF_RETRIP_T18	CBF Retrip T18	CBF Retrip T18			
1546	SW	DDB_CBF_BKTRIP_Z1	Z1 CBF Back Trip	Z1 CBF Back Trip			
1547	SW	DDB_CBF_BKTRIP_Z2	Z2 CBF Back Trip	Z2 CBF Back Trip			
1548	SW	DDB_REMOTE_TRIP_T1	T1 Remote Trip By Diff or CBF	T1 Remote Trip By Diff or CBF			
1549	SW	DDB_REMOTE_TRIP_T2	T2 Remote Trip By Diff or CBF	T2 Remote Trip By Diff or CBF			
1550	SW	DDB_REMOTE_TRIP_T3	T3 Remote Trip By Diff or CBF	T3 Remote Trip By Diff or CBF			
1551	SW	DDB_REMOTE_TRIP_T4	T4 Remote Trip By Diff or CBF	T4 Remote Trip By Diff or CBF			
1552	SW	DDB_REMOTE_TRIP_T5	T5 Remote Trip By Diff or CBF	T5 Remote Trip By Diff or CBF			
1553	SW	DDB_REMOTE_TRIP_T6	T6 Remote Trip By Diff or CBF	T6 Remote Trip By Diff or CBF			
1554	SW	DDB_REMOTE_TRIP_T7	T7 Remote Trip By Diff or CBF	T7 Remote Trip By Diff or CBF			
1555	SW	DDB_REMOTE_TRIP_T8	T8 Remote Trip By Diff or CBF	T8 Remote Trip By Diff or CBF			

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
1556	SW	DDB_REMOTE_TRIP_T9	T9 Remote Trip By Diff or CBF	T9 Remote Trip By Diff or CBF			
1557	SW	DDB_REMOTE_TRIP_T10	T10 Remote Trip By Diff or CBF	T10 Remote Trip By Diff or CBF			
1558	SW	DDB_REMOTE_TRIP_T11	T11 Remote Trip By Diff or CBF	T11 Remote Trip By Diff or CBF			
1559	SW	DDB_REMOTE_TRIP_T12	T12 Remote Trip By Diff or CBF	T12 Remote Trip By Diff or CBF			
1560	SW	DDB_REMOTE_TRIP_T13	T13 Remote Trip By Diff or CBF	T13 Remote Trip By Diff or CBF			
1561	SW	DDB_REMOTE_TRIP_T14	T14 Remote Trip By Diff or CBF	T14 Remote Trip By Diff or CBF			
1562	SW	DDB_REMOTE_TRIP_T15	T15 Remote Trip By Diff or CBF	T15 Remote Trip By Diff or CBF			
1563	SW	DDB_REMOTE_TRIP_T16	T16 Remote Trip By Diff or CBF	T16 Remote Trip By Diff or CBF			
1564	SW	DDB_REMOTE_TRIP_T17	T17 Remote Trip By Diff or CBF	T17 Remote Trip By Diff or CBF			
1565	SW	DDB_REMOTE_TRIP_T18	T18 Remote Trip By Diff or CBF	T18 Remote Trip By Diff or CBF			
1566	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
1567	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
1568	SW	DDB_NPSOC1_STAGE1_START	Negative Sequence Overcurrent 1 I2>1 Start	NPOC1 I2>1 Start	Yes	Yes	Yes
1569	SW	DDB_NPSOC1_STAGE2_START	Negative Sequence Overcurrent 1 I2>2 Start	NPOC1 I2>2 Start	Yes	Yes	Yes
1570	SW	DDB_NPSOC1_STAGE3_START	Negative Sequence Overcurrent 1 I2>3 Start	NPOC1 I2>3 Start	Yes	Yes	Yes
1571	SW	DDB_NPSOC1_STAGE4_START	Negative Sequence Overcurrent 1 I2>4 Start	NPOC1 I2>4 Start	Yes	Yes	Yes
1572	SW	DDB_NPSOC2_STAGE1_START	Negative Sequence Overcurrent 2 I2>1 Start	NPOC2 I2>1 Start	Yes	Yes	Yes
1573	SW	DDB_NPSOC2_STAGE2_START	Negative Sequence Overcurrent 2 I2>2 Start	NPOC2 I2>2 Start	Yes	Yes	Yes
1574	SW	DDB_NPSOC2_STAGE3_START	Negative Sequence Overcurrent 2 I2>3 Start	NPOC2 I2>3 Start	Yes	Yes	Yes
1575	SW	DDB_NPSOC2_STAGE4_START	Negative Sequence Overcurrent 2 I2>4 Start	NPOC2 I2>4 Start	Yes	Yes	Yes
1576	SW	DDB_NPSOC3_STAGE1_START	Negative Sequence Overcurrent 3 I2>1 Start	NPOC3 I2>1 Start		Yes	Yes
1577	SW	DDB_NPSOC3_STAGE2_START	Negative Sequence Overcurrent 3 I2>2 Start	NPOC3 I2>2 Start		Yes	Yes
1578	SW	DDB_NPSOC3_STAGE3_START	Negative Sequence Overcurrent 3 I2>3 Start	NPOC3 I2>3 Start		Yes	Yes
1579	SW	DDB_NPSOC3_STAGE4_START	Negative Sequence Overcurrent 3 I2>4 Start	NPOC3 I2>4 Start		Yes	Yes
1580	SW	DDB_PUV_1_3PH_START	1st Stage Phase U/V Start 3ph	V<1 Start		Yes	Yes
1581	SW	DDB_PUV_1_PH_A_START	1st Stage Phase U/V Start A/AB	V<1 Start A/AB		Yes	Yes
1582	SW	DDB_PUV_1_PH_B_START	1st Stage Phase U/V Start B/BC	V<1 Start B/BC		Yes	Yes
1583	SW	DDB_PUV_1_PH_C_START	1st Stage Phase U/V Start C/CA	V<1 Start C/CA		Yes	Yes

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
1584	SW	DDB_PUV_2_3PH_START	2nd Stage Phase U/V Start 3ph	V<2 Start		Yes	Yes
1585	SW	DDB_PUV_2_PH_A_START	2nd Stage Phase U/V Start A/AB	V<2 Start A/AB		Yes	Yes
1586	SW	DDB_PUV_2_PH_B_START	2nd Stage Phase U/V Start B/BC	V<2 Start B/BC		Yes	Yes
1587	SW	DDB_PUV_2_PH_C_START	2nd Stage Phase U/V Start C/CA	V<2 Start C/CA		Yes	Yes
1588	SW	DDB_POV_1_3PH_START	1st Stage Phase O/V Start 3ph	V>1 Start		Yes	Yes
1589	SW	DDB_POV_1_PH_A_START	1st Stage Phase O/V Start A/AB	V>1 Start A/AB		Yes	Yes
1590	SW	DDB_POV_1_PH_B_START	1st Stage Phase O/V Start B/BC	V>1 Start B/BC		Yes	Yes
1591	SW	DDB_POV_1_PH_C_START	1st Stage Phase O/V Start C/CA	V>1 Start C/CA		Yes	Yes
1592	SW	DDB_POV_2_3PH_START	2nd Stage Phase O/V Start 3ph	V>2 Start		Yes	Yes
1593	SW	DDB_POV_2_PH_A_START	2nd Stage Phase O/V Start A/AB	V>2 Start A/AB		Yes	Yes
1594	SW	DDB_POV_2_PH_B_START	2nd Stage Phase O/V Start B/BC	V>2 Start B/BC		Yes	Yes
1595	SW	DDB_POV_2_PH_C_START	2nd Stage Phase O/V Start C/CA	V>2 Start C/CA		Yes	Yes
1596	SW	DDB_RESOV_1_START	1st Stage Residual O/V Start	VN>1 Start		Yes	Yes
1597	SW	DDB_RESOV_2_START	2nd Stage Residual O/V Start	VN>2 Start		Yes	Yes
1598	SW	DDB_VPERHZ_ALARM_START_1	w1 V/Hz> Alarm Start	W1 V/Hz> Alm Stat		Yes	Yes
1599	SW	DDB_VPERHZ_1_START_1	w1 V/Hz>1 Start	W1 V/Hz>1 Start		Yes	Yes
1600	SW	DDB_VPERHZ_2_START_1	w1 V/Hz>2 Start	W1 V/Hz>2 Start		Yes	Yes
1601	SW	DDB_VPERHZ_3_START_1	w1 V/Hz>3 Start	W1 V/Hz>3 Start		Yes	Yes
1602	SW	DDB_VPERHZ_4_START_1	w1 V/Hz>4 Start	W1 V/Hz>4 Start		Yes	Yes
1603	SW	DDB_VPERHZ_ALARM_START_2	w2 V/Hz> Alarm Start	W2 V/Hz> Alm Stat	Yes	Yes	Yes
1604	SW	DDB_VPERHZ_1_START_2	w2 V/Hz>1 Start	W2 V/Hz>1 Start	Yes	Yes	Yes
1605	SW	DDB_VPERHZ_2_START_2	w2 V/Hz>2 Start	W2 V/Hz>2 Start	Yes	Yes	Yes
1606	SW	DDB_VPERHZ_3_START_2	w2 V/Hz>3 Start	W2 V/Hz>3 Start	Yes	Yes	Yes
1607	SW	DDB_VPERHZ_4_START_2	w2 V/Hz>4 Start	W2 V/Hz>4 Start	Yes	Yes	Yes
1608	SW	DDB_UFREQ_1_START	Under Frequency Stage 1 Start	F<1 Start	Yes	Yes	Yes
1609	SW	DDB_UFREQ_2_START	Under Frequency Stage 2 Start	F<2 Start	Yes	Yes	Yes
1610	SW	DDB_UFREQ_3_START	Under Frequency Stage 3 Start	F<3 Start	Yes	Yes	Yes
1611	SW	DDB_UFREQ_4_START	Under Frequency Stage 4 Start	F<4 Start	Yes	Yes	Yes
1612	SW	DDB_OFREQ_1_START	Over Frequency Stage 1 Start	F>1 Start	Yes	Yes	Yes
1613	SW	DDB_OFREQ_2_START	Over Frequency Stage 2 Start	F>2 Start	Yes	Yes	Yes
1614	SW	DDB_CL_INPUT_1_ALARM_START	Current Loop Input 1 Alarm Start	CLI1 Alarm Start	Yes	Yes	Yes
1615	SW	DDB_CL_INPUT_2_ALARM_START	Current Loop Input 2 Alarm Start	CLI2 Alarm Start	Yes	Yes	Yes
1616	SW	DDB_CL_INPUT_3_ALARM_START	Current Loop Input 3 Alarm Start	CLI3 Alarm Start	Yes	Yes	Yes
1617	SW	DDB_CL_INPUT_4_ALARM_START	Current Loop Input 4 Alarm Start	CLI4 Alarm Start	Yes	Yes	Yes
1618	SW	DDB_CL_INPUT_1_TRIP_START	Current Loop Input 1 Trip Start	CLI1 Trip Start	Yes	Yes	Yes
1619	SW	DDB_CL_INPUT_2_TRIP_START	Current Loop Input 2 Trip Start	CLI2 Trip Start	Yes	Yes	Yes
1620	SW	DDB_CL_INPUT_3_TRIP_START	Current Loop Input 3 Trip Start	CLI3 Trip Start	Yes	Yes	Yes
1621	SW	DDB_CL_INPUT_4_TRIP_START	Current Loop Input 4 Trip Start	CLI4 Trip Start	Yes	Yes	Yes
1622	SW	DDB_NPSOV_1_START	Negative Sequence Over Voltage Start	V2> Start	Yes	Yes	Yes
1623	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
1624	SW	DDB_DZ1_OC_PH_A_START	T1 Phase A DeadZone Over Current start	T1 Phase A DeadZone Over Current start			

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
1625	SW	DDB_DZ2_OC_PH_A_START	T2 Phase A DeadZone Over Current start	T2 Phase A DeadZone Over Current start			
1626	SW	DDB_DZ3_OC_PH_A_START	T3 Phase A DeadZone Over Current start	T3 Phase A DeadZone Over Current start			
1627	SW	DDB_DZ4_OC_PH_A_START	T4 Phase A DeadZone Over Current start	T4 Phase A DeadZone Over Current start			
1628	SW	DDB_DZ5_OC_PH_A_START	T5 Phase A DeadZone Over Current start	T5 Phase A DeadZone Over Current start			
1629	SW	DDB_DZ6_OC_PH_A_START	T6 Phase A DeadZone Over Current start	T6 Phase A DeadZone Over Current start			
1630	SW	DDB_DZ7_OC_PH_A_START	T7 Phase A DeadZone Over Current start	T7 Phase A DeadZone Over Current start			
1631	SW	DDB_DZ8_OC_PH_A_START	T8 Phase A DeadZone Over Current start	T8 Phase A DeadZone Over Current start			
1632	SW	DDB_DZ9_OC_PH_A_START	T9 Phase A DeadZone Over Current start	T9 Phase A DeadZone Over Current start			
1633	SW	DDB_DZ10_OC_PH_A_START	T10 Phase A DeadZone Over Current start	T10 Phase A DeadZone Over Current start			
1634	SW	DDB_DZ11_OC_PH_A_START	T11 Phase A DeadZone Over Current start	T11 Phase A DeadZone Over Current start			
1635	SW	DDB_DZ12_OC_PH_A_START	T12 Phase A DeadZone Over Current start	T12 Phase A DeadZone Over Current start			
1636	SW	DDB_DZ13_OC_PH_A_START	T13 Phase A DeadZone Over Current start	T13 Phase A DeadZone Over Current start			
1637	SW	DDB_DZ14_OC_PH_A_START	T14 Phase A DeadZone Over Current start	T14 Phase A DeadZone Over Current start			
1638	SW	DDB_DZ15_OC_PH_A_START	T15 Phase A DeadZone Over Current start	T15 Phase A DeadZone Over Current start			
1639	SW	DDB_DZ16_OC_PH_A_START	T16 Phase A DeadZone Over Current start	T16 Phase A DeadZone Over Current start			
1640	SW	DDB_DZ17_OC_PH_A_START	T17 Phase A DeadZone Over Current start	T17 Phase A DeadZone Over Current start			
1641	SW	DDB_DZ18_OC_PH_A_START	T18 Phase A DeadZone Over Current start	T18 Phase A DeadZone Over Current start			
1642	SW	DDB_DZ1_OC_PH_B_START	T1 Phase B DeadZone Over Current start	T1 Phase B DeadZone Over Current start			

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
1643	SW	DDB_DZ2_OC_PH_B_START	T2 Phase B DeadZone Over Current start	T2 Phase B DeadZone Over Current start			
1644	SW	DDB_DZ3_OC_PH_B_START	T3 Phase B DeadZone Over Current start	T3 Phase B DeadZone Over Current start			
1645	SW	DDB_DZ4_OC_PH_B_START	T4 Phase B DeadZone Over Current start	T4 Phase B DeadZone Over Current start			
1646	SW	DDB_DZ5_OC_PH_B_START	T5 Phase B DeadZone Over Current start	T5 Phase B DeadZone Over Current start			
1647	SW	DDB_DZ6_OC_PH_B_START	T6 Phase B DeadZone Over Current start	T6 Phase B DeadZone Over Current start			
1648	SW	DDB_DZ7_OC_PH_B_START	T7 Phase B DeadZone Over Current start	T7 Phase B DeadZone Over Current start			
1649	SW	DDB_DZ8_OC_PH_B_START	T8 Phase B DeadZone Over Current start	T8 Phase B DeadZone Over Current start			
1650	SW	DDB_DZ9_OC_PH_B_START	T9 Phase B DeadZone Over Current start	T9 Phase B DeadZone Over Current start			
1651	SW	DDB_DZ10_OC_PH_B_START	T10 Phase B DeadZone Over Current start	T10 Phase B DeadZone Over Current start			
1652	SW	DDB_DZ11_OC_PH_B_START	T11 Phase B DeadZone Over Current start	T11 Phase B DeadZone Over Current start			
1653	SW	DDB_DZ12_OC_PH_B_START	T12 Phase B DeadZone Over Current start	T12 Phase B DeadZone Over Current start			
1654	SW	DDB_DZ13_OC_PH_B_START	T13 Phase B DeadZone Over Current start	T13 Phase B DeadZone Over Current start			
1655	SW	DDB_DZ14_OC_PH_B_START	T14 Phase B DeadZone Over Current start	T14 Phase B DeadZone Over Current start			
1656	SW	DDB_DZ15_OC_PH_B_START	T15 Phase B DeadZone Over Current start	T15 Phase B DeadZone Over Current start			
1657	SW	DDB_DZ16_OC_PH_B_START	T16 Phase B DeadZone Over Current start	T16 Phase B DeadZone Over Current start			
1658	SW	DDB_CT1_PHASE_A_ZCD	CT1 Phase A Zero Cross Detector	CT1A ZCD	Yes	Yes	Yes
1659	SW	DDB_CT1_PHASE_B_ZCD	CT1 Phase B Zero Cross Detector	CT1B ZCD	Yes	Yes	Yes
1660	SW	DDB_CT1_PHASE_C_ZCD	CT1 Phase C Zero Cross Detector	CT1C ZCD	Yes	Yes	Yes
1661	SW	DDB_CT2_PHASE_A_ZCD	CT2 Phase A Zero Cross Detector	CT2A ZCD	Yes	Yes	Yes
1662	SW	DDB_CT2_PHASE_B_ZCD	CT2 Phase B Zero Cross Detector	CT2B ZCD	Yes	Yes	Yes
1663	SW	DDB_CT2_PHASE_C_ZCD	CT2 Phase C Zero Cross Detector	CT2C ZCD	Yes	Yes	Yes
1664	SW	DDB_CT3_PHASE_A_ZCD	CT3 Phase A Zero Cross Detector	CT3A ZCD		Yes	Yes
1665	SW	DDB_CT3_PHASE_B_ZCD	CT3 Phase B Zero Cross Detector	CT3B ZCD		Yes	Yes

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
1666	SW	DDB_CT3_PHASE_C_ZCD	CT3 Phase C Zero Cross Detector	CT3C ZCD		Yes	Yes
1667	SW	DDB_CT4_PHASE_A_ZCD	CT4 Phase A Zero Cross Detector	CT4A ZCD			Yes
1668	SW	DDB_CT4_PHASE_B_ZCD	CT4 Phase B Zero Cross Detector	CT4B ZCD			Yes
1669	SW	DDB_CT4_PHASE_C_ZCD	CT4 Phase C Zero Cross Detector	CT4C ZCD			Yes
1670	SW	DDB_CT5_PHASE_A_ZCD	CT5 Phase A Zero Cross Detector	CT5A ZCD			Yes
1671	SW	DDB_CT5_PHASE_B_ZCD	CT5 Phase B Zero Cross Detector	CT5B ZCD			Yes
1672	SW	DDB_CT5_PHASE_C_ZCD	CT5 Phase C Zero Cross Detector	CT5C ZCD			Yes
1673	SW	DDB_CT1_IN_ZCD	CT1 IN Zero Cross Detector	CT1 In ZCD	Yes	Yes	Yes
1674	SW	DDB_CT2_IN_ZCD	CT2 IN Zero Cross Detector	CT2 In ZCD	Yes	Yes	Yes
1675	SW	DDB_CT3_IN_ZCD	CT3 IN Zero Cross Detector	CT3 In ZCD		Yes	Yes
1676	SW	DDB_CT4_IN_ZCD	CT3 IN Zero Cross Detector	CT4 In ZCD			Yes
1677	SW	DDB_CT5_IN_ZCD	CT4 IN Zero Cross Detector	CT5 In ZCD			Yes
1678	SW	DDB_CT1_PHASE_A_UNDERCURRENT	Fast under current: CT1 Phase A	CT1A UndCurrent	Yes	Yes	Yes
1679	SW	DDB_CT1_PHASE_B_UNDERCURRENT	Fast under current: CT1 Phase B	CT1B UndCurrent	Yes	Yes	Yes
1680	SW	DDB_CT1_PHASE_C_UNDERCURRENT	Fast under current: CT1 Phase C	CT1C UndCurrent	Yes	Yes	Yes
1681	SW	DDB_CT2_PHASE_A_UNDERCURRENT	Fast under current: CT2 Phase A	CT2A UndCurrent	Yes	Yes	Yes
1682	SW	DDB_CT2_PHASE_B_UNDERCURRENT	Fast under current: CT2 Phase B	CT2B UndCurrent	Yes	Yes	Yes
1683	SW	DDB_CT2_PHASE_C_UNDERCURRENT	Fast under current: CT2 Phase C	CT2C UndCurrent	Yes	Yes	Yes
1684	SW	DDB_CT3_PHASE_A_UNDERCURRENT	Fast under current: CT3 Phase A	CT3A UndCurrent		Yes	Yes
1685	SW	DDB_CT3_PHASE_B_UNDERCURRENT	Fast under current: CT3 Phase B	CT3B UndCurrent		Yes	Yes
1686	SW	DDB_CT3_PHASE_C_UNDERCURRENT	Fast under current: CT3 Phase C	CT3C UndCurrent		Yes	Yes
1687	SW	DDB_CT4_PHASE_A_UNDERCURRENT	Fast under current: CT4 Phase A	CT4A UndCurrent			Yes
1688	SW	DDB_CT4_PHASE_B_UNDERCURRENT	Fast under current: CT4 Phase B	CT4B UndCurrent			Yes
1689	SW	DDB_CT4_PHASE_C_UNDERCURRENT	Fast under current: CT4 Phase C	CT4C UndCurrent			Yes
1690	SW	DDB_CT5_PHASE_A_UNDERCURRENT	Fast under current: CT5 Phase A	CT5A UndCurrent			Yes
1691	SW	DDB_CT5_PHASE_B_UNDERCURRENT	Fast under current: CT5 Phase B	CT5B UndCurrent			Yes
1692	SW	DDB_CT5_PHASE_C_UNDERCURRENT	Fast under current: CT5 Phase C	CT5C UndCurrent			Yes
1693	SW	DDB_HV_UNDERCURRENT	Fast under current: HV	HV UndCurrent	Yes	Yes	Yes
1694	SW	DDB_LV_UNDERCURRENT	Fast under current: LV	LV UndCurrent	Yes	Yes	Yes
1695	SW	DDB_TV_UNDERCURRENT	Fast under current: TV	TV UndCurrent	Yes	Yes	Yes
1696	SW	DDB_CT1_PHS_A_UC_CT_EXCLUSION	CT1 Phase A Undercurrent	CT1 PhA UnderCur	Yes	Yes	Yes
1697	SW	DDB_CT1_PHS_B_UC_CT_EXCLUSION	CT1 Phase B Undercurrent	CT1 PhB UnderCur	Yes	Yes	Yes

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
1698	SW	DDB_CT1_PHS_C_UC_CT_EXCLUSION	CT1 Phase C Undercurrent	CT1 PhC UnderCur	Yes	Yes	Yes
1699	SW	DDB_CT2_PHS_A_UC_CT_EXCLUSION	CT2 Phase A Undercurrent	CT2 PhA UnderCur	Yes	Yes	Yes
1700	SW	DDB_CT2_PHS_B_UC_CT_EXCLUSION	CT2 Phase B Undercurrent	CT2 PhB UnderCur	Yes	Yes	Yes
1701	SW	DDB_CT2_PHS_C_UC_CT_EXCLUSION	CT2 Phase C Undercurrent	CT2 PhC UnderCur	Yes	Yes	Yes
1702	SW	DDB_CT3_PHS_A_UC_CT_EXCLUSION	CT3 Phase A Undercurrent	CT3 PhA UnderCur	Yes	Yes	Yes
1703	SW	DDB_CT3_PHS_B_UC_CT_EXCLUSION	CT3 Phase B Undercurrent	CT3 PhB UnderCur	Yes	Yes	Yes
1704	SW	DDB_CT3_PHS_C_UC_CT_EXCLUSION	CT3 Phase C Undercurrent	CT3 PhC UnderCur	Yes	Yes	Yes
1705	SW	DDB_CT4_PHS_A_UC_CT_EXCLUSION	CT4 Phase A Undercurrent	CT4 PhA UnderCur	Yes	Yes	Yes
1706	SW	DDB_CT4_PHS_B_UC_CT_EXCLUSION	CT4 Phase B Undercurrent	CT4 PhB UnderCur	Yes	Yes	Yes
1707	SW	DDB_CT4_PHS_C_UC_CT_EXCLUSION	CT4 Phase C Undercurrent	CT4 PhC UnderCur	Yes	Yes	Yes
1708	SW	DDB_CT5_PHS_A_UC_CT_EXCLUSION	CT5 Phase A Undercurrent	CT5 PhA UnderCur	Yes	Yes	Yes
1709	SW	DDB_CT5_PHS_B_UC_CT_EXCLUSION	CT5 Phase B Undercurrent	CT5 PhB UnderCur	Yes	Yes	Yes
1710	SW	DDB_CT5_PHS_C_UC_CT_EXCLUSION	CT5 Phase C Undercurrent	CT5 PhC UnderCur	Yes	Yes	Yes
1711	SW	DDB_CT1_IN_UNDERCURRENT	Fast under current: CT1 IN	CT1 In Undercur	Yes	Yes	Yes
1712	SW	DDB_CT2_IN_UNDERCURRENT	Fast under current: CT2 IN	CT2 In Undercur	Yes	Yes	Yes
1713	SW	DDB_CT3_IN_UNDERCURRENT	Fast under current: CT3 IN	CT3 In Undercur	Yes	Yes	Yes
1714	SW	DDB_CT4_IN_UNDERCURRENT	Fast under current: CT4 IN	CT4 In Undercur	Yes	Yes	Yes
1715	SW	DDB_CT5_IN_UNDERCURRENT	Fast under current: CT5 IN	CT5 In Undercur	Yes	Yes	Yes
1716	SW	DDB_PHASE_COMP_Z1_BLOCK_A	Z1 Phase A Phase Comparision Block	Z1 Phase A Phase Comparision Block	Yes	Yes	Yes
1717	SW	DDB_PHASE_COMP_Z1_BLOCK_B	Z1 Phase B Phase Comparision Block	Z1 Phase B Phase Comparision Block	Yes	Yes	Yes
1718	SW	DDB_PHASE_COMP_Z1_BLOCK_C	Z1 Phase C Phase Comparision Block	Z1 Phase C Phase Comparision Block	Yes	Yes	Yes
1719	SW	DDB_PHASE_COMP_Z2_BLOCK_A	Z2 Phase A Phase Comparision Block	Z2 Phase A Phase Comparision Block	Yes	Yes	Yes
1720	SW	DDB_PHASE_COMP_Z2_BLOCK_B	Z2 Phase B Phase Comparision Block	Z2 Phase B Phase Comparision Block	Yes	Yes	Yes
1721	SW	DDB_PHASE_COMP_Z2_BLOCK_C	Z2 Phase C Phase Comparision Block	Z2 Phase C Phase Comparision Block	Yes	Yes	Yes
1722	SW	DDB_UNUSED	DDB_UNUSED		Yes		
1723	SW	DDB_CT_EXCLU_DISABLE_PROT	The relay will be disabled when this DDB is TRUE.	CTexcl disa prot	Yes	Yes	Yes
1724	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
1725	SW	DDB_VTS_VAB_OPERATED	Vab Over Threshold	VTS VAB>	Yes	Yes	Yes
1726	SW	DDB_VTS_VBC_OPERATED	Vbc Over Threshold	VTS VBC>	Yes	Yes	Yes
1727	SW	DDB_VTS_VCA_OPERATED	Vca Over Threshold	VTS VCA>	Yes		

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
1728	SW	DDB_RTD_1_ALARM	RTD 1 Alarm	RTD 1 Alarm	Yes	Yes	Yes
1728	FL	DDB_CBF_Z1_BLOCKED	Z1 CBF in Block Status	Z1 CBF in Block Status			
1729	SW	DDB_RTD_2_ALARM	RTD 2 Alarm	RTD 2 Alarm	Yes	Yes	Yes
1729	FL	DDB_CBF_Z2_BLOCKED	Z2 CBF in Block Status	Z2 CBF in Block Status			
1730	SW	DDB_RTD_3_ALARM	RTD 3 Alarm	RTD 3 Alarm	Yes	Yes	Yes
1730	SW	DDB_DIFF_CZ_C_BLOCKED	CZ Diff Phase C in Block Status	CZ Diff Phase C in Block Status			
1731	SW	DDB_RTD_4_ALARM	RTD 4 Alarm	RTD 4 Alarm	Yes	Yes	Yes
1731	SW	DDB_PHASE_COMP_Z1_BLOCK	Z1 Phase comparison block (OR gate of PhaseA,B,C)	PhComp Blk Z1	Yes	Yes	Yes
1732	SW	DDB_RTD_5_ALARM	RTD 5 Alarm	RTD 5 Alarm	Yes	Yes	Yes
1732	SW	DDB_PHASE_COMP_Z2_BLOCK	Z2 Phase comparison block (OR gate of PhaseA,B,C)	PhComp Blk Z2	Yes	Yes	Yes
1733	SW	DDB_RTD_6_ALARM	RTD 6 Alarm	RTD 6 Alarm	Yes	Yes	Yes
1734	SW	DDB_RTD_7_ALARM	RTD 7 Alarm	RTD 7 Alarm	Yes	Yes	Yes
1735	SW	DDB_RTD_8_ALARM	RTD 8 Alarm	RTD 8 Alarm	Yes	Yes	Yes
1736	SW	DDB_RTD_9_ALARM	RTD 9 Alarm	RTD 9 Alarm	Yes	Yes	Yes
1737	SW	DDB_RTD_10_ALARM	RTD 10 Alarm	RTD 10 Alarm	Yes	Yes	Yes
1738	FL	DDB_VTS_ACCELERATE_INPUT	VTS Accelerate Indication	VTS Acc Ind	Yes	Yes	Yes
1739	FL	DDB_VTS_ANY_VOLTAGE_DEP_FN	Any Voltage Dependent	VTS Volt Dep	Yes	Yes	Yes
1740	SW	DDB_VTS_IA_OPERATED	Ia Over Threshold	VTS IA>	Yes	Yes	Yes
1741	SW	DDB_VTS_IB_OPERATED	Ib Over Threshold	VTS IB>	Yes	Yes	Yes
1742	SW	DDB_VTS_IC_OPERATED	Ic Over Threshold	VTS IC>	Yes	Yes	Yes
1743	SW	DDB_VTS_VA_OPERATED	Va Over Threshold	VTS VA>		Yes	Yes
1744	SW	DDB_VTS_VB_OPERATED	Vb Over Threshold	VTS VB>		Yes	Yes
1745	SW	DDB_VTS_VC_OPERATED	Vc Over Threshold	VTS VC>		Yes	Yes
1746	SW	DDB_VTS_I2_OPERATED	I2 Over Threshold	VTS I2>	Yes	Yes	Yes
1747	SW	DDB_VTS_V2_OPERATED	V2 Over Threshold	VTS V2>	Yes	Yes	Yes
1748	SW	DDB_VTS_DELTA_IA_OPERATED	Superimposed Ia Over Threshold	VTS IA delta>	Yes	Yes	Yes
1749	SW	DDB_VTS_DELTA_IB_OPERATED	Superimposed Ib Over Threshold	VTS IB delta>	Yes	Yes	Yes
1750	SW	DDB_VTS_DELTA_IC_OPERATED	Superimposed Ic Over Threshold	VTS IC delta>	Yes	Yes	Yes
1751	SW	DDB_FREQ_ABOVE_RANGE_LIMIT	Freq High	Freq High	Yes	Yes	Yes
1752	SW	DDB_FREQ_BELOW_RANGE_LIMIT	Freq Low	Freq Low	Yes	Yes	Yes
1753	SW	DDB_FREQ_NOT_FOUND	Freq Not Found	Freq Not found	Yes	Yes	Yes
1754	PSL	DDB_CB1_NOT_READY	CB1 Healthy	CB1 Not Ready			
1755	PSL	DDB_CB2_NOT_READY	CB2 Healthy	CB2 Not Ready			
1756	PSL	DDB_CB3_NOT_READY	CB3 Healthy	CB3 Not Ready	Yes		
1757	PSL	DDB_CB4_NOT_READY	CB4 Healthy	CB4 Not Ready	Yes	Yes	
1758	PSL	DDB_CB5_NOT_READY	CB5 Healthy	CB5 Not Ready	Yes	Yes	
1759	PSL	DDB_CB6_NOT_READY	CB6 Healthy	CB6 Not Ready	Yes	Yes	Yes
1760	PSL	DDB_CB7_NOT_READY	CB7 Healthy	CB7 Not Ready	Yes	Yes	Yes
1761	PSL	DDB_CB8_NOT_READY	CB8 Healthy	CB8 Not Ready	Yes	Yes	Yes
1762	PSL	DDB_CB9_NOT_READY	CB9 Healthy	CB9 Not Ready	Yes	Yes	Yes

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
1763	PSL	DDB_CB10_NOT_READY	CB10 Healthy	CB10 Not Ready	Yes	Yes	Yes
1764	PSL	DDB_CB11_NOT_READY	CB11 Healthy	CB11 Not Ready	Yes	Yes	Yes
1765	PSL	DDB_CB12_NOT_READY	CB12 Healthy	CB12 Not Ready	Yes	Yes	Yes
1766	PSL	DDB_CB13_NOT_READY	CB13 Healthy	CB13 Not Ready	Yes	Yes	Yes
1767	PSL	DDB_CB14_NOT_READY	CB14 Healthy	CB14 Not Ready	Yes	Yes	Yes
1768	PSL	DDB_CB15_NOT_READY	CB15 Healthy	CB15 Not Ready	Yes	Yes	Yes
1769	PSL	DDB_CB16_NOT_READY	CB16 Healthy	CB16 Not Ready	Yes	Yes	Yes
1770	PSL	DDB_CB17_NOT_READY	CB17 Healthy	CB17 Not Ready	Yes	Yes	Yes
1771	PSL	DDB_CB18_NOT_READY	CB18 Healthy	CB18 Not Ready	Yes	Yes	Yes
1772	FL	DDB_T1_HEALTHY	Terminal 1 in Healthy	Terminal 1 in Healthy			
1772	SW	DDB_ALL_POLEDEAD	All Poles Dead	All Poles Dead	Yes	Yes	Yes
1773	FL	DDB_T2_HEALTHY	Terminal 2 in Healthy	Terminal 2 in Healthy	Yes	Yes	Yes
1773	SW	DDB_ANY_POLEDEAD	Any Pole Dead	Any Pole Dead	Yes	Yes	Yes
1774	FL	DDB_T3_HEALTHY	Terminal 3 in Healthy	Terminal 3 in Healthy			
1774	SW	DDB_PHASE_A_POLEDEAD	Pole Dead A	Pole Dead A	Yes	Yes	Yes
1775	FL	DDB_T4_HEALTHY	Terminal 4 in Healthy	Terminal 4 in Healthy	Yes	Yes	Yes
1775	SW	DDB_PHASE_B_POLEDEAD	Pole Dead B	Pole Dead B	Yes	Yes	Yes
1776	FL	DDB_T5_HEALTHY	Terminal 5 in Healthy	Terminal 5 in Healthy			
1776	SW	DDB_PHASE_C_POLEDEAD	Pole Dead C	Pole Dead C	Yes	Yes	Yes
1777	FL	DDB_T6_HEALTHY	Terminal 6 in Healthy	Terminal 6 in Healthy	Yes	Yes	Yes
1777	SW	DDB_THROUGH_FAULT_OC_START	Through fault START	TF OC Start	Yes	Yes	Yes
1778	FL	DDB_T7_HEALTHY	Terminal 7 in Healthy	Terminal 7 in Healthy			
1778	SW	DDB_THROUGH_FAULT_OC_RESET	Through fault OC END	TF OC End	Yes	Yes	Yes
1779	FL	DDB_T8_HEALTHY	Terminal 8 in Healthy	Terminal 8 in Healthy	Yes	Yes	Yes
1779	SW	DDB_THROUGH_FAULT_RECORDER	Through fault TRIGGER	TF Recorder trig	Yes	Yes	Yes
1780	FL	DDB_T9_HEALTHY	Terminal 9 in Healthy	Terminal 9 in Healthy			
1781	FL	DDB_T10_HEALTHY	Terminal 10 in Healthy	Terminal 10 in Healthy	Yes	Yes	Yes
1782	FL	DDB_T11_HEALTHY	Terminal 11 in Healthy	Terminal 11 in Healthy			
1783	FL	DDB_T12_HEALTHY	Terminal 12 in Healthy	Terminal 12 in Healthy	Yes	Yes	Yes
1784	FL	DDB_T13_HEALTHY	Terminal 13 in Healthy	Terminal 13 in Healthy			
1785	FL	DDB_T14_HEALTHY	Terminal 14 in Healthy	Terminal 14 in Healthy			
1786	FL	DDB_T15_HEALTHY	Terminal 15 in Healthy	Terminal 15 in Healthy	Yes	Yes	Yes

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
1787	FL	DDB_T16_HEALTHY	Terminal 16 in Healthy	Terminal 16 in Healthy			
1788	FL	DDB_T17_HEALTHY	Terminal 17 in Healthy	Terminal 17 in Healthy	Yes	Yes	Yes
1789	FL	DDB_T18_HEALTHY	Terminal 18 in Healthy	Terminal 18 in Healthy			
1790	FL	DDB_CBF_NON_CURRENT_STAGE_TRIP	CB1F Non I Tr-1	CB1F Non I Tr-1	Yes	Yes	Yes
1791	FL	DDB_CBF_NON_I_PROT_TRIP_T1	CB Fail Non current trip T1	CBFNonITrip T1	Yes	Yes	Yes
1792	FL	DDB_CBF_NON_I_PROT_TRIP_T2	CB Fail Non current trip T2	CBFNonITrip T2	Yes	Yes	Yes
1793	FL	DDB_CBF_NON_I_PROT_TRIP_T3	CB Fail Non current trip T3	CBFNonITrip T3		Yes	Yes
1794	FL	DDB_CBF_NON_I_PROT_TRIP_T4	CB Fail Non current trip T4	CBFNonITrip T4			Yes
1795	FL	DDB_CBF_NON_I_PROT_TRIP_T5	CB Fail Non current trip T5	CBFNonITrip T5			Yes
1796	SW	DDB_UNUSED	DDB_UNUSED				
1797	SW	DDB_NIC_LINK_1_FAIL	Network Interface Card link 1 fail indication	ETH Link 1 Fail	Yes	Yes	Yes
1798	SW	DDB_NIC_LINK_2_FAIL	Network Interface Card link 2 fail indication	ETH Link 2 Fail	Yes	Yes	Yes
1799	SW	DDB_NIC_LINK_3_FAIL	Network Interface Card link 3 fail indication	ETH Link 3 Fail	Yes	Yes	Yes
1800	SW	DDB_DIFF_FAULT_Z1	Z1 Diff has Fault	Z1 Diff has Fault			
1800	SW	DDB_VTS_FAST_BLOCK	VTS Fast Block	VTS Fast Block	Yes	Yes	Yes
1801	SW	DDB_DIFF_FAULT_Z1_A	Z1 Diff Phase A has Fault	Z1 Diff Phase A has Fault			
1801	SW	DDB_VTS_SLOW_BLOCK	VTS Slow Block	VTS Slow Block	Yes	Yes	Yes
1802	SW	DDB_DIFF_FAULT_Z1_B	Z1 Diff Phase B has Fault	Z1 Diff Phase B has Fault			
1803	SW	DDB_DIFF_FAULT_Z1_C	Z1 Diff Phase C has Fault	Z1 Diff Phase C has Fault			
1804	SW	DDB_DIFF_FAULT_Z2	Z2 Diff has Fault	Z2 Diff has Fault			
1805	SW	DDB_DIFF_FAULT_Z2_A	Z2 Diff Phase A has Fault	Z2 Diff Phase A has Fault			
1806	SW	DDB_DIFF_FAULT_Z2_B	Z2 Diff Phase B has Fault	Z2 Diff Phase B has Fault			
1807	SW	DDB_DIFF_FAULT_Z2_C	Z2 Diff Phase C has Fault	Z2 Diff Phase C has Fault			
1808	SW	DDB_DIFF_FAULT_CZ	CZ Diff has Fault	CZ Diff has Fault			
1809	SW	DDB_DIFF_FAULT_CZ_A	CZ Diff Phase A has Fault	CZ Diff Phase A has Fault			
1810	SW	DDB_DIFF_FAULT_CZ_B	CZ Diff Phase B has Fault	CZ Diff Phase B has Fault			
1811	SW	DDB_DIFF_FAULT_CZ_C	CZ Diff Phase C has Fault	CZ Diff Phase C has Fault			
1812	SW	DDB_DIFF_Z1_BLOCKED	Z1 Diff in Block Status	Z1 Diff in Block Status			
1813	SW	DDB_DIFF_Z1_A_BLOCKED	Z1 Diff Phase A in Block Status	Z1 Diff Phase A in Block Status			
1814	SW	DDB_DIFF_Z1_B_BLOCKED	Z1 Diff Phase B in Block Status	Z1 Diff Phase B in Block Status			

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
1815	SW	DDB_DIFF_Z1_C_BLOCKED	Z1 Diff Phase C in Block Status	Z1 Diff Phase C in Block Status			
1816	SW	DDB_DIFF_Z2_BLOCKED	Z2 Diff in Block Status	Z2 Diff in Block Status			
1817	SW	DDB_DIFF_Z2_A_BLOCKED	Z2 Diff Phase A in Block Status	Z2 Diff Phase A in Block Status			
1818	SW	DDB_DIFF_Z2_B_BLOCKED	Z2 Diff Phase B in Block Status	Z2 Diff Phase B in Block Status			
1819	SW	DDB_DIFF_Z2_C_BLOCKED	Z2 Diff Phase C in Block Status	Z2 Diff Phase C in Block Status			
1820	SW	DDB_DIFF_CZ_BLOCKED	CZ Diff in Block Status	CZ Diff in Block Status			
1821	SW	DDB_DIFF_CZ_A_BLOCKED	CZ Diff Phase A in Block Status	CZ Diff Phase A in Block Status			
1822	SW	DDB_DIFF_CZ_B_BLOCKED	CZ Diff Phase B in Block Status	CZ Diff Phase B in Block Status			
1823	SW	DDB_UNUSED	DDB_UNUSED		Yes	Yes	Yes
1824	SW	DDB_CONTROL_1	Control Input 1	Control Input 1	Yes	Yes	Yes
1825	SW	DDB_CONTROL_2	Control Input 2	Control Input 2	Yes	Yes	Yes
1826	SW	DDB_CONTROL_3	Control Input 3	Control Input 3	Yes	Yes	Yes
1827	SW	DDB_CONTROL_4	Control Input 4	Control Input 4	Yes	Yes	Yes
1828	SW	DDB_CONTROL_5	Control Input 5	Control Input 5	Yes	Yes	Yes
1829	SW	DDB_CONTROL_6	Control Input 6	Control Input 6	Yes	Yes	Yes
1830	SW	DDB_CONTROL_7	Control Input 7	Control Input 7	Yes	Yes	Yes
1831	SW	DDB_CONTROL_8	Control Input 8	Control Input 8	Yes	Yes	Yes
1832	SW	DDB_CONTROL_9	Control Input 9	Control Input 9	Yes	Yes	Yes
1833	SW	DDB_CONTROL_10	Control Input 10	Control Input 10	Yes	Yes	Yes
1834	SW	DDB_CONTROL_11	Control Input 11	Control Input 11	Yes	Yes	Yes
1835	SW	DDB_CONTROL_12	Control Input 12	Control Input 12	Yes	Yes	Yes
1836	SW	DDB_CONTROL_13	Control Input 13	Control Input 13	Yes	Yes	Yes
1837	SW	DDB_CONTROL_14	Control Input 14	Control Input 14	Yes	Yes	Yes
1838	SW	DDB_CONTROL_15	Control Input 15	Control Input 15	Yes	Yes	Yes
1839	SW	DDB_CONTROL_16	Control Input 16	Control Input 16	Yes	Yes	Yes
1840	SW	DDB_CONTROL_17	Control Input 17	Control Input 17	Yes	Yes	Yes
1841	SW	DDB_CONTROL_18	Control Input 18	Control Input 18	Yes	Yes	Yes
1842	SW	DDB_CONTROL_19	Control Input 19	Control Input 19	Yes	Yes	Yes
1843	SW	DDB_CONTROL_20	Control Input 20	Control Input 20	Yes	Yes	Yes
1844	SW	DDB_CONTROL_21	Control Input 21	Control Input 21	Yes	Yes	Yes
1845	SW	DDB_CONTROL_22	Control Input 22	Control Input 22	Yes	Yes	Yes
1846	SW	DDB_CONTROL_23	Control Input 23	Control Input 23	Yes	Yes	Yes
1847	SW	DDB_CONTROL_24	Control Input 24	Control Input 24	Yes	Yes	Yes
1848	SW	DDB_CONTROL_25	Control Input 25	Control Input 25	Yes	Yes	Yes
1849	SW	DDB_CONTROL_26	Control Input 26	Control Input 26	Yes	Yes	Yes
1850	SW	DDB_CONTROL_27	Control Input 27	Control Input 27	Yes	Yes	Yes
1851	SW	DDB_CONTROL_28	Control Input 28	Control Input 28	Yes	Yes	Yes
1852	SW	DDB_CONTROL_29	Control Input 29	Control Input 29	Yes	Yes	Yes

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
1853	SW	DDB_CONTROL_30	Control Input 30	Control Input 30	Yes	Yes	Yes
1854	SW	DDB_CONTROL_31	Control Input 31	Control Input 31	Yes	Yes	Yes
1855	SW	DDB_CONTROL_32	Control Input 32	Control Input 32	Yes	Yes	Yes
1856	SW	DDB_GOOSEIN_1	Virtual Input 01	Virtual Input 01	Yes	Yes	Yes
1857	SW	DDB_GOOSEIN_2	Virtual Input 02	Virtual Input 02	Yes	Yes	Yes
1858	SW	DDB_GOOSEIN_3	Virtual Input 03	Virtual Input 03	Yes	Yes	Yes
1859	SW	DDB_GOOSEIN_4	Virtual Input 04	Virtual Input 04	Yes	Yes	Yes
1860	SW	DDB_GOOSEIN_5	Virtual Input 05	Virtual Input 05	Yes	Yes	Yes
1861	SW	DDB_GOOSEIN_6	Virtual Input 06	Virtual Input 06	Yes	Yes	Yes
1862	SW	DDB_GOOSEIN_7	Virtual Input 07	Virtual Input 07	Yes	Yes	Yes
1863	SW	DDB_GOOSEIN_8	Virtual Input 08	Virtual Input 08	Yes	Yes	Yes
1864	SW	DDB_GOOSEIN_9	Virtual Input 09	Virtual Input 09	Yes	Yes	Yes
1865	SW	DDB_GOOSEIN_10	Virtual Input 10	Virtual Input 10	Yes	Yes	Yes
1866	SW	DDB_GOOSEIN_11	Virtual Input 11	Virtual Input 11	Yes	Yes	Yes
1867	SW	DDB_GOOSEIN_12	Virtual Input 12	Virtual Input 12	Yes	Yes	Yes
1868	SW	DDB_GOOSEIN_13	Virtual Input 13	Virtual Input 13	Yes	Yes	Yes
1869	SW	DDB_GOOSEIN_14	Virtual Input 14	Virtual Input 14	Yes	Yes	Yes
1870	SW	DDB_GOOSEIN_15	Virtual Input 15	Virtual Input 15	Yes	Yes	Yes
1871	SW	DDB_GOOSEIN_16	Virtual Input 16	Virtual Input 16	Yes	Yes	Yes
1872	SW	DDB_GOOSEIN_17	Virtual Input 17	Virtual Input 17	Yes	Yes	Yes
1873	SW	DDB_GOOSEIN_18	Virtual Input 18	Virtual Input 18	Yes	Yes	Yes
1874	SW	DDB_GOOSEIN_19	Virtual Input 19	Virtual Input 19	Yes	Yes	Yes
1875	SW	DDB_GOOSEIN_20	Virtual Input 20	Virtual Input 20	Yes	Yes	Yes
1876	SW	DDB_GOOSEIN_21	Virtual Input 21	Virtual Input 21	Yes	Yes	Yes
1877	SW	DDB_GOOSEIN_22	Virtual Input 22	Virtual Input 22	Yes	Yes	Yes
1878	SW	DDB_GOOSEIN_23	Virtual Input 23	Virtual Input 23	Yes	Yes	Yes
1879	SW	DDB_GOOSEIN_24	Virtual Input 24	Virtual Input 24	Yes	Yes	Yes
1880	SW	DDB_GOOSEIN_25	Virtual Input 25	Virtual Input 25	Yes	Yes	Yes
1881	SW	DDB_GOOSEIN_26	Virtual Input 26	Virtual Input 26	Yes	Yes	Yes
1882	SW	DDB_GOOSEIN_27	Virtual Input 27	Virtual Input 27	Yes	Yes	Yes
1883	SW	DDB_GOOSEIN_28	Virtual Input 28	Virtual Input 28	Yes	Yes	Yes
1884	SW	DDB_GOOSEIN_29	Virtual Input 29	Virtual Input 29	Yes	Yes	Yes
1885	SW	DDB_GOOSEIN_30	Virtual Input 30	Virtual Input 30	Yes	Yes	Yes
1886	SW	DDB_GOOSEIN_31	Virtual Input 31	Virtual Input 31	Yes	Yes	Yes
1887	SW	DDB_GOOSEIN_32	Virtual Input 32	Virtual Input 32	Yes	Yes	Yes
1888	SW	DDB_GOOSEIN_33	Virtual Input 33	Virtual Input 33	Yes	Yes	Yes
1889	SW	DDB_GOOSEIN_34	Virtual Input 34	Virtual Input 34	Yes	Yes	Yes
1890	SW	DDB_GOOSEIN_35	Virtual Input 35	Virtual Input 35	Yes	Yes	Yes
1891	SW	DDB_GOOSEIN_36	Virtual Input 36	Virtual Input 36	Yes	Yes	Yes
1892	SW	DDB_GOOSEIN_37	Virtual Input 37	Virtual Input 37	Yes	Yes	Yes
1893	SW	DDB_GOOSEIN_38	Virtual Input 38	Virtual Input 38	Yes	Yes	Yes
1894	SW	DDB_GOOSEIN_39	Virtual Input 39	Virtual Input 39	Yes	Yes	Yes
1895	SW	DDB_GOOSEIN_40	Virtual Input 40	Virtual Input 40	Yes	Yes	Yes
1896	SW	DDB_GOOSEIN_41	Virtual Input 41	Virtual Input 41	Yes	Yes	Yes

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
1897	SW	DDB_GOOSEIN_42	Virtual Input 42	Virtual Input 42	Yes	Yes	Yes
1898	SW	DDB_GOOSEIN_43	Virtual Input 43	Virtual Input 43	Yes	Yes	Yes
1899	SW	DDB_GOOSEIN_44	Virtual Input 44	Virtual Input 44	Yes	Yes	Yes
1900	SW	DDB_GOOSEIN_45	Virtual Input 45	Virtual Input 45	Yes	Yes	Yes
1901	SW	DDB_GOOSEIN_46	Virtual Input 46	Virtual Input 46	Yes	Yes	Yes
1902	SW	DDB_GOOSEIN_47	Virtual Input 47	Virtual Input 47	Yes	Yes	Yes
1903	SW	DDB_GOOSEIN_48	Virtual Input 48	Virtual Input 48	Yes	Yes	Yes
1904	SW	DDB_GOOSEIN_49	Virtual Input 49	Virtual Input 49	Yes	Yes	Yes
1905	SW	DDB_GOOSEIN_50	Virtual Input 50	Virtual Input 50	Yes	Yes	Yes
1906	SW	DDB_GOOSEIN_51	Virtual Input 51	Virtual Input 51	Yes	Yes	Yes
1907	SW	DDB_GOOSEIN_52	Virtual Input 52	Virtual Input 52	Yes	Yes	Yes
1908	SW	DDB_GOOSEIN_53	Virtual Input 53	Virtual Input 53	Yes	Yes	Yes
1909	SW	DDB_GOOSEIN_54	Virtual Input 54	Virtual Input 54	Yes	Yes	Yes
1910	SW	DDB_GOOSEIN_55	Virtual Input 55	Virtual Input 55	Yes	Yes	Yes
1911	SW	DDB_GOOSEIN_56	Virtual Input 56	Virtual Input 56	Yes	Yes	Yes
1912	SW	DDB_GOOSEIN_57	Virtual Input 57	Virtual Input 57	Yes	Yes	Yes
1913	SW	DDB_GOOSEIN_58	Virtual Input 58	Virtual Input 58	Yes	Yes	Yes
1914	SW	DDB_GOOSEIN_59	Virtual Input 59	Virtual Input 59	Yes	Yes	Yes
1915	SW	DDB_GOOSEIN_60	Virtual Input 60	Virtual Input 60	Yes	Yes	Yes
1916	SW	DDB_GOOSEIN_61	Virtual Input 61	Virtual Input 61	Yes	Yes	Yes
1917	SW	DDB_GOOSEIN_62	Virtual Input 62	Virtual Input 62	Yes	Yes	Yes
1918	SW	DDB_GOOSEIN_63	Virtual Input 63	Virtual Input 63	Yes	Yes	Yes
1919	SW	DDB_GOOSEIN_64	Virtual Input 64	Virtual Input 64	Yes	Yes	Yes
1920	PSL	DDB_PSLINT_1	PSL Internal connection	PSL Int. 1	Yes	Yes	Yes
1921	PSL	DDB_PSLINT_2	PSL Internal connection	PSL Int. 2	Yes	Yes	Yes
1922	PSL	DDB_PSLINT_3	PSL Internal connection	PSL Int. 3	Yes	Yes	Yes
1923	PSL	DDB_PSLINT_4	PSL Internal connection	PSL Int. 4	Yes	Yes	Yes
1924	PSL	DDB_PSLINT_5	PSL Internal connection	PSL Int. 5	Yes	Yes	Yes
1925	PSL	DDB_PSLINT_6	PSL Internal connection	PSL Int. 6	Yes	Yes	Yes
1926	PSL	DDB_PSLINT_7	PSL Internal connection	PSL Int. 7	Yes	Yes	Yes
1927	PSL	DDB_PSLINT_8	PSL Internal connection	PSL Int. 8	Yes	Yes	Yes
1928	PSL	DDB_PSLINT_9	PSL Internal connection	PSL Int. 9	Yes	Yes	Yes
1929	PSL	DDB_PSLINT_10	PSL Internal connection	PSL Int. 10	Yes	Yes	Yes
1930	PSL	DDB_PSLINT_11	PSL Internal connection	PSL Int. 11	Yes	Yes	Yes
1931	PSL	DDB_PSLINT_12	PSL Internal connection	PSL Int. 12	Yes	Yes	Yes
1932	PSL	DDB_PSLINT_13	PSL Internal connection	PSL Int. 13	Yes	Yes	Yes
1933	PSL	DDB_PSLINT_14	PSL Internal connection	PSL Int. 14	Yes	Yes	Yes
1934	PSL	DDB_PSLINT_15	PSL Internal connection	PSL Int. 15	Yes	Yes	Yes
1935	PSL	DDB_PSLINT_16	PSL Internal connection	PSL Int. 16	Yes	Yes	Yes
1936	PSL	DDB_PSLINT_17	PSL Internal connection	PSL Int. 17	Yes	Yes	Yes
1937	PSL	DDB_PSLINT_18	PSL Internal connection	PSL Int. 18	Yes	Yes	Yes
1938	PSL	DDB_PSLINT_19	PSL Internal connection	PSL Int. 19	Yes	Yes	Yes
1939	PSL	DDB_PSLINT_20	PSL Internal connection	PSL Int. 20	Yes	Yes	Yes
1940	PSL	DDB_PSLINT_21	PSL Internal connection	PSL Int. 21	Yes	Yes	Yes

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
1941	PSL	DDB_PSLINT_22	PSL Internal connection	PSL Int. 22	Yes	Yes	Yes
1942	PSL	DDB_PSLINT_23	PSL Internal connection	PSL Int. 23	Yes	Yes	Yes
1943	PSL	DDB_PSLINT_24	PSL Internal connection	PSL Int. 24	Yes	Yes	Yes
1944	PSL	DDB_PSLINT_25	PSL Internal connection	PSL Int. 25	Yes	Yes	Yes
1945	PSL	DDB_PSLINT_26	PSL Internal connection	PSL Int. 26	Yes	Yes	Yes
1946	PSL	DDB_PSLINT_27	PSL Internal connection	PSL Int. 27	Yes	Yes	Yes
1947	PSL	DDB_PSLINT_28	PSL Internal connection	PSL Int. 28	Yes	Yes	Yes
1948	PSL	DDB_PSLINT_29	PSL Internal connection	PSL Int. 29	Yes	Yes	Yes
1949	PSL	DDB_PSLINT_30	PSL Internal connection	PSL Int. 30	Yes	Yes	Yes
1950	PSL	DDB_PSLINT_31	PSL Internal connection	PSL Int. 31	Yes	Yes	Yes
1951	PSL	DDB_PSLINT_32	PSL Internal connection	PSL Int. 32	Yes	Yes	Yes
1952	PSL	DDB_PSLINT_33	PSL Internal connection	PSL Int. 33	Yes	Yes	Yes
1953	PSL	DDB_PSLINT_34	PSL Internal connection	PSL Int. 34	Yes	Yes	Yes
1954	PSL	DDB_PSLINT_35	PSL Internal connection	PSL Int. 35	Yes	Yes	Yes
1955	PSL	DDB_PSLINT_36	PSL Internal connection	PSL Int. 36	Yes	Yes	Yes
1956	PSL	DDB_PSLINT_37	PSL Internal connection	PSL Int. 37	Yes	Yes	Yes
1957	PSL	DDB_PSLINT_38	PSL Internal connection	PSL Int. 38	Yes	Yes	Yes
1958	PSL	DDB_PSLINT_39	PSL Internal connection	PSL Int. 39	Yes	Yes	Yes
1959	PSL	DDB_PSLINT_40	PSL Internal connection	PSL Int. 40	Yes	Yes	Yes
1960	PSL	DDB_PSLINT_41	PSL Internal connection	PSL Int. 41	Yes	Yes	Yes
1961	PSL	DDB_PSLINT_42	PSL Internal connection	PSL Int. 42	Yes	Yes	Yes
1962	PSL	DDB_PSLINT_43	PSL Internal connection	PSL Int. 43	Yes	Yes	Yes
1963	PSL	DDB_PSLINT_44	PSL Internal connection	PSL Int. 44	Yes	Yes	Yes
1964	PSL	DDB_PSLINT_45	PSL Internal connection	PSL Int. 45	Yes	Yes	Yes
1965	PSL	DDB_PSLINT_46	PSL Internal connection	PSL Int. 46	Yes	Yes	Yes
1966	PSL	DDB_PSLINT_47	PSL Internal connection	PSL Int. 47	Yes	Yes	Yes
1967	PSL	DDB_PSLINT_48	PSL Internal connection	PSL Int. 48	Yes	Yes	Yes
1968	PSL	DDB_PSLINT_49	PSL Internal connection	PSL Int. 49	Yes	Yes	Yes
1969	PSL	DDB_PSLINT_50	PSL Internal connection	PSL Int. 50	Yes	Yes	Yes
1970	PSL	DDB_PSLINT_51	PSL Internal connection	PSL Int. 51	Yes	Yes	Yes
1971	PSL	DDB_PSLINT_52	PSL Internal connection	PSL Int. 52	Yes	Yes	Yes
1972	PSL	DDB_PSLINT_53	PSL Internal connection	PSL Int. 53	Yes	Yes	Yes
1973	PSL	DDB_PSLINT_54	PSL Internal connection	PSL Int. 54	Yes	Yes	Yes
1974	PSL	DDB_PSLINT_55	PSL Internal connection	PSL Int. 55	Yes	Yes	Yes
1975	PSL	DDB_PSLINT_56	PSL Internal connection	PSL Int. 56	Yes	Yes	Yes
1976	PSL	DDB_PSLINT_57	PSL Internal connection	PSL Int. 57	Yes	Yes	Yes
1977	PSL	DDB_PSLINT_58	PSL Internal connection	PSL Int. 58	Yes	Yes	Yes
1978	PSL	DDB_PSLINT_59	PSL Internal connection	PSL Int. 59	Yes	Yes	Yes
1979	PSL	DDB_PSLINT_60	PSL Internal connection	PSL Int. 60	Yes	Yes	Yes
1980	PSL	DDB_PSLINT_61	PSL Internal connection	PSL Int. 61	Yes	Yes	Yes
1981	PSL	DDB_PSLINT_62	PSL Internal connection	PSL Int. 62	Yes	Yes	Yes
1982	PSL	DDB_PSLINT_63	PSL Internal connection	PSL Int. 63	Yes	Yes	Yes
1983	PSL	DDB_PSLINT_64	PSL Internal connection	PSL Int. 64	Yes	Yes	Yes
1984	PSL	DDB_PSLINT_65	PSL Internal connection	PSL Int. 65	Yes	Yes	Yes

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
1985	PSL	DDB_PSLINT_66	PSL Internal connection	PSL Int. 66	Yes	Yes	Yes
1986	PSL	DDB_PSLINT_67	PSL Internal connection	PSL Int. 67	Yes	Yes	Yes
1987	PSL	DDB_PSLINT_68	PSL Internal connection	PSL Int. 68	Yes	Yes	Yes
1988	PSL	DDB_PSLINT_69	PSL Internal connection	PSL Int. 69	Yes	Yes	Yes
1989	PSL	DDB_PSLINT_70	PSL Internal connection	PSL Int. 70	Yes	Yes	Yes
1990	PSL	DDB_PSLINT_71	PSL Internal connection	PSL Int. 71	Yes	Yes	Yes
1991	PSL	DDB_PSLINT_72	PSL Internal connection	PSL Int. 72	Yes	Yes	Yes
1992	PSL	DDB_PSLINT_73	PSL Internal connection	PSL Int. 73	Yes	Yes	Yes
1993	PSL	DDB_PSLINT_74	PSL Internal connection	PSL Int. 74	Yes	Yes	Yes
1994	PSL	DDB_PSLINT_75	PSL Internal connection	PSL Int. 75	Yes	Yes	Yes
1995	PSL	DDB_PSLINT_76	PSL Internal connection	PSL Int. 76	Yes	Yes	Yes
1996	PSL	DDB_PSLINT_77	PSL Internal connection	PSL Int. 77	Yes	Yes	Yes
1997	PSL	DDB_PSLINT_78	PSL Internal connection	PSL Int. 78	Yes	Yes	Yes
1998	PSL	DDB_PSLINT_79	PSL Internal connection	PSL Int. 79	Yes	Yes	Yes
1999	PSL	DDB_PSLINT_80	PSL Internal connection	PSL Int. 80	Yes	Yes	Yes
2000	PSL	DDB_PSLINT_81	PSL Internal connection	PSL Int. 81	Yes	Yes	Yes
2001	PSL	DDB_PSLINT_82	PSL Internal connection	PSL Int. 82	Yes	Yes	Yes
2002	PSL	DDB_PSLINT_83	PSL Internal connection	PSL Int. 83	Yes	Yes	Yes
2003	PSL	DDB_PSLINT_84	PSL Internal connection	PSL Int. 84	Yes	Yes	Yes
2004	PSL	DDB_PSLINT_85	PSL Internal connection	PSL Int. 85	Yes	Yes	Yes
2005	PSL	DDB_PSLINT_86	PSL Internal connection	PSL Int. 86	Yes	Yes	Yes
2006	PSL	DDB_PSLINT_87	PSL Internal connection	PSL Int. 87	Yes	Yes	Yes
2007	PSL	DDB_PSLINT_88	PSL Internal connection	PSL Int. 88	Yes	Yes	Yes
2008	PSL	DDB_PSLINT_89	PSL Internal connection	PSL Int. 89	Yes	Yes	Yes
2009	PSL	DDB_PSLINT_90	PSL Internal connection	PSL Int. 90	Yes	Yes	Yes
2010	PSL	DDB_PSLINT_91	PSL Internal connection	PSL Int. 91	Yes	Yes	Yes
2011	PSL	DDB_PSLINT_92	PSL Internal connection	PSL Int. 92	Yes	Yes	Yes
2012	PSL	DDB_PSLINT_93	PSL Internal connection	PSL Int. 93	Yes	Yes	Yes
2013	PSL	DDB_PSLINT_94	PSL Internal connection	PSL Int. 94	Yes	Yes	Yes
2014	PSL	DDB_PSLINT_95	PSL Internal connection	PSL Int. 95	Yes	Yes	Yes
2015	PSL	DDB_PSLINT_96	PSL Internal connection	PSL Int. 96	Yes	Yes	Yes
2016	PSL	DDB_PSLINT_97	PSL Internal connection	PSL Int. 97	Yes	Yes	Yes
2017	PSL	DDB_PSLINT_98	PSL Internal connection	PSL Int. 98	Yes	Yes	Yes
2018	PSL	DDB_PSLINT_99	PSL Internal connection	PSL Int. 99	Yes	Yes	Yes
2019	PSL	DDB_PSLINT_100	PSL Internal connection	PSL Int. 100	Yes	Yes	Yes
2020	PSL	DDB_PSLINT_101	PSL Internal connection	PSL Int. 101	Yes	Yes	Yes
2021	PSL	DDB_PSLINT_102	PSL Internal connection	PSL Int. 102	Yes	Yes	Yes
2022	PSL	DDB_PSLINT_103	PSL Internal connection	PSL Int. 103	Yes	Yes	Yes
2023	PSL	DDB_PSLINT_104	PSL Internal connection	PSL Int. 104	Yes	Yes	Yes
2024	PSL	DDB_PSLINT_105	PSL Internal connection	PSL Int. 105	Yes	Yes	Yes
2025	PSL	DDB_PSLINT_106	PSL Internal connection	PSL Int. 106	Yes	Yes	Yes
2026	PSL	DDB_PSLINT_107	PSL Internal connection	PSL Int. 107	Yes	Yes	Yes
2027	PSL	DDB_PSLINT_108	PSL Internal connection	PSL Int. 108	Yes	Yes	Yes
2028	PSL	DDB_PSLINT_109	PSL Internal connection	PSL Int. 109	Yes	Yes	Yes

DDB No	Source	Element Name	Description	English Text	P642	P643	P645
2029	PSL	DDB_PSLINT_110	PSL Internal connection	PSL Int. 110	Yes	Yes	Yes
2030	PSL	DDB_PSLINT_111	PSL Internal connection	PSL Int. 111	Yes	Yes	Yes
2031	PSL	DDB_PSLINT_112	PSL Internal connection	PSL Int. 112	Yes	Yes	Yes
2032	PSL	DDB_PSLINT_113	PSL Internal connection	PSL Int. 113	Yes	Yes	Yes
2033	PSL	DDB_PSLINT_114	PSL Internal connection	PSL Int. 114	Yes	Yes	Yes
2034	PSL	DDB_PSLINT_115	PSL Internal connection	PSL Int. 115	Yes	Yes	Yes
2035	PSL	DDB_PSLINT_116	PSL Internal connection	PSL Int. 116	Yes	Yes	Yes
2036	PSL	DDB_PSLINT_117	PSL Internal connection	PSL Int. 117	Yes	Yes	Yes
2037	PSL	DDB_PSLINT_118	PSL Internal connection	PSL Int. 118	Yes	Yes	Yes
2038	PSL	DDB_PSLINT_119	PSL Internal connection	PSL Int. 119	Yes	Yes	Yes
2039	PSL	DDB_PSLINT_120	PSL Internal connection	PSL Int. 120	Yes	Yes	Yes
2040	PSL	DDB_PSLINT_121	PSL Internal connection	PSL Int. 121	Yes	Yes	Yes
2041	PSL	DDB_PSLINT_122	PSL Internal connection	PSL Int. 122	Yes	Yes	Yes
2042	PSL	DDB_PSLINT_123	PSL Internal connection	PSL Int. 123	Yes	Yes	Yes
2043	PSL	DDB_PSLINT_124	PSL Internal connection	PSL Int. 124	Yes	Yes	Yes
2044	PSL	DDB_PSLINT_125	PSL Internal connection	PSL Int. 125	Yes	Yes	Yes
2045	PSL	DDB_PSLINT_126	PSL Internal connection	PSL Int. 126	Yes	Yes	Yes
2046	PSL	DDB_PSLINT_127	PSL Internal connection	PSL Int. 127	Yes	Yes	Yes
2047	PSL	DDB_PSLINT_128	PSL Internal connection	PSL Int. 128	Yes	Yes	Yes

Table 1 - Description of available logic nodes

2.1 Factory Default Programmable Scheme Logic (PSL)

The following section details the default settings of the PSL.
The P642/P643/P645 model options are shown in Table 2:

Model	Opto inputs	Relay outputs
P642xxxxxxxxxL	8-12	8-12
P643xxxxxxxxxM	16-24	16-24
P645xxxxxxxxxM	16-24	16-24

Table 2 - P642/P643/P645 model options

2.2 Logic Input Mapping

The default mappings for the opto-isolated inputs are shown in Table 3, Table 4 and Table 5.

2.2.1 Logic Input Mapping for P642

Opto-Input No	P642 Relay Text	Function
1	Input L1	(L1 Setting Group) DDB_SG_SELECTOR_X1
2	Input L2	(L2 Setting Group) DDB_SG_SELECTOR_1X
3	Input L3	(L3 Ext CB1 Trip) DDB_EXT_3PH_TRIP1
4	Input L4	(L4 Ext CB2 Trip) DDB_EXT_3PH_TRIP2
5	Input L5	(L5 RESET Rly & LEDS) DDB_RESET_RELAYS_LEDS
6	Input L6	(L6 Unused)
7	Input L7	(L7 CB1 Closed) DDB_CB1_AUX_3PH_CLOSED
8	Input L8	(L8 CB2 Closed) DDB_CB2_AUX_3PH_CLOSED

Table 3 - Logic input mappings for P642

2.2.2 Logic Input Mapping for P643

Opto-Input No	P643 Relay Text	Function
1	Input L1	(L1 Setting Group) DDB_SG_SELECTOR_X1
2	Input L2	(L2 Setting Group) DDB_SG_SELECTOR_1X
3	Input L3	(L3 Ext CB1 Trip) DDB_EXT_3PH_TRIP1
4	Input L4	(L4 Ext CB2 Trip) DDB_EXT_3PH_TRIP2
5	Input L5	(L5 RESET Rly & LEDS) DDB_RESET_RELAYS_LEDS
6	Input L6	(L6 Ext CB3 Trip) DDB_EXT_3PH_TRIP3
7	Input L7	(L7 CB1 Closed) DDB_CB1_AUX_3PH_CLOSED
8	Input L8	(L8 CB2 Closed) DDB_CB2_AUX_3PH_CLOSED
9	Input L9	(L9 CB3 Closed) DDB_CB3_AUX_3PH_CLOSED

Table 4 - Logic input mappings for P643

2.2.3 Logic Input Mapping for P645

Opto-Input No	P645 Relay Text	Function
1	Input L1	(L1 Setting Group) DDB_SG_SELECTOR_X1
2	Input L2	(L2 Setting Group) DDB_SG_SELECTOR_1X
3	Input L3	(L3 Ext CB1 Trip) DDB_EXT_3PH_TRIP1
4	Input L4	(L4 Ext CB2 Trip) DDB_EXT_3PH_TRIP2
5	Input L5	(L5 RESET Rly & LEDS) DDB_RESET_RELAYS_LEDS
6	Input L6	(L6 Ext CB3 Trip) DDB_EXT_3PH_TRIP3
7	Input L7	(L7 CB1 Closed) DDB_CB1_AUX_3PH_CLOSED
8	Input L8	(L8 CB1 Closed) DDB_CB2_AUX_3PH_CLOSED
9	Input L9	(L9 CB1 Closed) DDB_CB3_AUX_3PH_CLOSED
10	Input L10	(L10 CB1 Closed) DDB_CB4_AUX_3PH_CLOSED
11	Input L11	(L11 CB1 Closed) DDB_CB5_AUX_3PH_CLOSED
12	Input L12	(L12 Ext CB4 Trip) DDB_EXT_3PH_TRIP4
13	Input L13	(L13 Ext CB5 Trip) DDB_EXT_3PH_TRIP5

Table 5 - Logic input mappings for P645

2.3 Relay Output Contact Mapping

The default mappings for the relay output contacts are shown in Table 6.

Relay Model	Relay Contact No	Relay Text	Relay Conditioner	Function
P642, P643, P645	1	Output R1	Pickup (P642) Dwell Timer 100 ms (P643, P645)	DDB_OUTPUT_CON_1 (R1 HV Backup TRIP)
P642, P643, P645	2	Output R2	Pickup (P642) Dwell Timer 100 ms (P643, P645)	DDB_OUTPUT_CON_2 (R2 LV Backup TRIP)
P642, P643, P645	3	Output R3	Pickup (P642) Dwell Timer 100 ms (P643, P645)	DDB_OUTPUT_CON_3 (R3 ANY TRIP)
P642, P643, P645	4	Output R4	Pickup (P642) Delayed Drop-off timer 500 ms (P643, P645)	DDB_OUTPUT_CON_4 (R4 GENERAL ALARM)
P642, P643, P645	5	Output R5	Pickup (P642) Dwell Timer 100 ms (P643, P645)	DDB_OUTPUT_CON_5 (R5 CB FAIL)
P642, P643, P645	6	Output R6	Pickup (P642) Dwell Timer 100 ms (P643,P645)	DDB_OUTPUT_CON_6 (R6 CB FAIL)
P643, P645	7	Output R7	Pickup (P642) Dwell Timer 100 ms (P643, P645)	DDB_OUTPUT_CON_7 (R7 ANY DIFF TRIP)
P643, P645	8	Output R8	Pickup (P642) Dwell Timer 100 ms (P643, P645)	DDB_OUTPUT_CON_8 (R8 ANY DIFF TRIP)
P643, P645	9	Output R9	Dwell Timer 100 ms (P643, P645 only)	DDB_OUTPUT_CON_9 (R9 ANY TRIP)
P643, P645	10	Output R10	Dwell Timer 100 ms (P645 only)	DDB_OUTPUT_CON_10 (R10 ANY TRIP)
P643, P645	11	Output R11	Delayed Drop-off timer 500 ms (P643, P645 only)	DDB_OUTPUT_CON_11 (R11 V/Hz PRE-TRIP ALM)
P643, P645	12	Output R12	Delayed Drop-off timer 500 ms (P643, P645 only)	DDB_OUTPUT_CON_12 (R12 TOL PRE-TRIP ALM)
P643, P645	13	Output R13	Dwell Timer 100 ms (P643, P645 only)	DDB_OUTPUT_CON_13 (R13 TV BACKUP TRIP)
P643, P645	14	Output R14	Dwell Timer 100 ms (P643, P645 only)	DDB_OUTPUT_CON_14 (R14 CB FAIL)
P645	15	Output R15	Dwell Timer 100 ms (P645 only)	DDB_OUTPUT_CON_15 (R15 CB FAIL)
P645	16	Output R16	Dwell Timer 100 ms (P645 only)	DDB_OUTPUT_CON_16 (R16 CB FAIL)
P645	17 to 32	Not Used		

Note *To generate a fault record, connect one or several contacts to the "Fault Record Trigger" in PSL. The triggering contact should be 'self reset' and not latching. If a latching contact is used the fault record is not generated until the contact has fully reset.*

Table 6 - Relay output contact mapping

2.4 Programmable LED Output Mapping

The default mappings for the programmable LEDs are shown in Table 7.
The P642 has red LEDs only, whereas the P643 and P645 also have tri-colour LEDS (red/yellow/green).

Relay Model	LED No	LED Input Connection/Text	Latched	P645 LED Function Indication
P642, P643, P645	1	LED 1 Red	Yes	Diff Trip
P642, P643, P645	2	LED 2 Red	Yes	Ref Trip
P642, P643, P645	3	LED 3 Red	Yes	Top Oil and Spot Thermal Trip
P642, P643, P645	4	LED 4 Red	Yes	V or F Trip
P642, P643, P645	5	LED 5 Red	Yes	HV Backup Trip
P642, P643, P645	6	LED 6 Red	Yes	LV Backup Trip
P642, P643, P645	7	LED 7 Red	Yes	TV Backup Trip
P642, P643, P645	8	LED 8 Red	Yes	CB Fail
P643, P645	9	Fnkey Led1	No	Spare
P643, P645	10	Fnkey Led2	No	Spare
P643, P645	11	Fnkey LED3	No	Spare
P643, P645	12	Fnkey Led4 Red (Fnct Key is Toggled Mode)	No	Spare
P643, P645	13	Fnkey LED5 Red (Fnct Key is Toggled Mode)	No	Setting Group 2 Enabled
P643, P645	14	Fnkey LED6 Yellow	No	Overfluxing Reset
P643, P645	15	Fnkey LED7 Yellow (Fnct Key Is Normal Mode)	No	Thermal Overload Reset
P643, P645	16	Fnkey LED8 Yellow (Fnct Key Is Normal Mode)	No	Loss Of Life Reset
P643, P645	17	Fnkey LED9 Yellow (Fnct Key Is Normal Mode)	No	Relay and LED Reset
P643, P645	18	Fnkey LED10 Yellow (Fnct Key Is Normal Mode)	No	Disturbance Recorder Trigger
P643, P645	19 to 24	Not Used		

Table 7 - Programmable LED output mapping

2.5 Fault Recorder Start Mapping

The default mapping for the signal which initiates a fault record is shown in Table 8.

Initiating signals	Output from OR gate (fault trigger)
DDB_TRIP_INITIATE	DDB_FAULT_RECORDER_START (Initiate fault recording from main protection trip)
DDB_THROUGH_FAULT_ALM	

Table 8 - Fault recorder start mapping

2.6 PSL Data Column

The relay contains a PSL DATA column that can be used to track PSL modifications. A total of 12 cells are contained in the PSL DATA column, 3 for each setting group. The function for each cell is shown below:

Grp PSL Ref	When downloading a PSL to the relay, the user will be prompted to enter which groups the PSL is for and a reference ID. The first 32 characters of the reference ID will be displayed in this cell. The ◊ and ◊ keys can be used to scroll through 32 characters as only 16 can be displayed at any one time.
18 Nov 2002 08:59:32.047	This cell displays the date and time when the PSL was down loaded to the relay.
Grp 1 PSL ID - 2062813232	This is a unique number for the PSL that has been entered. Any change in the PSL will result in a different number being displayed.

Note *The above cells are repeated for each setting group.*

3 VIEWING AND PRINTING DEFAULT PSL DIAGRAMS

3.1 Typical Mappings

It is possible to view and print the default PSL diagrams for the device. Typically, these diagrams allow you to see these mappings:

- Opto Input Mappings
- Output Relay Mappings
- LED Mappings
- Start Indications
- Phase Trip Mappings
- System Check Mapping

Important	***The following PSL diagrams show the DDB numbers for a specific MiCOM product, with a specific software version to run on a specific hardware platform. Descriptions, DDB Numbers, Inputs and Outputs may vary for different products, software or hardware.***

3.2 Download and Print PSL Diagrams

To download and print the default PSL diagrams for the device:

1. Close Easergy Studio.
2. Select **Programs** > then navigate through to > **Easergy Studio** > **Data Model Manager**.
3. Click **Add** then **Next**.
4. Click **Internet** then **Next**.
5. Select your language then click **Next**.
6. From the tree view, select the model and software version.
7. Click **Install**. When complete click **OK**.
8. Close the Data Model Manager and start Easergy Studio.
9. Select Tools > PSL Editor (Px40).
10. In the PSL Editor select **File** > **Open**. The downloaded PSL files are in C:\Program Files\ directory located in the \Easergy Studio\Courier\PSL\Defaults sub-directory.
11. Highlight the required PSL diagram and select **File** > **Print**.

4 MICOM P642 PSL DIAGRAMS

4.1 Any Trip Mapping

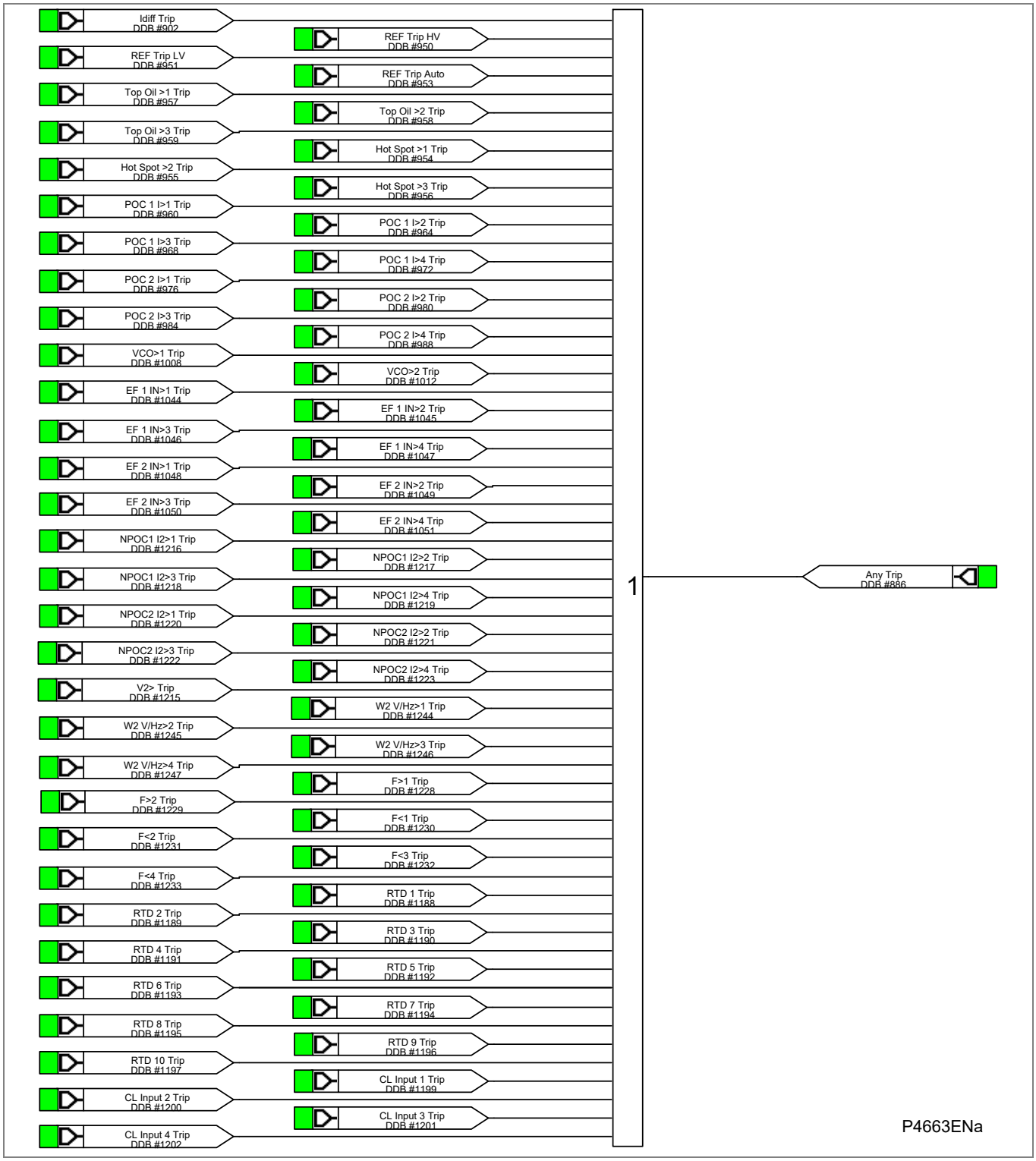


Figure 1 - P642 - Any trip mappings

4.2 Back up Trip Logic

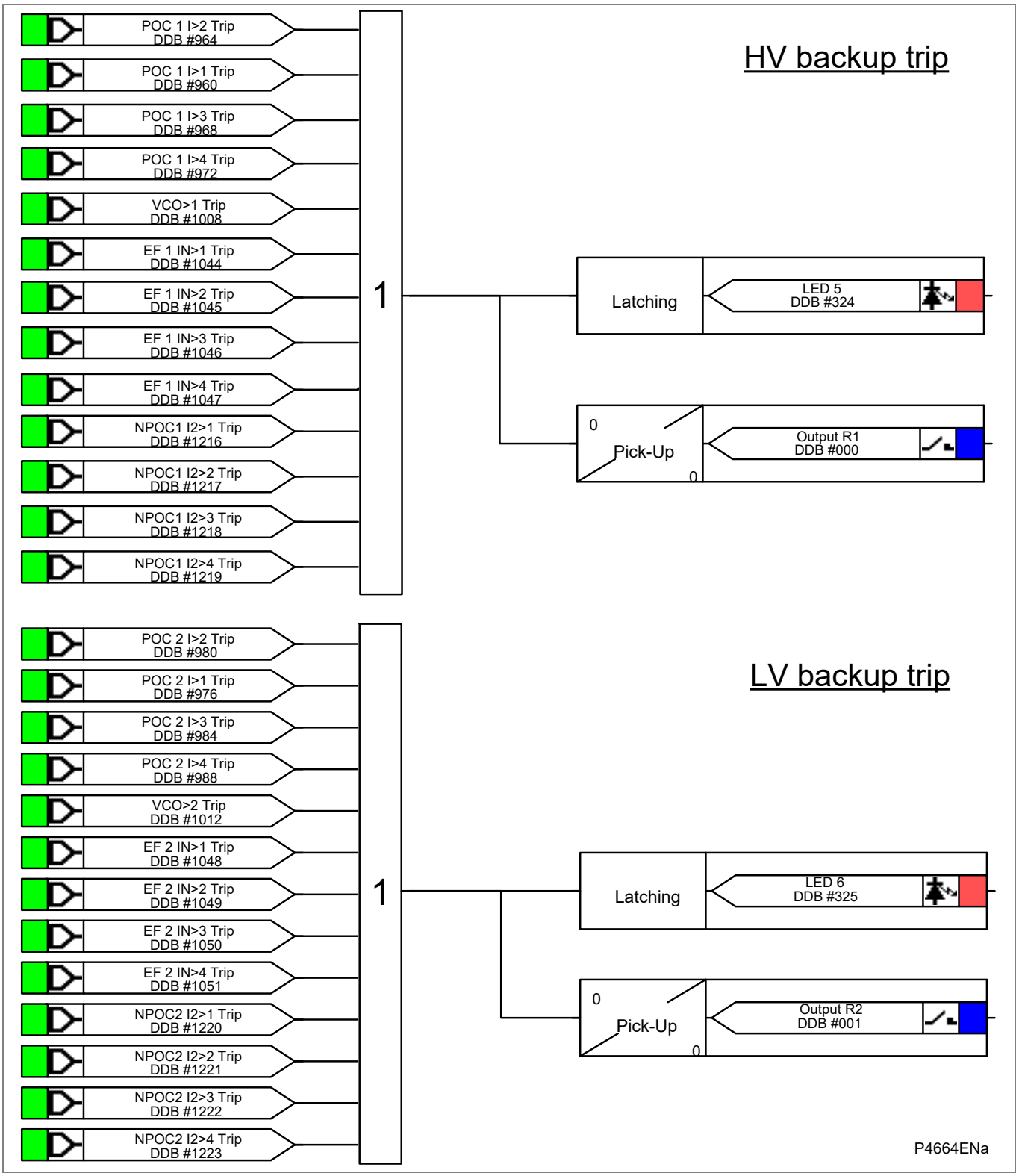


Figure 2 - P642 - Backup trip logic mappings

4.3 General Alarm

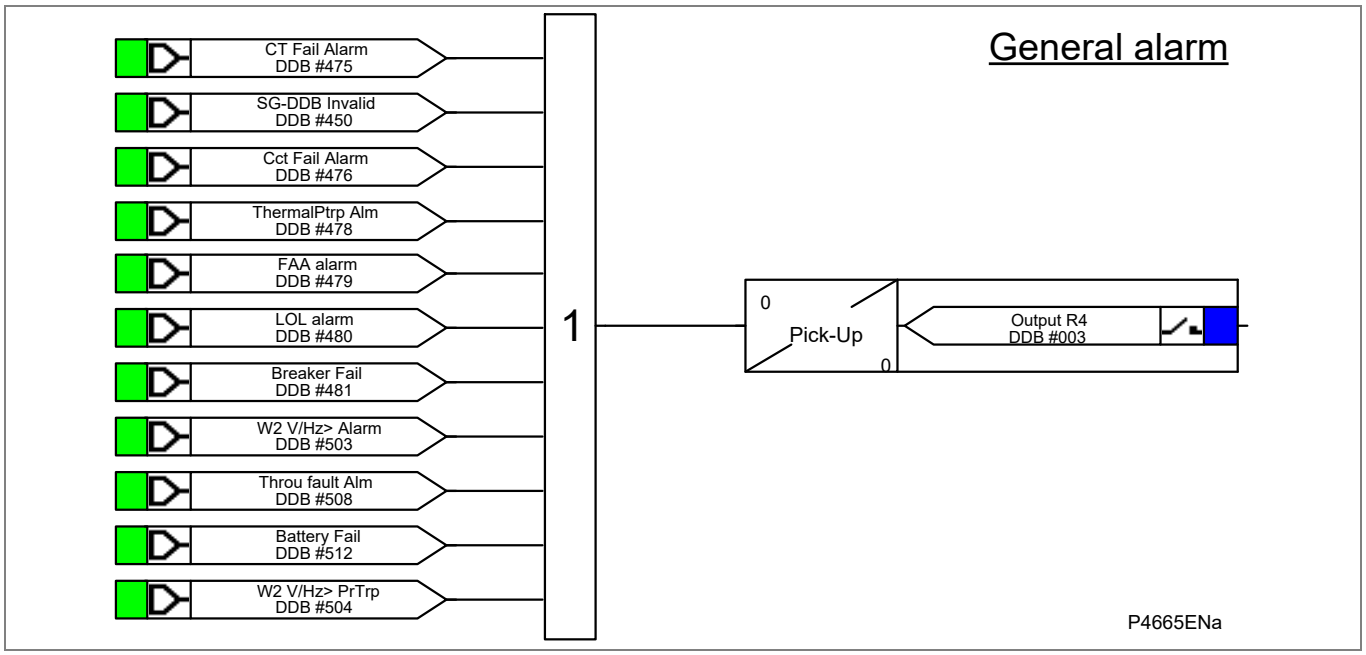


Figure 3 - P642 - General alarm mappings

4.4 Breaker Failure

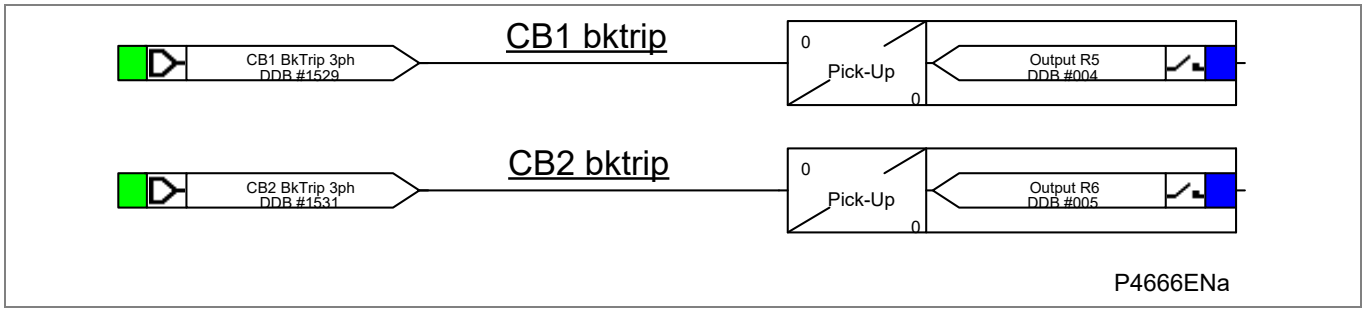


Figure 4 - P642 - Breaker failure mappings

4.5 Any Differential Trip

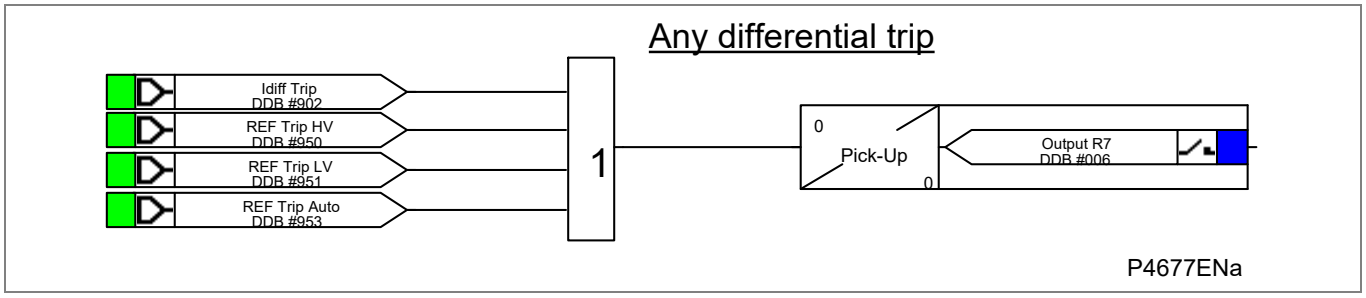


Figure 5 - P642 - Any differential trip mappings

4.6 Any Trip

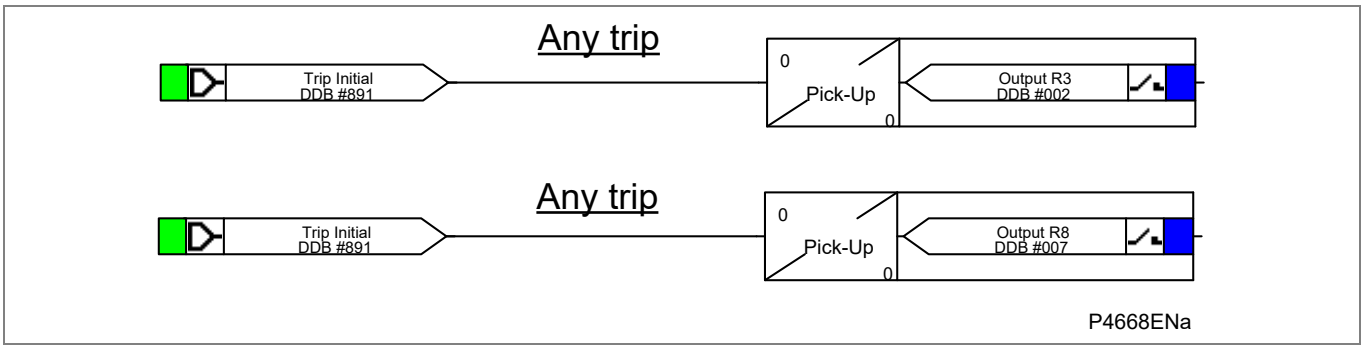


Figure 6 - P642 - Any trip mappings

4.7 Fault Recorder Trigger

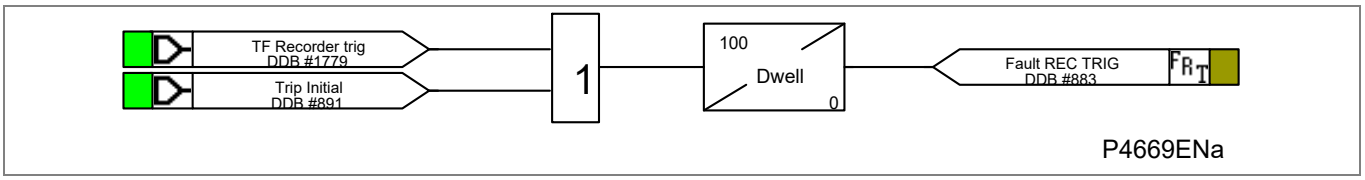


Figure 7 - P642 - Fault recorder trigger mappings

4.8 Opto Isolator Mappings

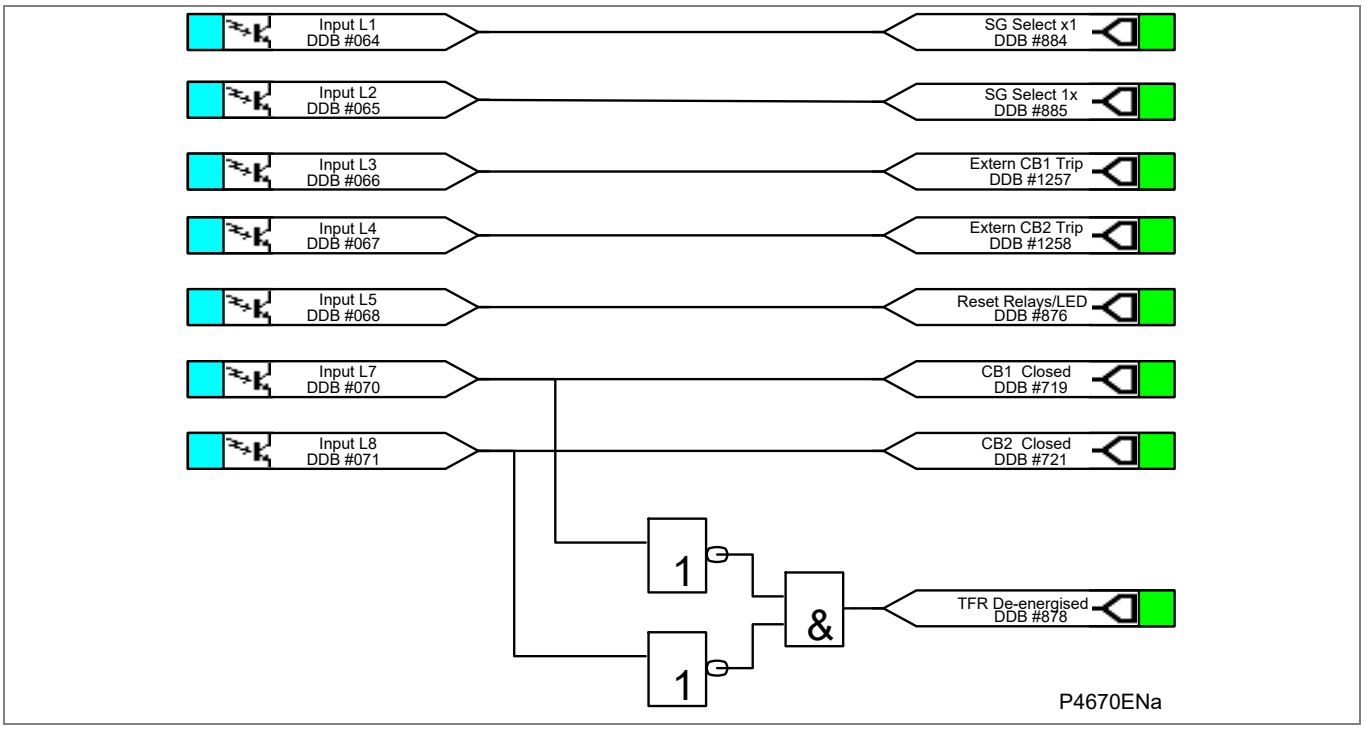


Figure 8 - P642 - Opto isolator mappings

4.9 LED Mapping

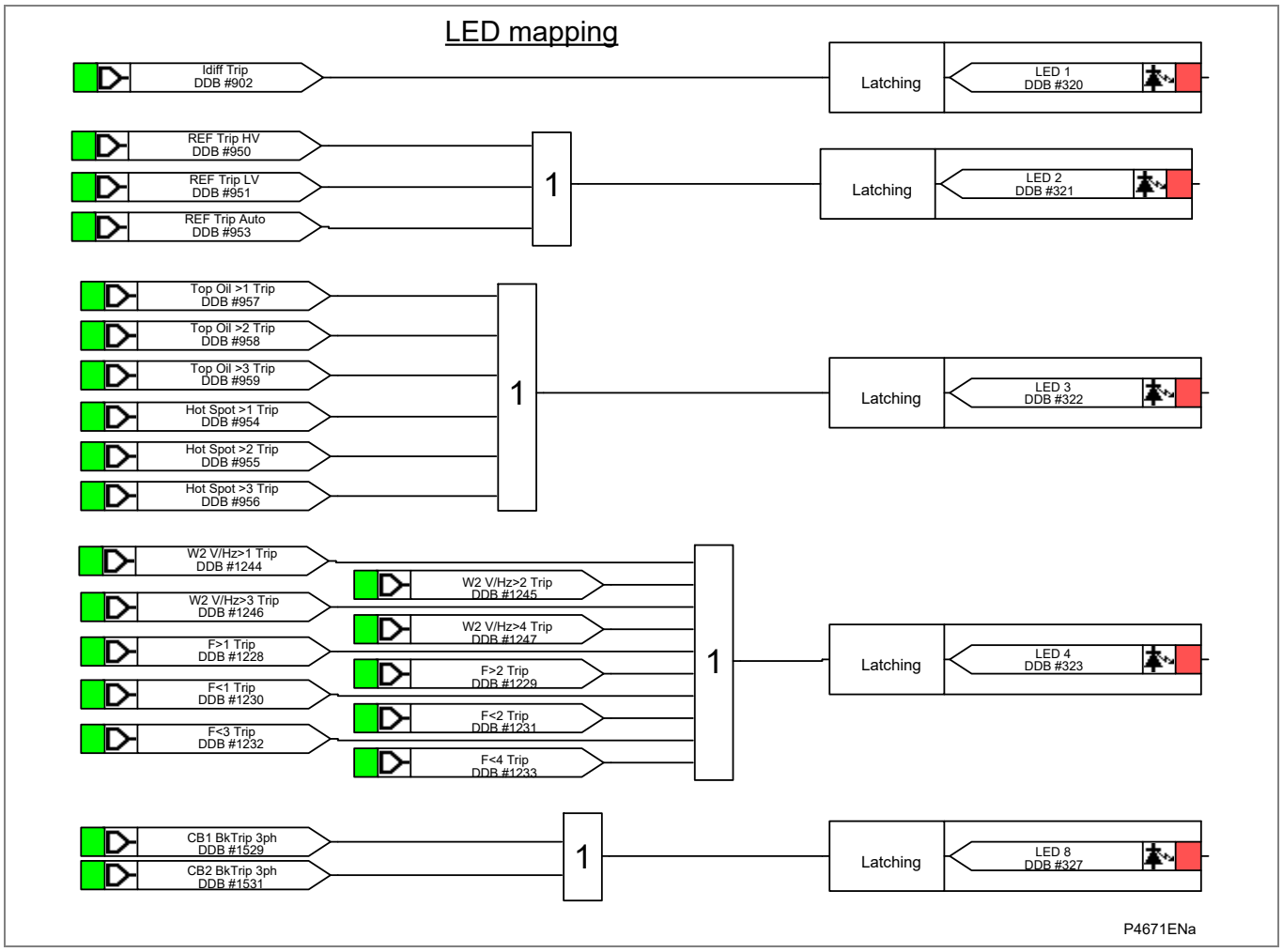


Figure 9 - P642 - LED mappings

4.10 Internal Trip CB Fail Initial Mappings

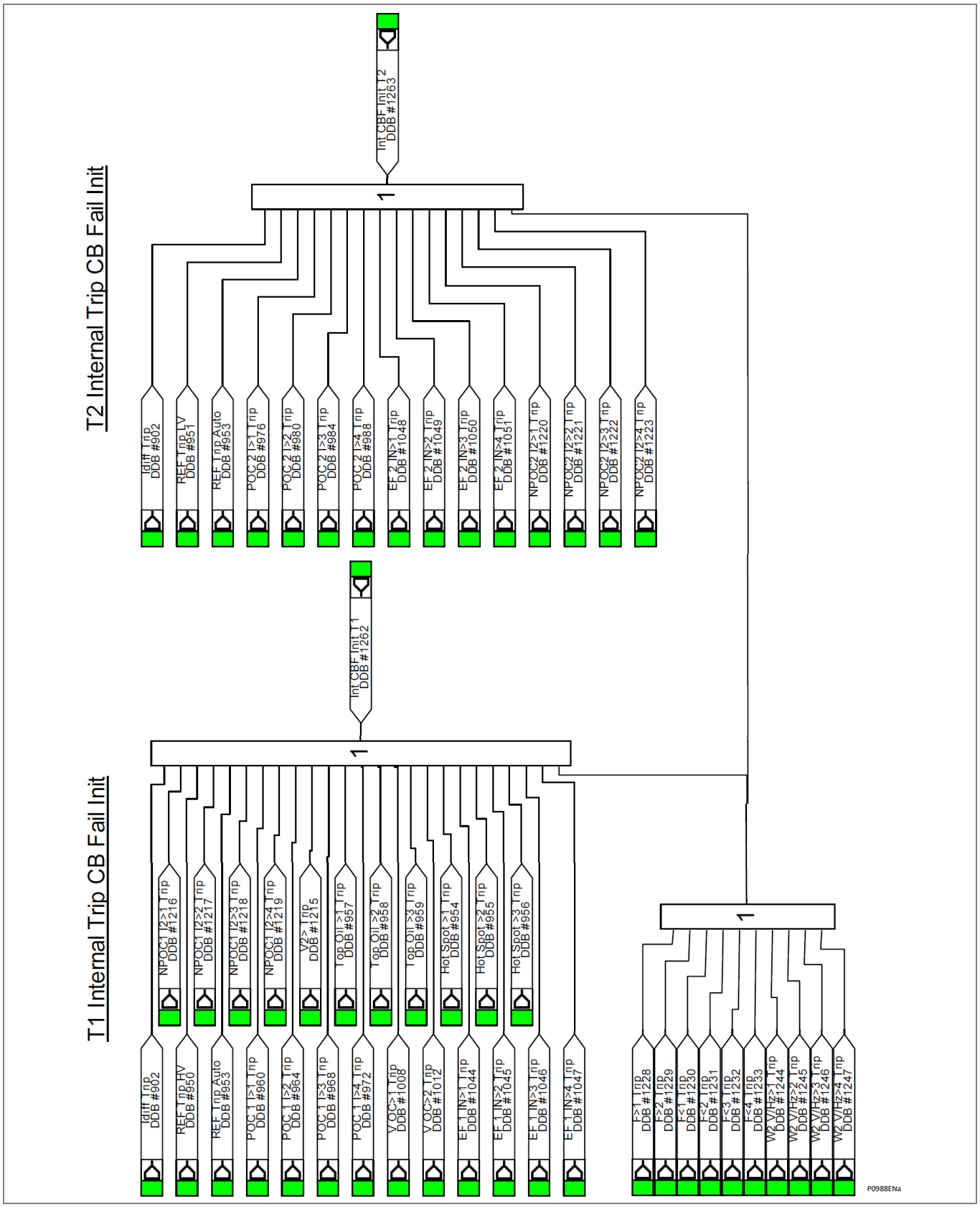


Figure 10 - P642 – T1 and T2 Internal Trip CB Fail Init mappings

5 MICOM P643 PSL DIAGRAMS

5.1 Any Trip Mapping

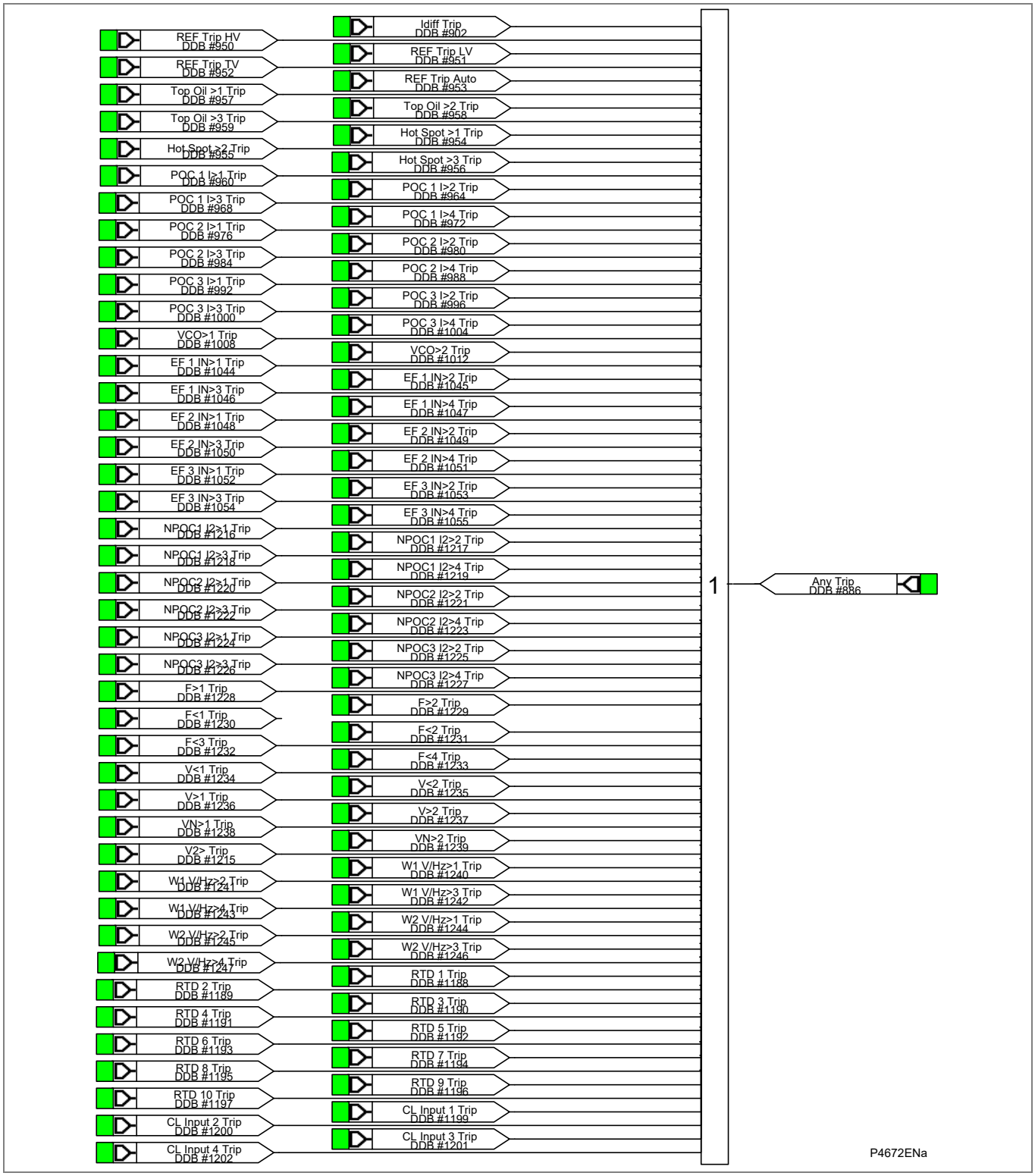


Figure 11 - P643 - Any trip mappings

5.2 Backup Trip Logic

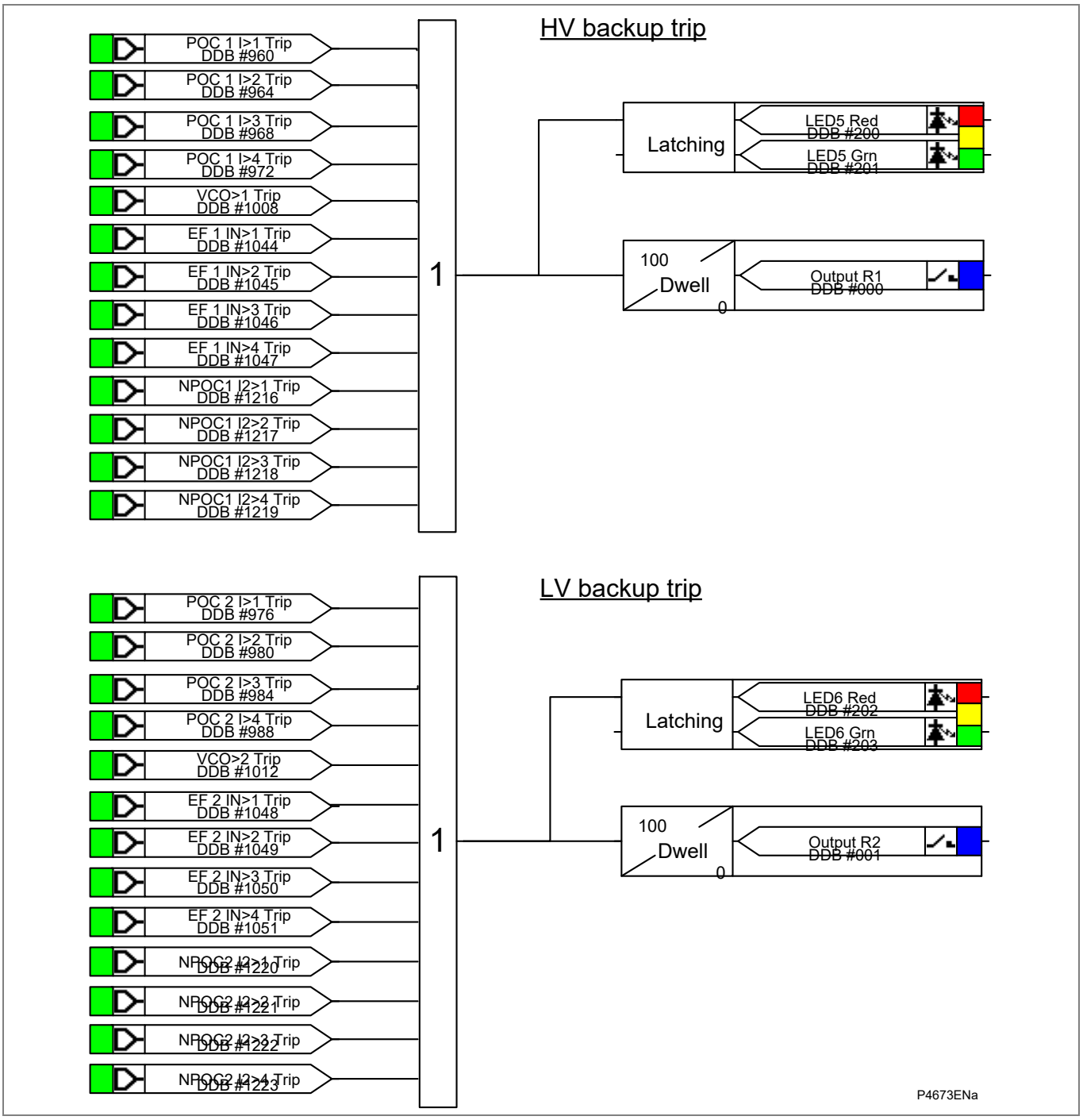


Figure 12 - P643 - HV and LV Backup trip logic mappings

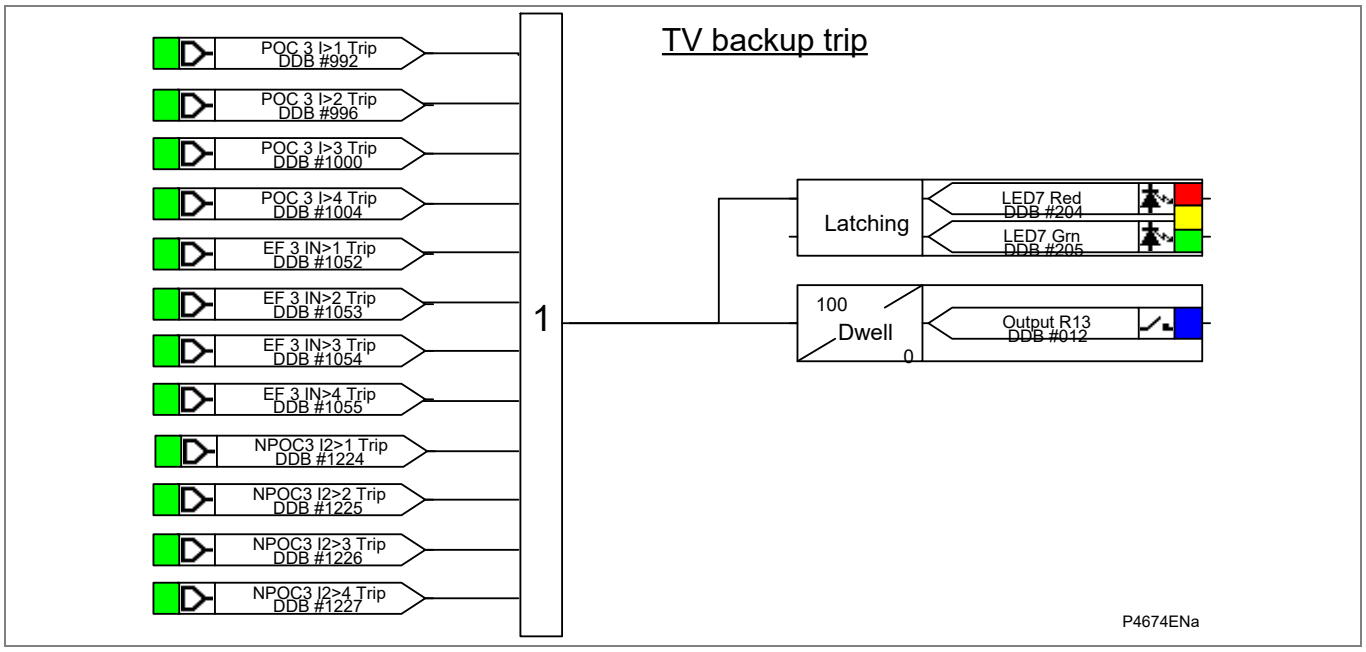


Figure 13 - P643 - TV Backup trip logic mappings

5.3 General Alarm

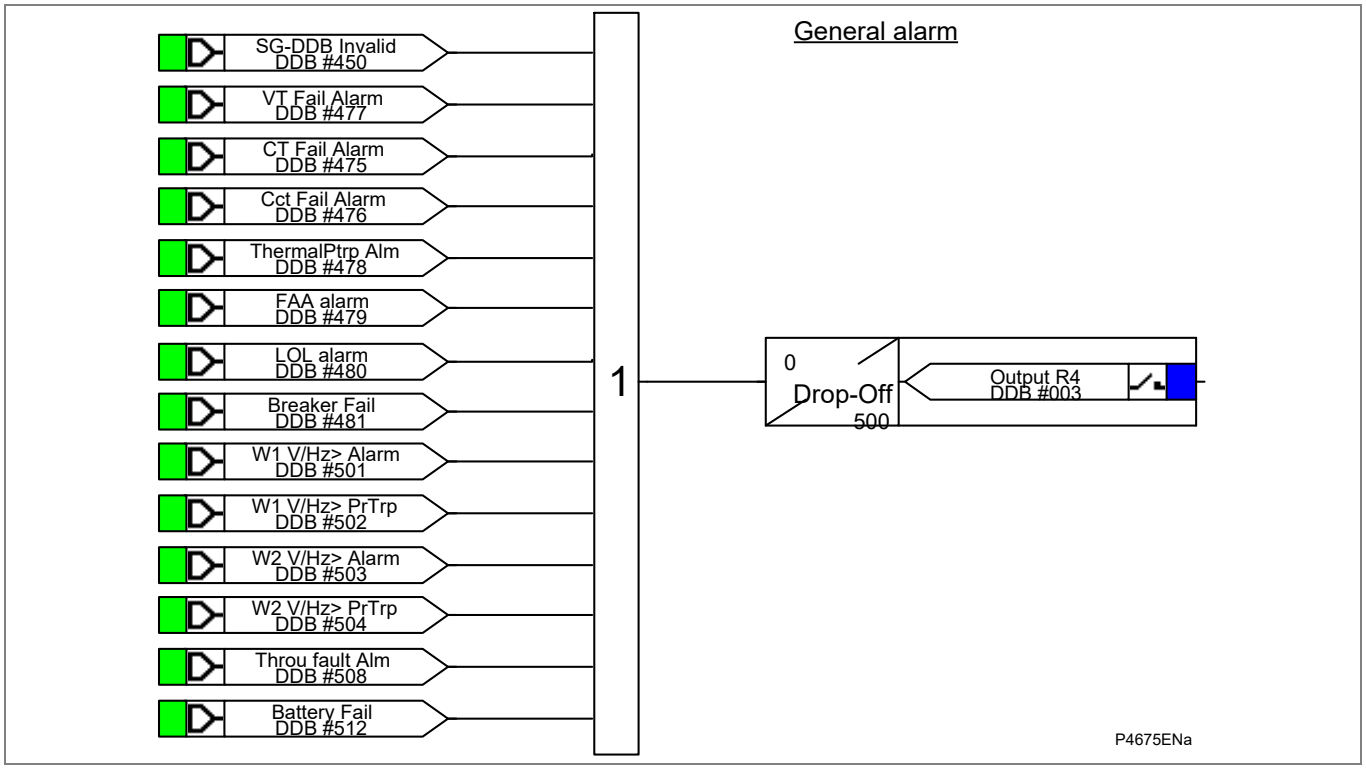


Figure 14 - P643 - General alarm mappings

5.4 Breaker Failure

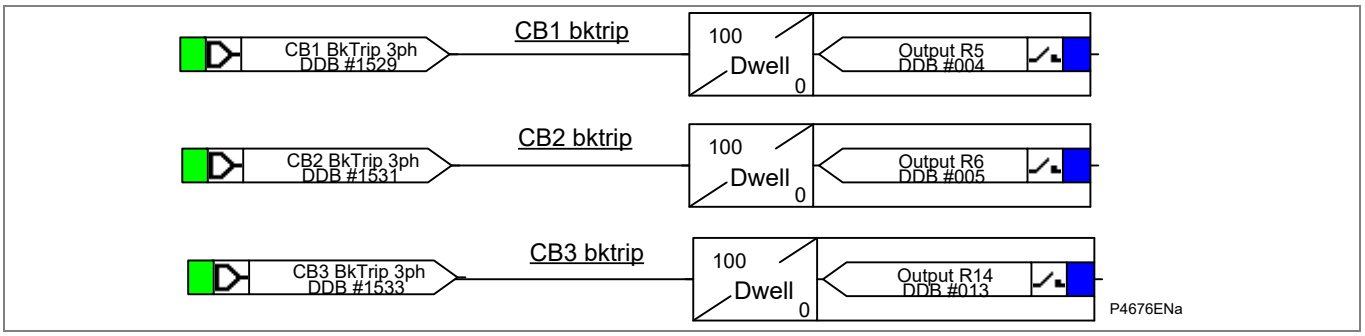


Figure 15 - P643 - Breaker failure mappings

5.5 Any Differential Trip

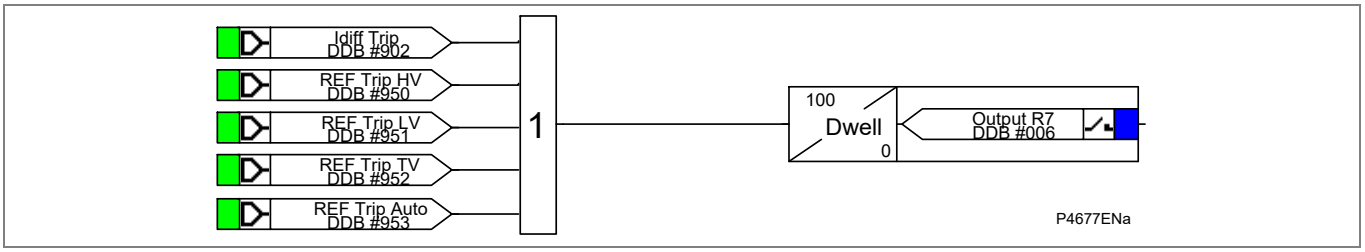


Figure 16 - P643 - Any differential trip mappings

5.6 Any Trip

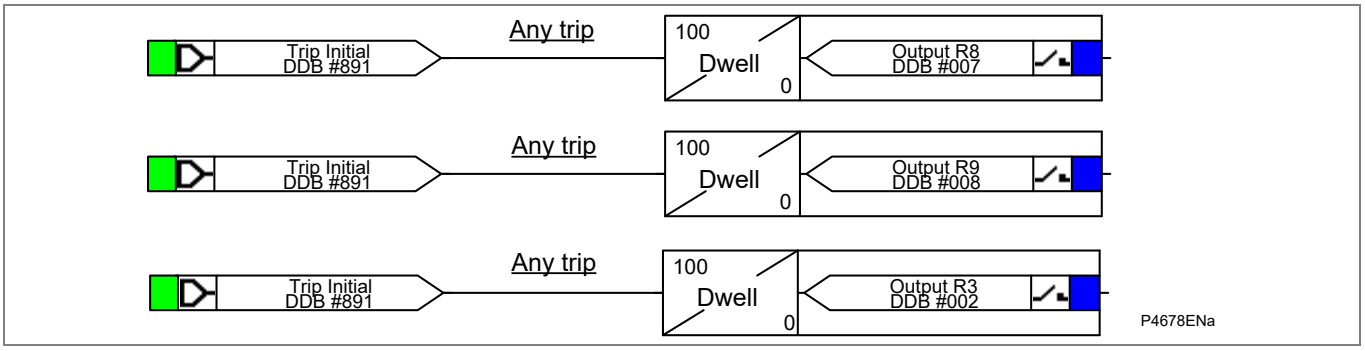


Figure 17 - P643 - Any trip mappings

5.7 Pretrip Alarms

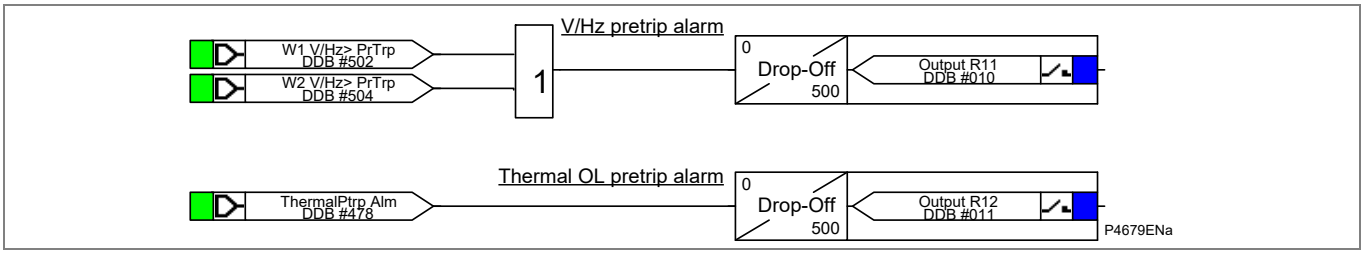


Figure 18 - P643 - Pretrip alarm mappings

5.8 Fault Recorder Trigger

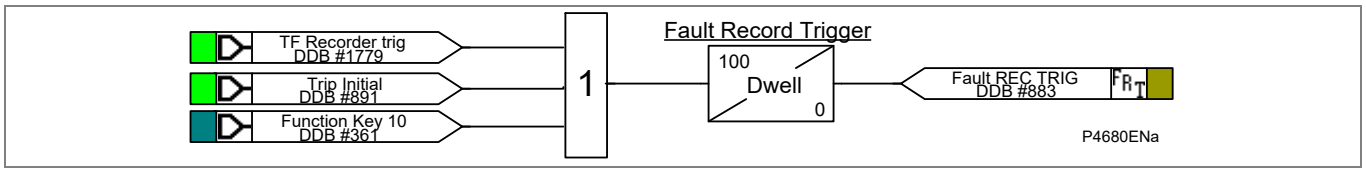


Figure 19 - P643 - Fault recorder trigger mappings

5.9 Opto Isolator Mappings

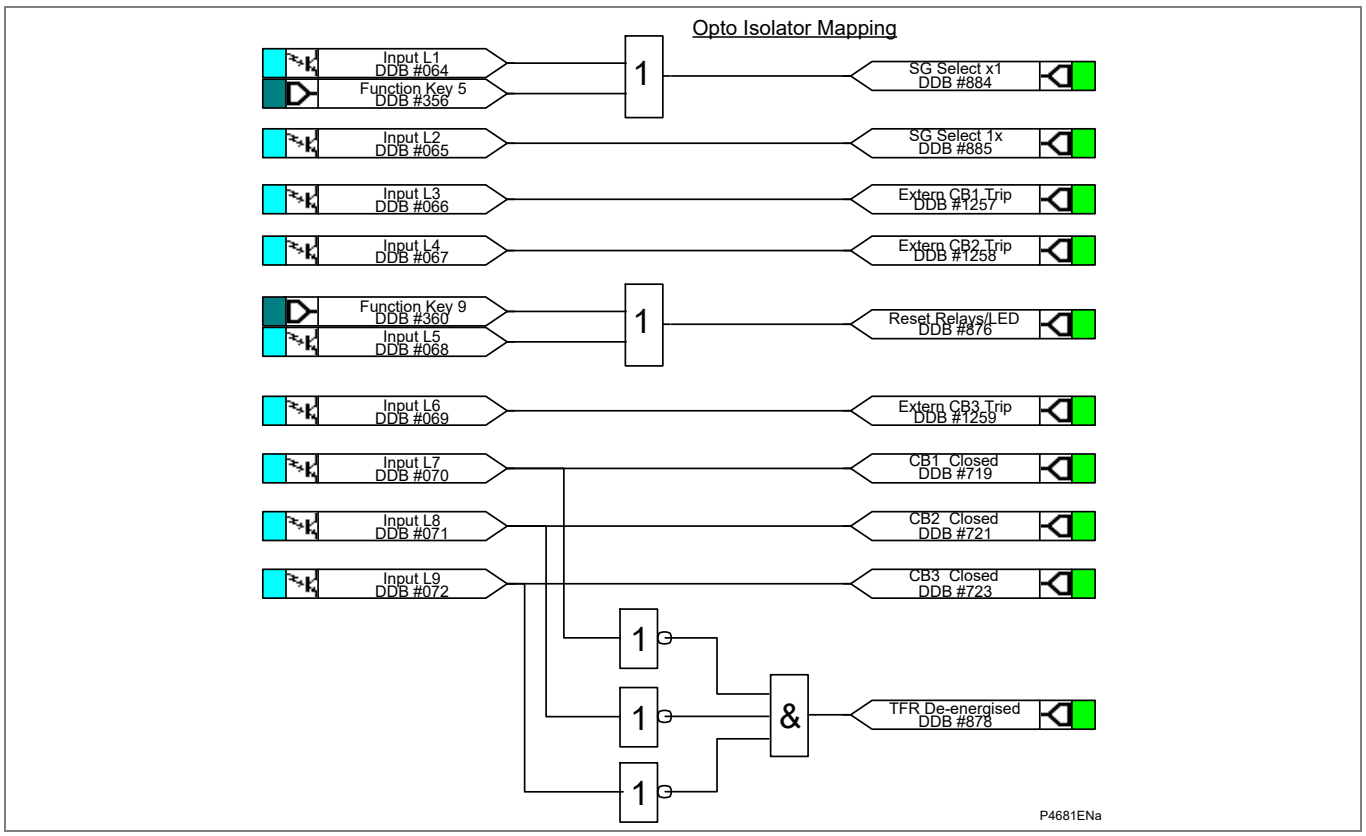


Figure 20 - P643 - Opto isolator mappings

5.10 LED Mappings

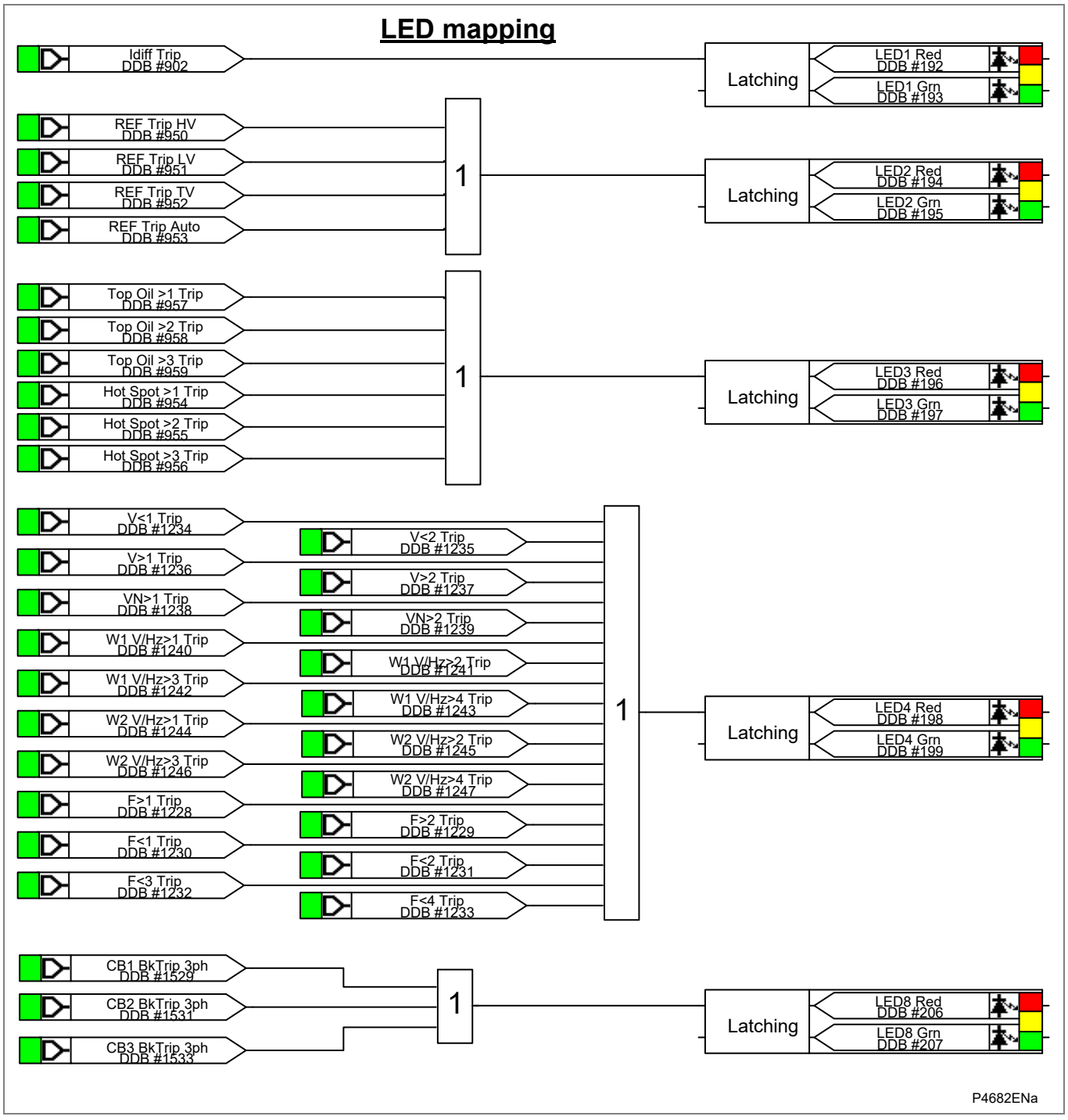


Figure 21 - P643 - LED mappings

5.11 Function Key and Function LED Mapping

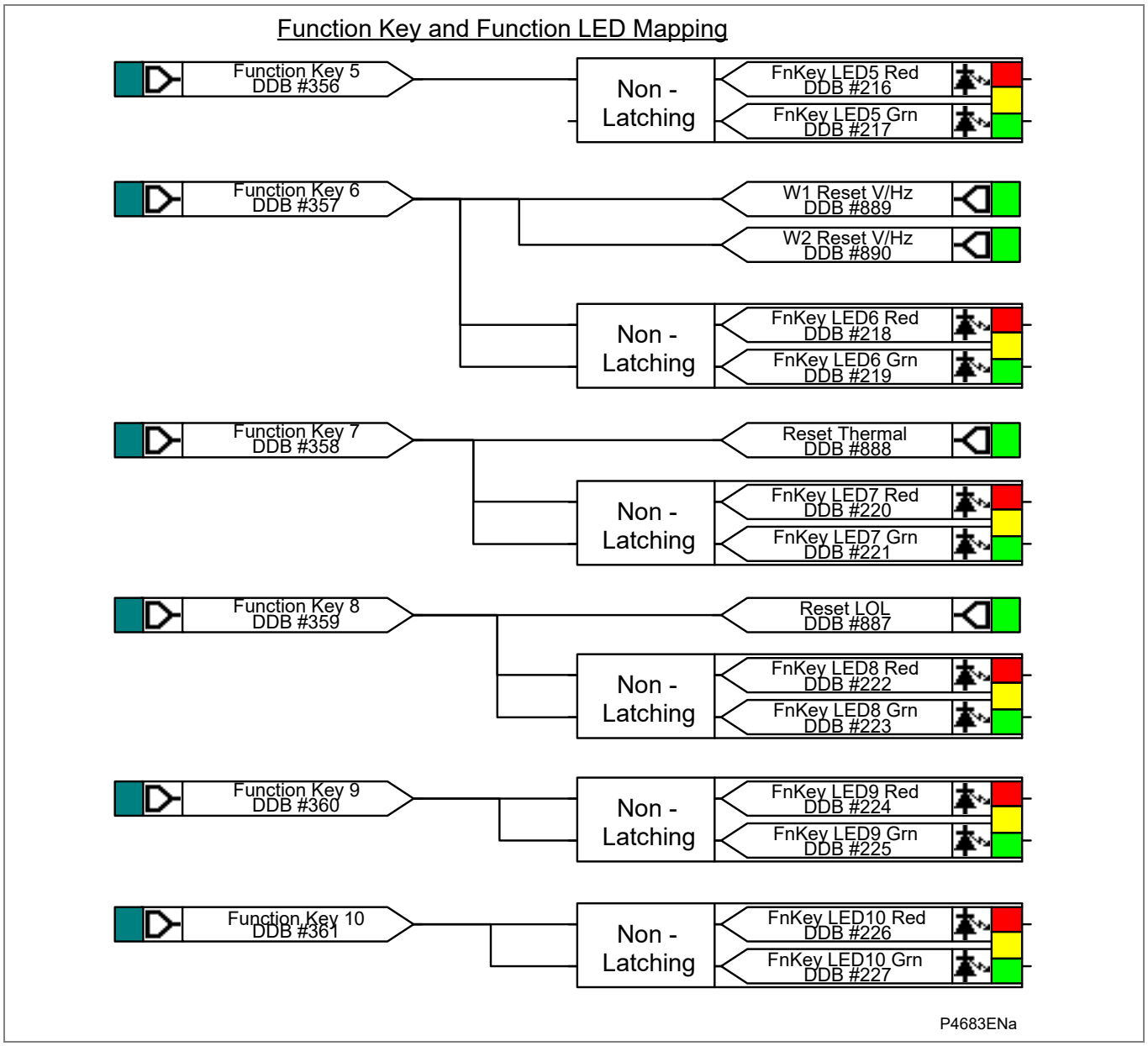


Figure 22 - P643 - Function key and function LED mappings

5.12 Internal Trip CB Fail Initial Mappings

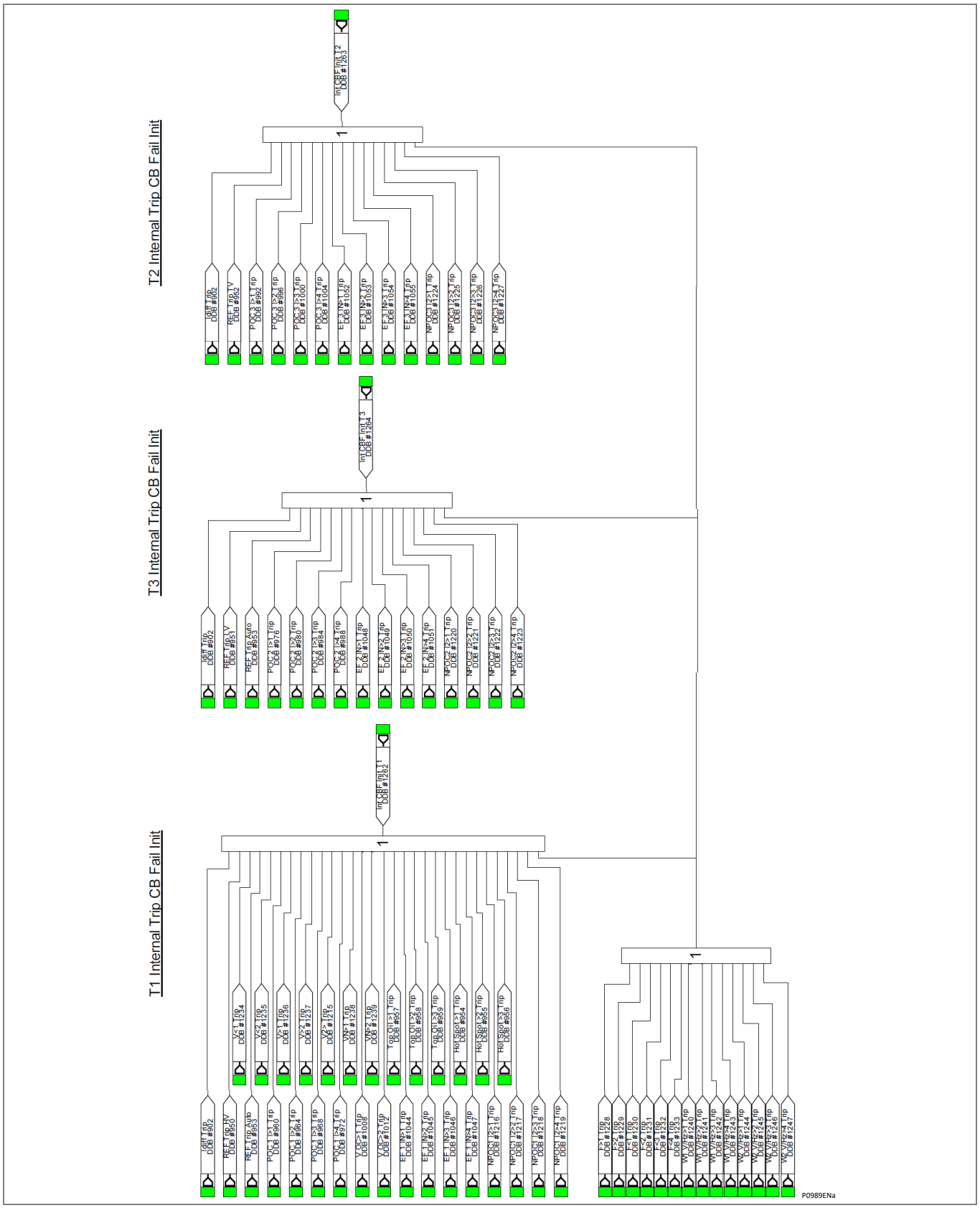


Figure 23 - P643 – T1, T2 and T3 Internal Trip CB Fail Init mappings

6 MICOM P645 PSL DIAGRAMS

6.1 Any Trip Mapping

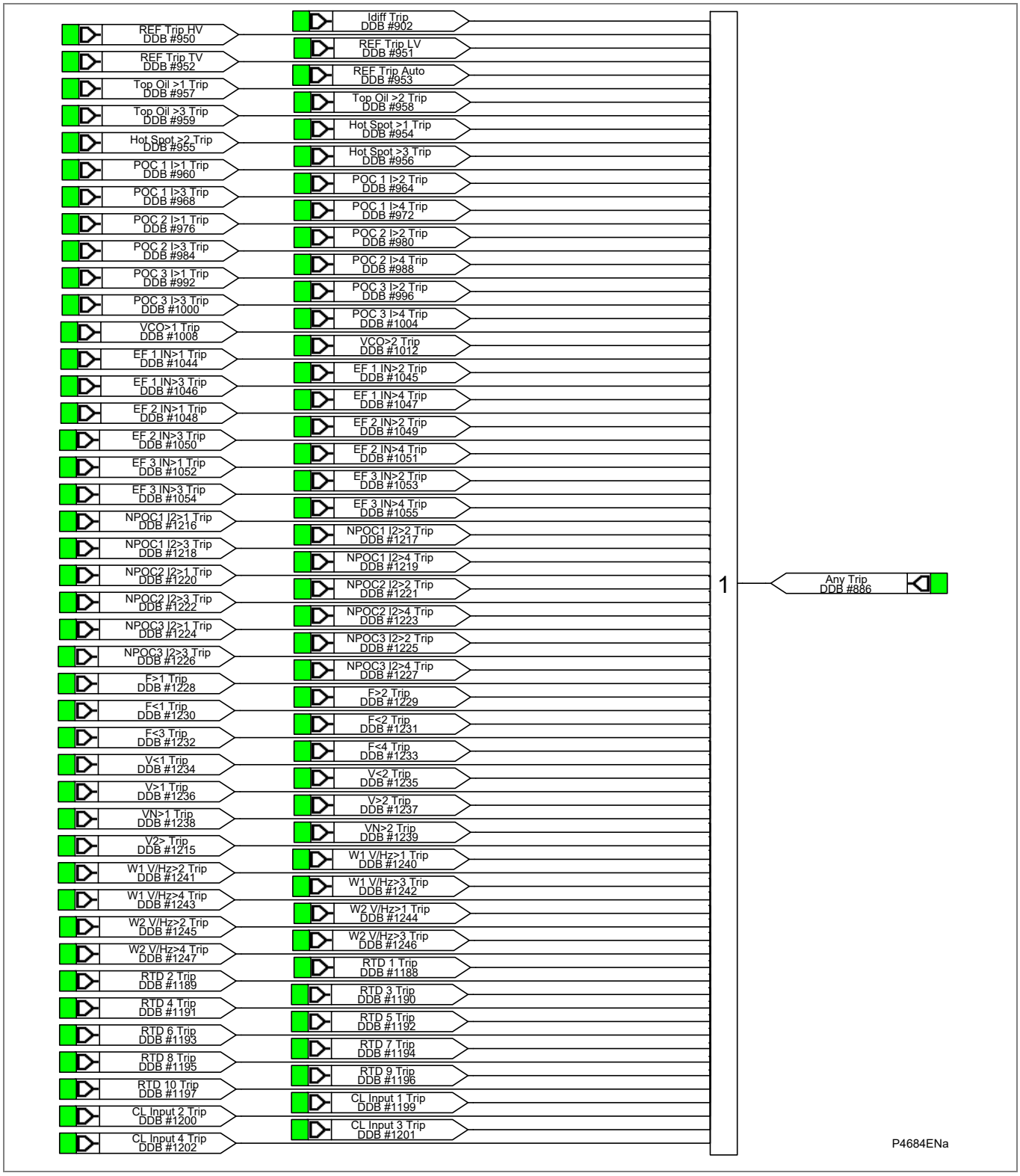


Figure 24 - P645 - Any trip mappings

6.2 Backup Trip Logic

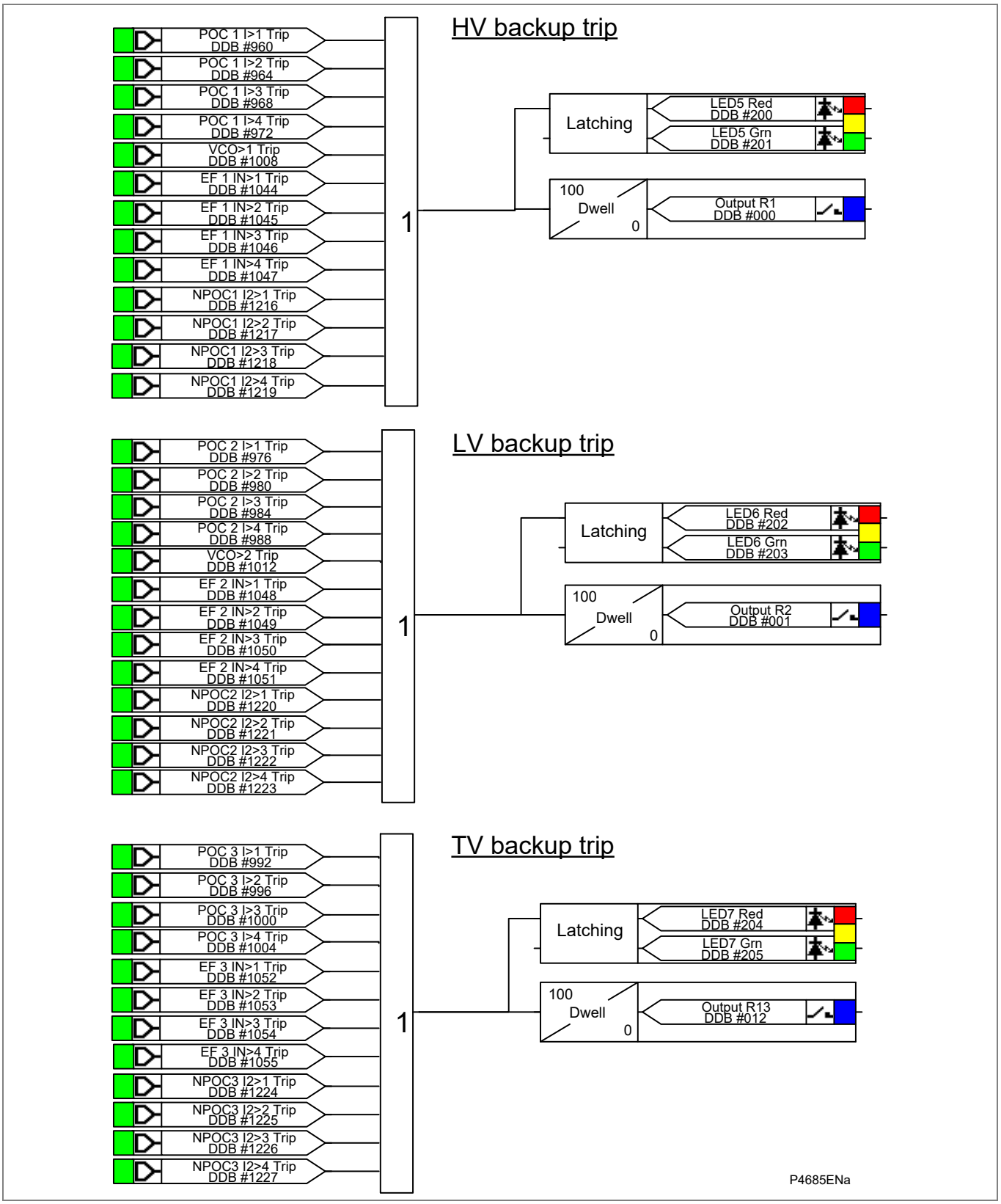


Figure 25 - P645 - Backup trip logic mappings

6.3 General Alarm

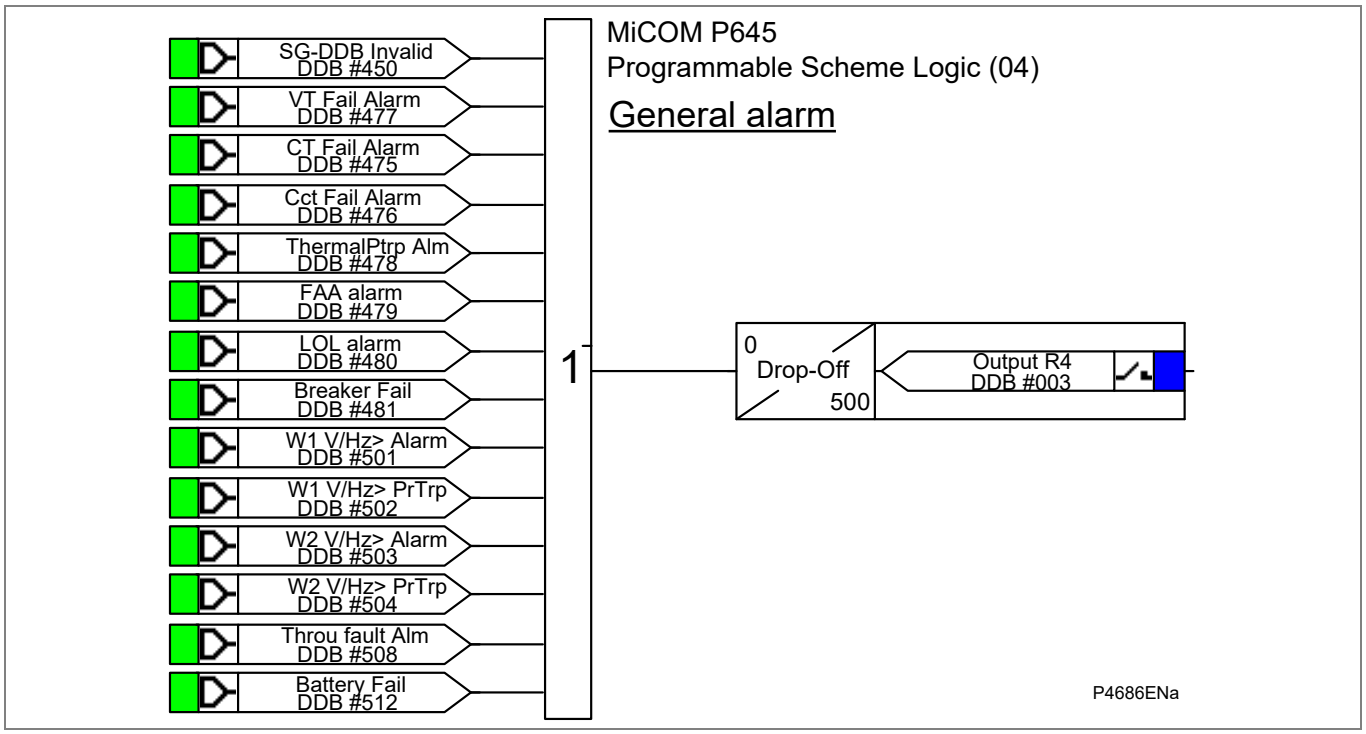


Figure 26 - P645 - General alarm mappings

6.4 Breaker Failure

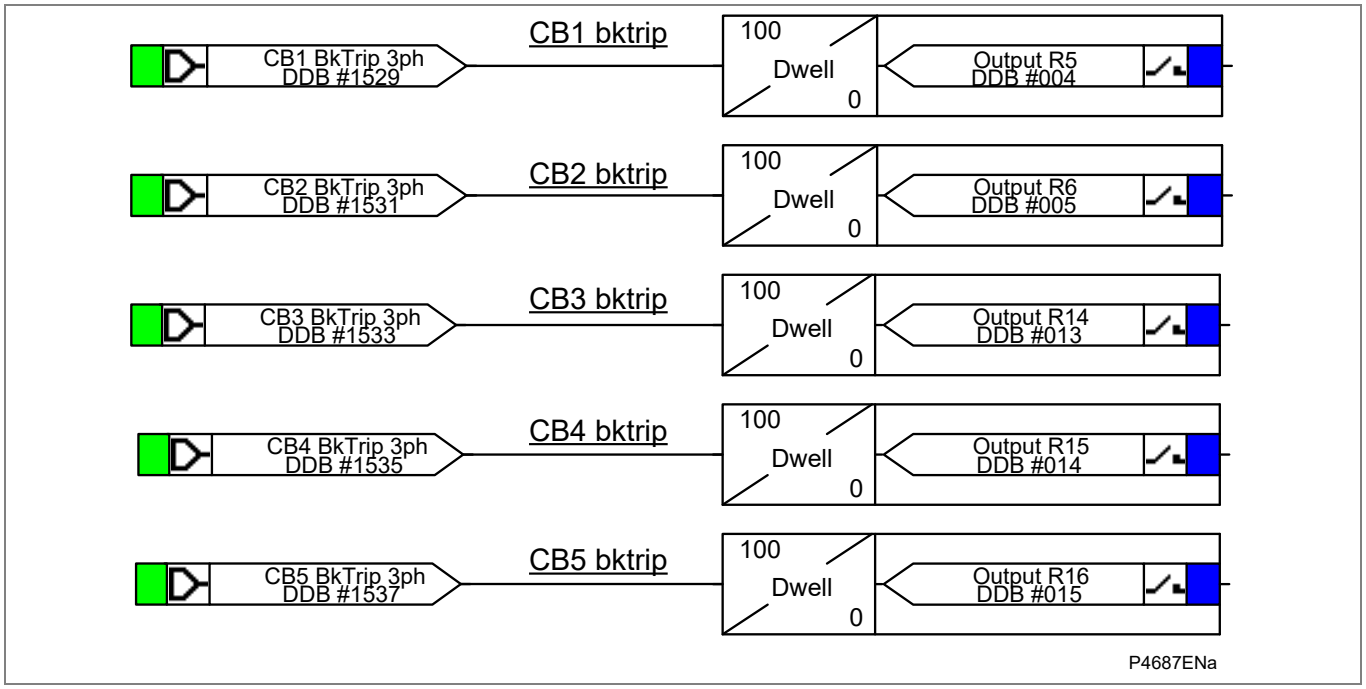


Figure 27 - P645 - Breaker failure mappings

6.5 Any Differential Trip

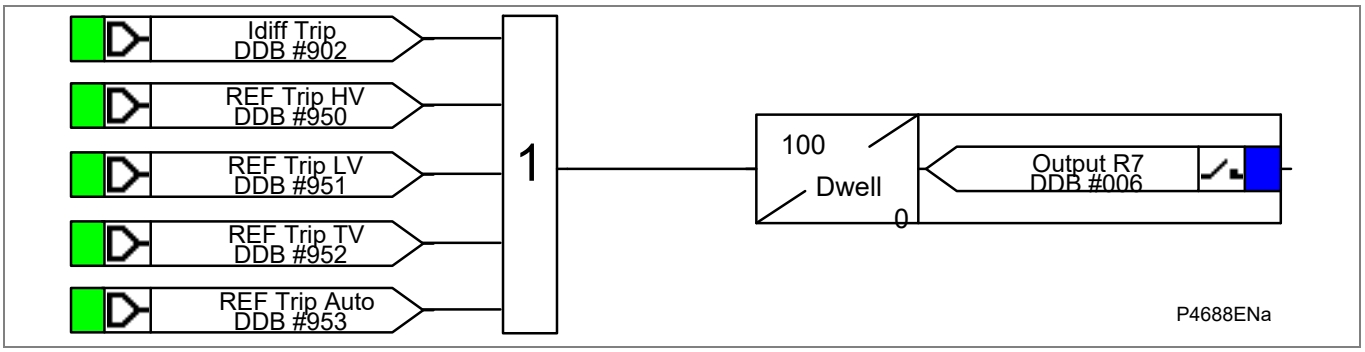


Figure 28 - P645 - Any differential trip mappings

6.6 Any Trip

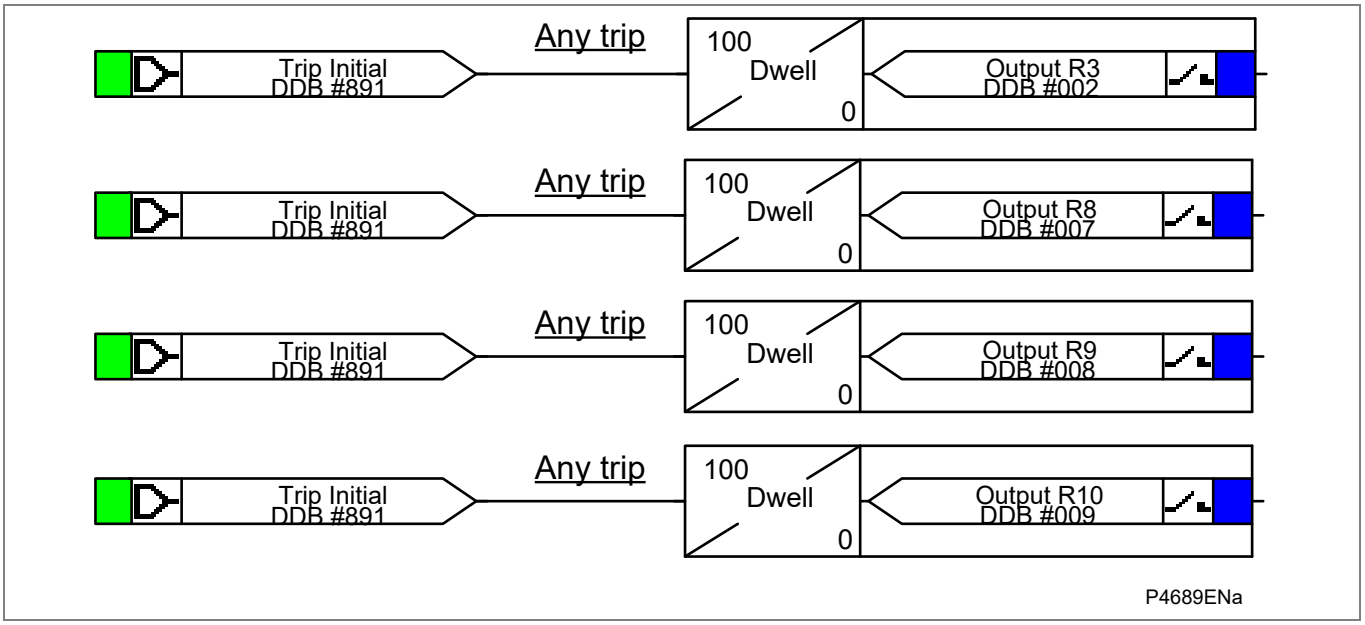


Figure 29 - P645 - Any trip mappings

6.7 Pretrip Alarms

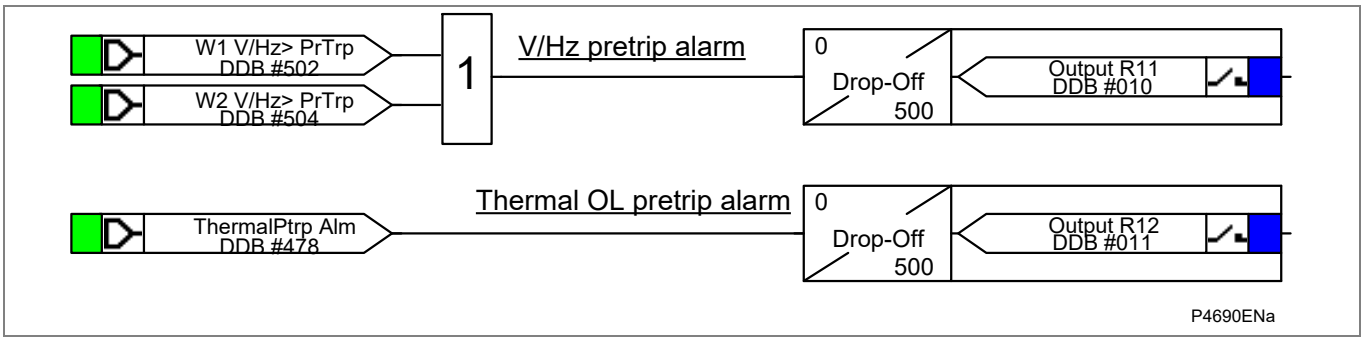


Figure 30 - P645 - Pretrip alarm mappings

6.8 Fault Record Trigger

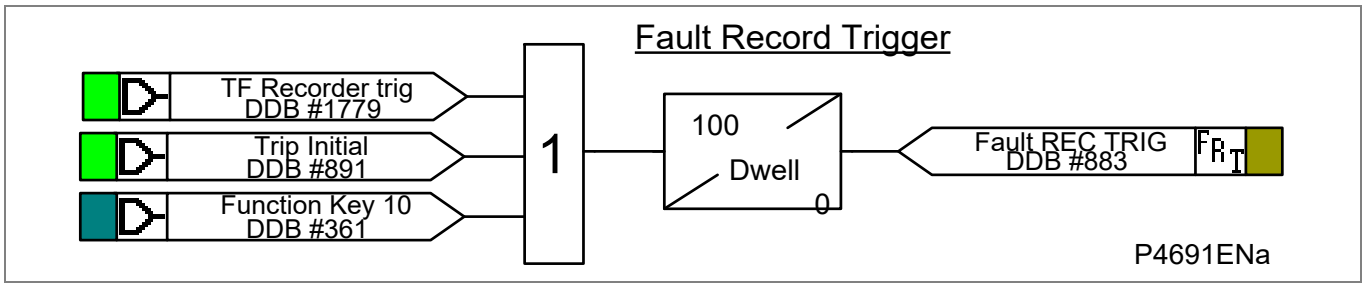


Figure 31 - P645 - Fault record trigger mappings

6.9 Opto Isolator Mappings

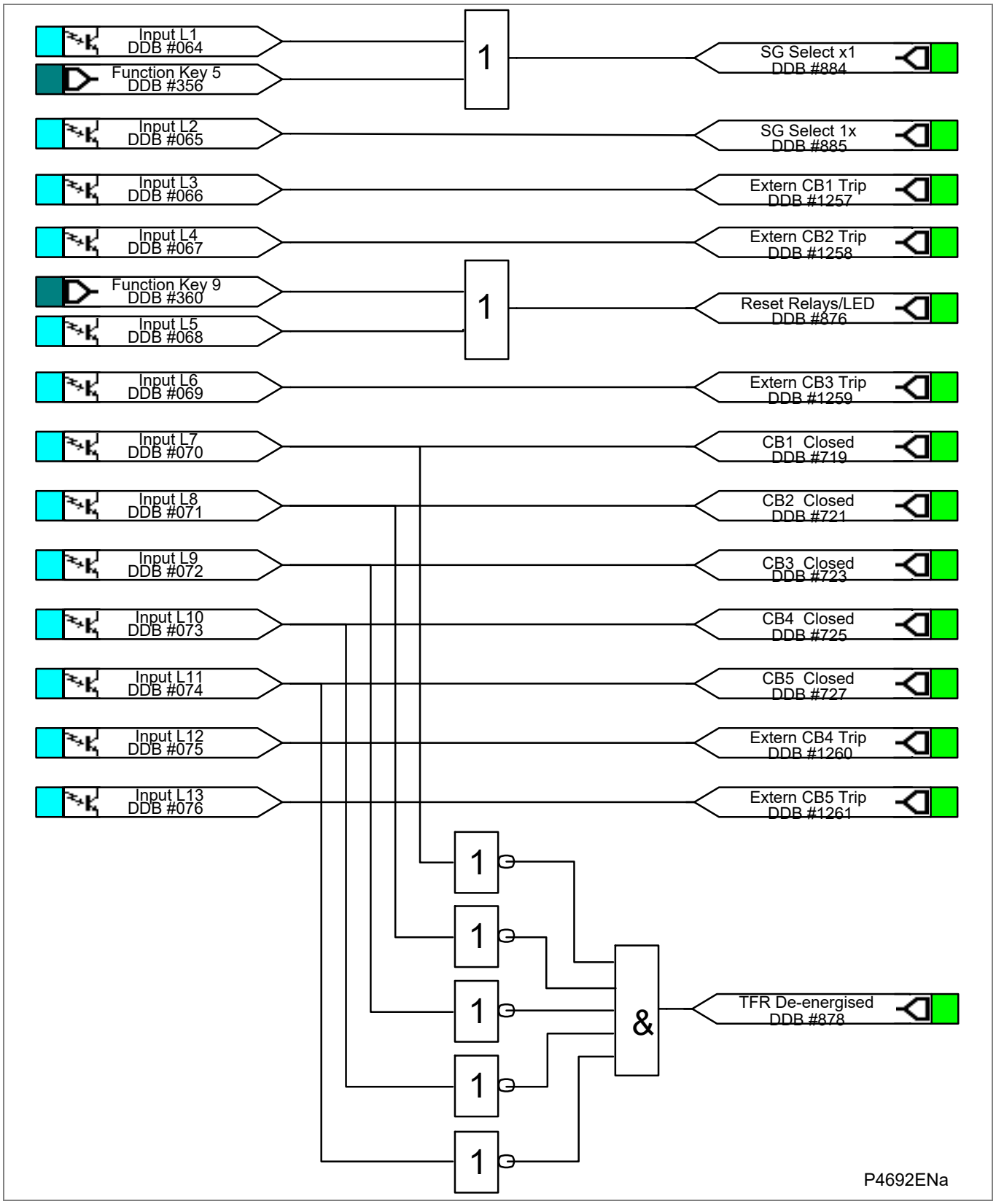


Figure 32 - P645 - Opto isolator mappings

6.10 LED Mappings

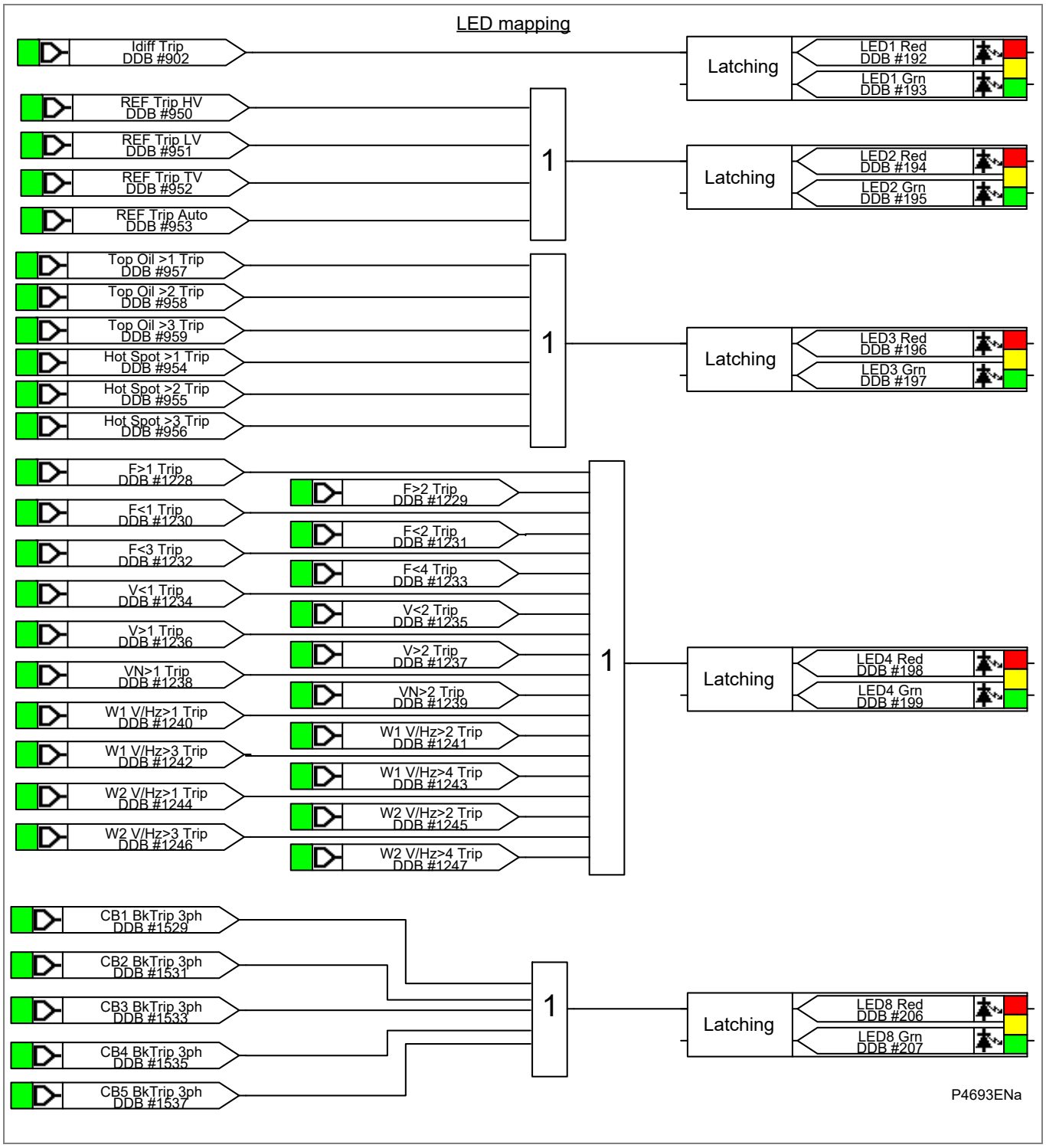


Figure 33 - P645 - LED mappings

6.11 Function Key and Function LED Mapping

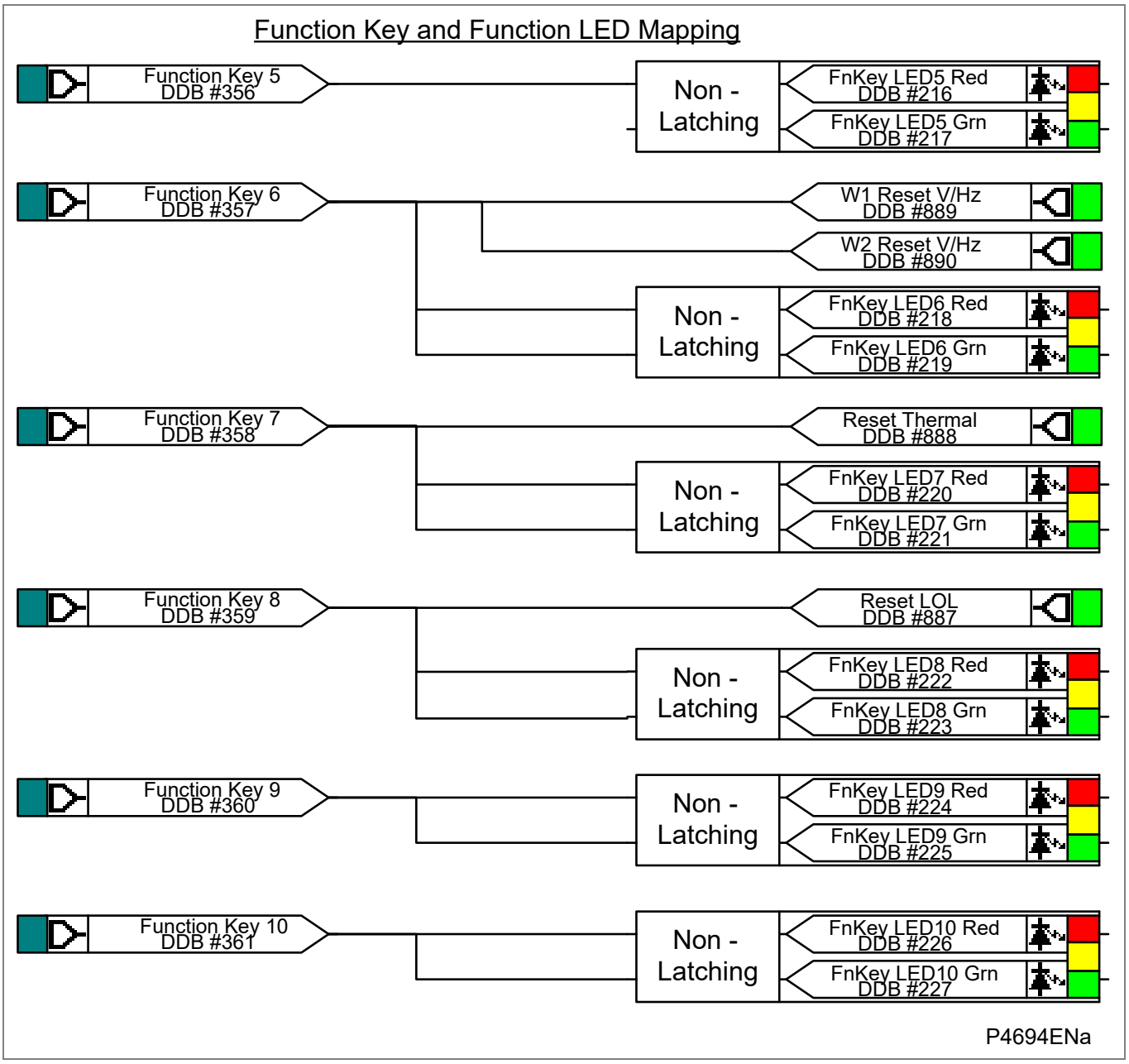


Figure 34 - P645 - Function key and function LED mappings

6.12 Internal Trip CB Fail Initial Mappings

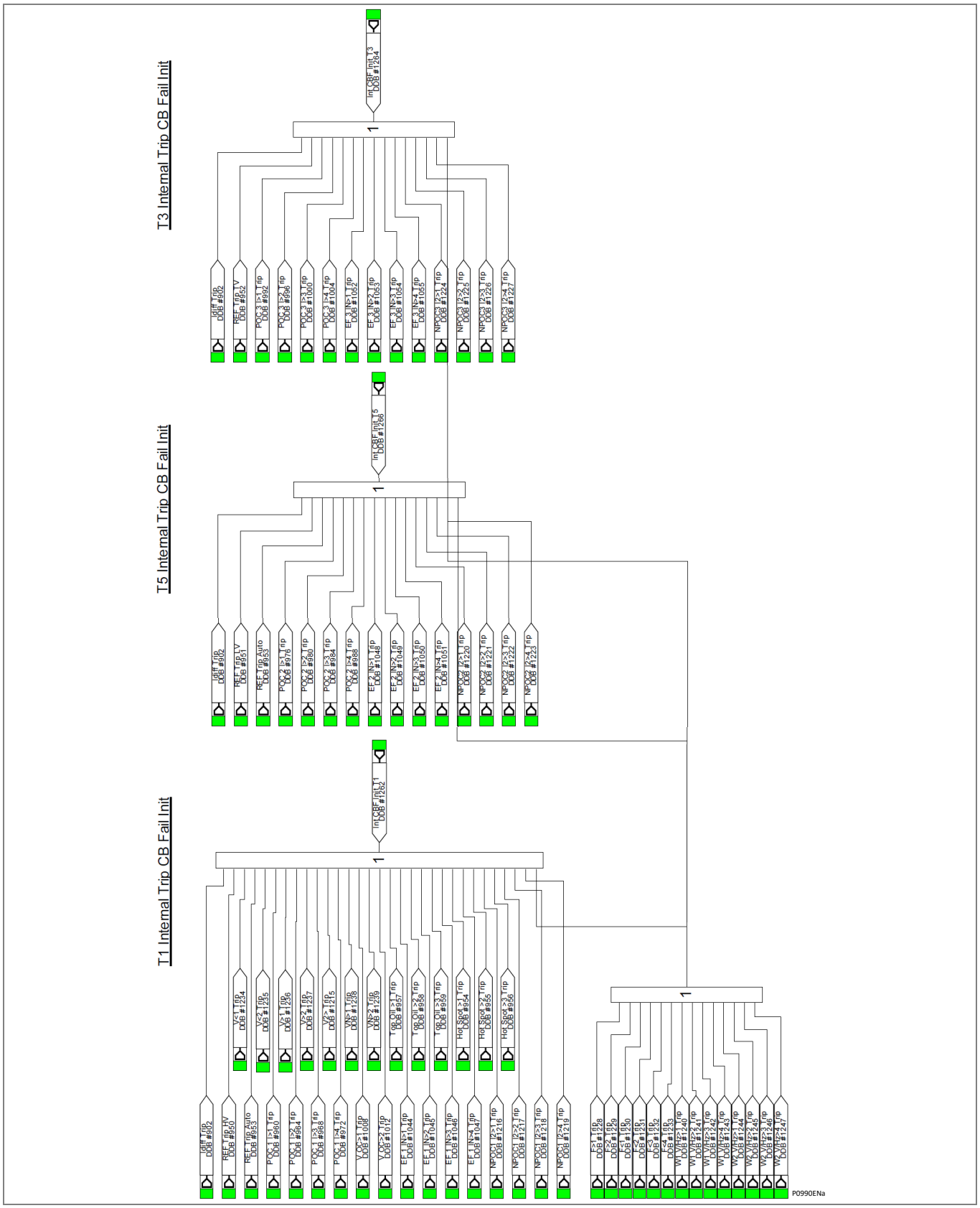


Figure 35 - P645 – T1, T2 and T3 Internal Trip CB Fail Init mappings

Notes:

MEASUREMENTS AND RECORDING

CHAPTER 9

Date:	07/2018
Products covered by this chapter:	This chapter covers the specific versions of the MiCOM products listed below. This includes ***only*** the following combinations of Software Version and Hardware Suffix.
Hardware Suffix:	L (P642) M (P643/P645)
Software Version:	B4 - P64x (P642, P643 & P645)
Connection Diagrams:	10P642xx (xx = 01 to 10) 10P643xx (xx = 01 to 06) 10P645xx (xx = 01 to 09)

CONTENTS

TABLES

1 INTRODUCTION

The relay is equipped with integral measurements, event, fault and disturbance recording facilities suitable for analysis of complex system disturbances.

The relay is flexible enough to allow for the programming of these facilities to specific user application requirements. These requirements are discussed in the sections which follow.

2 EVENT AND FAULT RECORDS

The relay records and time tags up to 250 or 512 events (only up to 250 events in the P24x and P44x) and stores them in non-volatile (battery-backed up) memory. This lets the system operator establish the sequence of events that occurred in the relay following a particular power system condition or switching sequence. When the available space is used up, the oldest event is automatically overwritten by the new one (i.e. first in, first out).

The relay's real-time clock provides the time tag to each event, to a resolution of 1 ms.

The event records can be viewed either from the front plate LCD or remotely using the communications ports (using any available protocols, such as Courier or MODBUS).

For local viewing on the LCD of event, fault and maintenance records, select the **VIEW RECORDS** menu column.

For extraction from a remote source using communications, see the *SCADA Communications* chapter or the MiCOM S1 Studio instructions.

For a full list of all the event types and the meaning of their values, see the Menu Database document.

Menu Text	Col	Row	Default Setting	Available Setting
Description				
VIEW RECORDS	01	00		
This column contains View Records settings				
Select Event	01	01	0	0 to 511 step 1
Setting range from 0 to 511. This selects the required event record from the possible 512 that can be stored. A value of 0 corresponds to the latest event				
Menu Cell Ref	01	02	(From Record)	Latched alarm active, Latched alarm inactive, Self reset alarm active, Self reset alarm inactive, Relay contact event, Opto-isolated input event, Protection event, General event, Fault record event, Maintenance record event
Indicates the type of event				
Time & Date	01	03	(From Record)	From record
Time & Date Stamp for the event given by the internal Real Time Clock				
Event Text	01	04	32-character string	32 character string
Up to 32 Character description of the Event. See the event sheet in the Measurements and Recording chapter, P64x/EN MR or the Menu Database document, P64x/EN/MD for details.				
Event Value	01	05	32-bit binary string	32-bit binary string - ON (1) or OFF (0) for status of relay contact or opto input or alarm or protection event depending on event type.
Unsigned integer is used for maintenance records. See the event sheet in the Measurements and Recording chapter, P64x/EN MR or the Menu Database document, P64x/EN/MD for details.				
Select Fault	01	06	0	0 to 19 step 1
Setting range from 0 to 19. This selects the required fault record from the possible 20 that can be stored. A value of 0 corresponds to the latest fault				
Faulted Phase	01	07	00000000	8-bit binary string
Displays the faulted phase as a binary string, bits 0 – 8 = Start A/B/C/N Trip A/B/C/N				
Start Elements1	01	08	00000000000000000000000000000000	32-bit binary string
32-bit binary string gives status of first 32 start signals. See Data type G84 in the Menu Database document, P64x/EN/MD for details.				
Start Elements2	01	09	00000000000000000000000000000000	32-bit binary string

Menu Text	Col	Row	Default Setting	Available Setting
Description				
32-bit binary string gives status of second 32 start signals. See Data type G107 in the Menu Database document, P64x/EN/MD for details.				
Start Elements3	01	0A	00000000000000000000000000000000	32-bit binary string
32-bit binary string gives status of third 32 start signals. See Data type G129 in the Menu Database document, P64x/EN/MD for details.				
Trip Elements1	01	10	00000000000000000000000000000000	32-bit binary string
32-bit binary string gives status of first 32 trip signals. See Data Type G85 in the Menu Database document, P64x/EN/MD for details.				
Trip Elements2	01	11	00000000000000000000000000000000	32-bit binary string
32-bit binary string gives status of second 32 trip signals. See Data Type G86 in the Menu Database document, P64x/EN/MD for details.				
Trip Elements3	01	12	00000000000000000000000000000000	32-bit binary string
32-bit binary string gives status of third 32 trip signals. See Data Type G130 in the Menu Database document, P64x/EN/MD for details.				
Fault Alarms	01	50	00000000000000000000000000000000	32-bit binary string
32-bit binary string gives status of fault alarm signals. See Data Type G87 in the Menu Database document, P64x/EN/MD for details.				
Fault Time	01	51	(From Record)	From record
Displays the Fault Time and Date.				
Fault Type	01	52	Data	Internal or External
Displays the Fault Type (internal or external).				
Active Group	01	53	Data	<Active group>
Displays the Active setting group 1-4.				
System Frequency	01	54	Data	<System frequency>
Displays the System frequency.				
Fault Duration	01	55	Data	<Fault duration>
Fault duration: Time from the start or trip until the undercurrent elements indicate the CB is open				
CB Operate Time	01	56	Data	<CB Operate time>
Circuit Breaker Operate Time: Time from protection trip to undercurrent elements indicating the CB is open				
Relay Trip Time	01	60	Data	<relay trip time>
Relay Trip Time: Time from protection start to protection trip				
IA-1 Magnitude	01	62		Not settable
This provides measurement information about the fault.				
IB-1 Magnitude	01	64		Not settable
This provides measurement information about the fault.				
IC-1 Magnitude	01	66		Not settable
This provides measurement information about the fault.				
IA-2 Magnitude	01	68		Not settable
This provides measurement information about the fault.				
IB-2 Magnitude	01	6A		Not settable
This provides measurement information about the fault.				
IC-2 Magnitude	01	6C		Not settable
This provides measurement information about the fault.				
IA-3 Magnitude	01	6E		Not settable

Menu Text	Col	Row	Default Setting	Available Setting
Description				
P643, P645 and P746 only. This provides measurement information about the fault.				
IB-3 Magnitude	01	70		Not settable
P643, P645 and P746 only. This provides measurement information about the fault.				
IC-3 Magnitude	01	72		Not settable
P643, P645 and P746 only. This provides measurement information about the fault.				
IA-4 Magnitude	01	74		Not settable
P645 and P746 only. This provides measurement information about the fault.				
IB-4 Magnitude	01	76		Not settable
P645 and P746 only. This provides measurement information about the fault.				
IC-4 Magnitude	01	78		Not settable
P645 and P746 only. This provides measurement information about the fault.				
IA-5 Magnitude	01	7A		Not settable
P645 and P746 only. This provides measurement information about the fault.				
IB-5 Magnitude	01	7C		Not settable
P645 and P746 only. This provides measurement information about the fault.				
IC-5 Magnitude	01	7E		Not settable
P645 and P746 only. This provides measurement information about the fault.				
IA-HV Magnitude	01	90		Not settable
This provides measurement information about the fault.				
IB-HV Magnitude	01	91		Not settable
This provides measurement information about the fault.				
IC-HV Magnitude	01	92		Not settable
This provides measurement information about the fault.				
IA-LV Magnitude	01	93		Not settable
This provides measurement information about the fault.				
IB-LV Magnitude	01	94		Not settable
This provides measurement information about the fault.				
IC-LV Magnitude	01	95		Not settable
This provides measurement information about the fault.				
IA-TV Magnitude	01	96		Not settable
P643 and P645 only. This provides measurement information about the fault.				
IB-TV Magnitude	01	97		Not settable
P643 and P645 only. This provides measurement information about the fault.				
IC-TV Magnitude	01	98		Not settable
P643 and P645 only. This provides measurement information about the fault.				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
I2-HV Magnitude	01	99		Not settable
This provides measurement information about the fault.				
I2-LV Magnitude	01	9A		Not settable
This provides measurement information about the fault.				
I2-TV Magnitude	01	9B		Not settable
P643 and P645 only. This provides measurement information about the fault.				
IN-HV Mea Mag	01	9C		Not settable
This provides measurement information about the fault.				
IN-LV Mea Mag	01	9D		Not settable
This provides measurement information about the fault.				
IN-TV Mea Mag	01	9E		Not settable
P643 and P645 only. This provides measurement information about the fault.				
VAN Magnitude	01	A0		Not settable
P643, P645 and P746 only. This provides measurement information about the fault.				
VBN Magnitude	01	A1		Not settable
P643, P645 and P746 only. This provides measurement information about the fault.				
VCN Magnitude	01	A2		Not settable
P643, P645 and P746 only. This provides measurement information about the fault.				
Vx Magnitude	01	A3		Not settable
This provides measurement information about the fault.				
V1 Magnitude	01	A4		Not settable
This provides measurement information about the fault.				
V2 Magnitude	01	A5		Not settable
This provides measurement information about the fault.				
VN Derived Mag	01	A6		Not settable
P643, P645 and P746 only. This provides measurement information about the fault.				
VAB Magnitude	01	A7		Not settable
This provides measurement information about the fault.				
VBC Magnitude	01	A8		Not settable
This provides measurement information about the fault.				
VCA Magnitude	01	A9		Not settable
This provides measurement information about the fault.				
IN-TN1 Mea Mag	01	AA		Not settable
This provides measurement information about the fault.				
IN-TN2 Mea Mag	01	AB		Not settable
This provides measurement information about the fault.				
IN-TN3 Mea Mag	01	AC		Not settable
P643 and P645 only. This provides measurement information about the fault.				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
IA Differential	01	B0		Not settable
This provides measurement information about the fault.				
IB Differential	01	B1		Not settable
This provides measurement information about the fault. IB Differential Current fault.				
IC Differential	01	B2		Not settable
This provides measurement information about the fault. IC Differential Current fault.				
IA Bias	01	B3		Not settable
This provides measurement information about the fault. IA Bias Current fault.				
IB Bias	01	B4		Not settable
This provides measurement information about the fault. IB Bias Current fault.				
IC Bias	01	B5		Not settable
This provides measurement information about the fault. IC Bias Current fault.				
IREF HV LoZ Diff	01	B9		Not settable
This provides measurement information about the fault. IREF HV LoZ Differential Current fault.				
IREF HV LoZ Bias	01	BA		Not settable
This provides measurement information about the fault. IREF HV LoZ Bias Current fault.				
IREF LV LoZ Diff	01	BB		Not settable
This provides measurement information about the fault. IREF LV LoZ Differential Current fault.				
IREF LV LoZ Bias	01	BC		Not settable
This provides measurement information about the fault. IREF LV LoZ Bias Current fault.				
IREF TV LoZ Diff	01	BD		Not settable
P643 and P645 only. This provides measurement information about the IREF TV LoZ Differential Current fault.				
IREF TV LoZ Bias	01	BE		Not settable
P643 and P645 only. This provides measurement information about the IREF TV LoZ Bias Current fault.				
IREF Auto LoZ Diff	01	BF		Not settable
This provides measurement information about the IREF Auto Loz Differential Current fault				
IREF Auto LoZ Bias	01	C0		Not settable
This provides measurement information about the IREF Auto Loz Bias Current fault				
IREF HV HighZ Op	01	C1		Not settable
This provides measurement information about the IREF HV HighZ Operation Current fault				
IREF LV HighZ Op	01	C2		Not settable
This provides measurement information about the IREF LV HighZ Operation Current fault				
IREF TV HighZ Op	01	C3		Not settable
This provides measurement information about the IREF TV TighZ Operation Current fault				
IREF Auto HighZ Op	01	C4		Not settable
This provides measurement information about the IREF Auto TighZ Operation Current fault				
IA Peak Mag	01	C5		Not settable
This provides measurement information about the IA Peak Magnitude fault.				
IB Peak Mag	01	C6		Not settable
This provides measurement information about the IB Peak Magnitude fault.				
IC Peak Mag	01	C7		Not settable
This provides measurement information about the IC Peak Magnitude fault.				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
I2t Phase A	01	C8		Not settable
This provides measurement information about the I2t Phase A fault.				
I2t Phase B	01	C9		Not settable
This provides measurement information about the I2t Phase B fault.				
I2t Phase C	01	CA		Not settable
This provides measurement information about the I2t Phase C fault.				
RTD 1	01	D0		Not settable
This provides measurement information about the RTD 1 fault.				
RTD 2	01	D1		Not settable
This provides measurement information about the RTD 2 fault.				
RTD 3	01	D2		Not settable
This provides measurement information about the RTD 3 fault.				
RTD 4	01	D3		Not settable
This provides measurement information about the RTD 4 fault.				
RTD 5	01	D4		Not settable
This provides measurement information about the RTD 5 fault.				
RTD 6	01	D5		Not settable
This provides measurement information about the RTD 6 fault.				
RTD 7	01	D6		Not settable
This provides measurement information about the RTD 7 fault.				
RTD 8	01	D7		Not settable
This provides measurement information about the RTD 8 fault.				
RTD 9	01	D8		Not settable
This provides measurement information about the RTD 9 fault.				
RTD 10	01	D9		Not settable
This provides measurement information about the RTD 10 fault.				
CLIO Input 1	01	DA		Not settable
This provides measurement information about the CLIO Input 1 fault.				
CLIO Input 2	01	DB		Not settable
This provides measurement information about the CLIO Input 2 fault.				
CLIO Input 3	01	DC		Not settable
This provides measurement information about the CLIO Input 3 fault.				
CLIO Input 4	01	DD		Not settable
This provides measurement information about the CLIO Input 4 fault.				
Evt Iface Source	01	FA		
Evt Access Level	01	FB		
Evt Extra Info	01	FC		
Evt Unique Id	01	FE		
Reset Indication	01	FF	No	No or Yes

Menu Text	Col	Row	Default Setting	Available Setting
Description				
Resets latched LEDs and latched relay contacts provided the relevant protection element has reset				

Table 1 - View Records

2.1 Types of Event

An event may be a change of state of a control input or output relay, an alarm condition, or a setting change. The following sections show the various items that constitute an event:

2.1.1 Change of State of Opto-Isolated Inputs

If one or more of the opto (logic) inputs has changed state since the last time the protection algorithm ran, the new status is logged as an event. When this event is selected to be viewed on the LCD, three cells appear, as in shown here:

```
Time & date of event
“LOGIC INPUTS1”
“Event Value 0101010101010101”
```

The Event Value is a multi-bit word (see note) showing the status of the opto inputs, where the least significant bit (extreme right) corresponds to opto input 1. The same information is present if the event is extracted and viewed using a PC.

Note	*For P24x or P44x the Event Value is an 8 or 16 bit word.* *For P34x or P64x it is an 8, 12, 16, 24 or 32-bit word.* *For P445 it is an 8, 12 or 16-bit word.* *For P44y, P54x, P547 or P841, it is an 8, 12, 16 or 24-bit word.* *For P74x it is a 12, 16, 24 or 32-bit word.* *For P746 or P849 it is a 32-bit word.*

2.1.2 Change of State of one or more Output Relay Contacts

If one or more of the output relay contacts have changed state since the last time the protection algorithm ran, the new status is logged as an event. When this event is selected to be viewed on the LCD, three cells appear, as shown here:

```
Time and Date of Event
Output Contacts
Event Value 01010101010101010101
```

The Event Value is a multi-bit word (see Note) showing the status of the output contacts, where the least significant bit (extreme right) corresponds to output contact 1, etc. The same information is present if the event is extracted and viewed using a PC.

Note *For P24x the Event Value is is a 7 or 16-bit word.*
For P34x or P64x it is an 7, 11, 14, 15, 16, 22, 24 or 32-bit word.
For P445 it is an 8, 12 or 16-bit word.
For P44x it is a 7, 14 or 21 bit word.
For P44y, P54x, P547 or P841, it is an 8, 12, 16, 24 or 32 bit word.
For P74x it is a 12, 16, 24 or 32 bit word.
For P746 or P849 it is a 24-bit word.

2.1.3 Relay Alarm Conditions

Any alarm conditions generated by the relays are logged as individual events. This table shows examples of some of the alarm conditions and how they appear in the event list:

Alarm condition	Resulting event	
	Event text	Event value
Alarm Status 1 (Alarms 1 to 32) (32 bits)		
Not used		Bit positions 0 to 1 in 32-bit field
Setting Group Via Opto Invalid	SG-DDB Invalid	Bit position 2 in 32-bit field
This alarm is not operative because the CB Monitoring function is not available	CB Status Alarm	Bit position 3 in 32-bit field
RTD Thermal Alarm	RTD Thermal Alm	Bit position 4 in 32-bit field
RTD Open Circuit Failure	RTD Open Cct	Bit position 5 in 32-bit field
RTD Short Circuit Failure	RTD Short Cct	Bit position 6 in 32-bit field
RTD Data Inconsistency Error	RTD data error	Bit position 7 in 32-bit field
RTD Board Failure	RTD board fail	Bit position 8 in 32-bit field
Current Loop Input 1 Alarm	CL Input 1 Alarm	Bit position 9 in 32-bit field
Current Loop Input 2 Alarm	CL Input 2 Alarm	Bit position 10 in 32-bit field
Current Loop Input 3 Alarm	CL Input 3 Alarm	Bit position 11 in 32-bit field
Current Loop Input 4 Alarm	CL Input 4 Alarm	Bit position 12 in 32-bit field
Current Loop Input 1 Undercurrent Fail Alarm	CL1 I< Fail Alm	Bit position 13 in 32-bit field
Current Loop Input 2 Undercurrent Fail Alarm	CL2 I< Fail Alm	Bit position 14 in 32-bit field
Current Loop Input 3 Undercurrent Fail Alarm	CL3 I< Fail Alm	Bit position 15 in 32-bit field
Current Loop Input 4 Undercurrent Fail Alarm	CL4 I< Fail Alm	Bit position 16 in 32-bit field
Protection Disabled	Prot'n Disabled ON/OFF	Bit positions 17 in 32-bit field
Frequency Out of Range	Freq out of Range ON/OFF	Bit positions 18 in 32-bit field
Not used		Bit positions 19 to 21 in 32-bit field
Current loop card input fail	CL Card I/P Fail	Bit positions 22 in 32-bit field
Current loop card output fail	CL Card O/P Fail	Bit positions 23 in 32-bit field
The current input configured in VCO>1	VCO> 1 Config err	Bit positions 24 in 32-bit field

Alarm condition	Resulting event	
	Event text	Event value
setting cell is not located at the same transformer terminal as the main VT.		
The current input configured in VCO>2 setting cell is not located at the same transformer terminal as the main VT.	VCO> 2 Config err	Bit positions 25 in 32-bit field
Not used		Bit positions 26 in 32-bit field
Current transformer supervision alarm	CT Fail Alarm	Bit position 27 in 32
Circuitry fail alarm	Cct Fail Alarm	Bit position 28 in 32
Voltage transformer supervision alarm	VT Fail Alarm	Bit position 29 in 32
Thermal pre-trip alarm	ThermalPretrp Alm	Bit position 30 in 32
Ageing acceleration factor alarm	FAA alarm	Bit position 31 in 32
Alarm Status 2 (Alarms 1 to 32) (32 bits)		
LOL alarm	LOL alarm	Bit position 0 in 32-bit field
CB Trip Fail Protection	Breaker Fail	Bit position 1 in 32-bit field
The ratio correction factor is out of range	Ct para mistmatch	Bit position 2 in 32-bit field
One current input is assigned to more than one terminal.	Ct Selection Alm	Bit position 3 in 32-bit field
Any of the single phase CTs is assigned at the same time to the high impedance REF and any other protection function such as earth fault current or circuit breaker failure.	SinglePha CT Alm	Bit position 4 in 32-bit field
Only one CT is left for the differential function.	Insuff No. of CT	Bit position 5 in 32-bit field
The CT stored status does not match the status after the power supply is re-established.	Disc CT invalid	Bit position 6 in 32-bit field
Scaling factor of HV low impedance REF is out of range	HV-LZREF sf OOR	Bit position 7 in 32-bit field
Scaling factor of LV low impedance REF is out of range	LV-LZREF sf OOR	Bit position 8 in 32-bit field
Scaling factor of TV low impedance REF is out of range	TV-LZREF sf OOR	Bit position 9 in 32-bit field
Scaling factor of autotransformer low impedance REF is out of range	AutoLZREF sf OOR	Bit position 10 in 32-bit field
Not used		Bit positions 11 to 20 in 32-bit field
W1 overfluxing element alarm	W1 V/Hz>1 Alarm	Bit position 21 in 32-bit field
W1 overfluxing element pretrip alarm	W1 V/Hz>2 PrTrp	Bit position 22 in 32-bit field
W2 overfluxing element alarm	W2 V/Hz>1 Alarm	Bit position 23 in 32-bit field
W2 overfluxing element pretrip alarm	W2 V/Hz>2 PrTrp	Bit position 24 in 32-bit field
Not used		Bit positions 25 to 26 in 32-bit field
Frequency Protection Alarm	Freq Prot Alm	Bit position 27 in 32-bit field
Through fault Alarm	Throu fault Alm	Bit position 28 in 32-bit field
unused		Bit positions 29 to 31 in 32-bit field
Alarm Status 3 (Alarms 1 to 32) (32 bits)		
Battery Fail	Battery Fail	Bit position 0 in 32-bit field
Field Voltage Fail	Field Volt Fail	Bit position 1 in 32-bit field
unused		Bit position 2 in 32-bit field
Enrolled GOOSE IED absent alarm indication	Goose IED Absent	Bit position 3 in 32-bit field
Network Interface Card not fitted/failed alarm	NIC not fitted	Bit position 4 in 32-bit field
Network Interface Card not responding alarm	NIC no response	Bit position 5 in 32-bit field
Network Interface Card fatal error alarm	NIC fatal error	Bit position 6 in 32-bit field

Alarm condition	Resulting event	
	Event text	Event value
indication		
Not used		Bit positions 7 to 9 in 32-bit field
Bad TCP/IP Configuration Alarm	Bad TCP/IP Cfg	Bit position 8 in 32-bit field
		Bit position 9 in 32-bit field
Network Interface Card link fail alarm indication Note This applies to Software Version 04, but it has been removed from Software Version B1.	NIC link fail	Bit position 10 in 32-bit field
Main card/NIC software mismatch alarm indication	NIC software mismatch	Bit position 11 in 32-bit field
IP address conflict alarm indication	IP Addr Conflict	Bit position 12 in 32-bit field
Not used		Bit positions 13 in 32-bit field
IEC 61850 Configuration file is invalid. Note This applies to Software Version B1, but does not apply to Software Version 04.	Invalid Config.	Bit positions 14 in 32-bit field
Not used		Bit positions 15 to 16 in 32-bit field
Error when writing the settings from RAM to Flash memory	Back up Setting	Bit position 17 in 32-bit field
It is only available when DNP3 over Ethernet is in used.	Bad DNP Settings	Bit positions 18 to 19 in 32-bit field
Commissions under test mode status. Note This applies to Software Version B1, but does not apply to Software Version 04.	Test Mode Alm	Bit positions 20 in 32-bit field
Commissions under Contracts Blocked status. Note This applies to Software Version B1, but does not apply to Software Version 04.	Contacts Blk Alm	Bit positions 21in 32-bit field
It is only available when DNP3 over Ethernet is in used.	Bad DNP Settings	Bit positions 22 to 31 in 32-bit field
Alarm Status 4 (Alarms 1 to 32) (32 bits)		
User alarm 1	User alarm 1	Bit position 0 in 32-bit field
User alarm 32	User alarm 32	Bit position 31 in 32-bit field

Table 2 - Relay alarm conditions

The previous table shows the abbreviated description given to the various alarm conditions and a corresponding value between 0 and 31. This value is appended to each alarm event in a similar way to the input and output events described previously. It is used by the event extraction software, such as MiCOM S1 Studio, to identify the alarm and is therefore invisible if the event is viewed on the LCD. ON or OFF is shown after the description to signify whether the particular condition has become operated or has reset.

The User Alarms can be operated from an opto input or a control input using the PSL. They can be useful to give an alarm LED and message on the LCD and an alarm indication through the communications of an external condition, for example trip circuit supervision alarm or rotor earth fault alarm. Label the user alarm in the setting file in MiCOM S1 Studio to give a more meaningful description on the LCD.

2.1.4 Protection Element Starts and Trips

Any operation of protection elements, (either a start or a trip condition) is logged as an event record, consisting of a text string indicating the operated element and an event value. This value is intended for use by the event extraction software, such as MiCOM S1 Studio, rather than for the user, and is invisible when the event is viewed on the LCD.

2.1.5 General Events

Several events come under the heading of **General Events**. An example appears here.

Nature of event	Displayed text in event record	Displayed value
Password modified, either from the front or the rear port.	PW modified F, R or R2	0 F=11, R=16, R2=38. For P44x, the value displayed is 0.

A complete list of the General Events is in the Relay Menu Database document. This is a separate document, for each MiCOM Px4x product or product range. They are normally available for download from www.schneider-electric.com

2.1.6 Fault Records

Each time a fault record is generated, an event is also created. The event states that a fault record was generated, with a corresponding time stamp.

Further down the **VIEW RECORDS** column, select the **Select Fault** cell to view the actual fault record, which is selectable from up to 20 records. These records consist of fault flags, fault location, fault measurements, etc. The time stamp given in the fault record is more accurate than the corresponding stamp given in the event record as the event is logged some time after the actual fault record is generated.

The fault record is triggered from the **Fault REC. TRIG.** signal assigned in the default programmable scheme logic. Normally this is assigned to relay 3, protection trip. The fault measurements in the fault record are given at the time of the protection start.

These records consist of fault flags, fault location, fault measurements, etc. The time stamp given in the fault record is more accurate than the corresponding stamp given in the event record as the event is logged some time after the actual fault record is generated.

The latest fault record can also be retrieved over DNP3.0 and IEC61850, please refer to *Chapter 15 SCADA Communication* section 7.6 and section 8.3 for detailed information.

2.1.7 Setting Changes

Changes to any setting in the relay are logged as an event. For example:

Type of setting change	Displayed text in event record	Displayed value
Control/Support Setting	C & S Changed	22
Group # Change	Group # Changed	#
Where # = 1 to 4		

Note	*Control/Support settings are communications, measurement, CT/VT ratio settings etc, which are not duplicated in the setting groups. When any of these settings are changed, the event record is created simultaneously. Changes to protection or disturbance recorder settings only generate an event once the settings have been confirmed at the 'setting trap'.*

2.2 Resetting of Event or Fault Records

To delete the event, fault or maintenance reports, use the **RECORD CONTROL** column.

2.3 Viewing Event Records using MiCOM S1 Studio Support Software

When the event records are extracted and viewed on a PC they look slightly different than when viewed on the LCD. The following shows an example of how various events appear when displayed using MiCOM S1 Studio:

Monday 08 January 2001 18:45:28.633 GMT V<1 Trip A/AB ON

Schneider Electric: MiCOM P643
Model Number: P643314B2A0020A
Address: 001 Column: 0F Row: 26
Event Type: Setting event
Event Value: 00000001000000000000000000000000

Monday 08 January 2001 18:45:28.634 GMT Output Contacts

Schneider Electric: MiCOM P643
Model Number: P643314B2A0020A
Address: 001 Column: 00 Row: 21
Event Type: Device output changed state
Event Value: 00000000001100

OFF 0 Output R1
OFF 1 Output R2
ON 2 R3 Any Trip
ON 3 R4 General Alarm
OFF 4 R5 CB Fail
OFF 5 R6 E/F Trip
OFF 6 R7 Volt Trip
OFF 7 R8 Freq Trip
OFF 8 R9 Diff Trip
OFF 9 Output R10
OFF 10 R11 NPS Trip
OFF 11 Output R12
OFF 12 Output R13
OFF 13 R14 V/Hz Trip

Monday 08 January 2001 18:45:28.633 GMT Voltage Prot Alm ON

Schneider Electric: MiCOM P643
Model Number: P643314B2A0020A
Address: 001 Column: 00 Row: 22
Event Type: Alarm event
Event Value: 00001000000000000000000000000000

OFF 0 Battery Fail
OFF 1 Field Volt Fail
OFF 2 SG-opto Invalid
OFF 3 Prot'n Disabled
OFF 4 VT Fail Alarm
OFF 5 CT Fail Alarm
OFF 6 CB Fail Alarm
OFF 7 Not Used
OFF 8 Not Used
OFF 9 Not Used
OFF 10 Not Used
OFF 11 Not Used
OFF 12 Not Used
OFF 13 Fault Freq Lock
OFF 14 CB Status Alarm
OFF 15 Not Used
OFF 16 Not Used
OFF 17 Not Used
OFF 18 NPS Alarm
OFF 19 V/Hz Alarm
OFF 20 Field Fail Alarm

OFF 21 RTD Thermal Alm
OFF 22 RTD Open Cct
OFF 23 RTD short Cct
OFF 24 RTD Data Error
OFF 25 RTD Board Fail
OFF 26 Freq Prot Alm
ON 27 Voltage Prot Alm
OFF 28 User Alarm 1
OFF 29 User Alarm 2
OFF 30 User Alarm 3
OFF 31 User Alarm 4

The first line gives the description and time stamp for the event, while the additional information displayed below may be collapsed using the +/– symbol.

For further information regarding events and their specific meaning, refer to the *Menu Database* document. This standalone document not included in this manual.

2.4 Event Filtering

Event reporting can be disabled from all interfaces that support setting changes. The settings that control the various types of events are in the RECORD CONTROL column. The effect of setting each to disabled is in shown in the following table:

> *Note* *Some occurrences can result in more than one type of event, e.g. a battery failure will produce an alarm event and a maintenance record event.*

If the Protection Event setting is Enabled, a further set of settings is revealed which allow the event generation by individual DDB signals to be enabled or disabled.

For further information on events and their specific meaning, see the *Relay Menu Database* document.

Menu Text	Col	Row	Default Setting	Available Setting
Description				
RECORD CONTROL	0B	00		
This column contains RECORD CONTROL parameter				
Clear Events	0B	01	No	0 = No or 1 = Yes
Clear Event records				
Clear Faults	0B	02	No	0 = No or 1 = Yes
Clear Fault records				
Clear Maint	0B	03	No	0 = No or 1 = Yes
Clear Maintenance records				
Alarm Event	0B	04	Enabled	Enabled or Disabled
Disabling this setting means that no event is generated for all alarms				
Relay O/P Event	0B	05	Enabled	Enabled or Disabled
Disabling this setting means that no event is generated for any change in relay output contact state				
Opto Input Event	0B	06	Enabled	Enabled or Disabled
Disabling this setting means that no event is generated for any change in logic input state				
General Event	0B	07	Enabled	Enabled or Disabled
Disabling this setting means that no General Events is generated				
Fault Rec Event	0B	08	Enabled	Enabled or Disabled
Disabling this setting means that no event is generated for any fault that produces a fault record.				
Maint Rec Event	0B	09	Enabled	Enabled or Disabled
Disabling this setting means that no event is generated for any maintenance records				
Protection Event	0B	0A	Enabled	Enabled or Disabled
Disabling this setting means that no event is generated for any operation of the protection elements				
Clear Dist Recs	0B	30	No	0 = No or 1 = Yes
Clear Disturbance records				
Security Event	0B	31	Enabled	Enabled or Disabled
Disabling this setting means that any operation of security elements will not be logged as an event				
DDB 31 - 0	0B	40	0xFFFFFFFF	32-bit binary setting
Digital Data Bus (DDB) 1 = event recording Enabled, 0 = event recording Disabled				
DDB 63 - 32	0B	41	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 63 - 32 instead				
DDB 95 - 64	0B	42	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 95 - 64 instead				
DDB 127 - 96	0B	43	0xFFFFFFFF	32-bit binary setting

Menu Text	Col	Row	Default Setting	Available Setting
Description				
This setting works in the same way as DDB 31 - 0 but for DDB 127 - 96 instead				
DDB 159 - 128	0B	44	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 159 - 128 instead				
DDB 191 - 160	0B	45	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 191 - 160 instead				
DDB 223 - 192	0B	46	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 223 - 192 instead				
DDB 255 - 224	0B	47	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 255 - 224 instead				
DDB 287 - 256	0B	48	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 287 - 256 instead				
DDB 319 - 288	0B	49	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 319 - 288 instead				
DDB 351 - 320	0B	4A	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 351 - 320 instead				
DDB 383 - 352	0B	4B	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 383 - 352 instead				
DDB 415 - 384	0B	4C	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 415 - 384 instead				
DDB 447 - 416	0B	4D	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 447 - 416 instead				
DDB 479 - 448	0B	4E	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 479 - 448 instead				
DDB 511 - 480	0B	4F	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 511 - 480 instead				
DDB 543 - 512	0B	50	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 543 - 512 instead				
DDB 575 - 544	0B	51	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 575 - 544 instead				
DDB 607 - 576	0B	52	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 607 - 576 instead				
DDB 639 - 608	0B	53	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 639 - 608 instead				
DDB 671 - 640	0B	54	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 671 - 640 instead				
DDB 703 - 672	0B	55	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 703 - 672 instead				
DDB 735 - 704	0B	56	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 735 - 704 instead				
DDB 767 - 736	0B	57	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 767 - 736 instead				
DDB 799 - 768	0B	58	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 799 - 768 instead				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
DDB 831 - 800	0B	59	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 831 - 800 instead				
DDB 863 - 832	0B	5A	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 863 - 832 instead				
DDB 895 - 864	0B	5B	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 895 - 864 instead				
DDB 927 - 896	0B	5C	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 927 - 896 instead				
DDB 959 - 928	0B	5D	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 959 - 928 instead				
DDB 991 - 960	0B	5E	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 991 - 960 instead				
DDB 1023 - 992	0B	5F	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1023 - 992 instead				
DDB 1055-1024	0B	60	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1055-1024 instead				
DDB 1087-1056	0B	61	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1087-1056 instead				
DDB 1119-1088	0B	62	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1119-1088 instead				
DDB 1151-1120	0B	63	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1151-1120 instead				
DDB 1183-1152	0B	64	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1183-1152 instead				
DDB 1215-1184	0B	65	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1215-1184 instead				
DDB 1247-1216	0B	66	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1247-1216 instead				
DDB 1279-1248	0B	67	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1279-1248 instead				
DDB 1311-1280	0B	68	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1311-1280 instead				
DDB 1343-1312	0B	69	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1343-1312 instead				
DDB 1375-1344	0B	6A	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1375-1344 instead				
DDB 1407-1376	0B	6B	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1407-1376 instead				
DDB 1439-1408	0B	6C	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1439-1408 instead				
DDB 1471-1440	0B	6D	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1471-1440 instead				
DDB 1503-1472	0B	6E	0xFFFFFFFF	32-bit binary setting

Menu Text	Col	Row	Default Setting	Available Setting
Description				
This setting works in the same way as DDB 31 - 0 but for DDB 1503-1472 instead				
DDB 1535-1504	0B	6F	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1535-1504 instead				
DDB 1567-1536	0B	70	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1567-1536 instead				
DDB 1599-1568	0B	71	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1599-1568 instead				
DDB 1631-1600	0B	72	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1631-1600 instead				
DDB 1663-1632	0B	73	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1663-1632 instead				
DDB 1695-1664	0B	74	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1695-1664 instead				
DDB 1727-1696	0B	75	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1727-1696 instead				
DDB 1759-1728	0B	76	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1759-1728 instead				
DDB 1791-1760	0B	77	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1791-1760 instead				
DDB 1823-1792	0B	78	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1823-1792 instead				
DDB 1855-1824	0B	79	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1855-1824 instead				
DDB 1887-1856	0B	7A	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1887-1856 instead				
DDB 1919-1888	0B	7B	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1919-1888 instead				
DDB 1951-1920	0B	7C	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1951-1920 instead				
DDB 1983-1952	0B	7D	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 1983-1952 instead				
DDB 2015-1984	0B	7E	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 2015-1984 instead				
DDB 2047-2016	0B	7F	0xFFFFFFFF	32-bit binary setting
This setting works in the same way as DDB 31 - 0 but for DDB 2047-2016 instead				

Important	***The 0xFFFFFFFF setting represents a 32 bit setting to enable or disable the event recording for the relevant range of DDBs. For each bit 1 = event recording Enabled, bit 0 = event recording Disabled.***
Important	***Some occurrences result in more than one type of event, for example a battery failure produces an alarm event and a maintenance record event.***

Table 3 - Record control

3 DISTURBANCE RECORDER

The integral enhanced disturbance recorder has an area of memory specifically set aside for record storage. The number of records that may be stored by the relay is dependent on the selected recording duration and the installed software release.

The relay can typically store a pre-set minimum number of records, each of a pre-set duration. These may vary between different MiCOM products.

Disturbance records continue to be recorded until the available memory is exhausted, at which time the oldest record(s) are overwritten to make space for the newest one.

The recorder stores actual samples that are taken at a rate of pre-defined number of samples per cycle. Again, this may vary between different MiCOM products.

Each disturbance record consists of a number of analog data channels and digital data channels.

The relevant CT and VT ratios for the analog channels are also extracted to enable scaling to primary quantities. If a CT ratio is set less than unity, the relay will choose a scaling factor of zero for the appropriate channel.

Important	***The Default Setting can vary depending on the individual product. Where G31 is shown in the relevant cell in Table 4, the default settings are shown in Table 5 – G31.***

Menu Text	Col	Row	Default Setting	Available Setting
Description				
DISTURB RECORDER	0C	00		
This column contains DISTURBANCE RECORDER paramaters				
Duration	0C	52	1.5	0.1s to 10.5s step 0.01s
Overall recording time setting				
Trigger Position	0C	54	33.3	0% to 100% step 0.1%
Trigger point setting as a percentage of the duration. For example, the default settings show the overall recording time is set to 1.5 s with the trigger point being at 33.3% of this, giving 0.5 s pre-fault and 1 s post fault recording times				
Trigger Mode	0C	56	Single	Single or Extended
If set to single mode, and if a further trigger occurs while a recording is taking place, the recorder ignores the trigger. However, if this is set to Extended, the post trigger timer is reset to zero, extending the recording time				
Analog Channel 1	0C	58	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
Selects any available analog input to be assigned to this channel				
Analog Channel 2	0C	59	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
This works in the same way as Analog Channel 1 but for Analog Channel 2 instead.				
Analog Channel 3	0C	5A	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC

Menu Text	Col	Row	Default Setting	Available Setting
Description				
This works in the same way as Analog Channel 1 but for Analog Channel 3 instead.				
Analog Channel 4	0C	5B	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
This works in the same way as Analog Channel 1 but for Analog Channel 4 instead.				
Analog Channel 5	0C	5C	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
This works in the same way as Analog Channel 1 but for Analog Channel 5 instead.				
Analog Channel 6	0C	5D	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
This works in the same way as Analog Channel 1 but for Analog Channel 6 instead.				
Analog Channel 7	0C	5E	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
This works in the same way as Analog Channel 1 but for Analog Channel 7 instead.				
Analog Channel 8	0C	5F	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
This works in the same way as Analog Channel 1 but for Analog Channel 8 instead.				
Analog Channel 9	0C	60	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
This works in the same way as Analog Channel 1 but for Analog Channel 9 instead.				
AnalogChannel 10	0C	61	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
This works in the same way as Analog Channel 1 but for AnalogChannel 10 instead.				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
AnalogChannel 11	0C	62	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
This works in the same way as Analog Channel 1 but for AnalogChannel 11 instead.				
AnalogChannel 12	0C	63	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
This works in the same way as Analog Channel 1 but for AnalogChannel 12 instead.				
AnalogChannel 13	0C	64	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
This works in the same way as Analog Channel 1 but for AnalogChannel 13 instead.				
AnalogChannel 14	0C	65	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
This works in the same way as Analog Channel 1 but for AnalogChannel 14 instead.				
AnalogChannel 15	0C	66	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
This works in the same way as Analog Channel 1 but for AnalogChannel 15 instead.				
AnalogChannel 16	0C	67	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
This works in the same way as Analog Channel 1 but for AnalogChannel 16 instead.				
AnalogChannel 17	0C	68	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
This works in the same way as Analog Channel 1 but for AnalogChannel 17 instead.				
AnalogChannel 18	0C	69	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC

Menu Text	Col	Row	Default Setting	Available Setting
Description				
This works in the same way as Analog Channel 1 but for AnalogChannel 18 instead.				
AnalogChannel 19	0C	6A	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
This works in the same way as Analog Channel 1 but for AnalogChannel 19 instead.				
AnalogChannel 20	0C	6B	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
P643, P645 and P746 only. This works in the same way as Analog Channel 1 but for AnalogChannel 20 instead.				
AnalogChannel 21	0C	6C	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
P643, P645 and P746 only. This works in the same way as Analog Channel 1 but for AnalogChannel 21 instead.				
AnalogChannel 22	0C	6D	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
P643 and P645 only. This works in the same way as Analog Channel 1 but for AnalogChannel 22 instead.				
AnalogChannel 23	0C	6E	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
P643 and P645 only. This works in the same way as Analog Channel 1 but for AnalogChannel 23 instead.				
AnalogChannel 24	0C	6F	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
P643 and P645 only. This works in the same way as Analog Channel 1 but for AnalogChannel 24 instead.				
AnalogChannel 25	0C	70	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
P643 and P645 only. This works in the same way as Analog Channel 1 but for AnalogChannel 25 instead.				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
AnalogChannel 26	0C	71	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
P643 and P645 only. This works in the same way as Analog Channel 1 but for AnalogChannel 26 instead.				
AnalogChannel 27	0C	72	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
P645 only. This works in the same way as Analog Channel 1 but for AnalogChannel 27 instead.				
AnalogChannel 28	0C	73	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
P645 only. This works in the same way as Analog Channel 1 but for AnalogChannel 28 instead.				
AnalogChannel 29	0C	74	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
P645 only. This works in the same way as Analog Channel 1 but for AnalogChannel 29 instead.				
AnalogChannel 30	0C	75	G31	Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC
P645 only. This works in the same way as Analog Channel 1 but for AnalogChannel 30 instead.				
Digital Input 1	0C	80	Output R1	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
The digital channels can be mapped to any of the opto isolated inputs or output contacts, in addition to several internal relay digital signals such as protection starts and LEDs				
Input 1 Trigger	0C	81	No Trigger	No trigger, Trigger L/H or Trigger H/L
Any of the digital channels can be selected to trigger the disturbance recorder on either a low-to-high (L/H) or a high-to-low (H/L) transition				
Digital Input 2	0C	82	Output R2	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 2 instead.				
Input 2 Trigger	0C	83	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 2 Trigger instead.				
Digital Input 3	0C	84	Output R3	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals

Menu Text	Col	Row	Default Setting	Available Setting
Description				
This works in the same way as Digital Input 1 but for Digital Input 3 instead.				
Input 3 Trigger	0C	85	Trigger L/H	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 3 Trigger instead.				
Digital Input 4	0C	86	Output R4	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 4 instead.				
Input 4 Trigger	0C	87	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 4 Trigger instead.				
Digital Input 5	0C	88	Output R5	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 5 instead.				
Input 5 Trigger	0C	89	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 5 Trigger instead.				
Digital Input 6	0C	8A	Output R6	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 6 instead.				
Input 6 Trigger	0C	8B	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 6 Trigger instead.				
Digital Input 7	0C	8C	Output R7	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 7 instead.				
Input 7 Trigger	0C	8D	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 7 Trigger instead.				
Digital Input 8	0C	8E	Output R8	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 8 instead.				
Input 8 Trigger	0C	8F	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 8 Trigger instead.				
Digital Input 9	0C	90	Output R9	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 9 instead.				
Input 9 Trigger	0C	91	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 9 Trigger instead.				
Digital Input 10	0C	92	Input L3	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 10 instead.				
Input 10 Trigger	0C	93	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 10 Trigger instead.				
Digital Input 11	0C	94	Input L4	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 11 instead.				
Input 11 Trigger	0C	95	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 11 Trigger instead.				
Digital Input 12	0C	96	Input L5	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 12 instead.				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
Input 12 Trigger	0C	97	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 12 Trigger instead.				
Digital Input 13	0C	98	Input L6	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 13 instead.				
Input 13 Trigger	0C	99	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 13 Trigger instead.				
Digital Input 14	0C	9A	Input L7	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 14 instead.				
Input 14 Trigger	0C	9B	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 14 Trigger instead.				
Digital Input 15	0C	9C	Input L8	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 15 instead.				
Input 15 Trigger	0C	9D	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 15 Trigger instead.				
Digital Input 16	0C	9E	Unused	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 16 instead.				
Input 16 Trigger	0C	9F	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 16 Trigger instead.				
Digital Input 17	0C	A0	Unused	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 17 instead.				
Input 17 Trigger	0C	A1	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 17 Trigger instead.				
Digital Input 18	0C	A2	Unused	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 18 instead.				
Input 18 Trigger	0C	A3	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 18 Trigger instead.				
Digital Input 19	0C	A4	Unused	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 19 instead.				
Input 19 Trigger	0C	A5	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 19 Trigger instead.				
Digital Input 20	0C	A6	Unused	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 20 instead.				
Input 20 Trigger	0C	A7	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 20 Trigger instead.				
Digital Input 21	0C	A8	Unused	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 21 instead.				
Input 21 Trigger	0C	A9	No Trigger	No trigger, Trigger L/H or Trigger H/L

Menu Text	Col	Row	Default Setting	Available Setting
Description				
This works in the same way as Input 1 Trigger but for Input 21 Trigger instead.				
Digital Input 22	0C	AA	Unused	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 22 instead.				
Input 22 Trigger	0C	AB	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 22 Trigger instead.				
Digital Input 23	0C	AC	Unused	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 23 instead.				
Input 23 Trigger	0C	AD	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 23 Trigger instead.				
Digital Input 24	0C	AE	Unused	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 24 instead.				
Input 24 Trigger	0C	AF	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 24 Trigger instead.				
Digital Input 25	0C	B0	Unused	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 25 instead.				
Input 25 Trigger	0C	B1	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 25 Trigger instead.				
Digital Input 26	0C	B2	Unused	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 26 instead.				
Input 26 Trigger	0C	B3	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 26 Trigger instead.				
Digital Input 27	0C	B4	Unused	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 27 instead.				
Input 27 Trigger	0C	B5	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 27 Trigger instead.				
Digital Input 28	0C	B6	Unused	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
P746 only. This works in the same way as Digital Input 1 but for Digital Input 28 instead.				
Input 28 Trigger	0C	B7	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 28 Trigger instead.				
Digital Input 29	0C	B8	Unused	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 29 instead.				
Input 29 Trigger	0C	B9	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 29 Trigger instead.				
Digital Input 30	0C	BA	Unused	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 30 instead.				
Input 30 Trigger	0C	BB	No Trigger	No trigger, Trigger L/H or Trigger H/L

Menu Text	Col	Row	Default Setting	Available Setting
Description				
This works in the same way as Input 1 Trigger but for Input 30 Trigger instead.				
Digital Input 31	0C	BC	Unused	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 31 instead.				
Input 31 Trigger	0C	BD	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 31 Trigger instead.				
Digital Input 32	0C	BE	Unused	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals
This works in the same way as Digital Input 1 but for Digital Input 32 instead.				
Input 32 Trigger	0C	BF	No Trigger	No trigger, Trigger L/H or Trigger H/L
This works in the same way as Input 1 Trigger but for Input 32 Trigger instead.				

Table 4 - Disturbance recorder settings

Type G31	P642	P643	P645
Default Setting	Analog Channel No		
VA		0	0
VB		1	1
VC		2	2
VX	0	3	3
Unused	1	4	4
IA1	2	5	5
IB1	3	6	6
IC1	4	7	7
IN1	5	8	8
IA2	6	9	9
IB2	7	10	10
IC2	8	11	11
IN2	9	12	12
IA3		13	13
IB3		14	14
IC3		15	15
IN3		16	16
IA4			17
IB4			18
IC4			19
IA5			20
IB5			21
IC5			22
IA6			
IB6			
IC6			
IA Diff	10	17	23
IB Diff	11	18	24

Type G31	P642	P643	P645
Default Setting	Analog Channel No		
IC Diff	12	19	25
IA Bias	13	20	26
IB Bias	14	21	27
IC Bias	15	22	28
LoZ REF HV Diff	16	23	29
LoZ REF HV Bias	17	24	30
LoZ REF LV Diff	18	25	31
LoZ REF LV Bias	19	26	32
LoZ REF TV Diff		27	33
LoZ REF TV Bias		28	34
LoZ REF Auto Diff	20	29	35
LoZ REF Auto Bias	21	30	36
HighZ REF HV Op	22	31	37
HighZ REF LV Op	23	32	38
HighZ REF TV Op		33	39
HighZ REF Auto Op	24	34	40
Frequency	25	35	41
VAB	26		
VBC	27		

Table 5 – G31 default settings

The pre and post fault recording times are set by a combination of the **Duration** and **Trigger Position** cells. **Duration** sets the overall recording time and the **Trigger Position** sets the trigger point as a percentage of the duration.

- For example, the default settings show that the overall recording time is set to 1.5 s with the trigger point being at 33.3% of this, giving 0.5 s pre-fault and 1 s post-fault recording times.

If a further trigger occurs while a recording is taking place, the recorder ignores the trigger if the **Trigger Mode** is set to **Single**. However, if this is set to **Extended**, the post-trigger timer is reset to zero, extending the recording time.

As can be seen from the menu, each of the analog channels is selectable from the available analog inputs to the relay. The digital channels may be mapped to any of the opto isolated inputs or output contacts, in addition to several internal relay digital signals, such as protection starts and LEDs. The complete list of these signals may be found by viewing the available settings in the relay menu or using a setting file in MiCOM S1 Studio. Any of the digital channels may be selected to trigger the disturbance recorder on either a low-to-high or a high-to-low transition, using the **Input Trigger** cell. The default trigger settings are that any dedicated trip output contacts, such as relay 3, trigger the recorder.

It is not possible to view the disturbance records locally using the LCD; they must be extracted using suitable software such as MiCOM S1 Studio. This process is fully explained in the *SCADA Communications* chapter.

4 MEASUREMENTS

The relay produces a variety of both directly measured and calculated power system quantities. These measurement values are updated every second and can be viewed in the **Measurements** columns (up to three) of the relay or using the MiCOM S1 Studio Measurement viewer.

The relay can measure and display these quantities:

- Phase Voltages and Currents
- Phase to Phase Voltage and Currents
- Sequence Voltages and Currents
- Power and Energy Quantities
- Rms. Voltages and Currents
- Peak, Fixed and Rolling Demand Values

There are also measured values from the protection functions, which are also displayed under the measurement columns of the menu; these are described in the section on the relevant protection function.

4.1 Measured Voltages and Currents

The relay produces both phase-to-ground and phase-to-phase voltage and current values. They are produced directly from the Discrete Fourier Transform (DFT) used by the relay protection functions and present both magnitude and phase angle measurement.

4.2 Sequence Voltages and Currents

Sequence quantities are produced by the relay from the measured Fourier values; these are displayed as magnitude and phase angle values.

4.3 Power and Energy Quantities

Using the measured voltages and currents the relay calculates the apparent, real and reactive power quantities. These are produced phase-by-phase. Three-phase values are based on the sum of the three individual phase values. The signing of the real and reactive power measurements can be controlled using the measurement mode setting. The options are as follows.

Measurement mode	Parameter	Signing
0 (Default)	Export Power Import Power Lagging Vars Leading VArs	+ – + –
1	Export Power Import Power Lagging Vars Leading VArs	– + + –
2	Export Power Import Power Lagging Vars Leading VArs	+ – – +
3	Export Power Import Power Lagging Vars Leading VArs	– + – +

In addition to the measured power quantities, the relay calculates the power factor phase-by-phase, in addition to a three-phase power factor.

These power values are also used to increment the total real and reactive energy measurements. Separate energy measurements are maintained for the total exported and imported energy. The energy measurements are incremented up to maximum values of 1000 GWhr or 1000 GVARhr, at which point they reset to zero. It is also possible to reset these values using the menu or remote interfaces using the **Reset Demand** cell.

4.4 RMS Voltages and Currents

RMS phase voltage and current values are calculated by the relay using the sum of the samples squared over a cycle of sampled data.

4.5 Demand Values

The relay produces fixed, rolling and peak demand values. Using the reset demand menu cell it is possible to reset these quantities from the user interface or the remote communications.

4.5.1 Fixed Demand Values

The fixed demand value is the average value of a quantity over the specified interval; values are produced for each phase current and for three-phase real and reactive power. The fixed demand values displayed by the relay are those for the previous interval. The values are updated at the end of the fixed demand period.

4.5.2 Rolling Demand Values

The rolling demand values are similar to the fixed demand values, the difference being that a sliding window is used. The rolling demand window consists of several smaller sub-periods. The resolution of the sliding window is the sub-period length, with the displayed values updated at the end of each of the sub-periods.

4.5.3 Peak Demand Values

Peak demand values are produced for each phase current and the real and reactive power quantities. These display the maximum value of the measured quantity since the last reset of the demand values.

4.6 Settings

The settings shown under the heading **MEASURE'T SETUP** can be used to configure the relay measurement function. See the following Measurements table for more details:

Menu Text	Col	Row	Default Setting	Available Setting
Description				
MEASURE'T SETUP	0D	00		
This column contains MEASUREMENT SETTINGS				
Default Display	0D	01	User Banner	
Used to select the default display from a range of options				
Local Values	0D	02	Primary	Primary or Secondary
Controls whether measured local values from the rear communication port are displayed as primary or secondary quantities				
Remote Values	0D	03	Primary	Primary or Secondary
Controls whether measured remote values are displayed as primary or secondary quantities				
Measurement Ref	0D	04	IA1	Vx, VA, VB, VC, IA1, IB1, IC1, IA2, IB2, IC2, IA3, IB3, IC3, IA4, IB4, IC4, IA5, IB5, IC5, VAB or VBC
Measurement Ref				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
Measurement Mode	0D	05	0	0, 1, 2 or 3
This setting is used to control the signing of the real and reactive power quantities				

Table 6 - Measure't setup

In the firmware, the fix demand period has been fixed to 15min, the rolling demand to 1min and the number of rolling demand sub-periods 15.

4.7 Measurement Display Quantities

The relay has Measurement columns for viewing measurement quantities. These can also be viewed with MiCOM S1 Studio and are shown below.

- Measurements 1 Table 7 - Measurements 1
- Measurements 2 Table 8 - Measurements 2
- Measurements 3 Table 9 - Measurements 3

4.7.1 Measurements 1

Menu Text	Col	Row	Default Setting	Available Setting
Description				
MEASUREMENTS 1	02	00		
Measurement 1 group for P642, P643, P645				
IA-1 Magnitude	02	01	Data	Not settable
This records the IA-1 Magnitude measurement				
IA-1 Phase Angle	02	02	Data	Not settable
This records the IA-1 Phase Angle measurement				
IB-1 Magnitude	02	03	Data	Not settable
This records the IB-1 Magnitude measurement				
IB-1 Phase Angle	02	04	Data	Not settable
This records the IB-1 Phase Angle measurement				
IC-1 Magnitude	02	05	Data	Not settable
This records the IC-1 Magnitude measurement				
IC-1 Phase Angle	02	06	Data	Not settable
This records the IC-1 Phase Angle measurement				
IA-2 Magnitude	02	07	Data	Not settable
This records the IA-2 Magnitude measurement				
IA-2 Phase Angle	02	08	Data	Not settable
This records the IA-2 Phase Angle measurement				
IB-2 Magnitude	02	09	Data	Not settable
This records the IB-2 Magnitude measurement				
IB-2 Phase Angle	02	0A	Data	Not settable
This records the IB-2 Phase Angle measurement				
IC-2 Magnitude	02	0B	Data	Not settable
This records the IC-2 Magnitude measurement				
IC-2 Phase Angle	02	0C	Data	Not settable
This records the IC-2 Phase Angle measurement				
IA-3 Magnitude	02	0D	Data	Not settable
P643, P645 and P746 only. This records the IA-3 Magnitude measurement				
IA-3 Phase Angle	02	0E	Data	Not settable
P643, P645 and P746 only. This records the IA-3 Phase Angle measurement				
IB-3 Magnitude	02	0F	Data	Not settable

Menu Text	Col	Row	Default Setting	Available Setting
Description				
P643, P645 and P746 only. This records the IB-3 Magnitude measurement				
IB-3 Phase Angle	02	10	Data	Not settable
P643, P645 and P746 only. This records the IB-3 Phase Angle measurement				
IC-3 Magnitude	02	11	Data	Not settable
P643, P645 and P746 only. This records the IC-3 Magnitude measurement				
IC-3 Phase Angle	02	12	Data	Not settable
P643, P645 and P746 only. This records the IC-3 Phase Angle measurement				
IA-4 Magnitude	02	13	Data	Not settable
P645 and P746 only. This records the IA-4 Magnitude measurement				
IA-4 Phase Angle	02	14	Data	Not settable
P645 and P746 only. This records the IA-4 Phase Angle measurement				
IB-4 Magnitude	02	15	Data	Not settable
P645 and P746 only. This records the IB-4 Magnitude measurement				
IB-4 Phase Angle	02	16	Data	Not settable
P645 and P746 only. This records the IB-4 Phase Angle measurement				
IC-4 Magnitude	02	17	Data	Not settable
P645 and P746 only. This records the IC-4 Magnitude measurement				
IC-4 Phase Angle	02	18	Data	Not settable
P645 and P746 only. This records the IC-4 Phase Angle measurement				
IA-5 Magnitude	02	19	Data	Not settable
P645 and P746 only. This records the IA-5 Magnitude measurement				
IA-5 Phase Angle	02	1A	Data	Not settable
P645 and P746 only. This records the IA-5 Phase Angle measurement				
IB-5 Magnitude	02	1B	Data	Not settable
P645 and P746 only. This records the IB-5 Magnitude measurement				
IB-5 Phase Angle	02	1C	Data	Not settable
P645 and P746 only. This records the IB-5 Phase Angle measurement				
IC-5 Magnitude	02	1D	Data	Not settable
P645 and P746 only. This records the IC-5 Magnitude measurement				
IC-5 Phase Angle	02	1E	Data	Not settable
P645 and P746 only. This records the IC-5 Phase Angle measurement				
IA-HV Magnitude	02	50	Data	Not settable

Menu Text	Col	Row	Default Setting	Available Setting
Description				
This records the IA-HV Magnitude measurement				
IA-HV Phase Ang	02	51	Data	Not settable
This records the IA-HV Phase Ang measurement				
IB-HV Magnitude	02	52	Data	Not settable
This records the IB-HV Magnitude measurement				
IB-HV Phase Ang	02	53	Data	Not settable
This records the IB-HV Phase Ang measurement				
IC-HV Magnitude	02	54	Data	Not settable
This records the IC-HV Magnitude measurement				
IC-HV Phase Ang	02	55	Data	Not settable
This records the IC-HV Phase Ang measurement				
IA-LV Magnitude	02	56	Data	Not settable
This records the IA-LV Magnitude measurement				
IA-LV Phase Ang	02	57	Data	Not settable
This records the IA-LV Phase Ang measurement				
IB-LV Magnitude	02	58	Data	Not settable
This records the IB-LV Magnitude measurement				
IB-LV Phase Ang	02	59	Data	Not settable
This records the IB-LV Phase Ang measurement				
IC-LV Magnitude	02	5A	Data	Not settable
This records the IC-LV Magnitude measurement				
IC-LV Phase Ang	02	5B	Data	Not settable
This records the IC-LV Phase Ang measurement				
IA-TV Magnitude	02	5C	Data	Not settable
P643 and P645 only. This records the IA-TV Magnitude measurement				
IA-TV Phase Ang	02	5D	Data	Not settable
P643 and P645 only. This records the IA-TV Phase Ang measurement				
IB-TV Magnitude	02	5E	Data	Not settable
P643 and P645 only. This records the IB-TV Magnitude measurement				
IB-TV Phase Ang	02	5F	Data	Not settable
P643 and P645 only. This records the IB-TV Phase Ang measurement				
IC-TV Magnitude	02	60	Data	Not settable
P643 and P645 only. This records the IC-TV Magnitude measurement				
IC-TV Phase Ang	02	61	Data	Not settable
P643 and P645 only. This records the IC-TV Phase Ang measurement				
I0-1 Magnitude	02	62	Data zero sequence current	Not settable
This records the I0-1 Magnitude measurement				
I1-1 Magnitude	02	63	Data positive sequence current	Not settable
This records the I1-1 Magnitude measurement				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
I2-1 Magnitude	02	64	Data negative sequence current	Not settable
This records the I2-1 Magnitude measurement				
IN-HV Mea Mag	02	65	Data	Not settable
This records the IN-HV Mea Mag measurement				
IN-HV Mea Ang	02	66	Data	Not settable
This records the IN-HV Mea Ang measurement				
IN-HV Deriv Mag	02	67	Data	Not settable
This records the IN-HV Deriv Mag measurement				
IN-HV Deriv Ang	02	68	Data	Not settable
This records the IN-HV Deriv Ang measurement				
I0-2 Magnitude	02	69	Data zero sequence current	Not settable
This records the I0-2 Magnitude measurement				
I1-2 Magnitude	02	6A	Data positive sequence current	Not settable
This records the I1-2 Magnitude measurement				
I2-2 Magnitude	02	6B	Data negative sequence current	Not settable
This records the I2-2 Magnitude measurement				
IN-LV Mea Mag	02	6C	Data	Not settable
This records the IN-LV Mea Mag measurement				
IN-LV Mea Ang	02	6D	Data	Not settable
This records the IN-LV Mea Ang measurement				
IN-LV Deriv Mag	02	6E	Data	Not settable
This records the IN-LV Deriv Mag measurement				
IN-LV Deriv Ang	02	6F	Data	Not settable
This records the IN-LV Deriv Ang measurement				
I0-3 Magnitude	02	70	Data zero sequence current. P643,P645 and P746 only	Not settable
P643, P645 and P746 only. This records the I0-3 Magnitude measurement				
I1-3 Magnitude	02	71	Data positive sequence current. P643,P645 and P746 only	Not settable
P643, P645 and P746 only. This records the I1-3 Magnitude measurement				
I2-3 Magnitude	02	72	Data negative sequence current . P643, P645 and P746 only	Not settable
P643, P645 and P746 only. This records the I2-3 Magnitude measurement				
IN-TV Mea Mag	02	73	Data	Not settable
P643 and P645 only. This records the IN-TV Mea Mag measurement				
IN-TV Mea Ang	02	74	Data	Not settable
P643 and P645 only. This records the IN-TV Mea Ang measurement				
IN-TV Deriv Mag	02	75	Data	Not settable
P643 and P645 only. This records the IN-TV Deriv Mag measurement				
IN-TV Deriv Ang	02	76	Data	Not settable

Menu Text	Col	Row	Default Setting	Available Setting
Description				
P643 and P645 only. This records the IN-TV Deriv Ang measurement				
I0-4 Magnitude	02	77	Data zero sequence current. P645 and P746 only	Not settable
P645 and P746 only. This records the I0-4 Magnitude measurement				
I1-4 Magnitude	02	78	Data positive sequence current. P645 and P746 only	Not settable
P645 and P746 only. This records the I1-4 Magnitude measurement				
I2-4 Magnitude	02	79	Data negative sequence current . P645 and P746 only	Not settable
P645 and P746 only. This records the I2-4 Magnitude measurement				
I0-5 Magnitude	02	7C	Data zero sequence current. P645 and P746 only.	Not settable
P645 and P746 only. This records the I0-5 Magnitude measurement				
I1-5 Magnitude	02	7D	Data positive sequence current. P645 and P746 only.	Not settable
P645 and P746 only. This records the I1-5 Magnitude measurement				
I2-5 Magnitude	02	7E	Data negative sequence current . P645 and P746 only.	Not settable
P645 and P746 only. This records the I2-5 Magnitude measurement				
IA-HV RMS	02	86	Data	Not settable
This records the IA-HV RMS measurement				
IB-HV RMS	02	87	Data	Not settable
This records the IB-HV RMS measurement				
IC-HV RMS	02	88	Data	Not settable
This records the IC-HV RMS measurement				
IA-LV RMS	02	89	Data	Not settable
This records the IA-LV RMS measurement				
IB-LV RMS	02	8A	Data	Not settable
This records the IB-LV RMS measurement				
IC-LV RMS	02	8B	Data	Not settable
This records the IC-LV RMS measurement				
IA-TV RMS	02	8C	Data	Not settable
P643 and P645 only. This records the IA-TV RMS measurement				
IB-TV RMS	02	8D	Data	Not settable
P643 and P645 only. This records the IB-TV RMS measurement				
IC-TV RMS	02	8E	Data	Not settable
P643 and P645 only. This records the IC-TV RMS measurement				
VAN Magnitude	02	8F	Data	Not settable

Menu Text	Col	Row	Default Setting	Available Setting
Description				
P643, P645 and P746 only. This records the VAN Magnitude measurement				
VAN Phase Angle	02	90	Data	Not settable
P643, P645 and P746 only. This records the VAN Phase Angle measurement				
VBN Magnitude	02	91	Data	Not settable
P643, P645 and P746 only. This records the VBN Magnitude measurement				
VBN Phase Angle	02	92	Data	Not settable
P643, P645 and P746 only. This records the VBN Phase Angle measurement				
VCN Magnitude	02	93	Data	Not settable
P643, P645 and P746 only. This records the VCN Magnitude measurement				
VCN Phase Angle	02	94	Data	Not settable
P643, P645 and P746 only. This records the VCN Phase Angle measurement				
Vx Magnitude	02	95	Data	Not settable
This records the Vx Magnitude measurement				
Vx Phase Angle	02	96	Data	Not settable
This records the Vx Phase Angle measurement				
V1 Magnitude	02	97	Data. Positive sequence Voltage	Not settable
This records the V1 Magnitude measurement				
V2 Magnitude	02	98	Data Negative sequence Voltage	Not settable
This records the V2 Magnitude measurement				
V0 Magnitude	02	99	Data Zero sequence voltage	Not settable
P643, P645 and P746 only. This records the V0 Magnitude measurement				
VN Derived Mag	02	9A	Data	Not settable
P643, P645 and P746 only. This records the VN Derived Mag measurement				
VN Derived Angle	02	9B	Data	Not settable
P643, P645 and P746 only. This records the VN Derived Angle measurement				
VAB Magnitude	02	9C	Data	Not settable
This records the VAB Magnitude measurement				
VAB Phase Angle	02	9D	Data	Not settable
This records the VAB Phase Angle measurement				
VBC Magnitude	02	9E	Data	Not settable
This records the VBC Magnitude measurement				
VBC Phase Angle	02	9F	Data	Not settable
This records the VBC Phase Angle measurement				
VCA Magnitude	02	A0	Data	Not settable
This records the VCA Magnitude measurement				
VCA Phase Angle	02	A1	Data	Not settable
This records the VCA Phase Angle measurement				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
VAN RMS	02	A2	Data	Not settable
P643, P645 and P746 only. This records the VAN RMS measurement				
VBN RMS	02	A3	Data	Not settable
P643, P645 and P746 only. This records the VBN RMS measurement				
VCN RMS	02	A4	Data	Not settable
P643, P645 and P746 only. This records the VCN RMS measurement				
Frequency	02	AA	Data	Not settable
This records the Frequency measurement				
IN-T1 Deriv Mag	02	AB	Data	Not settable
P642, P643 and P645 only. This records the IN-T1 Derived Mag measurement.				
IN-T1 Deriv Ang	02	AC	Data	Not settable
P642, P643 and P645 only. This records the IN-T1 Derived Ang measurement.				
IN-T2 Deriv Mag	02	AD	Data	Not settable
P642, P643 and P645 only. This records the IN-T2 Derived Mag measurement.				
IN-T2 Deriv Ang	02	AE	Data	Not settable
P642, P643 and P645 only. This records the IN-T2 Derived Ang measurement.				
IN-T3 Deriv Mag	02	AF	Data	Not settable
P643 and P645 only. This records the IN-T3 Derived Mag measurement.				
IN-T3 Deriv Ang	02	B0	Data	Not settable
P643 and P645 only. This records the IN-T3 Derived Ang measurement.				
IN-T4 Deriv Mag	02	B1	Data	Not settable
P645 only. This records the IN-T4 Derived Mag measurement.				
IN-T4 Deriv Ang	02	B2	Data	Not settable
P645 only. This records the IN-T4 Derived Ang measurement.				
IN-T5 Deriv Mag	02	B3	Data	Not settable
P645 only. This records the IN-T5 Derived Mag measurement.				
IN-T5 Deriv Ang	02	B4	Data	Not settable
P645 only. This records the IN-T5 Derived Ang measurement.				
IN-TN1 Mea Mag	02	B5	Data	Not settable
This records the IN-TN1 Mea Mag measurement				
IN-TN1 Mea Ang	02	B6	Data	Not settable
This records the IN-TN1 Mea Ang measurement				
IN-TN2 Mea Mag	02	B7	Data	Not settable
This records the IN-TN2 Mea Mag measurement				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
IN-TN2 Mea Ang	02	B8	Data	Not settable
This records the IN-TN2 Mea Ang measurement				
IN-TN3 Mea Mag	02	B9	Data	Not settable
P643 and P645 only. This records the IN-TN3 Mea Mag measurement				
IN-TN3 Mea Ang	02	BA	Data	Not settable
P643 and P645 only. This records the IN-TN3 Mea Ang measurement				

Table 7 - Measurements 1

4.7.2 Measurements 2

Menu Text	Col	Row	Default Setting	Available Setting
Description				
MEASUREMENTS 2	03	00		
P643 and P645 only. Measurement 2 Group.				
A Phase Watts	03	01	Data	Not settable
P643 and P645 only. This records the A Phase Watts measurement				
A Phase Watts	03	02	Data	Not settable
P643 and P645 only. This records the A Phase Watts measurement				
A Phase Watts	03	03	Data	Not settable
P643 and P645 only. This records the A Phase Watts measurement				
B Phase Watts	03	04	Data	Not settable
P643 and P645 only. This records the B Phase Watts measurement				
B Phase Watts	03	05	Data	Not settable
P643 and P645 only. This records the B Phase Watts measurement				
B Phase Watts	03	06	Data	Not settable
P643 and P645 only. This records the B Phase Watts measurement				
C Phase Watts	03	07	Data	Not settable
P643 and P645 only. This records the C Phase Watts measurement				
C Phase Watts	03	08	Data	Not settable
P643 and P645 only. This records the C Phase Watts measurement				
C Phase Watts	03	09	Data	Not settable
P643 and P645 only. This records the C Phase Watts measurement				
A Phase VArs	03	0A	Data	Not settable
P643 and P645 only. This records the A Phase VArs measurement				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
A Phase VArs	03	0B	Data	Not settable
P643 and P645 only. This records the A Phase VArs measurement				
A Phase VArs	03	0C	Data	Not settable
P643 and P645 only. This records the A Phase VArs measurement				
B Phase VArs	03	0D	Data	Not settable
P643 and P645 only. This records the B Phase VArs measurement				
B Phase VArs	03	0E	Data	Not settable
P643 and P645 only. This records the B Phase VArs measurement				
B Phase VArs	03	0F	Data	Not settable
P643 and P645 only. This records the B Phase VArs measurement				
C Phase VArs	03	10	Data	Not settable
P643 and P645 only. This records the C Phase VArs measurement				
C Phase VArs	03	11	Data	Not settable
P643 and P645 only. This records the C Phase VArs measurement				
C Phase VArs	03	12	Data	Not settable
P643 and P645 only. This records the C Phase VArs measurement				
A Phase VA	03	13	Data	Not settable
P643 and P645 only. This records the A Phase VA measurement				
A Phase VA	03	14	Data	Not settable
P643 and P645 only. This records the A Phase VA measurement				
A Phase VA	03	15	Data	Not settable
P643 and P645 only. This records the A Phase VA measurement				
B Phase VA	03	16	Data	Not settable
P643 and P645 only. This records the B Phase VA measurement				
B Phase VA	03	17	Data	Not settable
P643 and P645 only. This records the B Phase VA measurement				
B Phase VA	03	18	Data	Not settable
P643 and P645 only. This records the B Phase VA measurement				
C Phase VA	03	19	Data	Not settable
P643 and P645 only. This records the C Phase VA measurement				
C Phase VA	03	1A	Data	Not settable
P643 and P645 only. This records the C Phase VA measurement				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
C Phase VA	03	1B	Data	Not settable
P643 and P645 only. This records the C Phase VA measurement				
3 Phase Watts	03	1C	Data	Not settable
P643 and P645 only. This records the 3 Phase Watts measurement				
3 Phase Watts	03	1D	Data	Not settable
P643 and P645 only. This records the 3 Phase Watts measurement				
3 Phase Watts	03	1E	Data	Not settable
P643 and P645 only. This records the 3 Phase Watts measurement				
3 Phase VArs	03	1F	Data	Not settable
P643 and P645 only. This records the 3 Phase VArs measurement				
3 Phase VArs	03	20	Data	Not settable
P643 and P645 only. This records the 3 Phase VArs measurement				
3 Phase VArs	03	21	Data	Not settable
P643 and P645 only. This records the 3 Phase VArs measurement				
3 Phase VA	03	22	Data	Not settable
P643 and P645 only. This records the 3 Phase VA measurement				
3 Phase VA	03	23	Data	Not settable
P643 and P645 only. This records the 3 Phase VA measurement				
3 Phase VA	03	24	Data	Not settable
P643 and P645 only. This records the 3 Phase VA measurement				
3Ph Power Factor	03	25	Data	Not settable
P643 and P645 only. This records the 3Ph Power Factor measurement				
APh Power Factor	03	26	Data	Not settable
P643 and P645 only. This records the APh Power Factor measurement				
BPh Power Factor	03	27	Data	Not settable
P643 and P645 only. This records the BPh Power Factor measurement				
CPh Power Factor	03	28	Data	Not settable
P643 and P645 only. This records the CPh Power Factor measurement				
3Ph WHours Fwd	03	29	Data	Not settable
P643 and P645 only. This records the 3Ph WHours Fwd measurement				
3Ph WHours Rev	03	2A	Data	Not settable
P643 and P645 only. This records the 3Ph WHours Rev measurement				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
3Ph VArHours Fwd	03	2B	Data	Not settable
P643 and P645 only. This records the 3Ph VArHours Fwd measurement				
3Ph VArHours Rev	03	2C	Data	Not settable
P643 and P645 only. This records the 3Ph VArHours Rev measurement				
3Ph W Fix Demand	03	2D	Data	Not settable
P643 and P645 only. This records the 3Ph W Fix Demand measurement				
3Ph VArs Fix Dem	03	2E	Data	Not settable
P643 and P645 only. This records the 3Ph VArs Fix Dem measurement				
3 Ph W Roll Dem	03	2F	Data	Not settable
P643 and P645 only. This records the 3 Ph W Roll Dem measurement				
3Ph VArs RollDem	03	30	Data	Not settable
P643 and P645 only. This records the 3Ph VArs RollDem measurement				
3Ph W Peak Dem	03	31	Data	Not settable
P643 and P645 only. This records the 3Ph W Peak Dem measurement				
3Ph VAr Peak Dem	03	32	Data	Not settable
P643 and P645 only. This records the 3Ph VAr Peak Dem measurement				
Reset Demand	03	50	No	No or Yes
P643 and P645 only. Reset Demand				

Table 8 - Measurements 2

4.7.3 Measurements 3

Menu Text	Col	Row	Default Setting	Available Setting
Description				
MEASUREMENTS 3	04	00		
P643 and P645 only. Measurement 3 Group.				
IA Differential	04	01	Data	Not settable
This records the IA Differential measurement				
IB Differential	04	02	Data	Not settable
This records the IB Differential measurement				
IC Differential	04	03	Data	Not settable
This records the IC Differential measurement				
IA Bias	04	04	Data	Not settable
This records the IA Bias measurement				
IB Bias	04	05	Data	Not settable
This records the IB Bias measurement				

Menu Text	Col	Row	Default Setting	Available Setting
Description				
IC Bias	04	06	Data	Not settable
This records the IC Bias measurement				
IA Diff 2H	04	07	Data	Not settable
This records the IA Diff 2H measurement				
IB Diff 2H	04	08	Data	Not settable
This records the IB Diff 2H measurement				
IC Diff 2H	04	09	Data	Not settable
This records the IC Diff 2H measurement				
IA Diff 5H	04	0A	Data	Not settable
This records the IA Diff 5H measurement				
IB Diff 5H	04	0B	Data	Not settable
This records the IB Diff 5H measurement				
IC Diff 5H	04	0C	Data	Not settable
This records the IC Diff 5H measurement				
IREF HV LoZ Diff	04	0D	Data	Not settable
This records the IREF HV LoZ Diff measurement				
IREF HV LoZ Bias	04	0E	Data	Not settable
This records the IREF HV LoZ Bias measurement				
IREF LV LoZ Diff	04	0F	Data	Not settable
This records the IREF LV LoZ Diff measurement				
IREF LV LoZ Bias	04	10	Data	Not settable
This records the IREF LV LoZ Bias measurement				
IREF TV LoZ Diff	04	11	Data.	Not settable
P643 and P645 only. This records the IREF TV LoZ Diff measurement				
IREF TV LoZ Bias	04	12	Data	Not settable
P643 and P645 only. This records the IREF TV LoZ Bias measurement				
IREF Auto LoZ Diff	04	13	Data	Not settable
This records the IREF Auto LoZ Diff measurement				
IREF Auto LoZ Bias	04	14	Data	Not settable
This records the IREF Auto LoZ Bias measurement				
IREF HV HighZ Op	04	15	Data	Not settable
This records the HV High measurement				
IREF LV HighZ Op	04	16	Data	Not settable
This records the LV HighZ measurement				
IREF TV HighZ Op	04	17	Data	Not settable
P643 and P645 only. This records the IREF TV HighZ Operation measurement				
IREF Auto HighZ Op	04	18	Data	Not settable
This records the IREF Auto measurement				
Thermal Overload	04	27	Sub-Heading	Sub-Heading
Sub-Heading				
Hot Spot T	04	28	Data	Not settable

Menu Text	Col	Row	Default Setting	Available Setting
Description				
This records the Hot Spot T measurement				
Top Oil T	04	2A	Data	Not settable
This records the Top Oil T measurement				
Reset Thermal	04	2B	No	No or Yes
Reset Thermal Overload command. Resets thermal state to 0.				
Ambient T	04	2C	Data	Not settable
This records the Ambient T measurement				
TOL Pretrip left	04	2D	Data	Not settable
Thermal OverLoad pre-trip time left. This records the TOL Pretrip left measurement				
LOL status	04	2F	Data	Not settable
Accumulated Loss Of Life. Invisible only when the turbine abnormal frequency protection is not enabled.				
Reset LOL	04	30	No	No or Yes
Reset Loss Of Life (LOL) command. Resets state to 0.				
Rate of LOL	04	31	Data	Not settable
This records the Rate of LOL (ROLOL) measurement				
LOL Aging Factor	04	32	Data	Not settable
Aging Acceleration Factor (FAA). This records the LOL Aging Factor measurement				
Lres at designed	04	33	Data	Not settable
Residual life hours at design temperature QH,r. This records the Lres at designed measurement				
FAA,m	04	34	Data	Not settable
Mean Aging Acceleration Factor (FAA,m). This records the FAA,m measurement				
Lres at FAA,m	04	35	Data	Not settable
Residual life hours at FAA,m (LRES(FAA,m)). This records the Lres at FAA,m measurement				
Volts/Hz	04	38	Sub-Heading	Sub-Heading
Sub-Heading				
Volts/Hz W1	04	39	Data	Not settable
P643 and P645 only. This records the Volts/Hz W1 measurement				
V/Hz W1 tPretrip	04	3A	Data	Not settable
P643 and P645 only. This records the V/Hz W1 tPretrip measurement				
V/Hz W1 Thermal	04	3B	Data	Not settable
P643 and P645 only. This records the V/Hz W1 Thermal measurement				
Reset V/Hz W1	04	3C	No	No or Yes
P643 and P645 only. Reset V/Hz W1				
Volts/Hz W2	04	3D	Data	Not settable
This records the Volts/Hz W2 measurement				
V/Hz W2 tPretrip	04	3E	Data	Not settable
This records the V/Hz W2 tPretrip measurement				
V/Hz W2 Thermal	04	3F	Data	Not settable
This records the V/Hz W2 Thermal measurement				
Reset V/Hz W2	04	40	No	No or Yes

Menu Text	Col	Row	Default Setting	Available Setting
Description				
Reset V/Hz W2				
RTD 1 label	04	60	Data	Not settable
This records the RTD 1 label measurement				
RTD 2 label	04	61	Data	Not settable
This records the RTD 2 label measurement				
RTD 3 label	04	62	Data	Not settable
This records the RTD 3 label measurement				
RTD 4 label	04	63	Data	Not settable
This records the RTD 4 label measurement				
RTD 5 label	04	64	Data	Not settable
This records the RTD 5 label measurement				
RTD 6 label	04	65	Data	Not settable
This records the RTD 6 label measurement				
RTD 7 label	04	66	Data	Not settable
This records the RTD 7 label measurement				
RTD 8 label	04	67	Data	Not settable
This records the RTD 8 label measurement				
RTD 9 label	04	68	Data	Not settable
This records the RTD 9 label measurement				
RTD 10 label	04	69	Data	Not settable
This records the RTD 10 label measurement				
RTD Open Cct	04	6A	0000000000	Not settable
Displays the status of the eight RTDs as a binary string. 0 = No Open Circuit, 1 = Open Circuit. The Open Cct alarms are latched.				
RTD Short Cct	04	6B	0000000000	Not settable
Displays the status of the eight RTDs as a binary string. 0 = No Short Circuit, 1 = Short Circuit. The Short Cct alarms are latched.				
RTD Data Error	04	6C	0000000000	Not settable
Displays the status of the eight RTDs as a binary string. 0 = No Data Error, 1 = Data Error. The Data Error alarms are latched.				
Reset RTD Flags	04	6D	No	No or Yes
Reset RTD alarms command. Resets latched RTD Open Cct, Short Cct, Data Error alarms.				
CLIO Input 1	04	70	Data	Not settable
This records the CLIO Input 1 measurement				
CLIO Input 2	04	71	Data	Not settable
This records the CLIO Input 2 measurement				
CLIO Input 3	04	72	Data	Not settable
This records the CLIO Input 3 measurement				
CLIO Input 4	04	73	Data	Not settable
This records the CLIO Input 4 measurement				

Table 9 - Measurements 3

PRODUCT DESIGN

CHAPTER 10

Date:	07/2018
Products covered by this chapter:	This chapter covers the specific versions of the MiCOM products listed below. This includes ***only*** the following combinations of Software Version and Hardware Suffix.
Hardware Suffix:	L (P642) M (P643/P645)
Software Version:	B4 - P64x (P642, P643 & P645)
Connection Diagrams:	10P642xx (xx = 01 to 10) 10P643xx (xx = 01 to 06) 10P645xx (xx = 01 to 09)

CONTENTS

Page (PD) 10-

FIGURES

TABLES

1 RELAY SYSTEM OVERVIEW

1.1 Hardware Overview

The relay is based on a modular hardware design where each module performs a separate function. This section describes the functional operation of the various hardware modules. Some modules are essential while others are optional depending on the user's requirements (see *Product Specific Options* and *Hardware Communications Options*).

All modules are connected by a parallel data and address bus which allows the processor board to send and receive information to and from the other modules as required.

There is also a separate serial data bus for transferring sample data from the input module to the processor. See the *Relay modules* diagram.

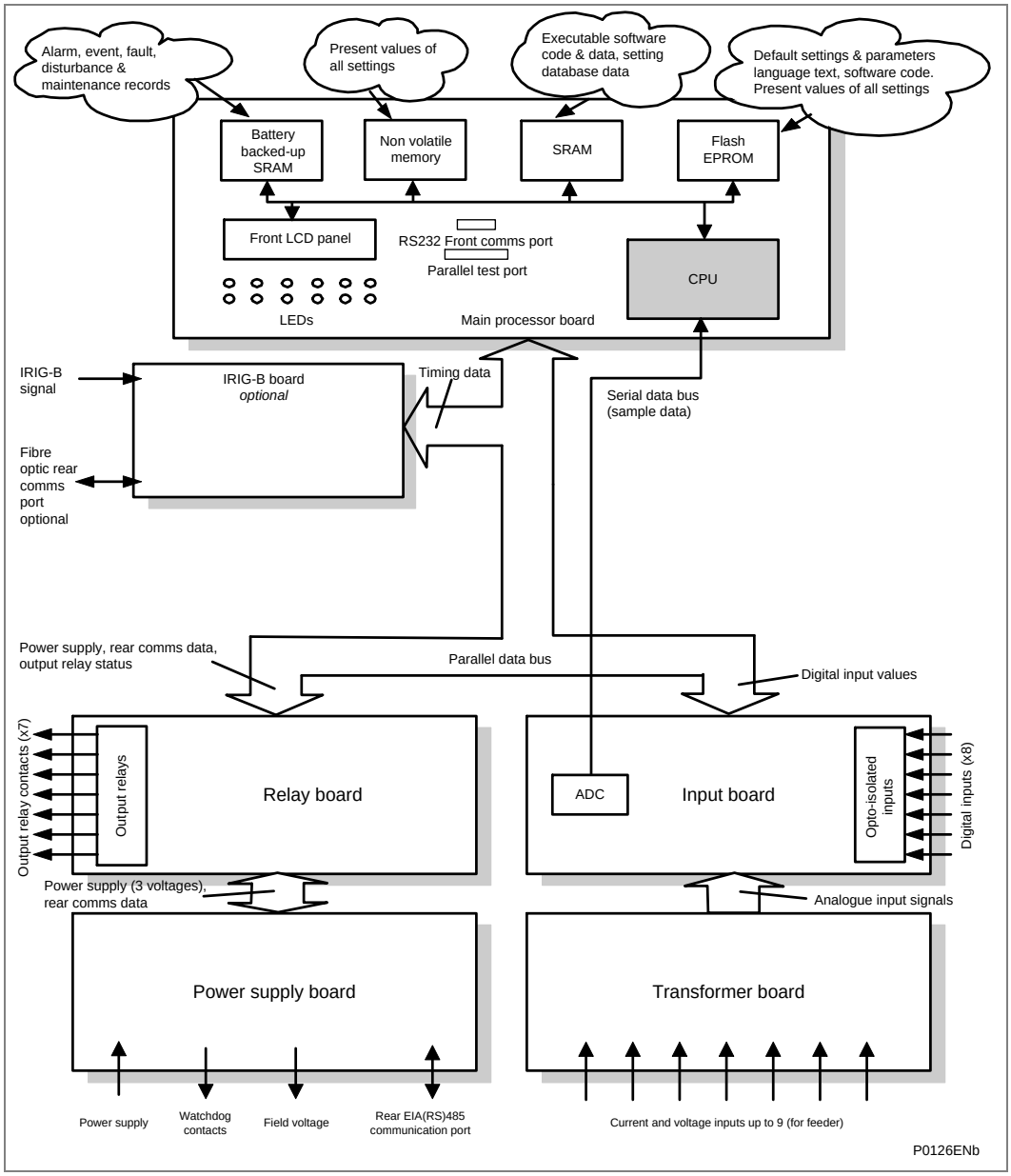


Figure 1 - Relay modules

1.2 Mechanical Layout

The relay case is pre-finished steel with a conductive covering of aluminum and zinc. This provides good earthing at all joints with a low impedance path to earth that is essential for shielding from external noise. The boards and modules use multi-point grounding (earthing) to improve immunity to external noise and minimize the effect of circuit noise. Ground planes are used on boards to reduce impedance paths and spring clips are used to ground the module metalwork.

Heavy duty terminal blocks are used at the rear of the relay for the current and voltage signal connections. Medium duty terminal blocks are used for the digital logic input signals, output relay contacts, power supply and rear communication port. A BNC connector is used for the optional IRIG-B signal. 9-pin and 25-pin female D-connectors are used at the front of the relay for data communication.

Inside the relay the boards plug into the connector blocks at the rear, and can be removed from the front of the relay only. The connector blocks to the relay's CT inputs have internal shorting links inside the relay. These automatically short the current transformer circuits before they are broken when the board is removed.

The front panel consists of a membrane keypad with tactile dome keys, an LCD and 12 or 22 LEDs (depending on the model) mounted on an aluminum backing plate.

1.3 Processor Board

The processor board performs all calculations for the relay and controls the operation of all other modules in the relay. The processor board also contains and controls the user interfaces (LCD, LEDs, keypad and communication interfaces).

The relay is based around a TMS320VC33-150MHz (peak speed), floating-point, 32-bit Digital Signal Processor (DSP) operating at a clock frequency of half this speed. This processor performs all of the calculations for the relay, including the protection functions, control of the data communication and user interfaces including the operation of the LCD, keypad and LEDs.

There are two models of processor board, one with function keys for the P643 and P645, and one without function keys for the P642. The processor board is directly behind the relay's front panel. This allows the LCD and LEDs and front panel communication ports to be mounted on the processor board. These ports are:

- The 9-pin D-connector for EIA(RS)232 serial communications used for MiCOM S1 Studio and Courier communications.
- The 25-pin D-connector relay test port for parallel communication.

All serial communication is handled using a Field Programmable Gate Array (FPGA).

The main processor board has:

- 2 MB SRAM for the working area. This is fast access (zero wait state) volatile memory used to temporarily store and execute the processor software.
- 4 MB flash ROM to store the software code, text, configuration data, default settings, and present settings.
- 4 MB battery-backed SRAM to store disturbance, event, fault and maintenance records.

Note	*With hardware revisions L and M, the SRAM size has changed from 2MB to 8MB; and the Flash size has changed from 4MB to 8MB.*

1.4 Internal Communication Buses

The relay has two internal buses for the communication of data between different modules. The main bus is a parallel link that is part of a 64-way ribbon cable. The ribbon cable carries the data and address bus signals in addition to control signals and all power supply lines. Operation of the bus is driven by the main processor board that operates as a master while all other modules in the relay are slaves.

The second bus is a serial link that is used exclusively for communicating the digital sample values from the input module to the main processor board. The DSP has a built-in serial port that is used to read the sample data from the serial bus. The serial bus is also carried on the 64-way ribbon cable.

1.5 Input Module

The input module provides the interface between the relay processor board(s) and the analog and digital signals coming into the relay. The input module consists of the main input board and the transformer board.

1.5.1 Transformer Board

The transformer board holds up to two Voltage Transformers (VTs) and up to nine Current Transformers (CTs). The auxiliary transformer board used on some model options and can add up to two more VTs and up to nine more CTs.

Model	Option	Alternative Option
P642	1 VT, 8 CTs	2 VTs, 8CTs
P643	2 VTs, 3 CTs	2 VTs, 9 CTs
P645	2 VTs, 9 CTs	

The current inputs will accept either 1A or 5A nominal current (observe menu and wiring options) and the voltage inputs can be specified for either 110V or 440V nominal voltage (order option). The transformers are used both to step-down the currents and voltages to levels appropriate to the relay's electronic circuitry and to provide effective isolation between the relay and the power system. The connection arrangements of both the current and voltage transformer secondary's provide differential input signals to the main input board to reduce noise.

1.5.2 Input Board

The main input board is shown as a block diagram in the *Main input board* diagram. It provides the circuitry for the digital input signals and the Analog-to-Digital (A-D) conversion for the analog signals. It takes the differential analog signals from the CTs and VTs on the transformer board(s), converts these to digital samples and transmits the samples to the main processor board through the serial data bus. On the input board, the analog signals are converted using a dedicated sigma-delta A-D convertor for each channel. This allows all of the channels to be sampled concurrently with no sampling skew between channels. The sampled signals are then digitally filtered prior to the data being sent to the main processor via the serial link. In relay models using the second transformer board, a second input board is also fitted to provide the A-D conversion for the additional channels

The sample rate is kept at 24 samples per cycle of the power waveform by a logic control circuit driven by the frequency tracking function on the main processor board. The calibration non-volatile memory holds the calibration coefficients that are used by the processor board to correct for any amplitude or phase error introduced by the transformers and analog circuitry.

The digital input signals are opto isolated on the main input board to prevent excessive voltages on these inputs causing damage to the relay's internal circuitry. The design of the opto input circuit allows the operating voltage to be configured for each input using the relay menu from a choice of five nominal battery voltages. Depending on the relay model, more than eight digital input signals can be accepted by the relay. This is achieve by additional opto-board containing the same provision for eight isolated digital inputs as the main input board, but with no provision for the analogue inputs.

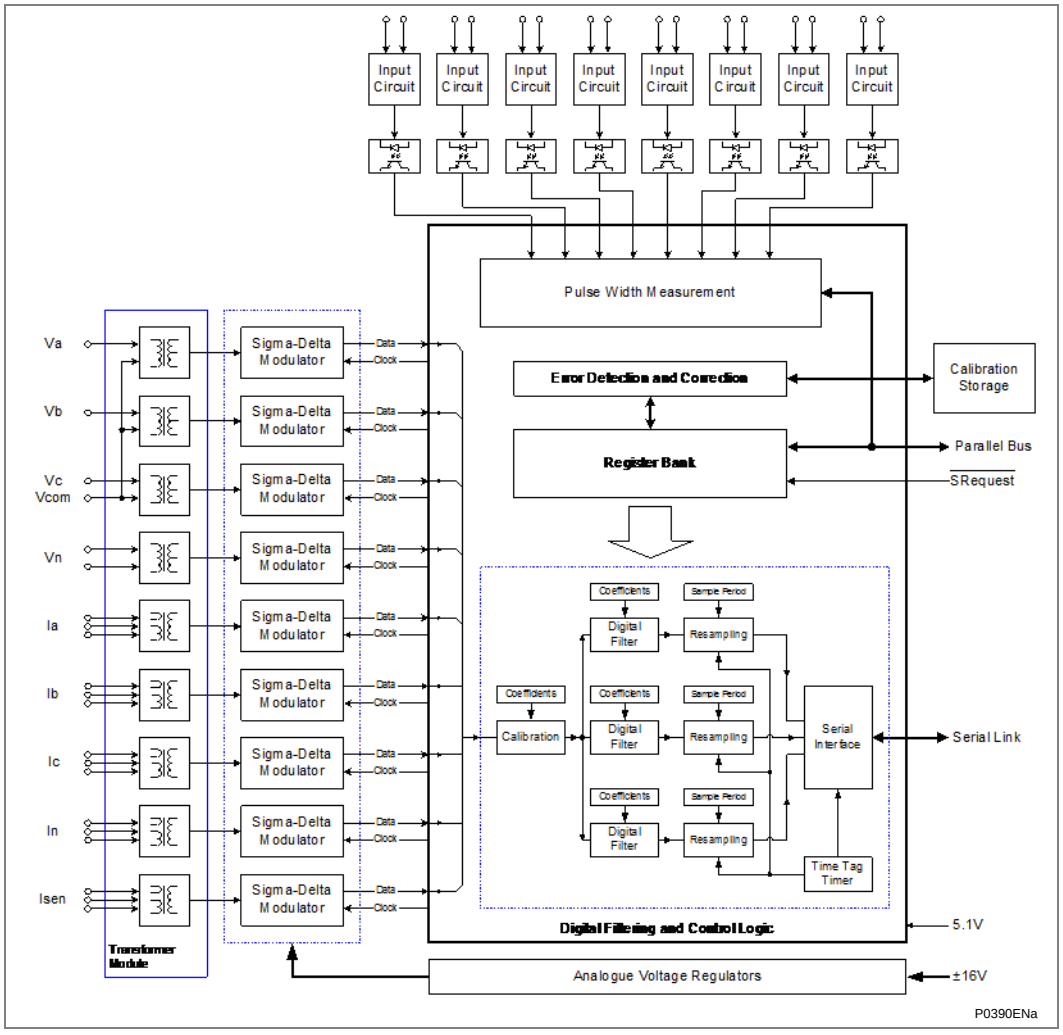


Figure 2 - Main input board

The other function of the input board is to read the signals on the digital inputs and send them through the parallel data bus to the processor board. The input board holds eight optical isolators for connecting up to eight digital input signals. Opto-isolators are used with digital signals for the same reason as transformers are used with analog signals: to isolate the relay's electronics from the power system environment. A 48 V 'field voltage' supply at the back of the relay is used to drive the digital opto-inputs. The input board has hardware filters to remove noise from the digital signals. The digital signals are then buffered so they can be read on the parallel data bus. Depending on the relay model, more than eight digital input signals can be accepted by the relay. This is done using an additional opto-board that contains the same provision for eight isolated digital inputs as the main input board, but does not contain any of the circuits for analog signals which are provided on the main input board.

1.5.3 Universal Opto Isolated Logic Inputs

This series of relays have universal opto-isolated logic inputs that can be programmed for the nominal battery voltage of the circuit of which they are a part. This allows different voltages for different circuits such as signaling and tripping. They can also be programmed as Standard 60% - 80% or 50% - 70% to satisfy different operating constraints.
Threshold levels are shown in this table:

Nominal battery voltage (Vdc)	Standard 60% - 80%		50% - 70%	
	No operation (Logic 0) Vdc	Operation (Logic 1) Vdc	No operation (Logic 0) Vdc	Operation (Logic 1) Vdc
24/27	<16.2	>19.2	<12.0	>16.8
30/34	<20.4	>24.0	<15.0	>21.0
48/54	<32.4	>38.4	<24.0	>33.6
110/125	<75.0	>88.0	<55.0	>77.0
220/250	<150.0	>176.0	<110	>154

Table 1 - Threshold Levels

This lower value eliminates fleeting pick-ups that may occur during a battery earth fault, when stray capacitance may present up to 50% of battery voltage across an input.

Each input also has selectable filtering. This allows a pre-set ½ cycle filter to be used to prevent induced noise on the wiring. However, although the ½ cycle filter is secure it can be slow, particularly for intertripping. If the ½ cycle filter is switched off to improve speed, double pole switching or screened twisted cable may be needed on the input to reduce ac noise.

1.6 Power Supply Module (including Output Relays)

The power supply module contains two boards, one for the power supply unit and the other for the output relays. It provides power to all of the other modules in the relay, as well as the EIA(RS)485 electrical connection for the rear communication port. The second board of the power supply module contains the relays that provide the output contacts.

1.6.1 Power Supply Board (including EIA(RS)485 Communication Interface)

One of three different configurations of the power supply board can be fitted to the relay. This will be specified at the time of order and depends on the nature of the supply voltage that will be connected to the relay. The options are shown in the following table:

Nominal dc range	Nominal ac range
24 - 32 V dc	dc only
48 - 110 V dc	dc only
110 - 250 V dc	100 - 240 V ac rms

Table 2 - Power supply options

The output from all versions of the power supply module are used to provide isolated power supply rails to all of the other modules in the relay. Three voltage levels are used in the relay: 5.1 V for all of the digital circuits, ±16 V for the analog electronics such as on the input board, and 22 V for driving the output relay coils and the RTD board if fitted. All power supply voltages including the 0 V earth line are distributed around the relay through the 64-way ribbon cable. The power supply board also provides the 48 V field voltage. This is brought out to terminals on the back of the relay so that it can be used to drive the optically-isolated digital inputs.

The two other functions provided by the power supply board are the EIA(RS)485 communications interface and the watchdog contacts for the relay. The EIA(RS)485 interface is used with the relay's rear communication port to provide communication using one of either Courier, MODBUS, IEC60870-5-103, or DNP3.0 protocols. The EIA(RS)485 hardware supports half-duplex communication and provides optical isolation of the serial data that is transmitted and received. All internal communication of data from the power supply board is through the output relay board connected to the parallel bus.

The watchdog facility has two output relay contacts, one Normally Open (N/O)and one Normally Closed (N/C). These are driven by the main processor board and indicate that the relay is in a healthy state.

The power supply board incorporates inrush current limiting. This limits the peak inrush current, during energization, to approximately 10 A.

1.6.2 Output Relay Board

The output relay board has eight relays, six normally open contacts and two changeover contacts.

The relays are driven from the 22 V power supply line. The relays' state is written to or read from using the parallel data bus.

Depending on the relay model, up to three output relay boards may be fitted to the P145 relay to provide a total number of 32 relay outputs.

1.6.3 High Break Relay Board

The 'high break' output relay board has four normally open output contacts. It is optional in the P642, P643 and P645. The P642 can have a maximum of one board and the P643 and P645 can have up to two boards.

This board uses a hybrid of MOSFET Solid State Devices (SSD) in parallel with high capacity relay output contacts. The MOSFET has a varistor across it to provide protection which is required when switching off inductive loads because the stored energy in the inductor causes a reverse high voltage which could damage the MOSFET.

When there is a control input command to operate an output contact, the miniature relay is operated at the same time as the SSD. The miniature relay contact closes in nominally 3.5 ms and is used to carry the continuous load current; the SSD operates in <0.2 ms and is switched off after 7.5 ms. When the control input resets to open the contacts, the SSD is again turned on for 7.5 ms. The miniature relay resets in nominally 3.5 ms before the SSD so the SSD is used to break the load. The SSD absorbs the energy when breaking inductive loads and so limits the resulting voltage surge. This contact arrangement is for switching dc circuits only. As the SSD comes on very fast (<0.2 ms) these high break output contacts have the added advantage of being very fast operating. See the *High break contact operation* diagram below:

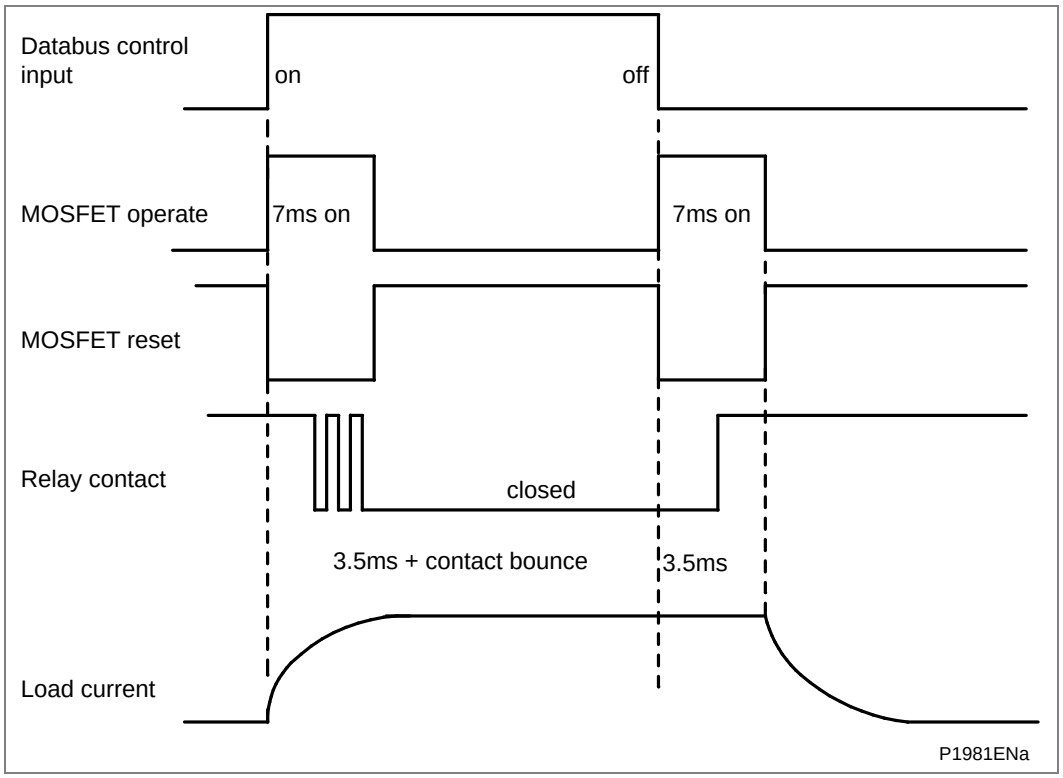


Figure 3 - High break contact operation

1.6.3.1 High Break Contact Applications

1. Efficient Scheme Engineering

   In traditional hardwired scheme designs, high break capability could only be achieved using external electromechanical trip relays. External tripping relays can be used or the high break contacts inside MiCOM relays can be used, reducing panel space.

2. Accessibility of CB Auxiliary Contacts

   Common practice is to use circuit breaker 52a (CB Closed) auxiliary contacts to break the trip coil current on breaker opening, easing the duty on the protection contacts. In cases such as operation of disconnectors, or retrofitting, 52a contacts may be unavailable or unreliable. High break contacts can be used to break the trip coil current in these applications.

3. Breaker Fail

   The technique to use 52a contacts in trip circuits was described above. However, in the event of failure of the local circuit breaker (stuck breaker), or defective auxiliary contacts (stuck contacts), the 52a contact action is incorrect. The interrupting duty at the local breaker then falls on the relay output contacts which may not be rated to perform this duty. MiCOM high break contacts will avoid the risk of burnt relay contacts.

4. Initiation of Teleprotection

   The MiCOM high break contacts also offer fast making, which can provide faster tripping. Also fast keying of teleprotection is a benefit. Fast keying bypasses the usual contact operation time so that permissive, blocking and intertrip commands can be routed faster.

1.6.4 Input/Output (4 + 4) Relay Board

The input/output relay board has four isolated digital inputs and four output relays. Two of the relays have normally open contacts and two have changeover contacts. The output relays are driven from the 22 V power supply line. The relays' state is written to or read from using the parallel data bus.

This board is an option on the P642, giving 12 opto inputs and 12 output relay contacts.

1.7 Product Specific Options

Product Specific Options may mean that an additional board may be present if it was specified when the relay was ordered. The product specific options commonly allow a choice of RTD, CLIO, different numbers of Optos, Relays (including High Break relays). These options are shown in the *Ordering Options* section in *Chapter 1 – Introduction*.

The options are described in more details in the following sections

- Resistance Temperature Detectors (RTD) Board Option
- Current Loop Input Output (CLIO) Board Option

1.8 Resistance Temperature Detectors (RTD) Board Option

The optional Resistance Temperature Detectors (RTD) board is used to monitor the winding and ambient temperature readings from up to ten PT100 RTD that are each connected using a 3-wire connection. The board is powered from the 22 V power rail that is used to drive the output relays. The RTD board includes two redundant channels that are connected to high stability resistors to provide reference readings. These are used to check the operation of the RTD board. The temperature data is read by the processor through the parallel data bus, and is used to provide thermal protection of the windings.

1.9 Current Loop Input Output (CLIO) Board Option

The Current Loop Input Output (CLIO) board is an order option. The CLIO board is powered from the 22 V power rail that is used to drive the output relays.

Four analog (or current loop) inputs are provided for transducers with ranges of 0 to 1 mA, 0 to 10 mA, 0 to 20 mA or 4 to 20 mA. The input current data is read by the processor through the parallel data bus, and is used to provide measurements from various transducers such as vibration monitors, tachometers and pressure transducers.

For each of the four current loop inputs there are two separate input circuits, 0 to 1 mA and 0 to 20 mA. The latter is also used for 0 to 10 mA and 4 to 20 mA transducer inputs. The anti-alias filters have a nominal cut-off frequency (3 dB point) of 23 Hz to reduce power system interference from the incoming signals. Four analog current outputs are provided with ranges of 0 to 1 mA, 0 to 10 mA, 0 to 20 mA or 4 to 20 mA which can alleviate the need for separate transducers. These may be used to feed standard moving coil ammeters for analog indication of certain measured quantities or into a SCADA using an existing analog RTU.

Each of the four current loop outputs provides one 0 to 1 mA output, one 0 to 20 mA output and one common return. Suitable software scaling of the value written to the board allows the 0 to 20 mA output to also provide 0 to 10 mA and 4 to 20 mA. Screened leads are recommended for use on the current loop output circuits.

The refresh interval for the outputs is nominally 50 ms. Any measurements that do not fit this timing are updated once every second.

All external connections to the current loop I/O board are made using the same 15-way light duty I/O connector SL3.5/15/90F used on the RTD board. Two such connectors are used, one for the current loop outputs and one for the current loop inputs.

The I/O connectors accommodate wire sizes in the range 1/0.85 mm (0.57 mm^2) to 1/1.38 mm (1.5 mm^2) and their multiple conductor equivalents. The use of screened cable is recommended. The screen terminations should be connected to the case earth of the relay.

Basic Insulation (300 V) is provided between analog inputs or outputs and earth, and between analog inputs and outputs. However, there is no insulation between one input and another or one output and another.

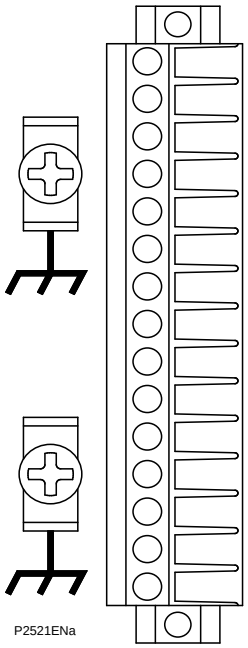
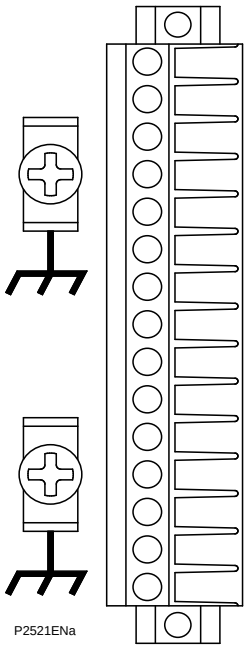
Connection	IO blocks	Connection
Outputs		
		0 - 10/0 - 20/4 – 20 mA channel 1
Screen channel 1		0 – 1 mA channel 1
		Common return channel 1
		0 - 10/0 - 20/4 – 20 mA channel 2
Screen channel 2		0 – 1 mA channel 2
		Common return channel 2
		0 - 10/0 - 20/4 – 20 mA channel 3
Screen channel 3		0 – 1 mA channel 3
		Common return channel 3
		0 - 10/0 - 20/4 – 20 mA channel 4
Screen channel 4		0 – 1 mA channel 4
		Common return channel 4
	P2521ENa	
Inputs		
		0 - 10/0 - 20/4 – 20 mA channel 1
Screen channel 1		0 – 1 mA channel 1
		Common channel 1
		0 - 10/0 - 20/4 – 20 mA channel 2
Screen channel 2		0 – 1 mA channel 2
		Common channel 2
		0 - 10/0 - 20/4 – 20 mA channel 3
Screen channel 3		0 – 1 mA channel 3
		Common channel 3
		0 - 10/0 - 20/4 – 20 mA channel 4
Screen channel 4		0 – 1 mA channel 4
		Common channel 4
	P2521ENa	

Table 3 - Current Loop Input Output (CLIO) board

1.10 Hardware Communications Options

The Hardware Communications Options could mean that a second additional board is present if it was specified when the relay was ordered. Any such board is fitted into Slot A, as this is the optional communications slot.

The hardware options board commonly allows a choice of IRIG-B, Ethernet and Second Rear Comms Ports. Some of these choices are mutually exclusive whereas others provide more than one option on the same board. An up-to-date list of the available combinations for the Hardware/Software combination of this product is shown in the *Ordering Options* section in *Chapter 1 – Introduction*.

The main options are described in more detail in the these sections:

- IRIG-B Modulated and/or Un-modulated Board (Optional)
- Second Rear Communications Board (Optional)
- Ethernet Board (Options)

1.11 IRIG-B Modulated or Un-modulated Board (Optional)

The optional IRIG-B board is an order option that can be fitted to provide an accurate timing reference for the relay. This can be used wherever an IRIG-B signal is available. The IRIG-B signal is connected to the board with a BNC connector on the back of the relay. The timing information is used to synchronize the relay's internal real-time clock to an accuracy of 1 ms. The internal clock is then used for the time tagging of the event, fault maintenance and disturbance records. The IRIG-B board can also be specified with a fiber optic or Ethernet rear communication port.

1.12 Second Rear Comms. Board (Optional)

For relays with Courier, MODBUS, IEC60870-5-103 or DNP3.0 protocol on the first rear communications port there is the hardware option of a second rear communications port, which runs the Courier language. This can be used over one of three physical links: twisted pair K-BUS (non-polarity sensitive), twisted pair EIA(RS)485 (connection polarity sensitive) or EIA(RS)232.

This optional second rear port is designed typically for dial-up modem access by protection engineers and operators, when the main port is reserved for SCADA traffic.

The port supports full local or remote protection and control access by MiCOM S1 Studio software. The second rear port is also available with an on board IRIG-B input.

The second rear communications board, Ethernet and IRIG-B boards are mutually exclusive since they use the same hardware slot. For this reason two versions of second rear communications and Ethernet boards are available; one with an IRIG-B input and one without. The second rear communications board is shown in the following diagram.

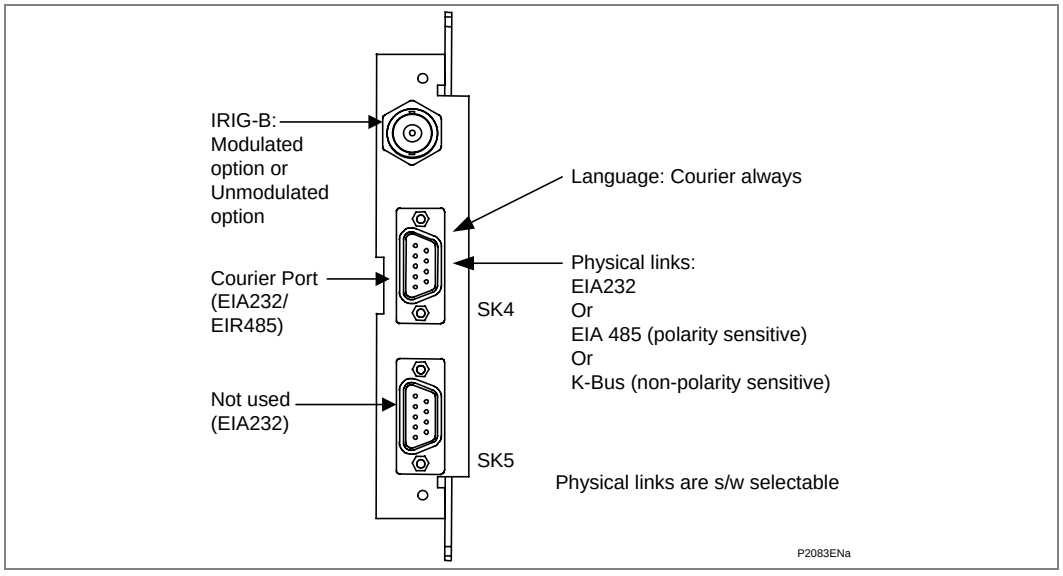


Figure 4 - Second rear comms. Port

1.13 Ethernet Board (Options)

This optional board is required for providing network connectivity using IEC 61850. There are a variety of different boards which provide Ethernet connectivity.

Important	**The choice of communication board options varies according to the Hardware Suffix and the Software Version of the MiCOM product. These are shown in the *Ordering Options* section in *Chapter 1 – Introduction*.**

By way of example, the board options may include:

- single-port Ethernet boards (which use 100 Mbits/s Copper and modulated/unmodulated IRIG-B connectivity)
- Redundant Ethernet with PRP/HSR/Dual IP and a mixture of LC/RJ45 ports and modulated/unmodulated IRIG-B connectivity

These options are mutually exclusive.

Note	*Each Ethernet board has a unique MAC address used for each Ethernet communication interface. The MAC address is printed on the rear of the board, next to the Ethernet sockets.*

Note	*The 100 Mbits/s Fiber Optic ports use LC type connectors and are suitable for 1310 nm multi-mode fiber type.*

Copper ports use RJ45 type connectors. When using copper Ethernet, it is important to use Shielded Twisted Pair (STP) or Foil Twisted Pair (FTP) cables, to shield the IEC 61850 communications against electromagnetic interference. The RJ45 connector at each end of the cable must be shielded, and the cable shield must be connected to this RJ45 connector shield, so that the shield is grounded to the relay case. Both the cable and the RJ45 connector at each end of the cable must be Category 5 minimum, as specified by the IEC 61850 standard.

It is recommended that each copper Ethernet cable is limited to a maximum length of 3 m and confined to one bay or cubicle.

When using IEC61850 communications through the Ethernet board, the rear EIA(RS)485 and front EIA(RS)232 ports are available for simultaneous use. The front port always uses the Courier protocol. The rear port protocol depends upon the protocol option selected.

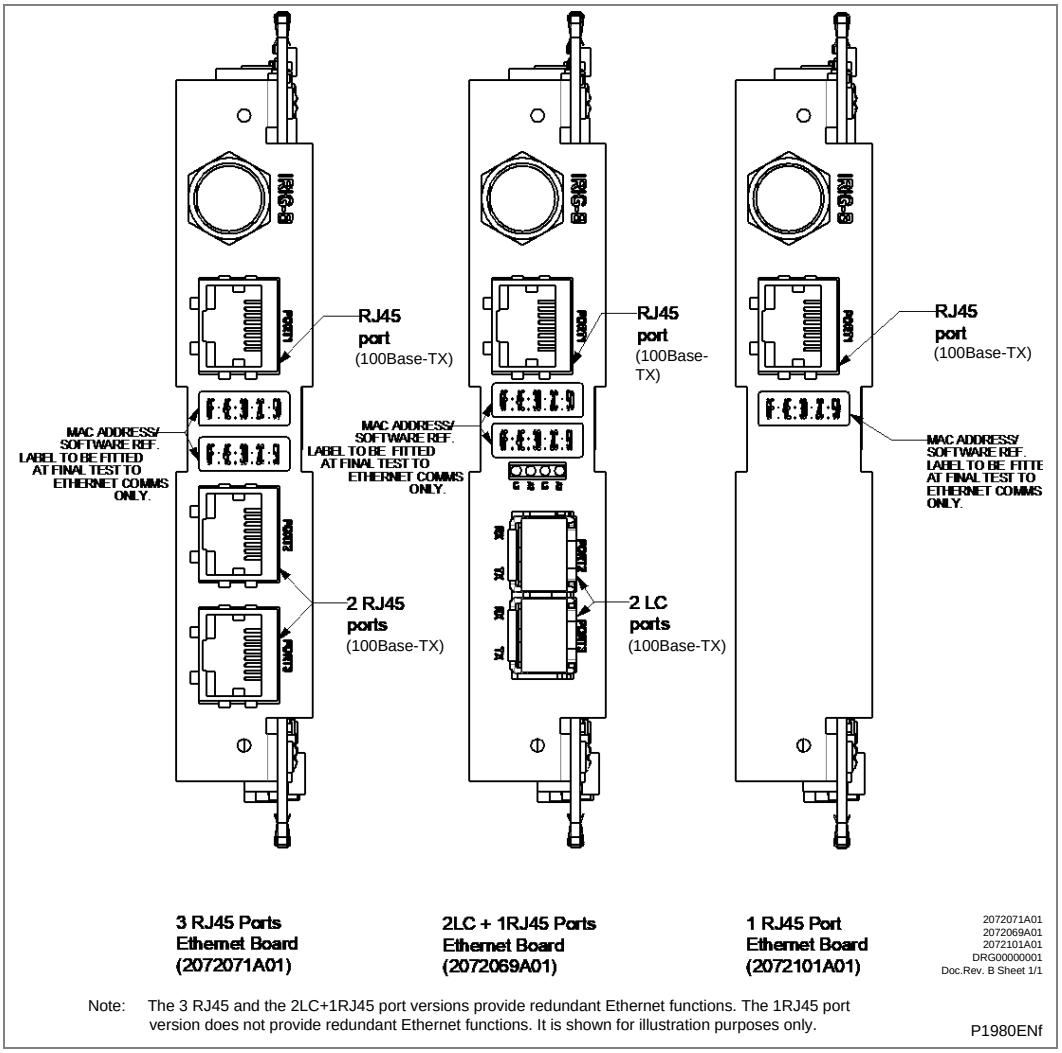


Figure 5 - Ethernet board connectors (3 RJ45 or 2 LC + RJ45 or 1 RJ45)

2 RELAY SOFTWARE

The relay software was introduced in the overview of the relay at the start of this chapter. The software can be considered to be made up of these sections:

- The real-time operating system
- The system services software
- The platform software
- The protection and control software

These four elements are all processed by the same processor board.This section describes in detail the ***platform software*** and the ***protection and control software***, which between them control the functional behavior of the relay. The following *Relay software structure* diagram shows the structure of the relay software.

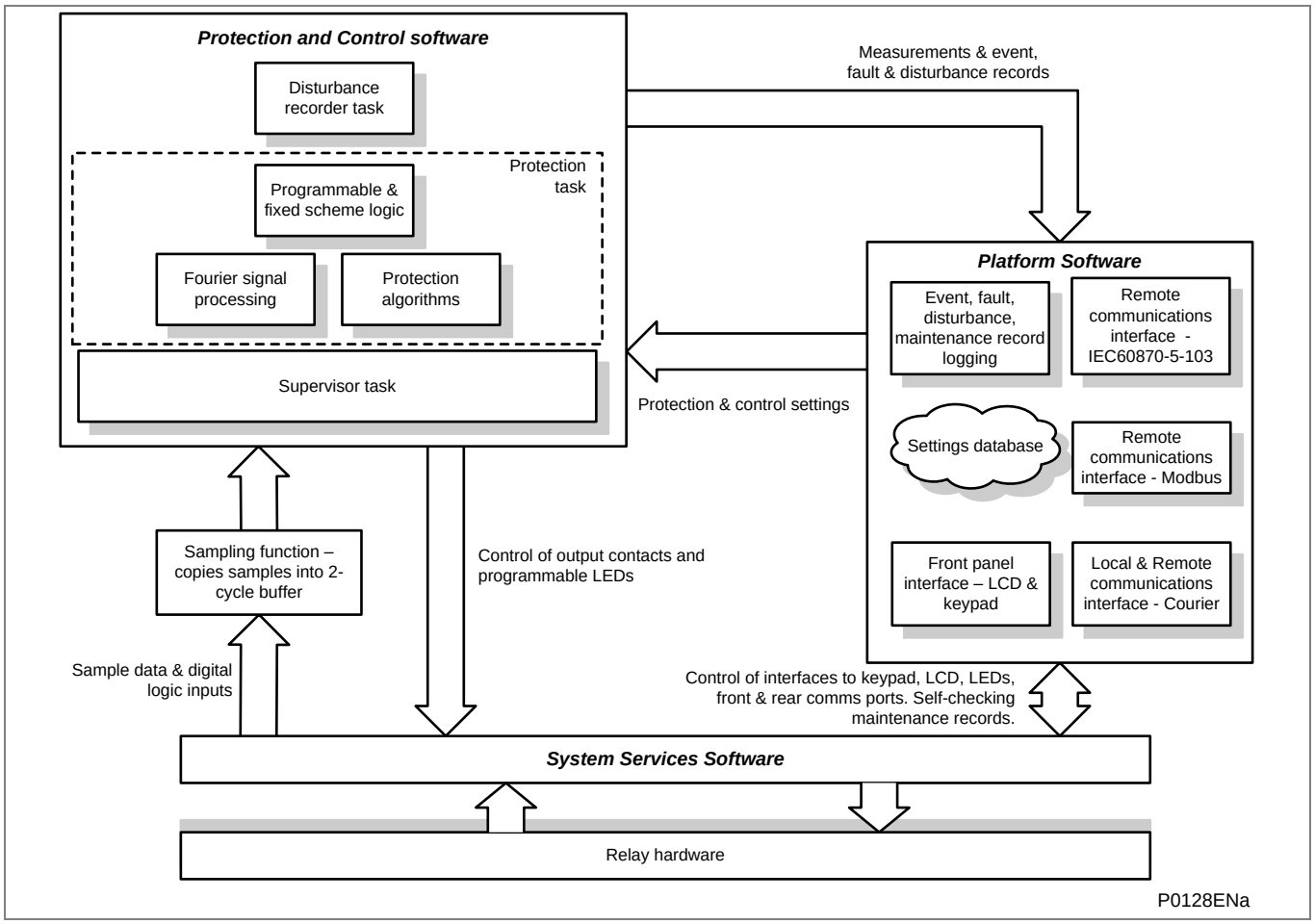


Figure 6 - Relay software structure

2.1 Real-Time Operating System

The real-time operating system provides a framework for the different parts of the relay's software to operate in.

The software is split into tasks; the real-time operating system is used to schedule the processing of the tasks to ensure that they are processed in the time available and in the desired order of priority. The operating system is also responsible in part for controlling the communication between the software tasks through the use of operating system messages.

2.2 System Services Software

As shown in the above *Relay software structure* diagram, the system services software provides the low-level control of the relay hardware. It also provides the interface between the relay's hardware and the higher-level functionality of the platform software and the protection and control software.

For example, the system services software provides drivers for items such as the LCD display, the keypad and the remote communication ports. It also controls the boot of the processor and downloading of the processor code into SRAM from non-volatile flash EPROM at power up.

2.3 Platform Software

The platform software has these main functions:

- To deal with the management of the relay settings.
- To control the logging of all records that are generated by the protection software, including alarms and event, fault, disturbance and maintenance records.
- To store and maintain a database of all of the relay's settings in non-volatile memory.
- To provide the internal interface between the settings database and each of the relay's user interfaces. These interfaces are the front panel interface and the front and rear communication ports, using whichever communication protocol has been specified (Courier, MODBUS, IEC60870-5-103 and DNP3.0). The platform software converts the information from the database into the format required.

The platform software notifies the protection and control software of all settings changes and logs data as specified by the protection and control software.

2.3.1 Record Logging

The logging function is provided to store all alarms, events, faults and maintenance records. The records for all of these incidents are logged in battery backed-up SRAM in order to provide a non-volatile log of what has happened. The relay maintains four logs: one each for up to 32 alarms, 512 event records, 5 fault records and 5 maintenance records. The logs are maintained such that the oldest record is overwritten with the newest record.

The logging function can be initiated from the protection software or the platform software, and is responsible for logging of a maintenance record in the event of a relay failure. This includes errors that have been detected by the platform software itself or error that are detected by either the system services or the protection software functions. See also the section on *Self-Testing and Diagnostics* later in this section.

2.3.2 Settings Database

The settings database contains all of the settings and data for the relay, including the protection, disturbance recorder and control and support settings. The settings are maintained in non-volatile memory. The platform software's management of the settings database make sure that only one user interface modifies the database settings at any one time. This feature is used to avoid confusion between different parts of the software during a setting change. For changes to protection settings and disturbance recorder settings, the platform software operates a 'scratchpad' in SRAM memory. This allows a number of setting changes to be made in any order but applied to the protection elements, disturbance recorder and saved in the database in non-volatile memory, at the same time. If a setting change affects the protection and control task, the database advises it of the new values.

The database is directly compatible with Courier communications.

2.3.3 Database Interface

The other function of the platform software is to implement the relay's internal interface between the database and each of the relay's user interfaces. The database of settings and measurements must be accessible from all of the relay's user interfaces to allow read and modify operations. The platform software presents the data in the appropriate format for each user interface.

2.4 Protection and Control Software

The protection and control software interfaces with the platform software for settings changes and logging of records, and with the system services software for acquisition of sample data and access to output relays and digital opto-isolated inputs. It also performs the calculations for all of the protection algorithms of the relay. This includes digital signal processing such as Fourier filtering and ancillary tasks such as the disturbance recorder.

The protection and control software task processes all of the protection elements and measurement functions of the relay. It has to communicate with both the system services software and the platform software, and organize its own operations. The protection software has the highest priority of any of the software tasks in the relay, to provide the fastest possible protection response. It also has a supervisor task that controls the start-up of the task and deals with the exchange of messages between the task and the platform software.

2.4.1 Overview - Protection and Control Scheduling

After initialization at start-up, the protection and control task is suspended until there are sufficient samples available for it to process. The acquisition of samples is controlled by a '**sampling function**' which is called by the system services software and takes each set of new samples from the input module and stores them in a two-cycle buffer. The protection and control software resumes execution when the number of unprocessed samples in the buffer reaches a certain number. For the P14x feeder protection relay, the protection task is executed twice per cycle, i.e. after every 12 samples for the sample rate of 24 samples per power cycle used by the relay. The protection and control software is suspended again when all of its processing on a set of samples is complete. This allows operations by other software tasks to take place.

2.4.2 Signal Processing

The sampling function filters the digital input signals from the opto-isolators and tracks the frequency of the analog signals. The digital inputs are checked against their previous value over a period of half a cycle. Therefore a change in the state of one of the inputs must be maintained over at least half a cycle before it is registered with the protection and control software.

The frequency tracking of the analog input signals is achieved by a recursive Fourier algorithm which is applied to one of the input signals, and works by detecting a change in the measured signal's phase angle. The calculated value of the frequency is used to modify the sample rate being used by the input module to achieve a constant sample rate of 24 samples per cycle of the power waveform. The value of the frequency is also stored for use by the protection and control task.

When the protection and control task is re-started by the sampling function, it calculates the Fourier components for the analog signals. The Fourier components are calculated using a one-cycle, 24-sample Discrete Fourier Transform (DFT). The DFT is always calculated using the last cycle of samples from the 2-cycle buffer, which is the most recent data. Used in this way, the DFT extracts the power frequency fundamental component from the signal and produces the magnitude and phase angle of the fundamental in rectangular component format. The DFT provides an accurate measurement of the fundamental frequency component, and effective filtering of harmonic frequencies and noise. This performance is achieved with the relay input module which provides hardware anti-alias filtering to attenuate frequencies above the half sample rate, and frequency tracking to maintain a sample rate of 24 samples per cycle. The Fourier components of the input current and voltage signals are stored in memory so they can be accessed by all of the protection elements' algorithms. The samples from the input module are also used in an unprocessed form by the disturbance recorder for waveform recording and to calculate true RMS values of current, voltage and power for metering purposes.

2.4.3 Frequency Response

With the exception of the RMS measurements, all other measurements and protection functions are based on the Fourier-derived fundamental component. The fundamental component is extracted by using a 24-sample DFT. This gives good harmonic rejection for frequencies up to the 23rd harmonic. The 23rd is the first predominant harmonic that is not attenuated by the Fourier filter and this is known as an 'Alias'. However, the Alias is attenuated by approximately 85% by an additional, analog, 'anti-aliasing' filter (low pass filter). The combined affect of the anti-aliasing and Fourier filters is shown in the following *Frequency response* diagram.

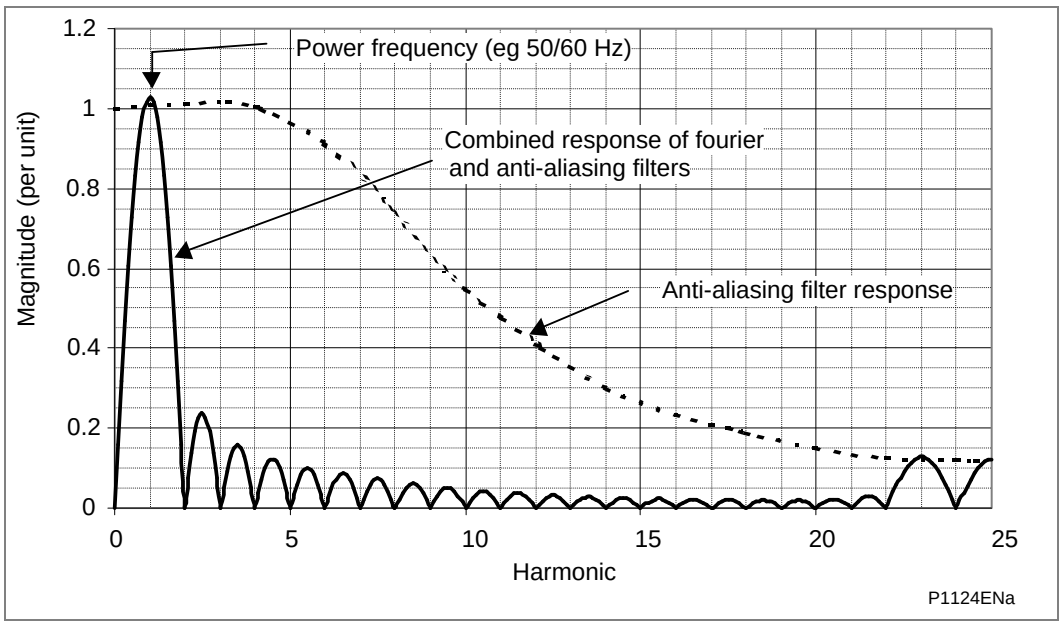


Figure 7 - Frequency response

For power frequencies that are not equal to the selected rated frequency, the harmonics are attenuated to zero amplitude. For small deviations of ±1Hz, this is not a problem but to allow for larger deviations, frequency tracking is used.

Frequency tracking automatically adjusts the sampling rate of the analog to digital conversion to match the applied signal. In the absence of a suitable signal to amplitude track, the sample rate defaults to the selected rated frequency (Fn). If the a signal is in the tracking range of 45 to 66 Hz, the relay locks onto the signal and the measured frequency coincides with the power frequency as shown in the above *Frequency response* diagram. The outputs for harmonics up to the 23rd are zero. The relay frequency tracks off any voltage or current in the order VA/VB/VC/IA/IB/IC down to 10% Vn for voltage and 5%In for current.

2.4.4 Programmable Scheme Logic (PSL)

The Programmable Scheme Logic (PSL) allows the relay user to configure an individual protection scheme to suit their own particular application. This is done with programmable logic gates and delay timers.

The input to the PSL is any combination of the status of the digital input signals from the opto-isolators on the input board, the outputs of the protection elements such as protection starts and trips, and the outputs of the fixed PSL. The fixed PSL provides the relay's standard protection schemes. The PSL consists of software logic gates and timers. The logic gates can be programmed to perform a range of different logic functions and can accept any number of inputs. The timers are used either to create a programmable delay or to condition the logic outputs, such as to create a pulse of fixed duration on the output, regardless of the length of the pulse on the input. The outputs of the PSL are the LEDs on the front panel of the relay and the output contacts at the rear.

The execution of the PSL logic is event driven: the logic is processed whenever any of its inputs change, for example as a result of a change in one of the digital input signals or a trip output from a protection element. Also, only the part of the PSL logic that is affected by the particular input change that has occurred is processed. This reduces the amount of processing time that is used by the PSL. The protection and control software updates the logic delay timers and checks for a change in the PSL input signals every time it runs.

This system provides flexibility for the user to create their own scheme logic design. However, it also means that the PSL can be configured into a very complex system, and because of this setting of the PSL is implemented through the PC support package Easergy Studio/MiCOM S1 Studio.

2.4.5 Function Key Interface (P643 and P645 only)

The ten function keys interface directly into the PSL as digital input signals and are processed based on the PSLs event-driven execution. However, a change of state is only recognized when a key press is executed, on average for longer than 200 ms. The time to register a change of state depends on whether the function key press is executed at the start or the end of a protection task cycle, with the additional hardware and software scan time included. A function key press can provide a latched (toggled mode) or output on key press only (normal mode) depending on how it is programmed and can be configured to individual protection scheme requirements. The latched state signal for each function key is written to non-volatile memory and read from non-volatile memory during relay power up, allowing the function key state to be reinstated after power-up if the relay power is lost.

2.4.5.1 PSL Data

In the PSL editor in MiCOM S1 Studio, when a PSL file is downloaded to the relay the user can specify the group to download the file and a 32 character PSL reference description. This PSL reference is shown in the **Grp. 1/2/3/4 PSL Ref.** cell in the **PSL DATA** menu in the relay. The download date and time and file checksum for each group's PSL file is also shown in the **PSL DATA** menu in cells **Date/Time** and **Grp. 1/2/3/4 PSL ID**. The PSL data can be used to show if a PSL has been changed and can be useful in providing information for version control of PSL files.

The default PSL Reference description is **Default PSL** followed by the model number, for example, Default PSL **P64x??????0yy0?** where x refers to the model such as 1, 2, 3 and yy refers to the software version such as 05. This is the same for all protection setting groups (since the default PSL is the same for all groups). Since the LCD display (bottom line) only has space for 16 characters, the display must be scrolled to see all 32 characters of the PSL Reference description.

The default date and time is the date and time when the defaults were loaded.

Note	*The PSL DATA column information is only supported by Courier and MODBUS, but not DNP3.0 or IEC60870-5-103.*

2.4.6 Event, Fault and Maintenance Recording

A change in any digital input signal or protection element output signal is used to indicate that an event has taken place. When this happens, the protection and control task sends a message to the supervisor task to show that an event is available to be processed. The protection and control task writes the event data to a fast buffer in SRAM that is controlled by the supervisor task. When the supervisor task receives either an event or fault record message, it instructs the platform software to create the appropriate log in battery backed-up SRAM. The supervisor's buffer is faster than battery backed-up SRAM, therefore the protection software is not delayed waiting for the records to be logged by the platform software. However, if a large number of records to be logged are created in a short time, some may be lost if the supervisor's buffer is full before the platform software is able to create a new log in battery backed-up SRAM. If this occurs, an event is logged to indicate this loss of information.

Maintenance records are created in a similar manner with the supervisor task instructing the platform software to log a record when it receives a maintenance record message. However, it is possible that a maintenance record may be triggered by a fatal error in the relay, in which case it may not be possible to successfully store a maintenance record, depending on the nature of the problem. See the *Self-Testing and Diagnostics* section.

Fault records are stored in the sequence of events. They can be viewed locally or remotely and include:

- Faulty phase(s)
- Protection Tripped
- Protection Started
- Fault duration
- Fault type (internal or external fault)
- Operating time
- Primary or Secondary RMS values of prefault phase and neutral currents or angle of each winding
- Primary or Secondary RMS values of fault phase and neutral currents or angle of each winding
- Primary or Secondary RMS values of differential and biased current of each phase

2.4.7 Disturbance Recorder

The analog values and logic signals are routed from the protection and control software to the disturbance recorder software. The platform software interfaces with the disturbance recorder to allow the stored records to be extracted.

The disturbance recording is started from any relay start or trip, or any specific opto-isolator input or internal information. The recording time is user selectable up to a maximum of 10 seconds. The disturbance recorder operates as a separate task to the protection and control task. It can record the waveforms for up to 21 analog channels and the values of up to 32 digital signals. The disturbance recorder is supplied with data once per cycle by the protection and control task. The disturbance recorder collates the data that it receives into the required length disturbance record. The disturbance records that can also store the data in COMTRADE format can be extracted using MiCOM S1 Studio, allowing the use of other packages to view the recorded data.

3 SELF-TESTING AND DIAGNOSTICS

The relay includes several self-monitoring functions to check the operation of its hardware and software when it is in service. These are included so that if an error or fault occurs in the relay's hardware or software, the relay is able to detect and report the problem and attempt to resolve it by performing a reboot. The relay must therefore be out of service for a short time, during which the **Healthy** LED on the front of the relay is OFF and, the watchdog contact at the rear is ON. If the reboot fails to resolve the problem, the relay takes itself permanently out of service; the **Healthy** LED stays OFF and watchdog contact stays ON.

If a problem is detected by the self-monitoring functions, the relay stores a maintenance record in battery backed-up SRAM.

The self-monitoring is implemented in two stages:

- firstly a thorough diagnostic check that is performed when the relay is booted-up
- secondly a continuous self-checking operation that checks the operation of the relay's critical functions while it is in service.

3.1 Start-Up Self-Testing

The self-testing that is carried out when the relay is started takes a few seconds to complete, during which time the relay's protection is unavailable. This is shown by the **Healthy** LED on the front of the relay which is ON when the relay has passed all tests and entered operation. If the tests detect a problem, the relay remains out of service until it is manually restored to working order.

The operations that are performed at start-up are:

- System Boot
- Initialization Software
- Platform Software Initialization and Monitoring

3.1.1 System Boot

The integrity of the flash memory is verified using a checksum before the program code and data are copied into SRAM and executed by the processor. When the copy is complete the data then held in SRAM is checked against that in flash memory to ensure they are the same and that no errors have occurred in the transfer of data from flash memory to SRAM. The entry point of the software code in SRAM is then called which is the relay initialization code.

3.1.2 Initialization Software

The initialization process includes the operations of initializing the processor registers and interrupts, starting the watchdog timers (used by the hardware to determine whether the software is still running), starting the real-time operating system and creating and starting the supervisor task.

In the initialization process the relay checks the following.

- The status of the battery
- The integrity of the battery backed-up SRAM that stores event, fault and disturbance records
- The voltage level of the field voltage supply that drives the opto-isolated inputs
- The operation of the LCD controller
- The watchdog operation

When the initialization software routine is complete, the supervisor task starts the platform software.

3.1.3 Platform Software Initialization and Monitoring

In starting the platform software, the relay checks the integrity of the data held in non-volatile memory with a checksum, the operation of the real-time clock, and the IRIG-B board if fitted. The final test that is made concerns the input and output of data; the presence and healthy condition of the input board is checked and the analog data acquisition system is checked through sampling the reference voltage.

At the successful conclusion of all of these tests the relay is entered into service and the protection started-up.

3.2 Continuous Self-Testing

When the relay is in service, it continually checks the operation of the critical parts of its hardware and software. The checking is carried out by the system services software (see section on relay software earlier in this section) and the results reported to the platform software.

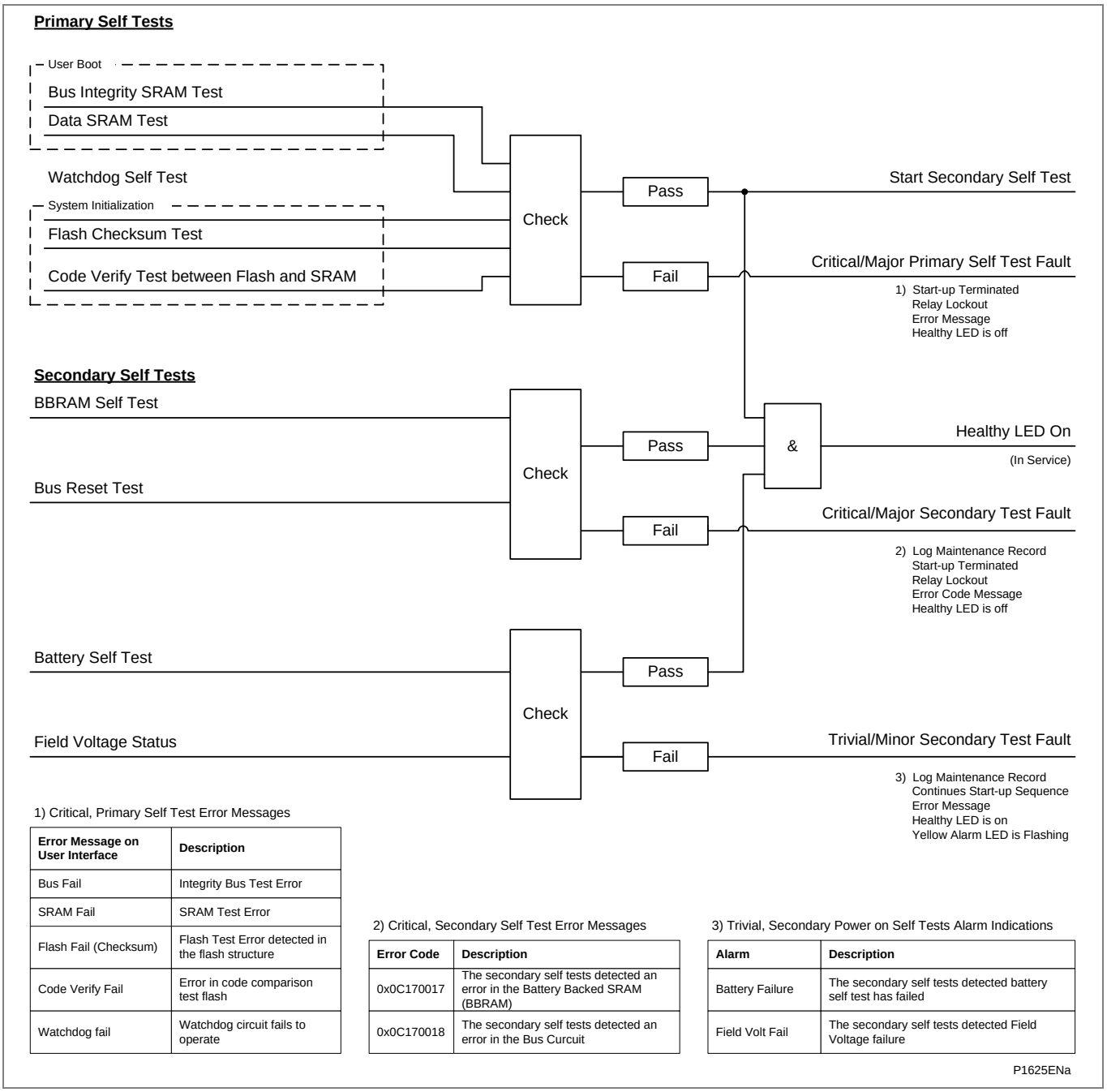
The functions that are checked are as follows:

- The flash EPROM containing all program code and language text is verified by a checksum
- The code and constant data held in SRAM is checked against the corresponding data in flash EPROM to check for data corruption
- The SRAM containing all data other than the code and constant data is verified with a checksum
- The non-volatile memory containing setting values is verified by a checksum, whenever its data is accessed
- The battery status
- The level of the field voltage
- The integrity of the digital signal I/O data from the opto-isolated inputs and the relay contacts, is checked by the data acquisition function every time it is executed. The operation of the analog data acquisition system is checked by the acquisition function every time it is executed. This is done by sampling the reference voltage on a spare multiplexed channel
- The operation of the IRIG-B board is checked, where it is fitted, by the software that reads the time and date from the board

If the Ethernet board is fitted, it is checked by the software on the main processor board. If the Ethernet board fails to respond, an alarm is raised and the board is reset in an attempt to resolve the problem

Also, the correct operation of the CLIO board is checked, where it is fitted.

In the unlikely event that one of the checks detects an error in the relay's subsystems, the platform software is notified and it will attempt to log a maintenance record in battery backed-up SRAM. If the problem is with the battery status or the IRIG-B board, the relay continues in operation. However, for problems detected in any other area the relay shuts down and reboots. This result in a period of up to 12 seconds when protection is unavailable, but the complete restart of the relay including all initializations should clear most problems that could occur. An integral part of the start-up procedure is a thorough diagnostic self-check. If this detects the same problem that caused the relay to restart, the restart has not cleared the problem and the relay takes itself permanently out of service. This is indicated by the **Healthy** LED on the front of the relay which goes OFF, and the watchdog contact that goes ON.



1) Critical, Primary Self Test Error Messages

Error Message on User Interface	Description
Bus Fail	Integrity Bus Test Error
SRAM Fail	SRAM Test Error
Flash Fail (Checksum)	Flash Test Error detected in the flash structure
Code Verify Fail	Error in code comparison test flash
Watchdog fail	Watchdog circuit fails to operate

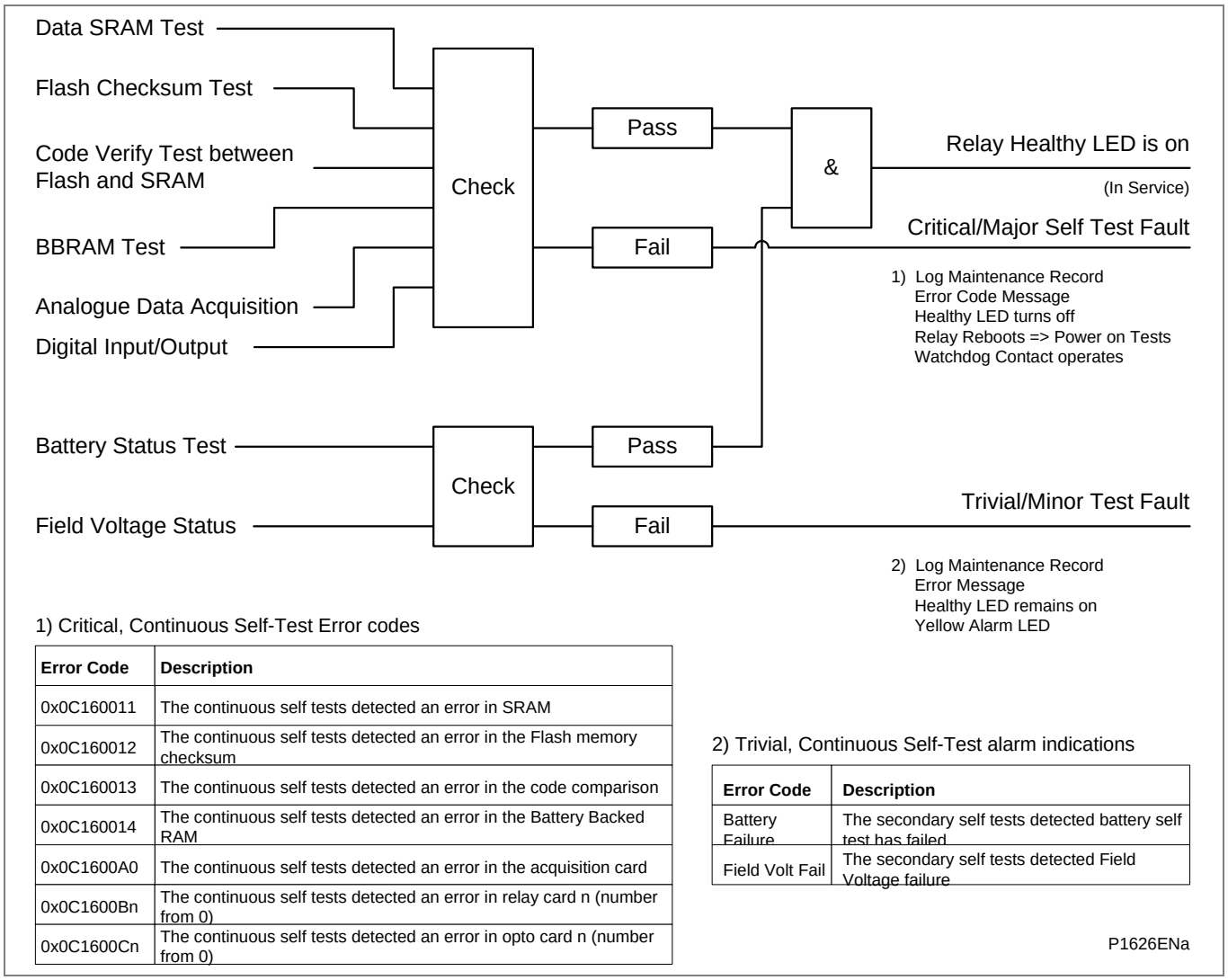
2) Critical, Secondary Self Test Error Messages

Error Code	Description
0x0C170017	The secondary self tests detected an error in the Battery Backed SRAM (BBRAM)
0x0C170018	The secondary self tests detected an error in the Bus Curcuit

3) Trivial, Secondary Power on Self Tests Alarm Indications

Alarm	Description
Battery Failure	The secondary self tests detected battery self test has failed
Field Volt Fail	The secondary self tests detected Field Voltage failure

Figure 8 - Start-up self-testing logic



1) Critical, Continuous Self-Test Error codes

Error Code	Description
0x0C160011	The continuous self tests detected an error in SRAM
0x0C160012	The continuous self tests detected an error in the Flash memory checksum
0x0C160013	The continuous self tests detected an error in the code comparison
0x0C160014	The continuous self tests detected an error in the Battery Backed RAM
0x0C1600A0	The continuous self tests detected an error in the acquisition card
0x0C1600Bn	The continuous self tests detected an error in relay card n (number from 0)
0x0C1600Cn	The continuous self tests detected an error in opto card n (number from 0)

2) Trivial, Continuous Self-Test alarm indications

Error Code	Description
Battery Failure	The secondary self tests detected battery self test has failed
Field Volt Fail	The secondary self tests detected Field Voltage failure

Figure 9 - Continuous self-testing logic

Notes:

COMMISSIONING

CHAPTER 11

Date:	07/2018
Products covered by this chapter:	This chapter covers the specific versions of the MiCOM products listed below. This includes ***only*** the following combinations of Software Version and Hardware Suffix.
Hardware Suffix:	L (P642) M (P643/P645)
Software Version:	B4 - P64x (P642, P643 & P645)
Connection Diagrams:	10P642xx (xx = 01 to 10) 10P643xx (xx = 01 to 06) 10P645xx (xx = 01 to 09)

CONTENTS

FIGURES

TABLES

1 INTRODUCTION

MiCOM P40 relays are fully numerical in their design, implementing all protection and non-protection functions in software. The relays use a high degree of self-checking and give an alarm in the unlikely event of a failure. Therefore, the commissioning tests do not need to be as extensive as with non-numeric electronic or electro-mechanical relays.

To commission numeric relays, you only need to verify that the hardware is functioning correctly and the application-specific software settings have been applied to the relay. You don't need to test every function of the relay if the settings have been verified by one of these methods:

- Extracting the settings applied to the relay using appropriate setting software (preferred method)
- Using the operator interface

To confirm that the product is operating correctly once the application-specific settings have been applied, perform a test on a single protection element.

Unless previously agreed to the contrary, the customer is responsible for determining the application-specific settings to be applied to the relay and for testing any scheme logic applied by external wiring or configuration of the relay's internal Programmable Scheme Logic (PSL).

Blank commissioning test and setting records are available for completion as needed.

As the relay's menu language is user-selectable, the Commissioning Engineer can change it to allow accurate testing as long as the menu is restored to the customer's preferred language on completion.

To simplify the specifying of menu cell locations in these Commissioning Instructions, they are given in the form [courier reference: COLUMN HEADING, Cell Text]. For example, the cell for selecting the menu language (first cell under the column heading) is in the System Data column (column 00) so it is given as [0001: SYSTEM DATA, Language].

Warning	**Before carrying out any work on the equipment, you should be familiar with the contents of the latest issue of the Safety Guide, Safety Information and Technical Data chapters and the equipment rating label(s).**

Caution	***The relay must not be disassembled in any way during commissioning.***

2 SETTING FAMILIARIZATION

When first commissioning a relay, allow sufficient time to become familiar with how to apply the settings.

The *Menu Database document* and the *Introduction* or *Settings* chapters contain a detailed description of the menu structure of Schneider Electric relays. The menu database is a separate document which can be downloaded from our website:

www.schneider-electric.com

With the secondary front cover in place, all keys except the ↵ key are accessible. All menu cells can be read. LEDs and alarms can be reset. However, no protection or configuration settings can be changed, or fault and event records cleared.

Removing the secondary front cover allows access to all keys so that settings can be changed, LEDs and alarms reset, and fault and event records cleared. However, to make changes to menu cells, the appropriate user role and password is needed.

Alternatively, if a portable PC with suitable setting software is available (such as Easergy Studio), the menu can be viewed one page at a time, to display a full column of data and text. This PC software also allows settings to be entered more easily, saved to a file for future reference, or printed to produce a settings record. Refer to the PC software user manual for details. If the software is being used for the first time, allow sufficient time to become familiar with its operation.

3 COMMISSIONING TEST MENU

To help minimize the time needed to test MiCOM relays the relay provides several test facilities under the '**COMMISSION TESTS**' menu heading. There are menu cells which allow the status of the opto-isolated inputs, output relay contacts, internal Digital Data Bus (DDB) signals and user-programmable LEDs to be monitored. Additionally there are cells to test the operation of the output contacts, user-programmable LEDs and, where available, the auto-reclose cycles.

The following table shows the relay menu of commissioning tests, including the available setting ranges and factory defaults. Each of the main menu tests are described in more detail in the following sections.

COMMISSION TESTS for P64x		
Menu Text	**Default Setting**	**Settings**
Opto I/P Status	-	-
Relay O/P Status	-	-
Test Port Status	-	-
LED Status	-	-
Monitor Bit 1	64 - (LED 1)	0 to 2047
Monitor Bit 2	65 - (LED 2)	0 to 2047
Monitor Bit 3	66 - (LED 3)	0 to 2047
Monitor Bit 4	67 - (LED 4)	0 to 2047
Monitor Bit 5	68 - (LED 5)	0 to 2047
Monitor Bit 6	69 - (LED 6)	0 to 2047
Monitor Bit 7	70 - (LED 7)	0 to 2047
Monitor Bit 8	71 - (LED 8)	0 to 2047
Test Mode	Disabled	Disabled, Test Mode, Contacts Blocked
Test Pattern	All bits set to 0	0 = Not Operated, 1 = Operated
Contact Test	No Operation	No Operation, Apply Test, Remove Test
Test LEDs	No Operation	No Operation, Apply Test
Test Auto-reclose	No Operation	No Operation, 3 Pole Test
Red LED Status	P643/P645 only	-
Green LED Status	P643/P645 only	-
Note	*See Relay Menu Database for details of DDB signals*	

Table 1 - Commission Tests

3.1 Opto I/P Status

This menu cell displays the status of the relay's opto-isolated inputs as a binary string, a '**1**' indicating an energized opto-isolated input and a '**0**' a de-energized one. If the cursor is moved along the binary numbers the corresponding label text will be displayed for each logic input.

It can be used during commissioning or routine testing to monitor the status of the opto-isolated inputs whilst they are sequentially energized with a suitable dc voltage.

3.2 Relay O/P Status

This menu cell displays the status of the Digital Data Bus (DDB) signals that result in energization of the output relays as a binary string, a '**1**' indicating an operated state and '**0**' a non-operated state. If the cursor is moved along the binary numbers the corresponding label text will be displayed for each relay output.

The information displayed can be used during commissioning or routine testing to indicate the status of the output relays when the relay is '**in service**'. Additionally fault finding for output relay damage can be performed by comparing the status of the output contact under investigation with it's associated bit.

Note	*When the '**Test Mode**' cell is set to '**Enabled**' this cell will continue to indicate which contacts would operate if the relay was in-service, it does not show the actual status of the output relays.*

3.3 Test Port Status

This menu cell displays the status of the eight Digital Data Bus (DDB) signals that have been allocated in the '**Monitor Bit**' cells. If the cursor is moved along the binary numbers the corresponding DDB signal text string will be displayed for each monitor bit.

By using this cell with suitable monitor bit settings, the state of the DDB signals can be displayed as various operating conditions or sequences are applied to the relay. Thus the Programmable Scheme Logic (PSL) can be tested.

As an alternative to using this cell, the optional monitor/download port test box can be plugged into the monitor/download port located behind the bottom access cover. Details of the monitor/download port test box can be found in the *Using a Monitor/Download Port Test Box* section of this chapter.

3.4 LED Status (P642 only)

The '**LED Status**' is an eight bit binary strings that indicate which of the user-programmable LEDs on the relay are illuminated when accessing the relay from a remote location, a '**1**' indicating a particular LED is lit and a '**0**' not lit.

3.5 Monitor Bits 1 to 8

The eight '**Monitor Bit**' cells allow the user to select the status of which digital data bus signals can be observed in the '**Test Port Status**' cell or via the monitor/download port.

Each '**Monitor Bit**' is set by entering the required Digital Data Bus (DDB) signal number from the list of available DDB signals in the Programmable Logic chapter. The pins of the monitor/download port used for monitor bits are given in the following table. The signal ground is available on pins 18, 19, 22 and 25.

Note	*The required Digital Data Bus (DDB) signal numbers are as follows:* *0 - 1022 for P14x/P24x* *0 - 2027 for P34x* *0 - 2047 for P44x* *0 - 1791 for P44y/P445/P54x/P547/P841* *0 – 511 for P64x*

Monitor bit	1	2	3	4	5	6	7	8
Monitor/download port pin	11	12	15	13	20	21	23	24

Table 2 - Monitor Bits

Warning	**The monitor/download port is not electrically isolated against induced voltages on the communications channel. It should therefore only be used for local communications.**

3.6 Test Mode

The **Test Mode** menu cell (in the **COMMISSION TESTS** column) is used to allow secondary injection testing to be performed on the relay.

To select test mode set the Test Mode menu cell to '**Test Mode**'. It causes an alarm condition to be recorded, the yellow ALARM LED to light and an alarm message '**Test Mode Alm**' to be generated.

Test Mode freezes any information stored in the **CB CONDITION** column and (in IEC60870-5-103 builds) changes the Cause Of Transmission (COT) to Test Mode. For relays supporting IEC 61850 Edition 2, the test bit for data quality attribute shall set to TRUE, and the Logical Device Mode will set to test.

Test mode can also be enabled by energizing an opto mapped to the **Test Mode** signal.

To enable testing of output contacts set the **Test Mode** cell to **Contacts Blocked**. It causes an alarm condition to be recorded, the yellow ALARM LED to light and an alarm message '**Contacts Blk Alm**' to be generated.

In **Contact Blocked** mode, the protection function still works but the contacts will not operate. Also the **test pattern** and contact test functions are visible, which can be used to manually operate the output contacts. For relays supporting IEC 61850 Edition 2, the test bit for data quality attribute shall set to TRUE, and the Logical Device Mode will set to test/blocked.

Contacts Blocked can also be enabled by energizing an opto mapped to the **Contacts Blocked** signal.

Once testing is complete the cell must be set back to '**Disabled**' to restore the relay back to service.

WARNING **If you use or enable Test Mode, you must disable Test Mode before putting the relay back into active service. IT IS POTENTIALLY EXTREMELY UNSAFE TO ATTEMPT TO USE ANY RELAY WHICH IS STILL IN TEST MODE IN ACTIVE SERVICE.**

3.7 Test Pattern

The '**Test Pattern**' cell is used to select the output relay contacts that will be tested when the '**Contact Test**' cell is set to '**Apply Test**'. The cell has a binary string with one bit for each user-configurable output contact which can be set to '**1**' to operate the output under test conditions and '**0**' to not operate it.

3.8 Contact Test

When the '**Apply Test**' command in this cell is issued the contacts set for operation (set to '**1**') in the '**Test Pattern**' cell change state. After the test has been applied the command text on the LCD will change to '**No Operation**' and the contacts will remain in the Test State until reset issuing the '**Remove Test**' command. The command text on the LCD will again revert to '**No Operation**' after the '**Remove Test**' command has been issued.

Note *When the '**Test Mode**' cell is set to '**Enabled**' the '**Relay O/P Status**' cell does not show the current status of the output relays and hence can not be used to confirm operation of the output relays. Therefore it will be necessary to monitor the state of each contact in turn.*

3.9 Test LEDs

When the '**Apply Test**' command in this cell is issued the eight/eighteen user-programmable LEDs will illuminate for approximately 2 seconds before they extinguish and the command text on the LCD reverts to '**No Operation**'.

3.10 Red LED Status and Green LED Status (P643/P645)

The **Red LED Status** and **Green LED Status** cells are 18-bit binary strings that show which of the user-programmable LEDs on the relay are ON when accessing the relay from a remote location. **1** indicates a particular LED is ON and a **0** OFF. When the status of a particular LED in both cells is **1**, this means the LED is yellow.

3.11 Using a Monitor/Download Port Test Box

A monitor/download port test box containing 8 LEDs and a switchable audible indicator is available from Schneider Electric, or one of their regional sales offices. It is housed in a small plastic box with a 25-pin male D-connector that plugs directly into the relay's monitor/download port. There is also a 25-pin female D-connector which allows other connections to be made to the monitor/download port whilst the monitor/download port test box is in place.

Each LED corresponds to one of the monitor bit pins on the monitor/download port with '**Monitor Bit 1**' being on the left hand side when viewing from the front of the relay. The audible indicator can either be selected to sound if a voltage appears on any of the eight monitor pins or remain silent so that indication of state is by LED alone.

4 EQUIPMENT REQUIRED FOR COMMISSIONING

4.1 Minimum Equipment Required

The minimum equipment needed varies slightly, depending on the features provided by each type of MiCOM product. The list of minimum equipment is given below:

- A portable PC, with an RS232 port as well as appropriate software
- Multifunctional dynamic current and voltage injection test set
- Multimeter with suitable ac current range, and ac and dc voltage ranges of 0 - 440V and 0 - 250V respectively
- Continuity tester (if not included in multimeter)
- Phase angle meter
- Phase rotation meter

Note	*Modern test equipment may contain many of the above features in one unit.*

4.2 Optional Equipment

- Fiber optic power meter (and fibre optic test leads may be required depending upon application).
- Multi-finger test plug type Easergy test plug (if Easergy test block type is installed)
- An electronic or brushless insulation tester with a dc output not exceeding 500 V (for insulation resistance testing when required)
- K-Bus to EIA(RS)232 protocol converter (if the first rear EIA(RS)485 K-Bus port or second rear port configured for K-Bus is being tested and one is not already installed)
- EIA(RS)485 to EIA(RS)232 converter (if first rear EIA(RS)485 port or second rear port configured for EIA(RS)485 is being tested)
- A printer, for printing a setting record from the portable PC

5 PRODUCT CHECKS

These product checks cover all aspects of the relay that need to be checked to ensure:

- that it has not been physically damaged before commissioning
- that it is functioning correctly and
- that all input quantity measurements are within the stated tolerances

If the application-specific settings have been applied to the relay before commissioning, it is advisable to make a copy of the settings to allow their restoration later.

If Programmable Scheme Logic (PSL) (other than the default settings with which the relay was supplied) has been applied, the default settings should be restored before commissioning. This can be done by:

- Obtaining a setting file from the customer. This requires a portable PC with appropriate setting software for transferring the settings from the PC to the relay.
- Extracting the settings from the relay itself. This requires a portable PC with appropriate setting software.
- Manually creating a setting record. This could be done by stepping through the front panel menu using the front panel user interface.

Warning **Before carrying out any work on the equipment, you should be familiar with the contents of the latest issue of the Safety Guide, Safety Information and Technical Data chapters and the equipment rating label(s).**

5.1 With the Relay De-Energized

The following group of tests should be carried out without the auxiliary supply applied to the relay and with the trip circuit isolated.

Before inserting the test plug, refer to the scheme diagram to ensure this will not cause damage or a safety hazard. For example, the test block may be associated with protection current transformer circuits. Before the test plug is inserted into the test block, make sure the sockets in the test plug which correspond to the current transformer secondary windings are linked.

Warning **The current and voltage transformer connections must be isolated from the relay for these checks. If a MiCOM P991 or an Easergy test block is provided, insert the Easergy or MiCOM P992 test plug, which open-circuits all wiring routed through the test block.**

Danger **Never open-circuit the secondary circuit of a current transformer because the high voltage produced may be lethal. It could also damage insulation.**

If a test block is not provided, isolate the voltage transformer supply to the relay using the panel links or connecting blocks. Short-circuit and disconnect the line current transformers from the relay terminals. Where means of isolating the auxiliary supply and trip circuit (such as isolation links, fuses and MCB) are provided, these should be used. If this is impossible, the wiring to these circuits must be disconnected and the exposed ends suitably terminated to prevent them from being a safety hazard.

5.1.1 Visual Inspection

Caution	**Check the rating information under the top access cover on the front of the relay. Check that the relay being tested is correct for the protected line or circuit. Ensure that the circuit reference and system details are entered onto the setting record sheet. Double-check the CT secondary current rating, and be sure to record the actual CT tap which is in use.**

Carefully examine the relay to see that no physical damage has occurred since installation.

Ensure that the case earthing connections, at the bottom left-hand corner at the rear of the relay case, are used to connect the relay to a local earth bar using an adequate conductor.

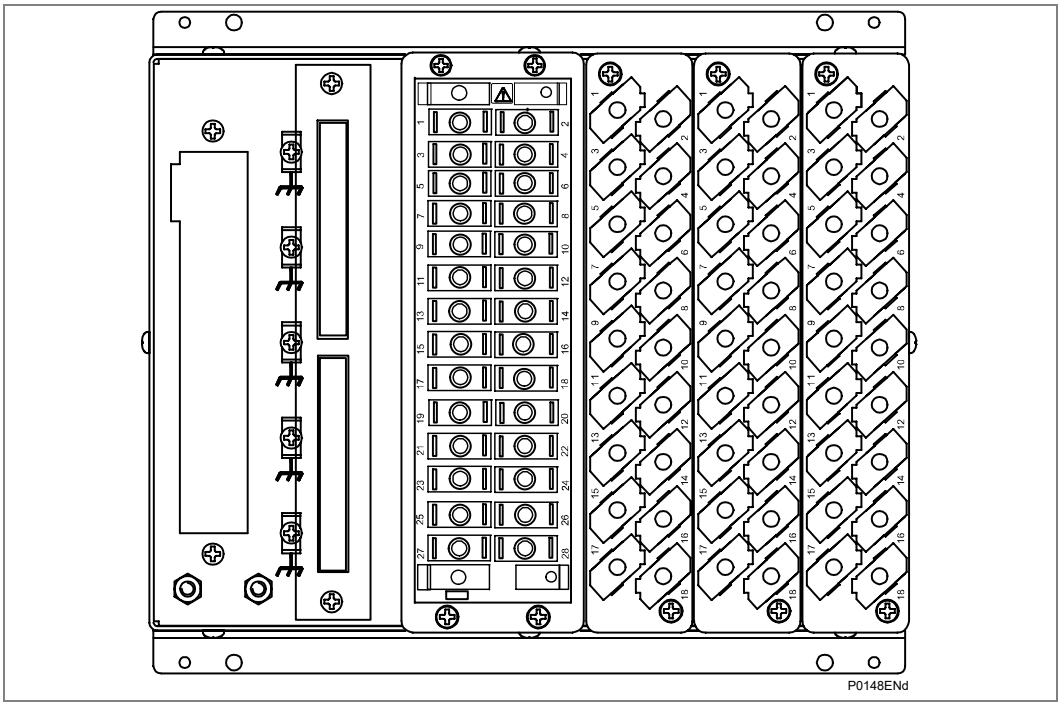


Figure 1 - Rear terminal blocks on size 40TE case

5.1.2 Current Transformer Shorting Contacts

If needed, the current transformer shorting contacts can be checked to ensure they close when the heavy-duty terminal block shown in the following figure is disconnected from the current input PCB. The heavy-duty terminal block location depends on the relay model.

P64x	*The P642 (40TE case) block references C uses heavy duty terminal blocks.* *The P643 & P645 (60TE case) block references C and E use heavy duty terminal blocks.* *The P645 (80TE case) block references D and F uses heavy duty terminal blocks.*

Current input	Shorting Contact Between Terminals		
	P642 (40TE)	P643/P645 (60TE)	P645 (80TE)
	1A / 5A CTs	1A / 5A CTs	1A / 5A CTs
IA1	C24-C23	C24-C23	D24-D23
IB1	C26-C25	C26-C25	D26-D25

Current input	Shorting Contact Between Terminals		
	P642 (40TE)	P643/P645 (60TE)	P645 (80TE)
IC1	C28-C27	C28-C27	D28-D27
IA2	C18-C17	C18-C17	D18-D17
IB2	C20-C19	C20-C19	D20-D19
IC2	C22-C21	C22-C21	D22-D21
IA3		E24-E23	F24-F23
IB3		E26-E25	F26-F25
IC3		E28-E27	F28-F27
IA4			F18-F17
IB4			F20-F19
IC4			F22-F21
IA5			F12-F11
IB5			F14-F13
IC5			F16-F15
IN-TV		C12-C11	D12-D11
IN-LV	C14-C13	C14-C13	D14-D13
IN-HV	C16-C15	C16-C15	D16-D15

Table 3 - Current transformer shorting contact locations

Heavy duty terminal blocks are fastened to the rear panel using four Pozidriv or PZ1 screws. These are at the top and bottom between the first and second, and third and fourth, columns of terminals (see the *Location of Securing Screws for Terminal Blocks* diagram below).

Note	*Use a magnetic-bladed screwdriver to avoid losing screws or leaving them in the terminal block.*

Pull the terminal block away from the rear of the case and check with a continuity tester that all the shorting switches being used are closed. The following table(s) shows the terminals between which shorting contacts are fitted.

Warning	***If external test blocks are connected to the relay, take great care when using the associated test plugs such as MMLB and MiCOM P992 since their use may make hazardous voltages accessible. CT* shorting links must be in place before the insertion or removal of MMLB test plugs, to avoid potentially lethal voltages.***

Note	*When a MiCOM P992 Test Plug is inserted into the MiCOM P991 Test Block, the secondaries of the line CTs are automatically shorted, making them safe.*

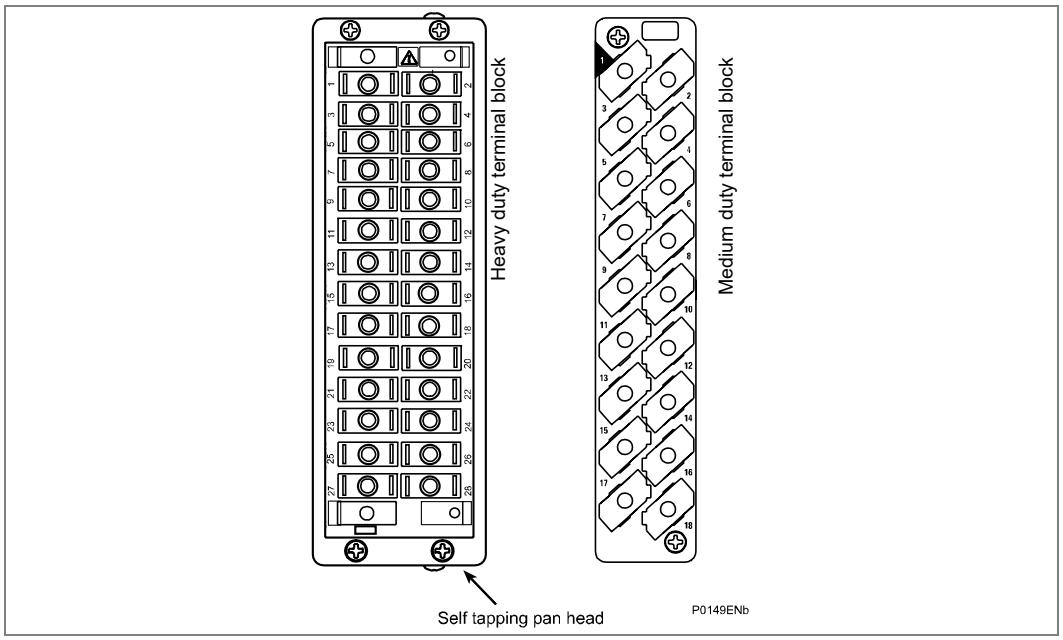


Figure 2 - Location of securing screws for terminal blocks

5.1.3 Insulation

Insulation resistance tests are only necessary during commissioning if it is required for them to be done and they haven't been performed during installation.

Isolate all wiring from the earth and test the insulation with an electronic or brushless insulation tester at a dc voltage not exceeding 500 V. Terminals of the same circuits should be temporarily connected together.

The main groups of relay terminals are:

- Voltage transformer circuits
- Current transformer circuits
- Auxiliary voltage supply
- Field voltage output and opto-isolated control inputs
- Relay contacts
- First rear EIA(RS)485 communication port
- RTD inputs (where available)
- Current Loop (analog) Inputs and Outputs (CLIO) (where available)
- Case earth

The insulation resistance should be greater than 100 MΩ at 500 V.

On completion of the insulation resistance tests, ensure all external wiring is correctly reconnected to the unit.

5.1.4 External Wiring

Caution	**Check that the external wiring is correct to the relevant relay diagram and scheme diagram. Ensure as far as practical that phasing/phase rotation appears to be as expected. The relay diagram number appears on the rating label under the top access cover on the front of the relay. Schneider Electric supply the corresponding connection diagram with the order acknowledgement for the relay.**

If a MiCOM P991 or an Easergy test block is provided, check the connections against the wiring diagram. It is recommended that the supply connections are to the live side of the test block (colored orange with the odd numbered terminals 1, 3, 5, 7, and so on). The auxiliary supply is normally routed through terminals 13 (supply positive) and 15 (supply negative), with terminals 14 and 16 connected to the relay's positive and negative auxiliary supply terminals respectively. However, check the wiring against the schematic diagram for the installation to ensure compliance with the customer's normal practice.

5.1.5 Watchdog Contacts

Using a continuity tester, check that the watchdog contacts are in the states shown in the *Watchdog contact status* table for a de-energized relay.

Terminals			Contact state	
			Relay de-energized	Relay energized
F11 - F12 J11 - J12 M11 - M12	P642 P643/P645 P645	40TE 60TE 80TE	Closed	Open
F13 - F14 J13 - J14 M13 - M14	P642 P643/P645 P645	40TE 60TE 80TE	Open	Closed

Table 4 - Watchdog contact status

5.1.6 Auxiliary Supply

Caution	***The relay can be operated from either a dc only or an ac/dc auxiliary supply depending on the relay's nominal supply rating. The incoming voltage must be within the operating range specified in the following table.***

Without energizing the relay, measure the auxiliary supply to ensure it is within the operating range.

Note	*The relay can withstand an ac ripple of up to 12% of the upper rated voltage on the dc auxiliary supply.*

Nominal Ranges	Operative dc Range	Operative ac Range
24 - 32V dc	10 to 38 V dc	-
48 - 125V dc	37 to 150 V dc	-
110 - 250V dc (100 - 240V ac rms) **	87 to 300 V dc	80 to 265 V ac
** rated for ac or dc operation		

Table 5 - Operational range of auxiliary supply Vx

Caution	***Do not energize the relay using the battery charger with the battery disconnected as this can irreparably damage the relay's power supply circuitry.***

Caution	**Energize the relay only if the auxiliary supply is within the operating range. If a test block is provided, it may be necessary to link across the front of the test plug to connect the auxiliary supply to the relay.**

5.2 With the Relay Energized

The following group of tests verify that the relay hardware and software is functioning correctly and should be carried out with the auxiliary supply applied to the relay.

Caution	***The current and voltage transformer connections must remain isolated from the relay for these checks. The trip circuit should also remain isolated to prevent accidental operation of the associated circuit breaker.***

Caution	***The InterMiCOM64 communication channel (when fitted) should be disconnected to prevent the remote end relay being affected during the tests.***

5.2.1 Watchdog Contacts

Using a continuity tester, check the watchdog contacts are in the states shown in Table 4 for an energized relay.

5.2.2 LCD Front Panel Display

The Liquid Crystal Display (LCD) is designed to operate in a wide range of substation ambient temperatures. For this purpose, the Px40 relays have an **LCD Contrast** setting. This allows the user to adjust the lightness or darkness of the displayed characters. The contrast is factory preset to account for a standard room temperature, however it may be necessary to adjust the contrast to give the best in-service display. To change the contrast, at the bottom of the **CONFIGURATION** column, use cell [09FF: LCD Contrast] to increment (darker) or decrement (lighter), as required.

Important	***Before applying a contrast setting, ensure that it does not make the display too light or dark so the menu text becomes unreadable. If this happens, it is possible to restore the display by downloading an Easergy Studio setting file, with the LCD Contrast set in the typical range of 7 to 11.***

5.2.3 Date and Time

Before setting the date and time, ensure that the factory-fitted battery isolation strip that prevents battery drain during transportation and storage has been removed. With the lower access cover open, the presence of the battery isolation strip can be checked by a red tab protruding from the positive side of the battery compartment. Lightly pressing the battery to prevent it falling out of the battery compartment, pull the red tab to remove the isolation strip.

The data and time should now be set to the correct values. The method of setting depends on whether accuracy is being maintained through the optional Inter-Range Instrumentation Group standard B (IRIG-B) port on the rear of the relay or by using IEEE1588 and SNTP via Ethernet.

5.2.3.1 With an IRIG-B Signal

Note	*For P741 the IRIG-B signal may apply to the Central Unit only.*

If a satellite time clock signal conforming to IRIG-B is provided and the relay has the optional IRIG-B port fitted, the satellite clock equipment should be energized.

To allow the relay's time and date to be maintained from an external IRIG-B source cell [DATE and TIME, IRIG-B Sync.] must be set to **Enabled**.

Ensure the relay is receiving the IRIG-B signal by checking that cell [DATE and TIME, IRIG-B Status] reads **Active**.

Once the IRIG-B signal is active, adjust the time offset of the universal coordinated time (satellite clock time) on the satellite clock equipment so that local time is displayed.

Check the time, date and month are correct in cell [0801: DATE and TIME, Date/Time]. The IRIG-B signal does not contain the current year so needs to be set manually in this cell.

If the auxiliary supply fails, with a battery fitted in the compartment behind the bottom access cover, the time and date is maintained. Therefore, when the auxiliary supply is restored, the time and date are correct and need not be set again.

To test this, remove the IRIG-B signal, then remove the auxiliary supply from the relay. Leave the relay de-energized for approximately 30 seconds. On re-energization, the time in cell [DATE and TIME, Date/Time] should be correct. Then reconnect the IRIG-B signal.

5.2.3.2 With SNTP

If SNTP time synch has been configured for IEC61850 or DNP3oE communications then check the SNTP Status in the DATE and TIME column.

Once the SNTP signal is active, adjust the time offset of the universal coordinated time (satellite clock time) on the satellite clock equipment so that local time is displayed. Check the time, date and month are correct in cell [0801: DATE and TIME, Date/Time].

5.2.3.3 Without an IRIG-B or SNTP Signal

Note	*For P741 the IRIG-B signal may not apply to the Central Unit only. For the P742/P743 it may apply to the Peripheral Unit only.*

If the time and date is not being maintained by an IRIG-B signal, ensure that cell [0804: DATE and TIME, IRIG-B Sync.] is set to **Disabled**.

Set the date and time to the correct local time and date using cell [0801: DATE and TIME, Date/Time].

If the auxiliary supply fails, with a battery fitted in the compartment behind the bottom access cover, the time and date are maintained. Therefore when the auxiliary supply is restored, the time and date are correct and need not be set again.

To test this, remove the auxiliary supply from the relay for approximately 30 seconds. On re-energization, the time in cell [0801: DATE and TIME, Date/Time] should be correct.

5.2.4 Light Emitting Diodes (LEDs)

On power-up, the green LED should switch on and stay on, indicating that the relay is healthy. The relay has non-volatile memory which stores the state (on or off) of the alarm, trip and, if configured to latch, user-programmable LED indicators when the relay was last energized from an auxiliary supply. Therefore, these indicators may also switch on when the auxiliary supply is applied.

If any of these LEDs are on, reset them before proceeding with further testing. If the LED successfully resets (the LED switches off), there is no testing required for that LED because it is known to be operational.

Note	*It is likely that alarms related to the communications channels will not reset at this stage.*

5.2.4.1 Testing the Alarm and Out Of Service LEDs

The alarm and out of service LEDs can be tested using the **COMMISSIONING TESTS** menu column. Set cell [0F0D: COMMISSIONING TESTS, Test Mode] to **Contacts Blocked**. Check that the out of service LED is on continuously and the alarm LED flashes.

It is not necessary to return cell [0F0D: COMMISSIONING TESTS, Test Mode] to **Disabled** at this stage because the test mode will be required for later tests.

5.2.4.2 Testing the Trip LED

The trip LED can be tested by initiating a manual circuit breaker trip from the relay. However, the trip LED will operate during the setting checks performed later. Therefore, no further testing of the trip LED is required at this stage.

5.2.4.3 Testing the User-Programmable LEDs

To test the user-programmable LEDs set cell [0F10: COMMISSIONING TESTS, Test LEDs] to **Apply Test**. Check that all the programmable LEDs on the relay switch on.

5.2.5 Field Voltage Supply

The relay generates a field voltage of nominally 48 V that can be used to energize the opto-isolated inputs (alternatively the substation battery may be used).

Measure the field voltage across terminals 7 and 9 on the terminal block shown in the following table. Check that the field voltage is in the range 40 V to 60 V when no load is connected and that the polarity is correct.

Repeat for terminals 8 and 10

Supply rail	Terminals		
	P642 (40TE)	P643/P645 (60TE)	P645 (80TE)
+ve	F7 & F8	J7 & J8	M7 & M8
-ve	F9 & F10	J9 & J10	M9 & M10

Table 6 - Field voltage terminals

5.2.6 Input Opto-Isolators

This test checks that all the opto-isolated inputs on the relay are functioning correctly.

Model	Opto-Insulated Inputs
P642 (40TE Case)	8 to 12
P643 (60TE Case)	16 to 24
P645 (60TE Case)	16 to 24
P645 (80TE Case)	24

Energize the opto-isolated inputs one at a time; see the external connection diagrams in the *Connection Diagrams* chapter for terminal numbers. Ensure that the correct opto input nominal voltage is set in the **Opto Config**. Menu. Ensure correct polarity and connect the field supply voltage to the appropriate terminals for the input being tested. Each opto input also has selectable filtering. This allows use of a pre-set filter of ½ cycle that renders the input immune to induced noise on the wiring.

Note	*The opto-isolated inputs may be energized from an external dc auxiliary supply (such as the station battery) in some installations. Check that this is not the case before connecting the field voltage, otherwise damage to the relay may result. If an external 24/27 V, 30/34 V, 48/54 V, 110/125 V, 220/250 V supply is being used it will be connected to the relay's optically isolated inputs directly. If an external supply is used it must be energized for this test, but only after confirming that it is suitably rated, with less than 12% ac ripple.*

The status of each opto-isolated input can be viewed using either cell [0020: SYSTEM DATA, Opto I/P Status] or [0F01: COMMISSIONING TESTS, Opto I/P Status], a **1** indicating an energized input and a **0** indicating a de-energized input. When each opto-isolated input is energized, one of the characters on the bottom line of the display changes, to indicate the new state of the inputs.

5.2.7 Output Relays

This test checks that all the output relays are functioning correctly.

Model	Outputs
P642 (40TE Case)	8 to 12
P643 (60TE Case)	16 to 24
P645 (60TE Case)	16 to 24
P645 (80TE Case)	24

Note	*The High-Break contacts are polarity sensitive. External wiring should, wherever possible, be verified against polarity requirements described in the external connection diagram to ensure correct high break operation when in service.*

Ensure that the cell [0F0D: COMMISSIONING TESTS, Test Mode] is set to **Contacts Blocked**.

The output relays should be energized one at a time. To select output relay 1 for testing, set cell [0F0E: COMMISSIONING TESTS, Test Pattern] to 00000000000000000000000000000001.

Connect a continuity tester across the terminals corresponding to output relay 1 as shown in the relevant external connection diagram in the *Connection Diagrams* chapter.

To operate the output relay, set cell [0F0F: COMMISSIONING TESTS, Contact Test] to **Apply Test**. Operation is confirmed by the continuity tester operating for a normally open contact and ceasing to operate for a normally closed contact. Measure the resistance of the contacts in the closed state.

Reset the output relay by setting cell [0F0F: COMMISSIONING TESTS, Contact Test] to **Remove Test**.

Note	*Ensure that the thermal ratings of anything connected to the output relays during the contact test procedure are not exceeded by the associated output relay being operated for too long. Keep the time between application and removal of contact test to a minimum.*

Repeat the test for the rest of the relays (the numbers depend on the model).

Return the relay to service by setting cell [0F0D: COMMISSIONING TESTS, Test Mode] to **Disabled**.

5.2.8 RTD Inputs

This test checks that all the RTD inputs are functioning correctly and is only performed on relays with the RTD board fitted.

A 100 Ω resistor, preferably with a tolerance of 0.1%, should be connected across each RTD in turn. The resistor needs to have a very small tolerance as RTDs complying with BS EN 60751 : 1995 typically have a change of resistance of 0.39 Ω per °C, therefore the use of a precision wire wound or metal film resistor is recommended. It is essential to connect the RTD common return terminal to the appropriate RTD input, otherwise the relay reports an RTD error because it assumes that the RTD wiring has been damaged. The connections required for testing each RTD input are shown in the following table.

Check that the corresponding temperature displayed in the **MEASUREMENTS 3** column of the menu is 0°C ±2°C. This range takes into account the 0.1% resistor tolerance and relay accuracy of ±1°C. If a resistor of lower accuracy is used during testing, the acceptable setting range needs to be increased.

RTD	Terminal connections		Measurement cell (in "Measurements 3" Column (04) of Menu)
	Resistor between	Wire between	
1	B1 and B2	B2 and B3	[0412: RTD 1 Label]
2	B4 and B5	B5 and B6	[0413: RTD 2 Label]
3	B7 and B8	B8 and B9	[0414: RTD 3 Label]
4	B10 and B11	B11 and B12	[0415: RTD 4 Label]
5	B13 and B14	B14 and B15	[0416: RTD 5 Label]
6	B16 and B17	B17 and B18	[0417: RTD 6 Label]
7	B19 and B20	B20 and B21	[0418: RTD 7 Label]
8	B22 and B23	B23 and B24	[0419: RTD 8 Label]
9	B25 and B26	B26 and B27	[041A: RTD 9 Label]
10	B28 and B29	B29 and B30	[041B: RTD 10 Label]

Table 7 - RTD input terminals

5.2.9 Current Loop Inputs

This test checks that all the current loop (analog) inputs are functioning correctly and is only performed on relays with the Current Loop Input Output (CLIO) board fitted.

For details of the relay terminal connections see the connection diagrams in the *Installation* chapter. Note that for the current loop inputs, the physical connection of the 0 to 1 mA input is different to that of the 0 to 10, 0 to 20, and 4 to 20 mA inputs, as shown in the connection diagrams.

An accurate dc current source can be used to apply various current levels to the current loop inputs. Another approach is to use the current loop output as a convenient and flexible dc current source to test the input protection functionality. Externally the current loop outputs can be fed into their corresponding current loop inputs. Then by applying a certain level of analog signal, such as V_A, to the relay the required dc output level can be obtained from the current loop output which is feeding the current loop input.

Enable the current loop input to be tested. Set the CLIx minimum and maximum settings and the CLIx Input type for the application.

Apply a dc current to the relay current loop input at 50% of the CLI input maximum range, 0.5 mA (0 to 1 mA CLI), 5 mA (0 to 10 mA CLI) or 10 mA (0 to 20, 4 to 20 mA CLI).

Check the accuracy of the current loop input using the MEASUREMENTS 3 - CLIO Input 1/2/3/4 column of the menu. The display should show (CLIx maximum + CLIx minimum)/2 ±1% full scale accuracy.

5.2.10 Current Loop Outputs

This test checks that all the current loop (analog) outputs are functioning correctly and is only performed on relays with the CLIO board fitted.

For details of the relay terminal connections, see the connection diagrams in the *Installation* chapter.

Note	*For the current loop outputs the physical connection of the 0 to 1 mA output is different to that of the 0 to 10, 0 to 20, and 4 to 20 mA outputs, as shown in the connection diagrams.*

Enable the current loop output to be tested. Set the CLOx parameter, CLOx minimum and maximum settings and the CLOx output type for the application. Apply the appropriate analog input parameter to the relay equals to (CLOx maximum + CLOx minimum)/2. The current loop output should be at 50% of its maximum rated output. Using a precision resistive current shunt and a high-resolution voltmeter, check that the current loop output is at 50% of its maximum rated output, 0.5 mA (0 to 1 mA CLO), 5 mA (0 to 10 mA CLO) or 10 mA (0 to 20, 4 to 20 mA CLO). The accuracy should be within ±0.5% of full scale + meter accuracy.

5.2.11 First Rear Communications Port

This test should only be performed where the relay is to be accessed from a remote location and varies depending on the communications standard adopted.

It is not the intention of the test to verify the operation of the complete system from the relay to the remote location, just the relay's rear communications port and any protocol converter necessary.

A variety of communications protocols may be available. For further details, please see whichever of these sections are relevant for the device you are commissioning:

5.2.11.1 Courier Communications

If a K-Bus to EIA(RS)232 KITZ protocol converter is installed, connect a portable PC running the appropriate software (such as MiCOM S1 Studio or PAS&T) to the incoming (remote from relay) side of the protocol converter.

If a KITZ protocol converter is not installed, it may not be possible to connect the PC to the relay installed. In this case a KITZ protocol converter and portable PC running appropriate software should be temporarily connected to the relay's first rear K-Bus port. The terminal numbers for the relay's first rear K-Bus port are shown in the following table. However, as the installed protocol converter is not being used in the test, only the correct operation of the relay's K-Bus port will be confirmed.

Connection		Terminal		
K-Bus	**MODBUS, VDEW or DNP3.0**	**P642 (40TE)**	**P643/P645 (60TE)**	**P643/P645 (80TE)**
Screen	Screen	F16	J16	M16
1	+ve	F17	J17	M17
2	-ve	F18	J18	M18

Table 8 - EIA(RS)485 terminals

Ensure that the communications baud rate and parity settings in the application software are set the same as those on the protocol converter (usually a KITZ but could be a SCADA RTU). The relay's Courier address in cell [0E02: COMMUNICATIONS, Remote Address] must be set to a value between 1 and 254.

Check that communications can be established with this relay using the portable PC.

If the relay has the optional fiber optic communications port fitted, the port to be used should be selected by setting cell [0E07: COMMUNICATIONS, Physical Link] to **Fiber Optic**. Ensure that the relay address and baud rate settings in the application software are set the same as those in cell [0E04 COMMUNICATIONS, Baud Rate] of the relay. Check, using the Master Station, that communications with the relay can be established.

5.2.11.2 MODBUS Communications

Connect a portable PC running the appropriate MODBUS Master Station software to the relay's first rear EIA(RS)485 port using an EIA(RS)485 to EIA(RS)232 interface converter. The terminal numbers for the relay's EIA(RS)485 port are shown in the *EIS(RS)485 terminals* table.

Ensure that the relay address, baud rate and parity settings in the application software are set the same as those in cells [0E02: COMMUNICATIONS, Remote Address], [0E04: COMMUNICATIONS, Baud Rate] and [0E05: COMMUNICATIONS, Parity] of the relay.

Check that communications with this relay can be established.

If the relay has the optional fiber optic communications port fitted, the port to be used should be selected by setting cell [0E07: COMMUNICATIONS, Physical Link] to **Fiber Optic**. Ensure that the relay address and baud rate settings in the application software are set the same as those in cell [0E04: COMMUNICATIONS, Baud Rate] of the relay. Check, using the Master Station, that communications with the relay can be established.

5.2.11.3 IEC60870-5-103 (VDEW) Communications

If the relay has the optional fiber optic communications port fitted, the port to be used should be selected by setting cell [0E07: COMMUNICATIONS, Physical Link] to **Fiber Optic** or **EIA(RS)485**.

IEC60870-5-103/VDEW communication systems are designed to have a local Master Station and this should be used to verify that the relay's rear fiber optic or EIA(RS)485 port, as appropriate, is working.

Ensure that the relay address and baud rate settings in the application software are set the same as those in cells [0E02: COMMUNICATIONS, Remote Address] and [0E04: COMMUNICATIONS, Baud Rate] of the relay.

Check, using the Master Station, that communications with the relay can be established.

5.2.11.4 DNP3.0 Communications

Connect a portable PC running the appropriate DNP3.0 Master Station Software to the relay's first rear EIA(RS)485 port using an EIA(RS)485 to EIA(RS)232 interface converter. The terminal numbers for the relay's EIA(RS)485 port are shown in the *EIA(RS)485 terminals* table.

Ensure that the relay address, baud rate and parity settings in the application software are set the same as those in cells [0E02: COMMUNICATIONS, Remote address], [0E04: COMMUNICATIONS, Baud Rate] and [0E05: COMMUNICATIONS, Parity] of the relay.

Check that communications with this relay can be established.

If the relay has the optional fiber optic communications port fitted, the port to be used should be selected by setting cell [0E07: COMMUNICATIONS, Physical Link] to **Fiber Optic**. Ensure that the relay address and baud rate settings in the application software are set the same as those in cell [0E04: COMMUNICATIONS, Baud Rate] of the relay. Check that, using the Master Station, communications with the relay can be established.

5.2.11.5 IEC 61850 COMMUNICATIONS

Connect a portable PC running the appropriate IEC61850 Master Station Software or MMS browser to the relay's Ethernet port (RJ45 or Fiber optic connection). The terminal numbers for the relay's Ethernet port are shown in the following *Signals on the Ethernet connector* table.

Configuration of the relay IP parameters (IP Address, Subnet Mask, Gateway) and SNTP time synchronization parameters (SNTP Server 1, SNTP Server 2) is performed by the IED Configurator tool. If these parameters are not available from an SCL file, they must be configured manually.

If the assigned IP address is duplicated elsewhere on the same network, the remote communications operates in an indeterminate way. However, the relay checks for a conflict on every IP configuration change and at power-up. An alarm is raised if an IP conflict is detected. The relay can be configured to accept data from networks other than the local network by using the **Gateway** setting.

Check that communications with this relay can be established.

To communicate with an IEC 61850 IED on Ethernet, it is necessary only to know its IP address. This can then be configured in either of the following:

- An IEC 61850 client (or master), such as a PACiS computer (MiCOM C264) or HMI
- An MMS browser, with which the full data model can be retrieved from the IED without any previous knowledge

Setting changes such as protection settings are not supported in the current IEC 61850 implementation. Such setting changes are done using MiCOM S1 Studio using the front port serial connection of the relay, or over the Ethernet link if preferred. This is known as tunneling. See the *SCADA Communications* chapter for more information on IEC 61850.

The connector for the Ethernet port is a shielded RJ45. The following shows the signals and pins on the connector:

Pin	Signal name	Signal definition
1	TXP	Transmit (positive)
2	TXN	Transmit (negative)
3	RXP	Receive (positive)
4	-	Not used
5	-	Not used
6	RXN	Receive (negative)
7	-	Not used
8	-	Not used

Table 9 - Signals on the Ethernet connector

5.2.12 Second Rear Communications Port

This test should only be performed where the relay is to be accessed from a remote location and varies depending on the communications standard being adopted.

It is not the intention of the test to verify the operation of the complete system from the relay to the remote location, just the relay's rear communications port and any protocol converter necessary.

A variety of communications protocols may be available. For further details, please see whichever of these sections are relevant for the device you are commissioning:

5.2.12.1 K-Bus Configuration

If a K-Bus to EIA(RS)232 KITZ protocol converter is installed, connect a portable PC running the appropriate software (MiCOM S1 Studio or PAS&T) to the incoming (remote from relay) side of the protocol converter.

If a KITZ protocol converter is not installed, it may not be possible to connect the PC to the relay installed. In this case a KITZ protocol converter and portable PC running appropriate software should be temporarily connected to the relay's second rear communications port configured for K-Bus. The terminal numbers for the relay's K-Bus port are shown in the following table. However, as the installed protocol converter is not being used in the test, only the correct operation of the relay's K-Bus port is confirmed.

Pin*	Connection
4	EIA(RS)485 - 1 (+ ve)
7	EIA(RS)485 - 2 (- ve)
* All other pins unconnected.	

Table 10 - Second rear communications port K-Bus terminals

Ensure that the communications baud rate and parity settings in the application software are set the same as those on the protocol converter (usually a KITZ but could be a SCADA RTU). The relay's Courier address in cell [0E90: COMMUNICATIONS, RP2 Address] must be set to a value between 1 and 254. The second rear communication's port configuration [0E88: COMMUNICATIONS RP2 Port Config.] must be set to K-Bus.

Check that communications can be established with this relay using the portable PC.

5.2.12.2 EIA(RS)485 Configuration

If an EIA(RS)485 to EIA(RS)232 converter (Schneider Electric CK222) is installed, connect a portable PC running the appropriate software (Easergy Studio) to the EIA(RS)232 side of the converter and the second rear communications port of the relay to the EIA(RS)485 side of the converter.

The terminal numbers for the relay's EIA(RS)485 port are shown in the *Second rear communications port EIA(RS)232 terminals* table.

Ensure that the communications baud rate and parity settings in the application software are the same as those in the relay. The relay's Courier address in cell [0E90: COMMUNICATIONS, RP2 Address] must be set to a value between 1 and 254. The second rear communications port's configuration [0E88: COMMUNICATIONS RP2 Port Config.] must be set to EIA(RS)485.

Check that communications can be established with this relay using the portable PC.

5.2.12.3 EIA(RS)232 Configuration

Connect a portable PC running the appropriate software (Easergy Studio) to the rear EIA(RS)232 port of the relay. This port is compliant with EIA(RS)574; the 9-pin version of EIA(RS)232, see www.tiaonline.org.

The second rear communications port connects using the 9-way female D-type connector (SK4). The connection is compliant with EIA(RS)574.

Pin	Connection
1	No Connection
2	RxD
3	TxD
4	DTR#
5	Ground
6	No Connection
7	RTS#
8	CTS#
9	No Connection
# These pins are control lines for use with a modem.	

Table 11 - Second rear communications port EIA(RS)232 terminals

Connections to the second rear port configured for EIA(RS)232 operation can be made using a screened multi-core communication cable up to 15 m long, or a total capacitance of 2500 pF. Terminate the cable at the relay end with a 9-way, metal-shelled, D-type male plug. The terminal numbers for the relay's EIA(RS)232 port are shown in the previous table.

Ensure that the communications baud rate and parity settings in the application software are set the same as those in the relay. The relay's Courier address in cell [0E90: COMMUNICATIONS, RP2 Address] must be set to a value between 1 and 254. The second rear communication's port configuration [0E88: COMMUNICATIONS RP2 Port Config] must be set to EIA(RS)232.

Check that communications can be established with this relay using the portable PC.

5.2.13 Current Inputs

This test verifies that the accuracy of current measurement is within acceptable tolerances.

All relays leave the factory set for operation at a system frequency of 50 Hz. If operation at 60 Hz is required, this must be set in cell [0009: SYSTEM DATA, Frequency].

Caution	***To avoid spurious operation of protection elements during injection testing, ensure that current operated elements are disabled.***

Apply current equal to the line current transformer secondary winding rating to each current transformer input of the corresponding rating in turn, checking its magnitude using a multimeter. Refer to the *Current input terminals* table for the corresponding reading in the relay's **MEASUREMENTS 1** columns, as appropriate, and record the value displayed.

The measured current values displayed on the relay LCD, or on a portable PC connected to the front communication port, are either in primary or secondary Amperes. If cell [0D02: MEASURE'T SETUP, Local Values] is set to **Primary**, the values displayed should be equal to the applied current multiplied by the corresponding current transformer ratio set in the **CT and VT RATIOS** menu column (see the *CT ratio settings* table). If cell [0D02: MEASURE'T SETUP, Local Values] is set to **Secondary**, the value displayed should be equal to the applied current.

Note	*In the case of a P841B (dual CT inputs), the "measured" value is taken from a combination of the two sets of CTs connected. The check should be performed by first injecting only into the CTs associated with CB1 (IA, IB, IC) and checking the measured IA, IB, and IC values, and then by injecting only into the CTs associated with CB2 (IA2, IB2, IC2) and checking the measured IA, IB, and IC values.*

MEASUREMENTS 1 Menu cell	P642 (40TE)	P643 (60TE)	P645 (60TE)	P645 (80TE)
	Apply current to			
	1A/5A CTs	1A/5A CTs	1A/5A CTs	1A/5A CTs
[0201: IA1 Magnitude]	C24-C23	C24-C23	C24-C23	D24-D23
[0203: IB1 Magnitude]	C26-C25	C26-C25	C26-C25	D26-D25
[0205: IC1 Magnitude]	C28-C27	C28-C27	C28-C27	D28-D27
[0207: IA2 Magnitude]	C18-C17	C18-C17	C18-C17	D18-D17
[0209: IB2 Magnitude]	C20-C19	C20-C19	C20-C19	D20-D19
[020B: IC2 Magnitude]	C22-C21	C22-C21	C22-C21	D22-D21
[020D: IA3 Magnitude]		E24-E23	E24-E23	F24-F23
[020F: IB3 Magnitude]		E26-E25	E26-E25	F26-F25
[0211: IC3 Magnitude]		E28-E27	E28-E27	F28-F27
[0213: IA4 Magnitude]			E18-E17	F18-F17
[0215: IB4 Magnitude]			E20-E19	F20-F19
[0217: IC4 Magnitude]			E22-E21	F22-F21
[0219: IA5 Magnitude]			E12-E11	F12-F11
[021B: IB5 Magnitude]			E14-E13	F14-F13
[021D: IC5 Magnitude]			E16-E15	F16-F15
[0265: IN-HV Measured Magnitude]	C16-C15			D16-D15
[026C: IN-LV Measured Magnitude]	C14-C13			D14-D13
[0273: IN-TV Measured Magnitude]				D12-D11

Table 12 - Current input terminals

Note	*If a PC connected to the relay's rear communications port is used to display the measured current, the process is similar. However, the setting of cell [0D03: MEASURE'T SETUP, Remote Values] determines whether the displayed values are in primary or secondary Amperes.*

The measurement accuracy of the relay is ±1% (5% for P741/P742/P743/P746). However, an additional allowance must be made for the accuracy of the test equipment being used.

Next check that all three-phase CTs associated with one winding are of the same polarity, the same current should be applied to phases A, B, and C - phase displaced as for a balanced 3-phase set. This is for phase angles ∠A = 0°, ∠B = -120°, ∠C = 120°, for a standard ABC phase rotation system. Starting from current bias input 1, apply the balanced current and check the measured residual current in the cell [IN-HV Deriv Mag], [IN-LV Deriv Mag], or [IN-TV Deriv Mag] depending on the transformer winding to which the current input is assigned. The residual current measured should be less than 0.05 p.u. If high residual current is measured, one or more of the CT circuits for the end concerned may have a problem (for example, an inverted connection). Repeat the same test on the rest of the current bias inputs.

	P64x
Menu cell	**Corresponding CT ratio (in VT and CT RATIO column (0A) of menu)**
[0201: IA1 Magnitude] [0203: IB1 Magnitude] [0205: IC1 Magnitude]	[0A12: Phase CT Primary] [0A13: Phase CT Secondary]
[0207: IA2 Magnitude] [0209: IB2 Magnitude] [020B: IC2 Magnitude]	[0A16: Phase CT Primary] [0A17: Phase CT Sec'y]
[020D: IA3 Magnitude] [020F: IB3 Magnitude] [0211: IC3 Magnitude]	[0A1A: Phase CT Primary] [0A1B: Phase CT Sec'y]
[0213: IA4 Magnitude] [0215: IB4 Magnitude] [0217: IC4 Magnitude]	[0A1E: Phase CT Primary] [0A1F: Phase CT Sec'y]
[0219: IA5 Magnitude] [021B: IB5 Magnitude] [021D: IC5 Magnitude]	[0A22: Phase CT Primary] [0A23: Phase CT Sec'y]
[0265: IN-HV Measured Magnitude]	[0A5A: E/F CT Primary] [0A5B: E/F CT Secondary]
[026C: IN-LV Measured Magnitude]	[0A5F: E/F CT Primary] [0A60: E/F CT Secondary]
[0273: IN-TV Measured Magnitude]	[0A64: E/F CT Primary] [0A65: E/F CT Secondary]

Table 13 - CT ratio settings

5.2.14 Voltage Inputs

This test verifies that the accuracy of voltage measurement is within the acceptable tolerances.

The following tests will be realized with the VT Connecting Mode set to 3 VT which is the most used configuration.

Apply rated voltage to each voltage transformer input in turn, checking its magnitude using a multimeter. Refer to the *Voltage Input Terminals* table for the corresponding reading in the relay's **MEASUREMENTS 1** column and record the value displayed.

	Voltage applied to		
Cell in Measurements 1 Column (02)	**P642 40TE**	**P643 60TE**	**P645 60TE/80TE**
[028F: VAN Magnitude]		D2-D1	D2-D1
[0291: VBN Magnitude]		D4-D3	D4-D3
[0293: Magnitude]		F2-F1	F2-F1
[0295: VX Measured Mag]		F4-F3	F4-F3
[0295]: VX Measured Mag] [029C]: VAB Measured Mag]	C4-C3		
[029E]: VBC Measured Mag]	C2-C1		
* Voltage reference for synchrocheck			

Table 14 - Voltage input terminals

The measured voltage values displayed on the relay LCD or a portable PC connected to the front communication port are either in primary or secondary volts. If cell [0D02: MEASURE'T SETUP, Local Values] is set to **Primary**, the values displayed should be equal to the applied voltage multiplied by the corresponding voltage transformer ratio set in the **VT and CT RATIOS** menu column (see the following *VT ratio settings* table). If cell [0D02: MEASURE'T SETUP, Local Values] is set to **Secondary**, the value displayed should be equal to the applied voltage.

Note	*If a PC connected to the relay's rear communications port is used to display the measured voltage, the process is similar. However, the setting of cell [0D03: MEASURE'T SETUP, Remote Values] determines whether the displayed values are in primary or secondary volts.*

The measurement accuracy of the relay is ±1%. However, an additional allowance must be made for the accuracy of the test equipment being used.

Cell in Measurements 1 column (02)	**Corresponding CT ratio (in 'CT and VT RATIOS' column (0A) of menu)**
	P64x
[021A: VAN Magnitude] [021C: VBN Magnitude] [021E: VCN Magnitude]	$\frac{\text{[0A03 : Main VT Primary]}}{\text{[0A04 : Main VT Secondary]}}$
[0220: VX Measured Mag]	$\frac{\text{[0A07 : Vx VT Primary]}}{\text{[0A08 : Vx VT Secondary]}}$

Table 15 - VT ratio settings

5.3 IEDs which use the Process Bus Interface

5.3.1 IED Configured with One Merging Unit (MU)

The settings for the Process Bus interface are in the IED menu ***IED Config***. See the Settings chapter.

1. If necessary, isolate or block any outgoing trips from the IED. If physical contacts from the IED are wired in the scheme, in ***COMMISSION TESTS*** menu, set ***Test Mode*** to *Contacts Blocked* if operation of the contacts is not desired. If GOOSE outputs are used, from the main IED menu COMMISIONING TEST column select ***Test Mode***.
2. Connect the IEDs Ethernet port on the Process Bus board to the Sampled Value source. If necessary this can be routed through an Ethernet switch.
3. Make a valid SV configuration (a CID file via **IED Configurator**) and download it to relay and activate the configuration bank.
4. Check that the MU configuration in the CID file matches the actual Sampled Value source (test kit or Merging Unit). Make any changes in the source Sampled Value configuration. This prevents mismatches in Sampled Value when the IED is put into service when testing existing schemes.
5. Set the IED ***Synchro Mode*** to *No SYNC CLK* so the IED accepts Sampled Value frames with or without synchronization.
6. Generate Sampled Value frames with the rated current and voltage as required in the IED's Sampled Value configuration.
7. In the ***MEASUREMENTS*** menu, check the magnitudes and phase angles are displayed correctly. The display may be in primary or secondary values. Also, the IED's CT ratio or VT ratio settings affect the display. A typical accuracy of 1% can be expected for magnitudes.
8. Change the SV configuration configured in the test kit or Merging Unit to mismatch the Sampled Value configuration of the relay. Check the data cell ***SV Absence Alm*** displays '*******1' (where * is a don't care state for this test, normally its value is 0) for the Merging Unit configured in the CID. Check that all ***MEASUREMENTS*** displays for voltage or current are zero.
9. Depending on the scheme, if Merging Unit is configured to publish SV in IEC61869 format, set ***SMV Version*** to *IEC61869*, if Merging Unit is configured to publish SV in IEC61850-9-2LE compatible format, set ***SMV Version*** to *IEC61850-9-2LE*.

5.3.2 IED Configured with Two or More Merging Units (MUs)

The settings for the IEC61850-9-2LE or IEC61869 interface are in the IED menu ***PB CONFIG***.

1. If necessary, isolate or block any outgoing trips from the IED. If physical contacts from the IED are wired in the scheme, in ***COMMISSION TESTS*** menu, set ***Test Mode*** to *Contacts Blocked* if operation of the contacts is not desired. If GOOSE outputs are used, from the main IED menu COMMISIONING TEST column select ***Test Mode***.
2. Connect the IEDs Ethernet port on Process Bus board to an Ethernet switch, which is connected to the Sampled Value sources. If necessary this can be routed through an Ethernet switch.
3. Make a valid SV configuration (a CID file via **IED Configurator**) and download it to relay and activate the configuration bank.
4. Check that the MU configuration in the CID file matches the actual Sampled Value source (test kit or Merging Unit). Make any changes in the source Sampled Value configuration. This prevents mismatches in Sampled Value when the IED is put into service when testing existing schemes.
5. Set the IED Synchro Alarm to 'Local Clock' so the IED accepts Sampled Value frames with local or global synchronization.
6. Check that the Sampled Value source (test kit or Merging Unit) is GPS synchronized.
7. Check the receipt of Sampled Value frames one by one for each Logical Node configured in the IED.

Repeat the following steps for each Merging Unit, configuring them one by one in the Sampled Value source(s).

1. Generate Sampled Value frames with the rated current and voltage as required in the IED's Logical Node configuration. You can check the receipt of Sampled Value frames for the configured Logical Node.
2. In the ***MEASUREMENTS*** menu, check the magnitudes and phase angles are displayed correctly. The display may be in primary or secondary values. Also, the IED's CT ratio or VT ratio settings affect the display. A typical accuracy of 1% can be expected for magnitudes.
3. Change the SV configuration configured in the test kit or Merging Unit to mismatch the Sampled Value configuration of the relay. Check the data cell ***SV Absence Alm*** displays '00000001' (where * is a don't care state for this test, normally its value is 0) for the first Merging Unit configured in the CID, or '******1*' (where * is a don't care state for this test, normally its value is 0) for the second Merging Unit configured in the CID. Check that all ***MEASUREMENTS*** displays for voltage or current are zero.

6 SETTING CHECKS

The setting checks ensure that all of the application-specific relay settings (both the relay's function and Programmable Scheme Logic (PSL) settings) for the particular installation have been correctly applied to the relay.

Important	***If the application-specific settings are not available, ignore sections 6.1 and 6.2.***

Caution	**The trip circuit should remain isolated during these checks to prevent accidental operation of the associated circuit breaker.**

6.1 Apply Application-Specific Settings

There are different methods of applying the settings:

- Transferring settings from a pre-prepared setting file to the relay using a laptop PC running the appropriate software (such as Easergy Studio). Use the front EIA(RS)232 port (under the bottom access cover), or the first rear communications port (Courier protocol with a protocol converter connected), or the second rear communications port. This is the preferred method for transferring function settings as it is much faster and there is less margin for error. If PSL other than the default settings with which the relay is supplied is used, this is the only way of changing the settings.

  If a setting file has been created for the particular application and provided on a memory device, the commissioning time is further reduced, especially if application-specific PSL is applied to the relay.
- Enter the settings manually using the relay's operator interface. This method is not suitable for changing the PSL.

Caution	***When the installation needs application-specific Programmable Scheme Logic (PSL), it is essential that the appropriate .psl file is downloaded (sent) to the relay, for each setting group that will be used. If the user fails to download the required .psl file to any setting group that may be brought into service, the factory default PSL will still be resident. This may have severe operational and safety consequences.***

6.2 Check Application-Specific Settings

Carefully check applied settings against the required application-specific settings to ensure they have been entered correctly. However, this is not considered essential if a customer-prepared setting file on a memory device has been transferred to the relay using a portable PC.

There are two methods of checking the settings:

- Extract the settings from the relay using a portable PC running the appropriate software (Easergy Studio) using the front EIA(RS)232 port, under the bottom access cover, or the first rear communications port (Courier protocol with a KITZ protocol converter connected), or the second rear communications port. Compare the settings transferred from the relay with the original written application-specific setting record (for cases where the customer has only provided a printed copy of the required settings but a portable PC is available).
- Step through the settings using the relay's operator interface and compare them with the original application-specific setting record.

Unless previously agreed to the contrary, the application-specific PSL is not checked as part of the commissioning tests.

Due to the versatility and possible complexity of the PSL, it is beyond the scope of these commissioning instructions to detail suitable test procedures. Therefore, when PSL tests must be performed, written tests that satisfactorily demonstrate the correct operation of the application-specific scheme logic should be devised by the engineer who created it. These tests should be provided to the Commissioning Engineer with the memory device containing the PSL setting file.

6.3 Demonstrate Correct Relay Operation

The purpose of these tests is as follows:

- To determine that the primary protection function of the relay, current differential, can trip according to the correct application settings.
- To verify correct setting of any backup phase/phase overcurrent protection.
- To verify correct assignment of the inputs, relays and trip contacts, by monitoring the response to a selection of fault injections.

6.4 Transformer Differential Protection (P642/P643/P645)

To avoid spurious operation of any other protection elements, all protection elements except the transformer differential protection should be disabled for the duration of the differential element tests. This is done in the relay's **CONFIGURATION** column. Make a note of which elements need to be re-enabled after testing.

The P642/P643/P645 transformer differential protection has three elements, one for each phase. The biased differential protection uses the maximum bias current in the three phases to bias the elements. The detailed bias characteristic is described in the *Operation* chapter *P64x/EN OP.*

6.4.1 Low Set Element Current Sensitivity (Is1)

Connect the equipment so that current can be injected through terminals D24 and D23. Slowly increase the current from 0 Amps and note the pick-up value at which the relay operates. Reduce the current slowly and note the drop-off value at which it resets. Check that the pick-up and drop-off are within the range shown in the *Low set element pick-up and drop-off* table below.

In the *Low set element pick-up and drop-off* table, $I = \frac{I_{s1}}{amplitude \;\; matching \;\; factor}$

Is1 is the low set setting which will be found in the cell [Is1] under the **GROUP 1 DIFF PROTECTION** menu heading. The amplitude matching factor is used to compensate for a mismatch in currents due to the line side current transformer ratios. There is one amplitude matching factor for the HV side, which is in the cell [Match Factor HV], one for the LV side found in the cell [Match Factor LV], and one for the TV side found in the cell [Match Factor TV]. These are under the **GROUP 1 SYSTEM CONFIG** menu heading. Use the appropriate amplitude matching factor to calculate the current to inject: this depends on whether it is being injected into the HV, LV, or TV current transformer inputs.

	Current level
Pick-up	0.90 x I to 1.1 x I
Drop-off	0.90 x pick-up to 1 x pick-up

Table 16 - Low set element pick-up and drop-off

Repeat the above test for each of the remaining phases on the HV side, and for all three phases on the LV and TV sides. These are shown in the *Characteristic operating times for Overcurrent1 I>1, Overcurrent2 I> and Overcurrent I>* table.

As the CT inputs to each phase have been verified by both the measurement checks and the low set differential trip checks, it is only necessary to check the operating time and the high set current sensitivity for each phase element on one side of the transformer only.

6.4.2 Low Set Element Operating Time

Connect the relay so that current can be injected through terminals D24 and D23, but in addition connect the relay contacts for this protection function to both trip the test set and to stop a timer. Configure the test set so that when the current is applied to the relay, the timer starts.

Inject 5 x I into the HV side A phase (terminals D24 & D23). Check that the operating time for the relay is within the range 30 ms to 35 ms. Repeat this test for both the remaining phases on the HV side, as shown in the *Current Input Terminals* table.

6.4.3 High Set Element Current Sensitivity (Is HS1)

Caution	***The relay may be damaged by applying excessive current for long durations during testing, or in recurrent bursts without allowing time for the relay to cool down.***

This test checks the instantaneous current sensitivity of the differential high set element. This test can only be performed if the test set can inject sufficient current into the relay to cause the element to trip at the calculated application setting.

The relay should be connected so that current can be injected through terminals D24 and D23. Also the output relay configured as Idiff HS1 Trip A (DDB 903) should be connected to trip the test set and to stop a timer.

Caution	***It is important to trip the test set to avoid sustained application of excessive currents.***

It is recommended that the low set differential is still enabled during this test. The timer should be started when the current is applied to the relay. As the setting is above the continuous current rating of the relay, DO NOT INCREASE THE CURRENT SLOWLY, since this may damage the relay before it can operate. Instead, set the current level then suddenly apply it. Two tests have to be performed for this particular protection function. These are shown in the following table:

Is HS1 (Trip)	Is HS1 (No Trip)
1.1 x I	0.90 x I

The first test to be performed is at the higher current level, to check that the instantaneous element operates.

In the above table, $I = \dfrac{Is \;\; HS1}{amplitude \;\; matching \;\; factor}$

Is HS1 is the high set setting which is in the cell [Is HS1] under the **GROUP 1 DIFF PROTECTION** menu heading. The amplitude matching factor is used to compensate for a mismatch in currents due to the line side current transformer ratios. This is found in the cell [Match Factor HV] under the **GROUP 1 SYSTEM CONFIG** menu heading.

Inject 1.1 x I and ensure that the selected output relay operates.

Caution	***For the second test it is important that the current is not applied for longer than one second.***

Inject 0.9 x I for one second and ensure that the selected output relay does not operate. Repeat the above two tests for the two remaining elements of the HV side of the transformer as shown in the *Current Input Terminals* table.

Table 17 - High set element sensitivity

6.4.4 High Set Element Operating Time

This test can only be performed if the test set can inject sufficient current into the relay to cause the element to trip at the calculated application setting. Connect the relay so that current can be injected through terminals D24 and D23, but in addition connect the relay contacts for this protection function to both trip the test set and to stop a timer. Configure the test set so that when the current is applied to the relay, the timer starts. Inject 3 x I into the HV side A phase terminals D24 and D23. Check that the operating time for the relay is within the range 10 ms to 15 ms.

Repeat this test for both of the remaining phases on the HV side, as shown in the *Current Input Terminals* table.

6.4.5 Differential through Fault Stability by Primary Injection

To check for through fault stability, it is preferable, especially for a new transformer installation to simulate a through-fed external fault, by a real primary fault simulation. This is achieved by placing a three-phase bolted short circuit on the downstream side of the LV CTs, and energizing the HV winding from a three-phase medium voltage supply. Typically, the HV winding is energized only from a voltage rated in the range 400 to 440 V, to limit the through fault current. In such a through fault situation, the relay should not trip.

Note	*The procedure for primary testing is not covered here, as it must respect utility safety rules, permits to work, and sanctions for testing.*

6.4.6 CT Secondary Wiring Differential through Fault Stability Test by Secondary Injection

Secondary injection can be used to verify settings. For a two-winding transformer, a fault current flowing out of the LV side is simulated, with a balancing set of currents on one or two phases flowing into the HV side. If all settings and CT orientations are correct, no trip should occur, and minimal differential current are measured by the relay.

For a relay with more than two bias inputs (P643 and P645 models), the external fault injection must be repeated for each additional set of CT inputs. For example, when a P643 is used to protect a three-winding transformer, there should be an injection for a through-fed fault Terminal 1 CT to Terminal 2 CT, then afterwards for Terminal 1 CT to Terminal 3 CT. When using a P643 to protect a two-winding transformer or a P645, it should be checked in [HV CT Terminals], [LV CT Terminals] and [TV CT Terminals] under the **GROUP 1 SYSTEM CONFIG** menu heading which CT inputs are configured to each transformer winding. The injection of through-fed faults is between CTs assigned to different transformer windings.

Caution	**During these tests, disable all the current operated protection functions except the differential protection. Make a note of all the functions that must be enabled after the testing is completed.**

6.4.6.1 Yy Transformers and Autotransformer

This test simulates current flowing through the transformer to an external fault.

Consider a two-winding transformer application, and that Terminal 1 CT (D23, D24) is assigned to the HV winding and Terminal 5 CT (F11, F12) is assigned to the LV winding. A fault current is injected, flowing out of phase A at Terminal 5 CT. The same zero sequence filtering setting is applied for the HV and LV windings; therefore, if the current simulated is 1 pu out of Terminal 5 CT, the input current to balance at Terminal 1 CT is also 1 pu.

Connect the test equipment as shown below for a Yy0 transformer connection:

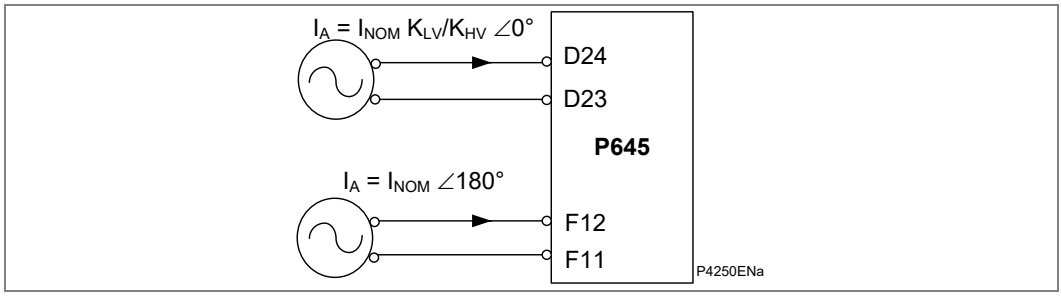


Figure 3 - Test equipment connection for a Yy0 transformer

A single phase current equal to the CT secondary rating (1 A or 5 A) is simulated to flow OUT on phase A, Terminal 5 CT. On an automatic test set, use I_{NOM} ∠180º.

To balance, a current is applied to one phase input at the HV CT connections (for P34x) or at Terminal 1 CT (for P64x). The magnitude should be a current equal to (K_{LV} / K_{HV}) x I_{NOM}, and at a phase angle shown in the *Injected current for Yy ends* table:

	Terminal 5 CT injected phase	LV current terminal 5 CT	Terminal 1 CT injected phase	HV current terminal 1 CT
Yy0, Autotransformer	A	I_{NOM} ∠180º	A	I_{NOM} . K_{LV} / K_{HV} ∠0º
Yy2	A	I_{NOM} ∠180º	C	I_{NOM} . K_{LV} / K_{HV} ∠180º
Yy4	A	I_{NOM} ∠180º	B	I_{NOM} . K_{LV} / K_{HV} ∠0º
Yy6	A	I_{NOM} ∠180º	A	I_{NOM} . K_{LV} / K_{HV} ∠180º
Yy8	A	I_{NOM} ∠180º	C	I_{NOM} . K_{LV} / K_{HV} ∠0º
Yy10	A	I_{NOM} ∠180º	B	I_{NOM} . K_{LV} / K_{HV} ∠180º

Table 18 - Injected current for Yy ends

The amplitude matching factors K_{HV} and K_{LV} can be found in [Match Factor HV] and [Match Factor LV] respectively under the **GROUP 1 SYSTEM CONFIG** menu heading.

Apply the fault currents for approximately one second.

- If end Terminal 1 CT and Terminal 5 CT are in the correct orientation no trip should occur.

It is important to read the displayed differential currents [IA Differential], [IB Differential] and [IC Differential] under **MEASUREMENT 3** menu heading to check that these measurements are low.

These measurements must show less than 0.1 pu (10%), to prove that a balance is achieved.

The reason that the differential currents must be read is that in certain busbar applications the Idiff> trip threshold may be set *higher* than I_{nom}, so that even an incorrect CT connection would not cause a trip.

It is not necessary to repeat the injection for other phases, because their orientation has already been checked in the *Current Inputs* section.

Figure 4 shows the transformer connections for the configurations shown in Table 18.

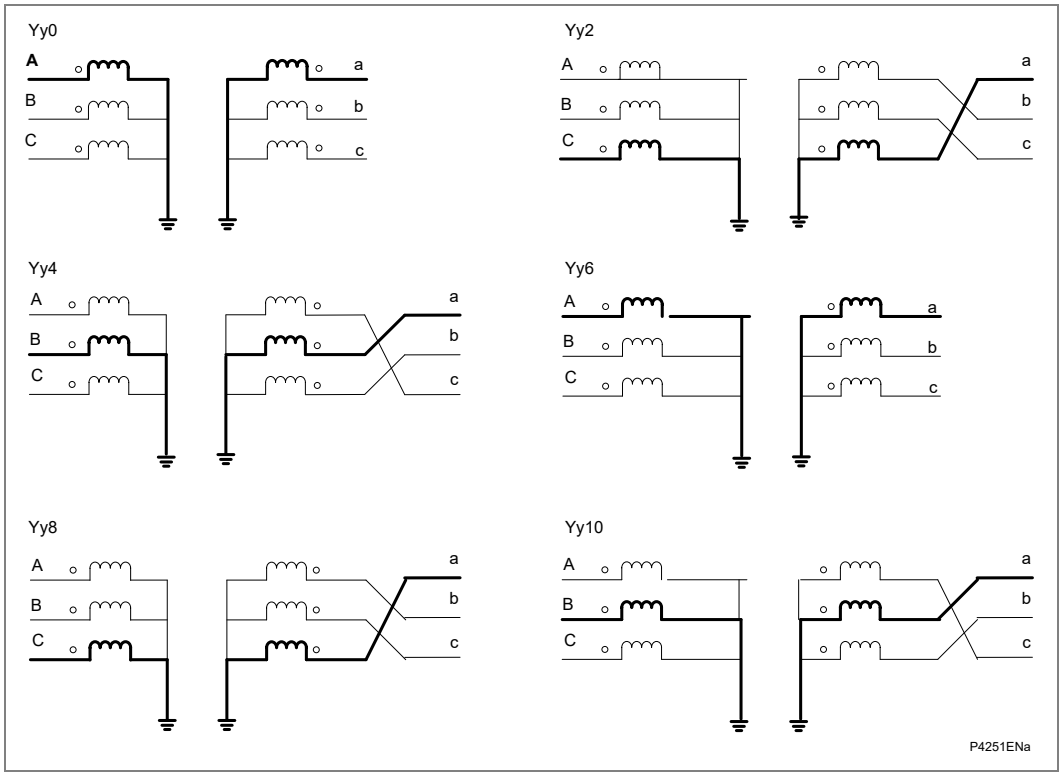


Figure 4 - Yy transformer connections

6.4.6.2 Dy and Yd Applications

This test simulates current flowing through the transformer to an external fault.

A fault current flowing out of the A phase on whichever winding is the star (wye) end is injected. For a Dy configuration it is the LV side, for a Yd configuration it is the HV side. The star winding phase A shares the same power transformer limb as two phases on the opposite side, so that a two-phase current loop needs to be injected to achieve a balance.

For ease of injection, a single phase current equal to the CT secondary rating (1 A or 5 A) is simulated to flow OUT on phase A of the wye end. On an automatic test set, use $I_{NOM} \angle 180^{o}$. To balance, a current is applied to two phase CT inputs (delta side).
The following *Injected current for delta-star ends* table shows the currents to be injected. The magnitude should be a current equal to
$[K_{wye} / (\sqrt{3}.K_{delta})] \times I_{NOM}$, and at the phase angles as shown in this table:

	Star end injected phase	Current (Star)	Delta side injected loop	Current
Dy1 or Yd11	A	$I_{NOM} \angle 180^o$	A-C	$I_A = I_{NOM} . K_{WYE} / \sqrt{3} K_{DELTA} \angle 0^o$ $I_C = I_{NOM} . K_{WYE} / \sqrt{3} K_{DELTA} \angle 180^o$
Dy3 or Yd9	A	$I_{NOM} \angle 180^o$	C-B	$I_C = I_{NOM} . K_{WYE} / \sqrt{3} K_{DELTA} \angle 0^o$ $I_B = I_{NOM} . K_{WYE} / \sqrt{3} K_{DELTA} \angle 180^o$
Dy5 or Yd7	A	$I_{NOM} \angle 180^o$	A-B	$I_A = I_{NOM} . K_{WYE} / \sqrt{3} K_{DELTA} \angle 0^o$ $I_B = I_{NOM} . K_{WYE} / \sqrt{3} K_{DELTA} \angle 180^o$
Dy7 or Yd5	A	$I_{NOM} \angle 180^o$	A-C	$I_A = I_{NOM} . K_{WYE} / \sqrt{3} K_{DELTA} \angle 0^o$ $I_C = I_{NOM} . K_{WYE} / \sqrt{3} K_{DELTA} \angle 180^o$
Dy9 or Yd3	A	$I_{NOM} \angle 180^o$	B-C	$I_B = I_{NOM} . K_{WYE} / \sqrt{3} K_{DELTA} \angle 0^o$ $I_C = I_{NOM} . K_{WYE} / \sqrt{3} K_{DELTA} \angle 180^o$
Dy11 or Yd1	A	$I_{NOM} \angle 180^o$	A-B	$I_A = I_{NOM} . K_{WYE} / \sqrt{3} K_{DELTA} \angle 0^o$ $I_B = I_{NOM} . K_{WYE} / \sqrt{3} K_{DELTA} \angle 180^o$

Table 19 - Injected current for delta-star ends

For a Yd1 configuration, connect the test equipment as shown in the following *Test equipment connection for a Yd1 transformer* diagram.

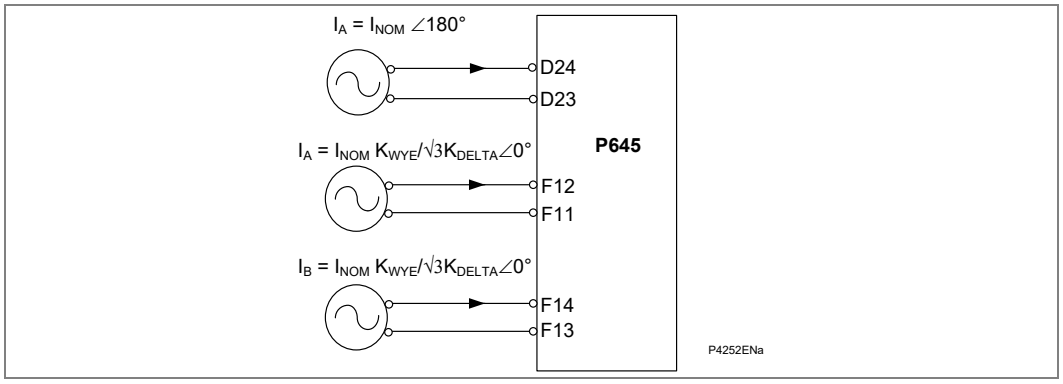


Figure 5 - Test equipment connection for a Yd1 transformer

The amplitude matching factors K_{wye} and K_{delta} can be found in [Match Factor HV] and [Match Factor LV] under the **GROUP 1 SYSTEM CONFIG** menu heading

The delta side loop current may be applied as two separate current outputs from a test set, or one current looped out through the first phase specified, and returning back through the latter phase input.

Apply the fault currents for approximately one second.

- If end Terminal 1 CT and Terminal 5 CT are in the correct orientation no trip should occur.

It is important to read the displayed differential currents [IA Differential], [IB Differential] and [IC Differential] under the **MEASUREMENT 3** menu heading to check that these measurements are low. These measurements must show less than 0.1 p.u. (10%), to prove that a balance is achieved.

It is not necessary to repeat the injection for other phases, because their orientation has already been checked in the *Current Inputs* section.

Figure 6 shows a Yd9 transformer with the current distribution for an AN external fault on the Y side of the transformer. During the test shown in Figure 5, the following current distribution occurs in the P64x.

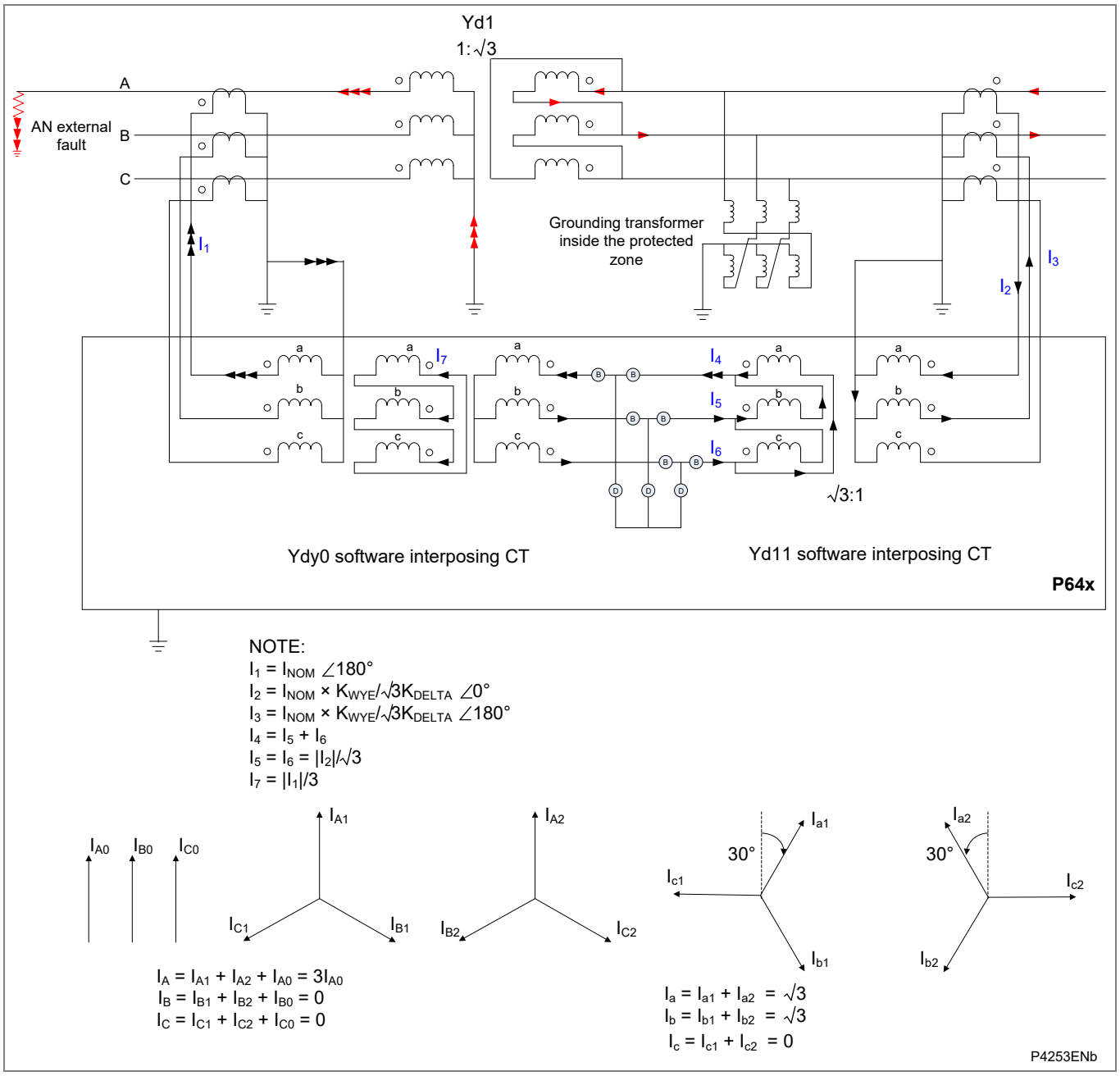
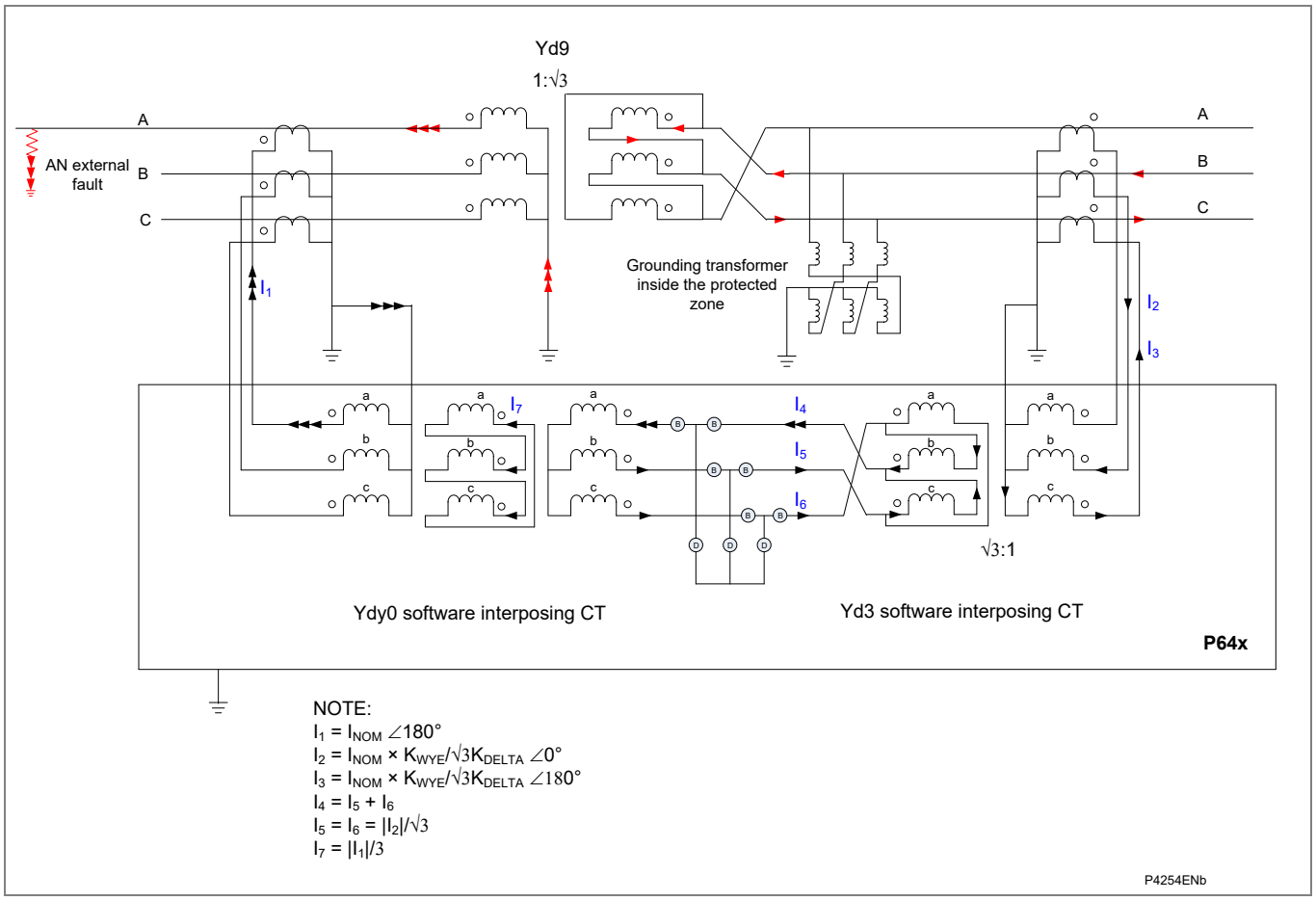


Figure 6 - Yd9 configuration AN external fault current distribution

Figure 7 shows the transformer connections for the configurations shown in Table 19.



NOTE:
$I_1 = I_{NOM} \angle 180°$
$I_2 = I_{NOM} \times K_{WYE}/\sqrt{3}K_{DELTA} \angle 0°$
$I_3 = I_{NOM} \times K_{WYE}/\sqrt{3}K_{DELTA} \angle 180°$
$I_4 = I_5 + I_6$
$I_5 = I_6 = |I_2|/\sqrt{3}$
$I_7 = |I_1|/3$

Figure 7 - Yd transformer connections

6.4.6.3 Dd Applications

This test simulates current flowing through the transformer to an external fault.

In many such applications, there may be in-zone earthing transformers, so it is easier to simulate an external phase-phase fault, to avoid simulating a zero sequence current.

If Terminal 1 CT is assigned to the HV end and Terminal 5 CT to the LV end, and the current simulated is 1 pu out of Terminal 5 CT, the input current to balance at Terminal 1 CT is easy to determine.

In the simplest application of a Dd0 transformer, an A-B fault is simulated flowing out of the LV side, fed by an A-B loop input on the HV side.

For ease of injection, a loop current equal to the CT secondary rating (1 A or 5 A) is simulated to flow OUT on phase A, Terminal 5 CT, and looping back through phase B, Terminal 5 CT. On an automatic test set, use $I_{NOM} \angle 180^{o}$. Because four-phase CT inputs to the relay are energized at once, it is necessary that the test set output current for this LV side is set as a single phase but looping through two phase CT inputs.

To balance, a loop current is applied at Terminal 1 CT (the HV winding). The magnitude should be a current equal to $(K_{LV}/K_{HV}) \times I_{NOM}$, and at a phase angle as shown below. The test set is configured to generate only one single phase output for this winding, looped through two phase CT inputs. Therefore in total, the output requirements can be satisfied by a test set typically having only up to three current outputs.

	Terminal 5 CT injected phase	LV current terminal 5 CT	Terminal 1 CT injected phase	HV current terminal 1 CT
Dd0	A-B	$I_{NOM} \angle 180^o$	A-B	$I_{NOM} . K_{LV} / K_{HV} \angle 0^o$
Dd2	A-B	$I_{NOM} \angle 180^o$	C-B	$I_{NOM} . K_{LV} / K_{HV} \angle 0^o$
Dd4	A-B	$I_{NOM} \angle 180^o$	C-A	$I_{NOM} . K_{LV} / K_{HV} \angle 0^o$
Dd6	A-B	$I_{NOM} \angle 180^o$	B-A	$I_{NOM} . K_{LV} / K_{HV} \angle 0^o$
Dd8	A-B	$I_{NOM} \angle 180^o$	B-C	$I_{NOM} . K_{LV} / K_{HV} \angle 0^o$
Dd10	A-B	$I_{NOM} \angle 180^o$	A-C	$I_{NOM} . K_{LV} / K_{HV} \angle 0^o$

Table 20 - Current injected for Dd ends

The amplitude matching factors K_{HV} and K_{LV} can be found in [Match Factor HV] and [Match Factor LV] respectively under the GROUP 1 SYSTEM CONFIG menu heading.

For the Dd0 configuration, connect the test equipment as shown in the *Test equipment connection for a Dd0 transformer* diagram below.

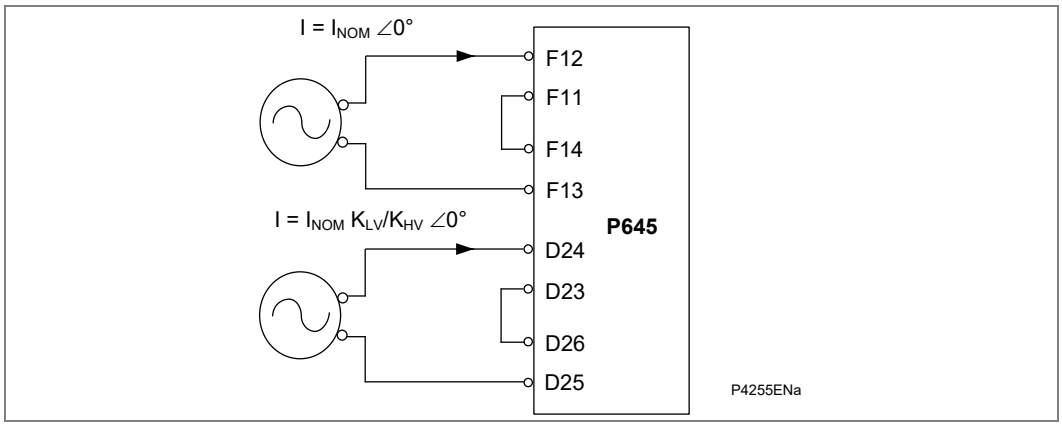


Figure 8 - Test equipment connection for a Dd0 transformer

Apply the fault currents for approximately one second. If end HV CT / Terminal 1 CT and LV CT / Terminal 5 CT are in the correct orientation no trip should occur. It is important to read the displayed differential currents [IA Differential], [IB Differential] and [IC Differential] under the **MEASUREMENT 3** (for P34x) or **MEASUREMENT 2** (for P64x) menu heading to check that these measurements are low. These measurements must show less than 0.1 p.u. (10%), to prove that a balance is achieved.

It is not necessary to repeat the injection for other phases, because their orientation has already been checked in the Current Inputs section.

Figure 9 shows the transformer connections for the configurations shown in Table 20.

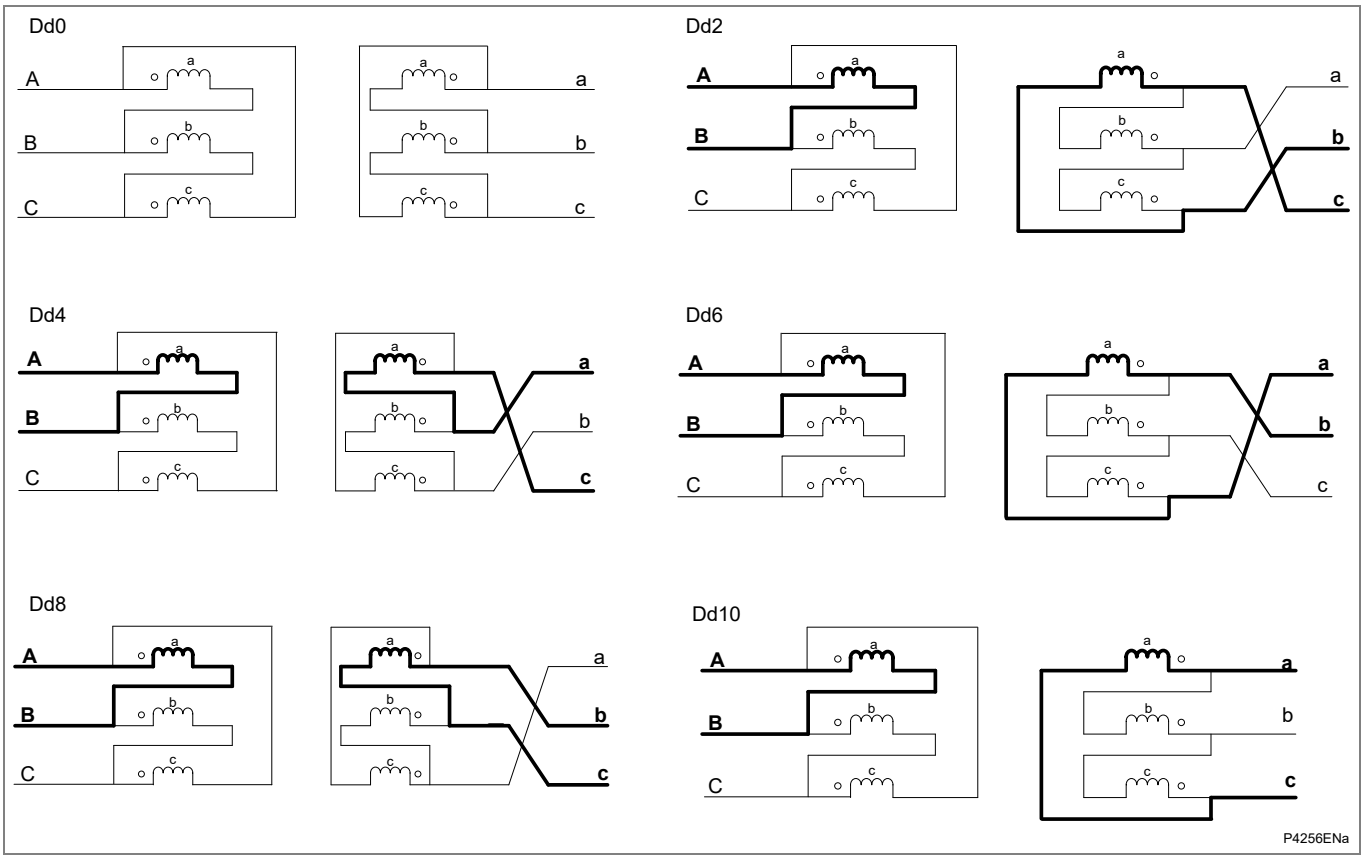


Figure 9 - Dd transformer connections

6.4.7 Low Set Element Bias Characteristic

This test checks the low set element bias characteristic. The relay has a three slope bias characteristic, therefore this test is performed at three points on the bias curve, one at 0% slope, at 30% slope, and at 80% slope, corresponding with bias currents of 0.4 p.u., 0.8 p.u., and 1.5 p.u. respectively.

If three LEDs have been assigned to give phase segregated trip information, Idiff Trip A, IDiff Trip B and IDiff Trip C (DDB 899, 900, 901), these may be used to indicate correct per-phase operation. If not, monitor options need to be used (see the next paragraph).

Go to the **COMMISSION TESTS** column in the menu, scroll down and change cells [0F07: Monitor Bit 1] to 899, [0F08: Monitor Bit 2] to 900 and [0F09: Monitor Bit 3] to 901. Cell [0F05: Test Port Status] will now appropriately set or reset the bits that now represent Phase A Trip (DDB 899), Phase B Trip (DDB 900) and Phase C Trip (DDB 901) with the rightmost bit representing Phase A Trip. From now on, monitor the indication of [0F05: Test Port Status].

It is important in this case that the injected currents are 180º out of phase. Connect the relay to the test equipment as shown in the following diagram.

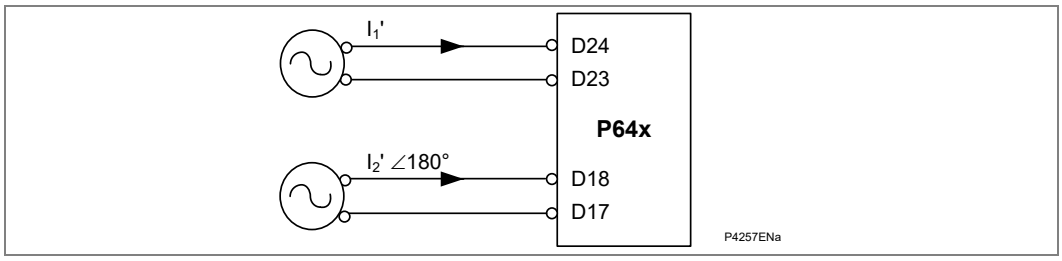


Figure 10 - Low set element bias characteristic test equipment connection

In total, six tests should be performed, one to cause the relay to trip and one to not cause the relay to trip, for the three sections of the bias curve. As shown in the following table, select the appropriate current values for each test, depending upon the setting and rating of the relay. Using the equations below, calculate the current values to apply to the relay, (I1' and I2'). In all cases the current should be applied for no longer than one second, and should be within ±5% of the calculated values.

$$I_1' = \frac{I_1}{K_{CT1}}$$

$$I_2' = \frac{I_2}{K_{CT2}}$$

In (amps)	Is1 (pu)	0%				K1 = 30%				K2 = 80%			
		Trip		No trip		Trip		No trip		Trip		No trip	
		I1	I2	I1	I2	I1	I2	I1	I2	I1	I2	I1	I2
1	0.2	0.51	0.29	0.49	0.31	0.94	0.67	0.91	0.69	1.89	1.12	1.82	1.19
5	0.2	2.55	1.45	2.45	1.55	4.7	3.35	4.55	3.45	9.45	5.6	9.1	5.95

Table 21 - Low set element bias characteristic test

6.4.8 Second-Harmonic Blocking

This test checks that the second harmonic blocking is functioning, and it requires a current source capable of generating second-harmonic current. Once enabled, it blocks the low set differential element if the percentage of second harmonic over fundamental component per phase basis exceeds the setting Ih(2)%>.

To run the test, proceed as follows:

1. Connect two current test sources to one phase of any current bias input. The following diagram shows the current sources connected to A phase of current bias input 1:
2. Inject 4 x I of fundamental current, where: $I = \frac{I_{s1}}{K_{CT1}}$

   Is1 is the low set setting, K_{CT1} is the Terminal 1 CT amplitude matching factor which is used to compensate for a mismatch in currents due to the line side current transformer ratios. This is found in the cell [Match Factor HV] under the **GROUP 1 SYSTEM CONFIG** menu heading.
3. Ensure that Id Bias Trip A [DDB 909] asserts.
4. Apply and ramp up second-harmonic current to dropout the low set differential element.
5. Turn on the second current source for second-harmonic current (120 Hz if Frequency = 60 and 100 Hz if Frequency = 50). Starting at zero current, slowly increase the magnitude of this second current source until Id Bias Trip A [DDB 909] resets.
6. Note the value of the applied current from the second test source. The current from the second-harmonic source is shown by:

$$\text{Second harmonic current} = \frac{Ih(2)\%}{100} \times \text{ fundamental current } \pm 10\%$$

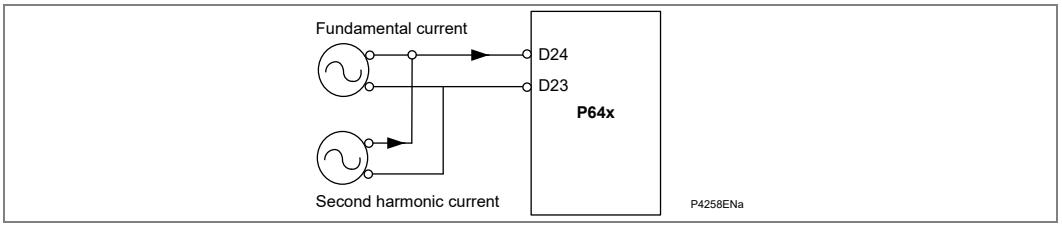


Figure 11 - Second harmonic test

6.4.9 Fifth-Harmonic Blocking

This test checks that the fifth-harmonic blocking is functioning, and it requires a current source capable of generating fifth-harmonic current. Once enabled, it blocks the low set differential element if the percentage of second harmonic over fundamental component per phase basis exceeds the setting Ih(5)%>.

Connect two current test sources to one phase of any current bias input. The following diagram shows the current sources connected to current bias input 1.

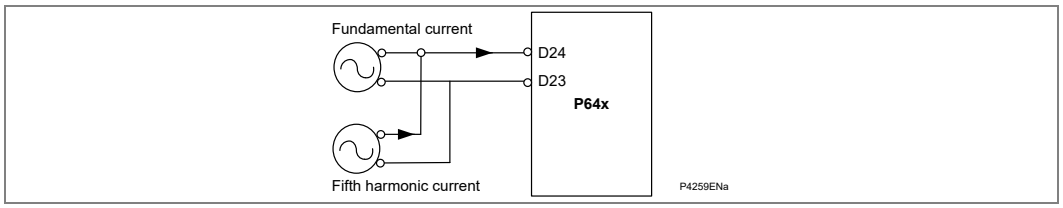


Figure 12 - Fifth-harmonic

Inject 4 x I of fundamental current, where: $I = \frac{I_{s1}}{K_{CT1}}$

Is1 is the low set setting. K_{CT1} is the Terminal 1 CT amplitude matching factor which is used to compensate for a mismatch in currents due to the line side current transformer ratios. This is found in the cell [Match Factor HV] under the **GROUP 1 SYSTEM CONFIG** menu heading. Ensure that Id Bias Trip A [DDB 909] asserts.

Apply and ramp up fifth-harmonic current to dropout the low-set differential element. Turn on the second current source for fifth-harmonic current (300 Hz if Frequency = 60, 250 Hz if Frequency = 50). Starting at zero current, slowly increase the magnitude of this second current source until Id Bias Trip A [DDB 909] resets. Note the value of the applied current from the second test source. The current from the fifth-harmonic source is given by:

$$\text{Fifth harmonic current} = \frac{Ih(5)\%}{100} \times \text{ fundamental current } \pm 10\%$$

6.5 Restricted Earth Fault (REF) Setting Checks

6.5.1 Checking Restricted Earth Fault (REF) Sensitivity

These tests are performed on a per-winding basis, for all elements (REF HV, REF LV, REF TV, REF Auto) that are used in the application. The tripping sensitivity for the REF differential protection of one winding with a single end infeed is given by:

$$I = \frac{\text{n Is1 set}}{\text{scaling factor}}$$

n Is1 set: HV, LV, TV, Auto REF setting

For HighZ REF fed on neutral CT2:

Scaling factor = K = 1

For LowZ REF fed on line CT or High Z REF:

Scaling factor = K = Neutral CT ratio / CTn ratio

Apply a current slightly less than I to the I_Y (HV) CT input. Observe that no trip should occur, and the red Trip LED remains OFF.

Ramp up the current until a trip occurs and the Trip LED switches ON.

Record the current at which the relay tripped. The measured current should be within ±10% of the HV Is1 setting.

Note	*If the REF provides low-impedance balanced earth fault protection for a delta winding, there is no I_Y input connected. In such cases, inject instead into the A phase CT input for the winding concerned. It may also be necessary to disable temporarily other protection elements that may trip, to view only the REF operation.*

Repeat the REF tests for each winding where it is implemented.

6.5.2 REF/BEF Primary Injection Tests

Primary injection tests are required to check that the current transformers are correctly connected.

Caution	The procedure for primary testing must respect utility safety rules, permits to work and sanctions for testing. It is important that the primary injection test is undertaken for the REF function, because even stability with loadflow cannot be used as a test of REF stability. While balanced load is flowing, there is no way of knowing whether the star point-ground CT is correctly oriented. Therefore an installation might falsely appear correct on-load until there is an external earth fault on the system, and a maloperation could occur.

6.5.2.1 Checking REF through Stability by Primary Injection

Where REF is providing *low-impedance* balanced earth fault protection for *delta* windings, no additional testing is required. This is because no I_Y CT input is connected, and all phase CT orientations have already been proven to be in the same sense for the differential protection.

In all applications to protect grounded star (wye) windings, it is not possible to prove that all CT inputs have the correct directionality, without a primary injection test.

To check for through stability, it is important, especially for a new transformer installation to simulate a through-fed external earth fault, by a primary fault simulation. This is achieved by temporarily shorting the entire A-phase winding to the star point, and then circulating fault current in a loop through the A-phase CT primary, the short, and the I_Y CT primary. In such a through-fault situation, the relay should not trip.

Before commencing any primary injection tests it is essential to ensure that the circuit is dead, isolated from the remainder of the system and that only those earth connections associated with the primary injection test equipment are in position.

The stability of the scheme can be checked by injecting through the neutral current transformer and each phase current transformer in turn. The following diagram shows the connections for the P64x when the relays are used in a high-impedance differential scheme.

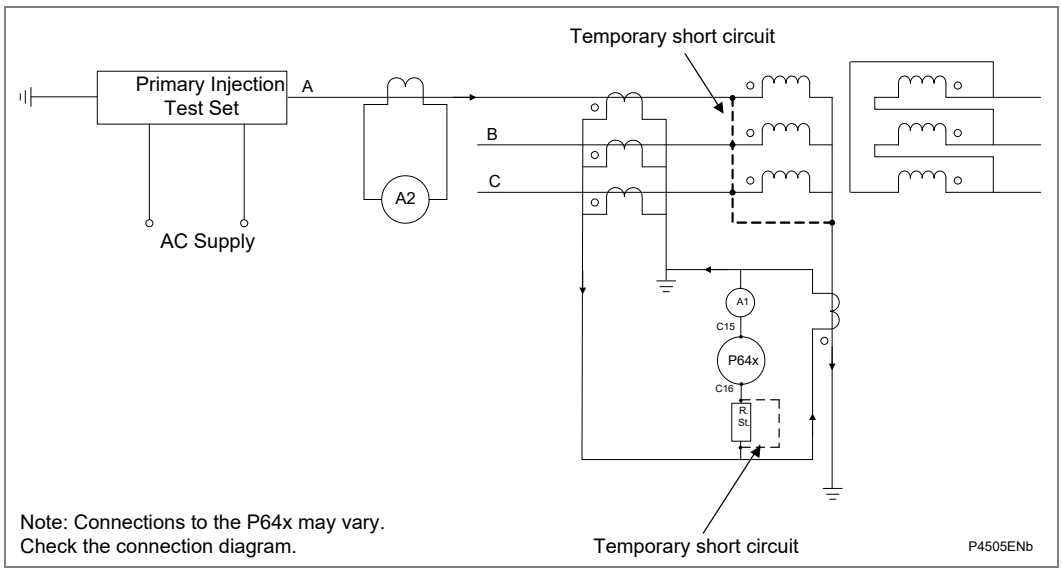


Figure 13 - REF - Primary injection - stability test set up

During the stability test, it is necessary to measure the spill current in the relay circuit, therefore the stabilising resistor should be shorted out. The current should be increased up to as near full load as possible and the current flowing through ammeter A1 noted. If the connections are correct, this current would be very low, only a few milliamps. A high reading, (twice the injected current, referred through the current transformer ratio) indicates that one of the current transformer connections is reversed. This test should be repeated for the B-phase CT and neutral CT, and then for the C-phase CT and neutral CT.

The sensitivity of the protection can be checked by injecting with the single phase test set through each of the main current transformers in turn. This is shown in the following diagram. While carrying out this test it is advisable to measure the voltage across the relay coil and stabilizing resistance, and so to check the approximate voltage developed by the main current transformer to cause relay operation.

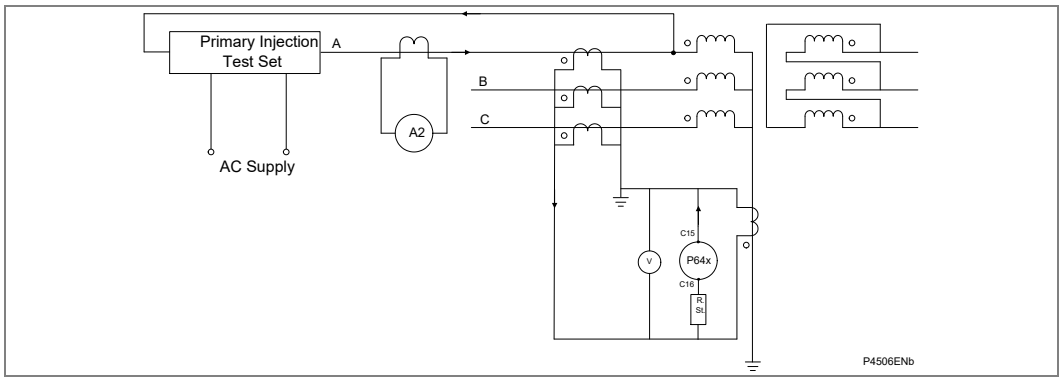


Figure 14 - REF/BEF - Primary injection - sensitivity test set up

6.6 Overflux Protection

The overflux protection has five independent elements, one is used to give an alarm indication and the other four are used to cause a trip.

6.6.1 Overflux Alarm Sensitivity

The one-phase VT is associated with the winding 2 overfluxing element, and the three-phase VT is associated with the winding 1 overfluxing element.

1. Configure the equipment so that an AC voltage (any phase-phase pair may be used) can be applied to terminals F4 and F3, starting a timer when the voltage is applied, and stopping the timer when the output relay energizes.
2. Configure an output relay in the PSL as W1 V/Hz> Alarm [DDB 501]. For a duration greater than the time set in the cell [V/Hz Alarm Delay], found in the **GROUP 1 OVERFLUXING** menu heading, **Volts/Hz W1** sub-heading, apply a voltage of:

   V = V/Hz Alm Set x f x 0.95

   to terminals F4 and F3, where V/Hz Alm Set is found in the **GROUP 1 OVERFLUXING** menu heading, **Volts/Hz W1** sub-heading, and f is the system frequency.
3. Ensure that the selected output relay does not energize.
4. Apply a voltage of:

   V = V/Hz Alm Set x f x 1.05

   to terminals F4 and F3 and ensure that the selected output relay does energize and that the time is within ±20% of the time set in the cell [V/Hz Alarm Delay], found in the **GROUP 1 OVERFLUXING** menu heading, **Volts/Hz W1** sub-heading.
5. Repeat the same test for the W2 V/Hz> Alarm [DDB 503] if applicable.

6.6.2 Overflux Trip Sensitivity

The first stage overfluxing element can be either definite time (DT) or inverse minimum definite time (IDMT). This will be found under the **GROUP 1 OVERFLUXING** menu heading, **Volts/Hz W1** sub-heading. If the cell [V/Hz>1 Function] is set to DT, operation of the output relay should occur in t ±20%, where t is the value in the cell [V/Hz>1 Delay] which is also found in the **GROUP 1 OVERFLUXING** menu heading, **Volts/Hz W1** sub-heading.

If the cell [V/Hz>1 Function] is set to IDMT, operation should occur in:

$$t = \frac{\text{V/Hz} > 1\,\text{Trip TMS}}{\left(\dfrac{\text{V/Hz}}{\text{V/Hz} > 1\,\text{Trip Set}} - 1\right)^2}$$

This characteristic is plotted on the graph shown in the following diagram.

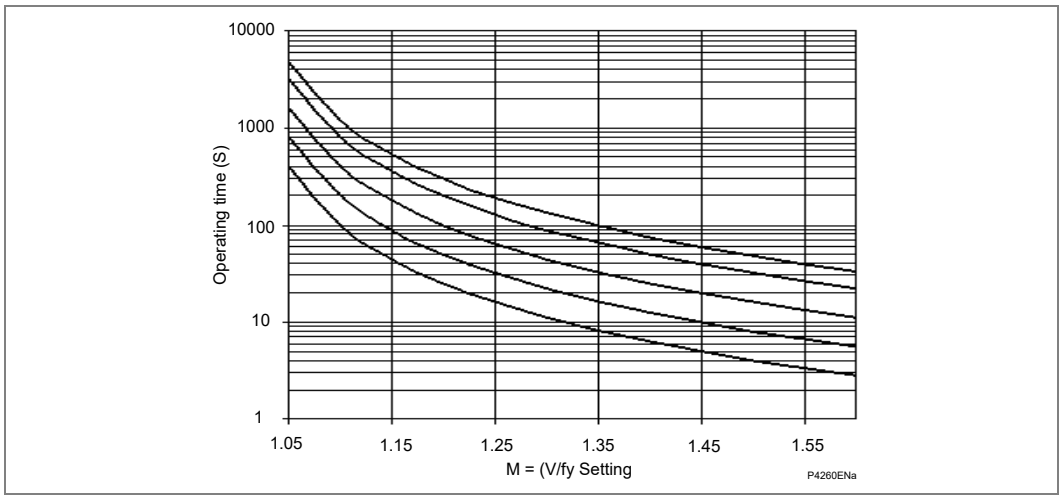


Figure 15 - IDMT overfluxing protection characteristic

For a duration greater than the time t calculated from the equation above, apply a voltage of:

V = V/Hz > 1 Trip Set x f x 0.95

where V/Hz>1 Trip Set is found in the **GROUP 1 OVERFLUXING** menu heading, **Volts/Hz W1** sub-heading and f is the system frequency. Ensure that the selected output relay does not energize.

Next, apply a voltage of:

V = V/Hz Trip Set x f x 1.05

then confirm that the selected output relay does energize and the time is within ±20% of the time t above.

6.7 Backup Phase Overcurrent Protection

The overcurrent protection function I > 1 element should be tested.

To avoid spurious operation of any other protection elements, all protection elements except the overcurrent protection should be disabled for the duration of the overcurrent element tests. This is done in the relay's **CONFIGURATION** column. Make a note of which elements need to be re-enabled after testing.

6.7.1 Connect the Test Circuit

Determine which output relay has been selected to operate when a I > 1 trip occurs by viewing the relay's Programmable Scheme Logic (PSL).

The PSL can only be changed using the appropriate software. If this software is not available, the default output relay allocations are still applicable.

If the trip outputs are phase-segregated (a different output relay allocated for each phase), the relay assigned for tripping on "A" phase faults should be used.

If stage 1 is not mapped directly to an output relay in the PSL, output relay 3 (H5 - H6 in the 60TE case and L5 - L6 in the 80TE case) should be used for the test.

HV Three Pole Tripping	DDB 960:	POC 1 I > 1 Trip
HV Single Pole Tripping	DDB 961:	POC 1 I > 1 Trip A
	DDB 962:	POC 1 I > 1 Trip B
	DDB 963:	POC 1 I > 1 Trip C
LV Three Pole Tripping	DDB 976:	POC 2 I > 1 Trip
LV Single Pole Tripping	DDB 977:	POC 2 I > 1 Trip A
	DDB 978:	POC 2 I > 1 Trip B
	DDB 979:	POC 2 I > 1 Trip C
TV Three Pole Tripping	DDB 992:	POC 3 I > 1 Trip
TV Single Pole Tripping	DDB 993:	POC 3 I > 1 Trip A
	DDB 994:	POC 3 I > 1 Trip B
	DDB 995:	POC 3 I > 1 Trip C

For details of the associated terminal numbers refer to the external connection diagrams in the *Connection Diagrams* chapter.

1. Connect the output relay so that its operation will trip the test set and stop the timer.
2. Connect the current output of the test set to the **HV-A** phase current transformer input of the relay to test the POC 1 I > 1 Trip.
3. Connect the current output of the test set to the **LV-A** phase current transformer input of the relay to test the POC 2 I > 1 Trip.
4. Connect the current output of the test set to the **TV-A** phase current transformer input of the relay to test the POC 3 I > 1 Trip.
5. Ensure that the timer starts when the current is applied to the relay.

6.7.2 Perform the Test

1. Ensure that the timer is reset.
2. Apply a current of twice the setting in cell [3505: GROUP 1 OVERCURRENT, I > 1 Current Set] to the relay and note the time displayed when the timer stops.
3. Check the red trip LED and yellow alarm LED come on when the relay operates.
4. Check "Alarms/Faults Present - Started Phase A, Tripped Phase A, POC 1 Start I > 1, POC 1 Trip I > 1" is on the display.
5. Reset all alarms.

6.7.3 Check the Operating Time

Check that the operating time recorded by the timer is in the range shown in the *Characteristic operating times for Overcurrent1 I>1, Overcurrent2 I> and Overcurrent I>* table below.

Note	*Except for the definite time characteristic, the operating times shown in following table are for a time multiplier or time dial setting of 1. Therefore, to obtain the operating time at other time multiplier or time dial settings, the time shown in the table must be multiplied by the setting of cell [3507: GROUP 1 OVERCURRENT1, I > 1 TMS], [3537: GROUP 1 OVERCURRENT2, I > 1 TMS] or [3567: GROUP 1 OVERCURRENT3, I > 1 TMS] for IEC or UK characteristics or cell [3508: GROUP 1 OVERCURRENT1, Time Dial], [3538: GROUP 1 OVERCURRENT2, I > 1 Time Dial] or [3568: GROUP 1 OVERCURRENT3, I > 1 Time Dial] for IEEE and US characteristics.*

Also, for definite time and inverse characteristics there is an additional delay of up to 0.02 seconds and 0.08 seconds respectively that may need to be added to the relay's acceptable range of operating times.

For all characteristics, allowance must be made for the accuracy of the test equipment being used.

On completion of the tests, any protection elements that were disabled for testing purposes must have their original settings restored in the **CONFIGURATION** column.

Characteristic	Operating time at twice current setting and time multiplier/time dial setting of 1.0	
	Nominal (seconds)	Range (seconds)
DT	[3506: I>1 Time Delay] setting	Setting ±5%
IEC S Inverse	10.03	9.53 - 10.53
IEC V Inverse	13.50	12.83 - 14.18
IEC E Inverse	26.67	25.34 - 28
UK LT Inverse	120.00	114.00 - 126.00
UK Rectifier	966.26	917.94-1014.57
RI	4.52	4.30-4.75
IEEE M Inverse	3.8	3.61 - 3.99
IEEE V Inverse	7.03	6.68 - 7.38
IEEE E Inverse	9.52	9.04 - 10
US Inverse	2.16	2.05 - 2.27
US ST Inverse	12.12	11.51 - 12.73

Table 22 - Characteristic operating times for Overcurrent1 I>1, Overcurrent2 I> and Overcurrent I>

6.8 Thermal Overload Protection

Consider a two winding transformer, with the thermal element monitoring the bias current. First, calculate the full load current through the HV winding and LV winding. The reference power and the nominal voltage of each winding should be considered.

$$FLC_{HV} = \frac{S_{ref}}{\sqrt{3} \times Vnon_{HV}} \qquad FLC_{LV} = \frac{S_{ref}}{\sqrt{3} \times Vnon_{LV}}$$

Where:
S_{ref} = reference power given in the setting cell **Ref Power S**.
V_{nonHV} = HV nominal voltage given in the setting cell **HV Nominal**.
V_{nonLV} = LV nominal voltage given in the setting cell **LV Nominal**.

A spreadsheet showing the theoretical operating time of the thermal element can be provided on request. If the monitored winding is the bias current, the Ku factor required in the spreadsheet is calculated as follows:

$$K_u = \frac{\frac{I_{HV}}{FLC_{HV}} + \frac{I_{LV}}{FLC_{LV}}}{2 \times IB}$$

Where:
I_{HV} = current flowing through the HV winding (this is the current to be injected through the CT assigned to the HV winding)
I_{LV} = current flowing through the LV winding (this is the current to be injected through the CT assigned to the LV winding)
IB = rated load in pu
K_u = ratio of ultimate load to rated load

Report the following measurements:

Top oil temperature at tripping:	
Hottest spot temperature at tripping:	
Thermal model operating time (spreadsheet):	
Operating time recorded by the test equipment:	
Error - top oil operating time:	
Error - hottest spot operating time:	

When the operating time of the top oil element is tested, set the hottest spot element operating time delay high enough to avoid any interference. When the operating time of the hottest spot element is tested, set the top oil element operating time delay high enough to avoid any interference.

If the monitor winding is set as either HV winding or LV winding, then K_u is calculated as follows:

$$K_u = \frac{I_{HV}}{IFLC_{HV} \times IB} \qquad K_u = \frac{I_{LV}}{IFLC_{LV} \times IB}$$

6.9 Current Transformer Supervision

Under configuration only enable the differential and supervision elements. Consider the CTS settings shown in the following table:

Parameter	Setting
Diff CTS	Enabled
CTS Status	Restrain
CTS Time Delay	2.000 s
CTS I1	10.00%
CTS I2/I1>1	20.00%
CTS I2/I1>2	40.00%

Table 23 - CTS settings

Consider a two winding transformer and that a P642 is being used. Inject full load current in inputs 1 and 2 simulating a load condition.

$$FLC_{HV} \times In = \frac{\frac{HVrating}{\sqrt{3} \times HVnominal}}{CT1_{prim}} \qquad FLC_{LV} \times In = \frac{\frac{LVrating}{\sqrt{3} \times LVnominal}}{CT2_{prim}}$$

Where:
HV rating = HV power
LV rating = LV power
HV nominal = HV nominal voltage
LV nominal = LV nominal voltage
CT1prim = CT1 nominal primary current
CT2prim = CT2 nominal primary current
In = CT nominal secondary current inject balance current in current input 1.
Ia = FLCHV × In ∠0° Ib = FLCHV × In ∠-120° Ic = FLCHV × In ∠120°
Inject balance current in current input 2:
Ia = FLCLV × In ∠210° Ib = FLCLV × In ∠90° Ic = FLCLV × In ∠330°

Notice that the differential element does not trip because a load condition is being simulated. To simulate a problem in the A phase wiring, suddenly decrease to zero the A phase current of current input 1:

Ia = 0 ∠0°
Ib = FLCHV × In ∠-120°
Ic = FLCHV × In ∠120°

Note that the CT fail alarm is asserted, and the differential function is blocked.

Measure current input 1 positive and negative sequence currents from the Measurement 1 column. The I2/I1 ratio should be ≥ 40%.

I1-1 Magnitude: _____
I2-1 Magnitude: _____
I2/I1 CT1 ratio: _____

Sufficient positive sequence current is flowing through the current inputs 1 and 2 (the threshold is 0.1 In). No inrush condition is present and the Inhibit CTS signal is low. As a result, the Is1 setting is increased to Is-CTS.

Measure the differential current and bias current from the Measurement 3 column:

Ia bias = _____ Ia diff = _____

Ib bias = _____ Ib diff = _____

Ic bias =_____ Ic diff = _____

Localize these points within the differential characteristic. Note that the differential function did not trip because the Is1 setting has been increased to Is-CTS.

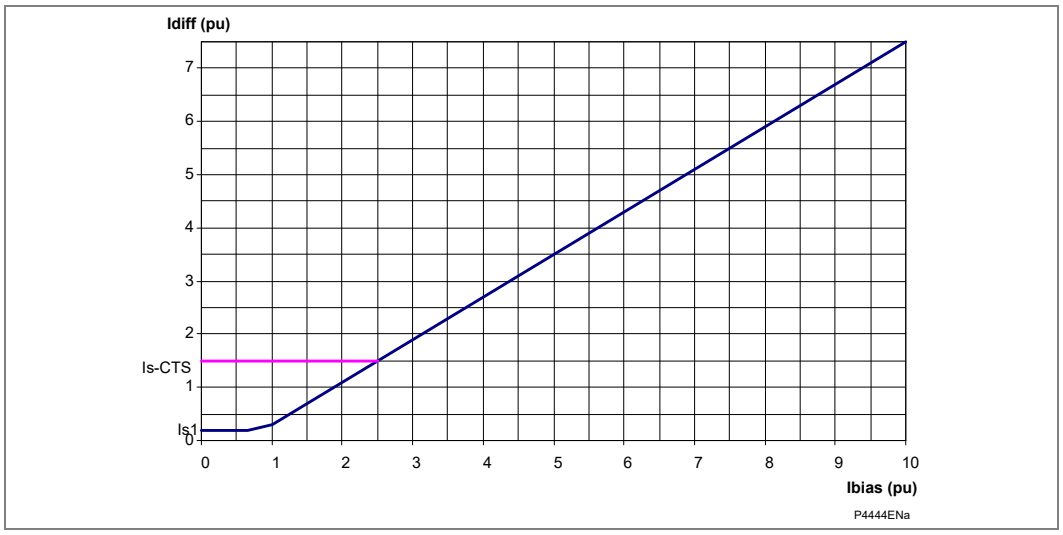


Figure 16 - CTS - Differential characteristic

Suddenly increase the A phase current from zero to 4 × FLCHV × In:

Ia = 4 × FLCHV × In ∠0°

Ib = FLCHV × In ∠-120°

Ic = FLCHV × In ∠120°

The differential element will trip. Record the differential and bias measurements and localize these points in the differential characteristic.

Ia bias = _____ Ia diff = _____

Ib bias = _____ Ib diff = _____

Ic bias = _____ Ic diff = _____

6.10 Through Fault Monitoring

Consider the through fault monitoring default settings shown in the following table:

Parameter	Setting
Through Fault	Enabled
Monitored Input	HV
TF I> Trigger	3.850 pu
TF I2t> Alarm	100 pu

Table 24 - Through fault monitoring settings

The I^2t is described as follows:

$$I^2t = \left(\frac{1}{x} \times FLC\right)^2 \times 2$$

Where:
X = transformer reactance, which would limit the through fault current flowing through the transformer
FLC = full load current of the winding being monitored. To calculate this current use the winding power rating and nominal voltage.
2 = maximum duration limit in seconds for the worst case of mechanical duty

If the reactance is 10% and the I2t> Alarm is 100 pu, then at 10 times FLC, the through fault alarm should be asserted. The test equipment should register the time elapsed from the beginning of the injection to the assertion of the alarm as 2 s. When a current less than the maximum through fault current flows, the time required by the alarm to be asserted is as follows:

$$t = \frac{\left(\frac{1}{X}\right)^2 \times 2}{I^2}$$

Where:
I = current flowing through the monitored winding in pu

Inject 4 A in current input 1:

Ia = 4 In $\angle 0°$
Ib = 4 In $\angle -120°$
Ic = 4 In $\angle 120°$

After 2 s approximately from the beginning of the injection, a through fault alarm is generated. A through fault event is generated as soon as the current through the monitor winding is above TF I> Trigger. To monitor the time, wire the relay output 4 to an input in the test equipment.

Time registered by the test equipment: _____
IA peak: _____
IB peak: _____
IC peak: _____
I2t A phase: _____
I2t B phase: _____
I2t C phase: _____

7 ON-LOAD CHECKS

The objectives of the on-load checks are to:

- Confirm the external wiring to the current and voltage inputs is correct.
- Measure the magnitude of capacitive current
- Ensure the on-load differential current is well below the relay setting
- Check the polarity of the line current transformers at each end is consistent.
- Directionality check for directional elements.

Caution	Remove all test leads and temporary shorting leads, and replace any external wiring that was removed to allow testing.

Caution	If any of the external wiring was disconnected from the relay to run any tests, make sure that all connections are restored according to the external connection or scheme diagram.

The following on-load measuring checks ensure the external wiring to the current and voltage inputs is correct but can only be carried out if there are no restrictions preventing the energisation of the plant being protected.

7.1 Voltage Connections

Caution	Using a multimeter, measure the voltage transformer secondary voltages to ensure they are correctly rated. Check that the system phase rotation is correct using a phase rotation meter.

Compare the values of the secondary phase voltages with the relay's measured values, which can be found in the **MEASUREMENTS 1** menu column.

If cell [0D02: MEASURE'T SETUP, Local Values] is set to **Secondary**, the values displayed on the relay LCD or a portable PC connected to the front EIA(RS)232 communication port should be equal to the applied secondary voltage. The values should be within 1% of the applied secondary voltages/currents (5% for P74x). However, an additional allowance must be made for the accuracy of the test equipment being used.

If cell [0D02: MEASURE'T SETUP, Local Values] is set to **Primary**, the values displayed should be equal to the applied secondary voltage multiplied the corresponding voltage transformer ratio set in the **CT & VT RATIOS** menu column (see the following table). Again, the values should be within 1% of the expected value (5% for P74x), plus an additional allowance for the accuracy of the test equipment being used.

Voltage	Cell in MEASUREMENTS 1 Column (02)	Corresponding VT ratio (in "VT and CT RATIO" Column (0A) of Menu)
V_{AB}	[029C: VAB Magnitude]	[0A03: Main VT Primary] [0A04: Main VT Sec'y]
V_{BC}	[029E: VBC Magnitude]	
V_{CA}	[02A0: VCA Magnitude]	
V_{AN}	[028F: VAN Magnitude]	
V_{BN}	[0291: VBN Magnitude]	
V_{CN}	[0293: VCN Magnitude]	
V_X	[0295: Vx Measured Mag]	[0A07: V_X VT Primary] [0A08: V_X VT Sec'y]

Table 25 - Measured voltages and VT ratio settings

7.2 Current Connections

Caution	**Measure the current transformer secondary values for each input using a multimeter connected in series with corresponding relay current input.**

Check that the current transformer polarities are correct by measuring the phase angle between the current and voltage, either against a phase meter already installed on site and known to be correct or by determining the direction of power flow by contacting the system control center.

Caution	**Ensure the current flowing in the neutral circuit of the current transformers is negligible.**

Compare the values of the secondary phase currents (and any phase angle) with the relay's measured values, which can be found in the **MEASUREMENTS 1** menu column.

Note	*Under normal load conditions the earth fault function measures little or no current. It is therefore necessary to simulate a phase-to-neutral fault. This can be achieved by temporarily disconnecting one or two of the line current transformer connections to the relay and shorting the terminals of these current transformer secondary windings.*

For P243, P34x and P64x, check that the IA/IB/IC Differential currents measured on the relay are less than 10% of the IA/IB/IC Bias currents, see the **MEASUREMENTS 3** menu. Check that the I2 Magnitude negative phase sequence current measured by the relay is not greater than expected for the particular installation, see the **MEASUREMENTS 1** menu. Check that the active and reactive power measured by the relay are correct, see the Measurements 2 menu. The power measurement modes are described in the *Measurements and Recording* chapter.

If cell [0D02: MEASURE'T SETUP, Local Values] is set to **Secondary**, the current displayed on the relay LCD or a portable PC connected to the front EIA(RS)232 communication port should be equal to the applied secondary current. The values should be within 1% (5% for the P741/P742/P743/P746) of the applied secondary currents. However, an additional allowance must be made for the accuracy of the test equipment being used.

If cell [0D02: MEASURE'T SETUP, Local Values] is set to **Primary**, the current displayed should be equal to the applied secondary current multiplied by the corresponding current transformer ratio set in the **CT & VT RATIOS** menu column (see the *Measured Voltages and VT Ratio Settings* table). Again the values should be within 10% (1% for the P34x, 5% for the P741/P742/P743/P746) of the expected value, plus an additional allowance for the accuracy of the test equipment being used.

Note	*If the relay is applied with a single dedicated current transformer for the earth fault function, it may not be possible to check the relay's measured values as the neutral current will be almost zero.*

8 FINAL CHECKS

The tests are now complete.

Caution	**Remove all test or temporary shorting leads. If it has been necessary to disconnect any of the external wiring from the relay to perform the wiring verification tests, make sure all connections are replaced according to the relevant external connection or scheme diagram.**

Ensure that the relay is restored to service by checking that cell [0F0F: COMMISSIONING TESTS, Test Mode] and [0F12: COMMISSION TESTS, Static Test] are set to '**Disabled**' (0F0D (not 0F0F) for P14x/P24x/P34x/P341/P44y/P54x/P841).

For P64x, if the relay is in a new installation, the thermal memory, transformer loss of life and overfluxing elements may be reset if required. These elements may be reset under the **MEASUREMENTS 3** menu heading. If the required access level is not active, the relay prompts for a password so that the setting change can be made.

If the menu language was changed to allow accurate testing, it must now be restored to the customer's preferred language.

If a MiCOM P991 or Easergy test block is installed, remove the MiCOM P992 or Easergy test plug and replace the test block cover so that the protection is put into service.

Ensure that all event records, fault records, disturbance records, alarms and LEDs have been reset before leaving the relay.

If applicable, replace the secondary front cover on the relay.

TEST AND SETTINGS RECORDS

CHAPTER 12

Date:	07/2018
Products covered by this chapter:	This chapter covers the specific versions of the MiCOM products listed below. This includes ***only*** the following combinations of Software Version and Hardware Suffix.
Hardware Suffix:	L (P642) M (P643/P645)
Software Version:	B4 - P64x (P642, P643 & P645)
Connection Diagrams:	10P642xx (xx = 01 to 10) 10P643xx (xx = 01 to 06) 10P645xx (xx = 01 to 09)

CONTENTS

Notes:

1 COMMISSIONING TEST RECORD

1.1 About this Chapter

The Commissioning chapter provides instructions on how to commission the relay – including how to calibrate it and how to establish that it is functioning as intended.

This chapter provides you with a series of templates. You can use this to record the tests which have been made and the settings which have been used. You should use this chapter in conjunction with the Commissioning chapter and any work instructions you have as to what functionality and settings the relay should use.

1.2 Date Record

Date:		Engineer:	
Station:		Circuit:	
		System Frequency:	…… Hz
VT Ratio:	…… / …… V	CT Ratio (tap in use):	…… /A

1.3 Front Plate Information

Relay type	MiCOM P……
Model number	
Serial number	
Rated current In	
Rated voltage Vn	
Auxiliary voltage Vx	

1.4 Test Equipment Used

This section should be completed to allow future identification of protective devices that have been commissioned using equipment that is later found to be defective or incompatible but may not be detected during the commissioning procedure.

Overcurrent test set	Model: Serial No:	
Injection test set	Model: Serial No:	
Phase angle meter	Model: Serial No:	
Phase rotation meter	Model: Serial No:	
Optical power meter	Model: Serial No:	
Insulation tester	Model: Serial No:	
Setting software:	Type: Version:	

1.5 Checklist

Have all relevant safety instructions been followed? Yes ☐ No ☐

5. PRODUCT CHECKS

5.1 With the relay de-energized

5.1.1 Visual inspection

Relay damaged?	Yes	☐	No	☐	
Rating information correct for installation?	Yes	☐	No	☐	
Case earth installed?	Yes	☐	No	☐	

5.1.2 Current transformer shorting contacts close? Yes ☐ No ☐ Not checked ☐

5.1.3 Insulation resistance >100 MΩ at 500 V dc Yes ☐ No ☐ Not tested ☐

5.1.4 External wiring

Wiring checked against diagram?	Yes	☐	No	☐	
Test block connections checked?	Yes	☐	No	☐	N/A ☐

5.1.5 Watchdog contacts (auxiliary supply off)

Terminals 11 and 12	Contact closed?	Yes	☐	No	☐
	Contact resistance	Ω	Not measured		☐
Terminals 13 and 14	Contact open?	Yes	☐	No	☐

5.1.6 Measured auxiliary supply V ac/dc

5.2 With the relay energized

5.2.1 Watchdog contacts (auxiliary supply on)

Terminals 11 and 12	Contact open?	Yes	☐	No	☐
Terminals 13 and 14	Contact closed?	Yes	☐	No	☐
	Contact resistance	Ω		Not measured	☐

5.2.2 LCD front panel display

LCD contrast setting used

5.2.3 Date and time

Clock set to local time?	Yes	☐	No	☐	
Time maintained when auxiliary supply removed?	Yes	☐	No	☐	

5.2.4 Light emitting diodes

Relay healthy (green) LED working?	Yes	☐	No	☐
Alarm (yellow) LED working?	Yes	☐	No	☐
Out of service (yellow) LED working?	Yes	☐	No	☐
Trip (red) LED working?	Yes	☐	No	☐
All programmable LEDs working? (may be 8 or 18 depending on the model)	Yes	☐	No	☐

5.2.5 Field supply voltage

Value measured between terminals 7 and 9	V dc
Value measured between terminals 8 and 10	V dc

5.2.6 Input opto-isolators (numbers vary depending on the product)

Opto input 1	working?	Yes ☐	No ☐			
Opto input 2	working?	Yes ☐	No ☐			
Opto input 3	working?	Yes ☐	No ☐			
Opto input 4	working?	Yes ☐	No ☐			
Opto input 5	working?	Yes ☐	No ☐			
Opto input 6	working?	Yes ☐	No ☐			
Opto input 7	working?	Yes ☐	No ☐			
Opto input 8	working?	Yes ☐	No ☐			
Opto input 9	working?	Yes ☐	No ☐	N/A	☐	
Opto input 10	working?	Yes ☐	No ☐	N/A	☐	
Opto input 11	working?	Yes ☐	No ☐	N/A	☐	
Opto input 12	working?	Yes ☐	No ☐	N/A	☐	
Opto input 13	working?	Yes ☐	No ☐	N/A	☐	
Opto input 14	working?	Yes ☐	No ☐	N/A	☐	
Opto input 15	working?	Yes ☐	No ☐	N/A	☐	
Opto input 16	working?	Yes ☐	No ☐	N/A	☐	
Opto input 17	working?	Yes ☐	No ☐	N/A	☐	
Opto input 18	working?	Yes ☐	No ☐	N/A	☐	
Opto input 19	working?	Yes ☐	No ☐	N/A	☐	
Opto input 20	working?	Yes ☐	No ☐	N/A	☐	
Opto input 21	working?	Yes ☐	No ☐	N/A	☐	
Opto input 22	working?	Yes ☐	No ☐	N/A	☐	
Opto input 23	working?	Yes ☐	No ☐	N/A	☐	
Opto input 24	working?	Yes ☐	No ☐	N/A	☐	
Opto input 25	working?	Yes ☐	No ☐	N/A	☐	
Opto input 26	working?	Yes ☐	No ☐	N/A	☐	
Opto input 27	working?	Yes ☐	No ☐	N/A	☐	
Opto input 28	working?	Yes ☐	No ☐	N/A	☐	
Opto input 29	working?	Yes ☐	No ☐	N/A	☐	
Opto input 30	working?	Yes ☐	No ☐	N/A	☐	
Opto input 31	working?	Yes ☐	No ☐	N/A	☐	
Opto input 32	working?	Yes ☐	No ☐	N/A	☐	

5.2.7 Output relays

Relay 1	working?		Yes ☐	No ☐	
	Contact resistance		Ω ☐	Not measured ☐	
Relay 2	working?		Yes ☐	No ☐	
	Contact resistance		Ω ☐	Not measured ☐	
Relay 3	working?		Yes ☐	No ☐	
	Contact resistance		Ω ☐	Not measured ☐	
Relay 4	working?		Yes ☐	No ☐	
	Contact resistance	(N/C)	Ω ☐	Not measured ☐	
		(N/O)	Ω ☐	Not measured ☐	
Relay 5	working?		Yes ☐	No ☐	
	Contact resistance	(N/C)	Ω ☐	Not measured ☐	
		(N/O)	Ω ☐	Not measured ☐	
Relay 6	working?		Yes ☐	No ☐	
	Contact resistance	(N/C)	Ω ☐	Not measured ☐	
		(N/O)	Ω ☐	Not measured ☐	
Relay 7	working?		Yes ☐	No ☐	
	Contact resistance	(N/C)	Ω ☐	Not measured ☐	
		(N/O)	Ω ☐	Not measured ☐	
Relay 8	working?		Yes ☐	No ☐	N/A ☐
	Contact resistance	(N/C)	Ω ☐	Not measured ☐	
		(N/O)	Ω ☐	Not measured ☐	

Relay 9	working?		Yes ☐	No ☐	N/A ☐
	Contact resistance		Ω ☐	Not measured ☐	
Relay 10	working?		Yes ☐	No ☐	N/A ☐
	Contact resistance		Ω ☐	Not measured ☐	
Relay 11	working?		Yes ☐	No ☐	N/A ☐
	Contact resistance	(N/C)	Ω ☐	Not measured ☐	
		(N/O)	Ω ☐	Not measured ☐	
Relay 12	working?		Yes ☐	No ☐	N/A ☐
	Contact resistance	(N/C)	Ω ☐	Not measured ☐	
		(N/O)	Ω ☐	Not measured ☐	
Relay 13	working?		Yes ☐	No ☐	N/A ☐
	Contact resistance	(N/C)	Ω ☐	Not measured ☐	
		(N/O)	Ω ☐	Not measured ☐	
Relay 14	working?		Yes ☐	No ☐	N/A ☐
	Contact resistance	(N/C)	Ω ☐	Not measured ☐	
		(N/O)	Ω ☐	Not measured ☐	
Relay 15	working?		Yes ☐	No ☐	N/A ☐
	Contact resistance	(N/C)	Ω ☐	Not measured ☐	
		(N/O)	Ω ☐	Not measured ☐	
Relay 16	working?		Yes ☐	No ☐	N/A ☐
	Contact resistance	(N/C)	Ω ☐	Not measured ☐	
		(N/O)	Ω ☐	Not measured ☐	

Relay 17	working?		Yes ☐	No ☐	N/A ☐
	Contact resistance		Ω ☐	Not measured ☐	
Relay 18	working?		Yes ☐	No ☐	N/A ☐
	Contact resistance		Ω ☐	Not measured ☐	
Relay 19	working?		Yes ☐	No ☐	N/A ☐
	Contact resistance		Ω ☐	Not measured ☐	
Relay 20	working?		Yes ☐	No ☐	N/A ☐
	Contact resistance		Ω ☐	Not measured ☐	
Relay 21	working?		Yes ☐	No ☐	N/A ☐
	Contact resistance		Ω ☐	Not measured ☐	
Relay 22	working?		Yes ☐	No ☐	N/A ☐
	Contact resistance		Ω ☐	Not measured ☐	
Relay 23	working?		Yes ☐	No ☐	N/A ☐
	Contact resistance	(N/C)	Ω ☐	Not measured ☐	
		(N/O)	Ω ☐	Not measured ☐	
Relay 24	working?		Yes ☐	No ☐	N/A ☐
	Contact resistance	(N/C)	Ω ☐	Not measured ☐	
		(N/O)	Ω ☐	Not measured ☐	

Relay 25	working?		Yes ☐	No ☐	N/A ☐
	Contact resistance		Ω ☐	Not measured ☐	
Relay 26	working?		Yes ☐	No ☐	N/A ☐
	Contact resistance		Ω ☐	Not measured ☐	
Relay 27	working?		Yes ☐	No ☐	N/A ☐
	Contact resistance		Ω ☐	Not measured ☐	
Relay 28	working?		Yes ☐	No ☐	N/A ☐
	Contact resistance		Ω ☐	Not measured ☐	
Relay 29	working?		Yes ☐	No ☐	N/A ☐
	Contact resistance		Ω ☐	Not measured ☐	
Relay 30	working?		Yes ☐	No ☐	N/A ☐
	Contact resistance		Ω ☐	Not measured ☐	
Relay 31	working?		Yes ☐	No ☐	N/A ☐
	Contact resistance	(N/C)	Ω ☐	Not measured ☐	
		(N/O)	Ω ☐	Not measured ☐	
Relay 32	working?		Yes ☐	No ☐	N/A ☐
	Contact resistance	(N/C)	Ω ☐	Not measured ☐	
		(N/O)	Ω ☐	Not measured ☐	

5.2.8 RTD inputs

Resistor tolerance

RTD 1 reading	[0460: RTD 1 Label]	°C
RTD 2 reading	[0461: RTD 2 Label]	°C
RTD 3 reading	[0462: RTD 3 Label]	°C
RTD 4 reading	[0463: RTD 4 Label]	°C
RTD 5 reading	[0464: RTD 5 Label]	°C
RTD 6 reading	[0465: RTD 6 Label]	°C
RTD 7 reading	[0466: RTD 7 Label]	°C
RTD 8 reading	[0467: RTD 8 Label]	°C
RTD 9 reading	[0468: RTD 9 Label]	°C
RTD 10 reading	[0469: RTD 10 Label]	°C

5.2.9 Current Loop Inputs (CLI)

CLI input type 0-1mA ☐ 0-10mA ☐ 0-20mA ☐ 4-20mA ☐

CLI1 reading at 50% CLI maximum range
[0470: CLI1 Input Label]

CLI2 reading at 50% CLI maximum range
[0471: CLI2 Input Label]

CLI3 reading at 50% CLI maximum range
[0472: CLI3 Input Label]

CLI4 reading at 50% CLI maximum range
[0473: CLI4 Input Label]

5.2.10 Current loop outputs 0-1mA ☐ 0-10mA ☐ 0-20mA ☐ 4-20mA ☐

CLO output type	mA
CLO1 output current at 50% of rated output	mA
CLO2 output current at 50% of rated output	mA
CLO3 output current at 50% of rated output	mA
CLO4 output current at 50% of rated output	mA

5.2.11 First rear communications port

Communication standard

K-Bus ☐ MODBUS ☐
IEC60870-5-103 ☐ IEC61850 ☐
DNP3* ☐

Communications established? Yes ☐ No ☐

Protocol converter tested? Yes ☐ No ☐ N/A ☐

5.2.12 Second rear communications port

K-Bus ☐ EIA(RS)485 ☐
EIA(RS)232 ☐

Communication port configuration Yes ☐ No ☐

Communications established? Yes ☐ No ☐

Protocol converter tested? Yes ☐ No ☐ N/A ☐

5.2.13 Current inputs

Displayed current		Primary ☐	Secondary ☐
Phase T1 CT ratio	Phase CT Primary / Phase CT Secondary		N/A ☐
Phase T2 CT ratio	Phase CT Primary / Phase CT Secondary		N/A ☐
Phase T3 CT ratio	Phase CT Primary / Phase CT Secondary		N/A ☐
Phase T4 CT ratio	Phase CT Primary / Phase CT Secondary		N/A ☐
Phase T5 CT ratio	Phase CT Primary / Phase CT Secondary		N/A ☐
TN1 CT ratio	[IY HV CT Primary / IY HV CT Secondary]		N/A ☐
TN2 CT ratio	[IY LV CT Primary / IY LV CT Secondary]		N/A ☐
IY (TV) CT ratio	[IY TV CT Primary / IY TV CT Secondary]		N/A ☐

Input CT	Applied value	Displayed value		
IA (1)	A	A		
IB (1)	A	A		
IC (1)	A	A		
IA (2)	A	A		
IB (2)	A	A		
IC (2)	A	A		
IA (3) (P643/5)	A	A	N/A	☐
IB (3) (P643/5)	A	A	N/A	☐
IC (3) (P643/5)	A	A	N/A	☐
IA (4) (P645)	A	A	N/A	☐
IB (4) (P645)	A	A	N/A	☐
IC (4) (P645)	A	A	N/A	☐
IA (5) (P645)	A	A	N/A	☐
IB (5) (P645)	A	A	N/A	☐
IC (5) (P645)	A	A	N/A	☐
IN HV (TN1 CT)	A	A	N/A	☐
IN LV (TN2 CT)	A	A	N/A	☐
IN TV (TN3 CT)	A	A	N/A	☐

5.2.14 Voltage inputs

Displayed voltage		Primary ☐	Secondary ☐
Main VT ratio	[Main VT Primary / Main VT Secondary]	V	N/A ☐
VX VT ratio	[V_xVT Primary / V_xVT Secondary]	V	N/A ☐

Input VT	Applied Value	Displayed value
Va (optional P643/P645)	V	V
Vb (optional P643/P645)	V	V
Vc (optional P643/P645)	V	V
Vx (P642/P643/P645)	V	V

6. SETTING CHECKS

Apply Application-Specific Settings

6.1	Application-specific function settings verified?	Yes	☐	No	☐	N/A	☐
6.2	Application-specific PSL tested?	Yes	☐	No	☐	N/A	☐

6.3	Demonstrate correct relay operation					
6.3.1	Transformer differential protection (P642/P643/P645)					
6.3.1.2	Transformer Differential lower slope pickup		A			
6.3.1.3	Transformer Differential upper slope pickup		A			
6.3.2.1	Transformer Differential Phase A contact routing OK?	Yes	☐	No	☐	
	Transformer Differential Phase A trip time		s			
6.3.2.2	Transformer Differential Phase B contact routing OK?	Yes	☐	No	☐	
	Transformer Differential Phase B trip time		s			
6.3.2.3	Transformer Differential Phase C contact routing OK?	Yes	☐	No	☐	
	Transformer Differential Phase C trip time		s			
	Average trip time, Phases A, B and C		s			

6.3.3	Overcurrent Protection (P642/P643/P645)					
	Protection function timing tested?	Yes or No				
	Overcurrent type (set in cell [I>1 Direction])	Directional or Non-Directional				
	Applied current		A			
	Expected operating time		s			
	Measured operating time		s			

7. ON-LOAD CHECKS

Test wiring removed?	Yes	☐	No	☐	N/A	☐
Disturbed customer wiring re-checked?	Yes	☐	No	☐	N/A	☐
On-load test performed?	Yes	☐	No	☐		

7.1

VT wiring checked?	Yes	☐	No	☐	N/A	☐
Phase rotation correct?	Yes	☐	No	☐		
Displayed voltage	Primary	☐	Secondary	☐		

Main VT ratio $\left[\frac{\text{[Main VT Primary]}}{\text{[Main VT Secondary]}}\right]$	V	N/A	☐	
Vx VT ratio $\left[\frac{\text{[}V_x\text{VT Primary]}}{\text{[}V_x\text{VT Secondary]}}\right]$	V	N/A	☐	

Voltages	Applied Value	Displayed value
V_{AN}/V_{AB}	V	V
V_{BN}/V_{BC}	V	V
V_{CN}/V_{CA}	V	V
V_X	V	V

7.2

CT wiring checked?	Yes	☐	No	☐	N/A	☐
CT polarities correct?	Yes	☐	No	☐		
Displayed current	Primary	☐	Secondary	☐		

Phase CT (1) ratio $\frac{\text{Phase CT Primary}}{\text{Phase CT Secondary}}$	or	N/A	☐	
Phase CT (2) ratio $\frac{\text{Phase CT Primary}}{\text{Phase CT Secondary}}$	or	N/A	☐	
Phase CT (3) ratio $\frac{\text{Phase CT Primary}}{\text{Phase CT Secondary}}$	or	N/A	☐	
Phase CT (4) ratio $\frac{\text{Phase CT Primary}}{\text{Phase CT Secondary}}$	or	N/A	☐	
Phase CT (5) ratio $\frac{\text{Phase CT Primary}}{\text{Phase CT Secondary}}$	or	N/A	☐	
TN1 CT ratio $\left[\frac{\text{IY HV CT Primary}}{\text{IY HV CT Secondary}}\right]$	or	N/A	☐	
TN2 CT ratio $\left[\frac{\text{IY LV CT Primary}}{\text{IY LV CT Secondary}}\right]$	or	N/A	☐	
TN3 CT ratio $\left[\frac{\text{IY TV CT Primary}}{\text{IY TV CT Secondary}}\right]$	or	N/A	☐	

Input CT	Applied Value	Displayed value		
IA (1)	A	A		
IB (1)	A	A		
IC (1)	A	A		
IA (2)	A	A		
IB (2)	A	A		
IC (2)	A	A		
IA (3) P643/P645	A	A	N/A	☐
IB (3) P643/P645	A	A	N/A	☐
IC (3) P643/P645	A	A	N/A	☐
IA (4) P645	A	A	N/A	☐
IB (4) P645	A	A	N/A	☐
IC (4) P645	A	A	N/A	☐
IA (5) P645	A	A	N/A	☐
IB (5) P645	A	A	N/A	☐
IC (5) P645	A	A	N/A	☐
TN1 |CT	A	A	N/A	☐
TN2 CT	A	A	N/A	☐
TN3 CT	A	A	N/A	☐

8. FINAL CHECKS

All Test equipment, leads, shorts, test blocks and other test wiring removed?	Yes	☐	No	☐	N/A	☐
Disturbed customer wiring re-checked?	Yes	☐	No	☐	N/A	☐
All commissioning tests disabled?	Yes	☐	No	☐		
Test mode disabled?	Yes	☐	No	☐		
Circuit breaker operations counter reset?	Yes	☐	No	☐	N/A	☐
Current counters reset?	Yes	☐	No	☐	N/A	☐
Event records reset?	Yes	☐	No	☐		
Fault records reset?	Yes	☐	No	☐		
Disturbance records reset?	Yes	☐	No	☐		
Alarms reset?	Yes	☐	No	☐		
LEDs reset?	Yes	☐	No	☐		
Secondary front cover replaced?	Yes	☐	No	☐	N/A	☐

COMMENTS #
(# Optional, for site observations or utility-specific notes).

Commissioning Engineer
Date:

Customer Witness
Date:

2 CREATING A SETTING RECORD

You often need to create a record of what settings have been applied to a device. In the past, you could have used paper printouts of all the available settings, and mark up the ones you had used. Keeping such a paper-based Settings Records can be time-consuming and prone to error (e.g. due to being settings written down incorrectly).

The Easergy Studio software lets you read/write MiCOM devices.

- **Extract** lets you download all the settings from a MiCOM Px40 device. A summary is given in Extract Settings from a MiCOM Px40 Device below.
- **Send** lets you send the settings you currently have open in the Easergy Studio software. A summary is given in Send Settings to a MiCOM Px40 Device below.

The Easergy Studio product is updated periodically. These updates provide support for new features (such as allowing you to manage new MiCOM products, as well as using new software releases and hardware suffixes). The updates may also include fixes. **Accordingly, we strongly advise customers to use the latest Schneider Electric version of Easergy Studio.**

In most cases, it will be quicker and less error prone to extract settings electronically and store them in a settings file on a memory stick. In this way, there will be a digital record which is certain to be accurate. It is also possible to archive these settings files in a repository; so they can be used again or adapted for another use.

Full details of how to do these tasks is provided in the Easergy Studio help.

A quick summary of the main steps is given below.

In each case you need to make sure that:

- Your computer includes the Easergy Studio software.
- Your computer and the MiCOM device are powered on.
- You have used a suitable cable to connect your computer to the MiCOM device (Front Port, Rear Port, Ethernet port or Modem as available).

2.1 Extract Settings from a MiCOM Px40 Device

Full details of how to do this is provided in the Easergy Studio help.

As a quick guide, you need to do the following:

1. In Easergy Studio, click the Quick Connect… button.
2. Select the relevant Device Type in the Quick Connect dialog box.
3. Click the relevant port in the Port Selection dialog box.
4. Enter the relevant connection parameters in the Connection Parameters dialog box and click the Finish button
5. Easergy Studio will try to communicate with the Px40 device. It will display a connected message if the connection attempt is successful.
6. The device will appear in the Studio Explorer pane on the top-left of the interface.
7. Click the + button to expand the options for the device, then click on the Settings folder.
8. Right-click on Settings and select the Extract Settings link to read the settings on the device and store them on your computer or a memory stick.
9. After retrieving the settings file, close the dialog box by clicking the Close button.

2.2 Send Settings to a MiCOM Px40 Device

Full details of how to do this is provided in the Easergy Studio help.

As a quick guide, you need to do the following:

1. In Easergy Studio, click the Quick Connect… button.
2. Select the relevant Device Type in the Quick Connect dialog box.
3. Click the relevant port in the Port Selection dialog box.
4. Enter the relevant connection parameters in the Connection Parameters dialog box and click the Finish button
5. Easergy Studio will try to communicate with the Px40 device. It will display a connected message if the connection attempt is successful.
6. The device will appear in the Studio Explorer pane on the top-left hand side of the interface.
7. Click the + button to expand the options for the device and then right-click on the Settings link.
8. To add an existing file, right-click the settings folder and choose Add Existing File.
9. To create a new file, right-click the settings folder and select Add. A file with the next sequential number will be created. Double-click the file to edit.
10. Right-click on the device name and select the Send link.

Note	*When you send settings to a MiCOM Px40 device, the data is stored in a temporary location at first. This temporary data is tested to make sure it is complete. If the temporary data is complete, it will be programmed into the MiCOM Px40 device. This avoids the risk of a device being programmed with incomplete or corrupt settings.*

11. In the Send To dialog box, select the settings file(s) you wish to send, then click the Send button.
12. Close the Send To dialog box by clicking the Close button.

MAINTENANCE

CHAPTER 13

Date:	09/2016	
Products covered by this chapter:	This chapter covers the specific versions of the MiCOM products listed below. This includes ***only*** the following combinations of Software Version and Hardware Suffix.	
Hardware suffix:	All MiCOM Px4x products	
Software version:	All MiCOM Px4x products	
Connection diagrams:	P14x (P141, P142, P143 & P145): 10P141xx (xx = 01 to 02) 10P142xx (xx = 01 to 05) 10P143xx (xx = 01 to 11) 10P145xx (xx = 01 to 11) P24x (P241, P242 & P243): 10P241xx (xx = 01 to 02) 10P242xx (xx = 01) 10P243xx (xx = 01) P34x (P342, P343, P344, P345 & P391): 10P342xx (xx = 01 to 17) 10P343xx (xx = 01 to 19) 10P344xx (xx = 01 to 12) 10P345xx (xx = 01 to 07) 10P391xx (xx = 01 to 02) P445: 10P445xx (xx = 01 to 04) P44x (P441, P442 & P444): 10P44101 (SH 1 & 2) 10P44201 (SH 1 & 2) 10P44202 (SH 1) 10P44203 (SH 1 & 2) 10P44401 (SH 1) 10P44402 (SH 1) 10P44403 (SH 1 & 2) 10P44404 (SH 1) 10P44405 (SH 1) 10P44407 (SH 1 & 2) P44y (P443 & P446): 10P44303 (SH 01 and 03) 10P44304 (SH 01 and 03) 10P44305 (SH 01 and 03) 10P44306 (SH 01 and 03) 10P44600 10P44601 (SH 1 to 2) 10P44602 (SH 1 to 2) 10P44603 (SH 1 to 2)	P54x (P543, P544, P545 & P546): 10P54302 (SH 1 to 2) 10P54303 (SH 1 to 2) 10P54400 10P54404 (SH 1 to 2) 10P54405 (SH 1 to 2) 10P54502 (SH 1 to 2) 10P54503 (SH 1 to 2) 10P54600 10P54604 (SH 1 to 2) 10P54605 (SH 1 to 2) 10P54606 (SH 1 to 2) P547: 10P54702xx (xx = 01 to 02) 10P54703xx (xx = 01 to 02) 10P54704xx (xx = 01 to 02) 10P54705xx (xx = 01 to 02) P64x (P642, P643 & P645): 10P642xx (xx = 1 to 10) 10P643xx (xx = 1 to 6) 10P645xx (xx = 1 to 9) P74x (P741, P742 & P743): 10P740xx (xx = 01 to 07) P746: 10P746xx (xx = 00 to 21) P841: 10P84100 10P84101 (SH 1 to 2) 10P84102 (SH 1 to 2) 10P84103 (SH 1 to 2) 10P84104 (SH 1 to 2) 10P84105 (SH 1 to 2) P849: 10P849xx (xx = 01 to 06)

CONTENTS

Page (MT) 13-

Notes:

1 MAINTENANCE PERIOD

Warning **Before inspecting any wiring, performing any tests or carrying out any work on the equipment, you should be familiar with the contents of the Safety Information and Technical Data sections and the information on the equipment's rating label.**

It is recommended that products supplied by Schneider Electric receive periodic monitoring after installation. In view of the critical nature of protective and control equipment, and their infrequent operation, it is desirable to confirm that they are operating correctly at regular intervals.

Schneider Electric protection and control equipment is designed for a life in excess of 20 years.

MiCOM relays are self-supervising and so require less maintenance than earlier designs. Most problems will result in an alarm so that remedial action can be taken. However, some periodic tests should be done to ensure that the equipment is functioning correctly and the external wiring is intact.

If the customer's organization has a preventative maintenance policy, the recommended product checks should be included in the regular program. Maintenance periods depend on many factors, such as:

- The operating environment
- The accessibility of the site
- The amount of available manpower
- The importance of the installation in the power system
- The consequences of failure

2 MAINTENANCE CHECKS

Although some functionality checks can be performed from a remote location by using the communications ability of the equipment, these are predominantly restricted to checking that the equipment, is measuring the applied currents and voltages accurately, and checking the circuit breaker maintenance counters. Therefore it is recommended that maintenance checks are performed locally (i.e. at the equipment itself).

Warning **Before carrying out any work on the equipment, you should be familiar with the contents of the Safety Information chapter/Safety Guide SFTY/5L M/L11 or later issue, the Technical Data chapter and the ratings on the equipment rating label.**

Warning **If a P391 is used, you should also be familiar with the ratings and warning statements in the P391 technical manual.**

2.1 Alarms

The alarm status LED should first be checked to identify if any alarm conditions exist. If so, press the read key (⏎) repeatedly to step through the alarms.

Clear the alarms to extinguish the LED.

2.2 Opto-Isolators

The opto-isolated inputs can be checked to ensure that the equipment responds to energization by repeating the commissioning test detailed in the Commissioning chapter.

2.3 Output Relays

The output relays can be checked to ensure that they operate by repeating the commissioning test detailed in the Commissioning chapter.

2.4 Measurement Accuracy

If the power system is energized, the values measured by the equipment can be compared with known system values to check that they are in the approximate range that is expected. If they are, the analog/digital conversion and calculations are being performed correctly by the relay. Suitable test methods can be found in the Commissioning chapter.

Alternatively, the values measured by the equipment can be checked against known values injected via the test block, if fitted, or injected directly into the equipment terminals. Suitable test methods can be found in the Commissioning chapter. These tests will prove the calibration accuracy is being maintained.

3 METHOD OF REPAIR

If the equipment should develop a fault whilst in service, depending on the nature of the fault, the watchdog contacts will change state and an alarm condition will be flagged. Due to the extensive use of surface-mount components, faulty Printed Circuit Boards (PCBs) should be replaced, as it is not possible to perform repairs on damaged PCBs. Therefore either the complete equipment module or just the faulty PCB (as identified by the in-built diagnostic software), can be replaced. Advice about identifying the faulty PCB can be found in the Troubleshooting chapter.

The preferred method is to replace the complete equipment module as it ensures that the internal circuitry is protected against electrostatic discharge and physical damage at all times and overcomes the possibility of incompatibility between replacement PCBs. However, it may be difficult to remove installed equipment due to limited access in the back of the cubicle and the rigidity of the scheme wiring.

Replacing PCBs can reduce transport costs but requires clean, dry conditions on site and higher skills from the person performing the repair. If the repair is not performed by an approved service center, the warranty will be invalidated.

Warning **Before carrying out any work on the equipment, you should be familiar with the contents of the Safety Information chapter/Safety Guide SFTY/5L M/L11 or later issue, the Technical Data chapter and the ratings on the equipment rating label.**

This should ensure that no damage is caused by incorrect handling of the electronic components.

3.1 Replacing the Complete Equipment IED/Relay

The case and rear terminal blocks have been designed to facilitate removal of the IED/relay should replacement or repair become necessary without having to disconnect the scheme wiring.

Warning **Before working at the rear of the equipment, isolate all voltage and current supplies to the equipment.**

Note *The MiCOM range has integral current transformer shorting switches which will close when the heavy duty terminal block is removed.*

1. Disconnect the equipment's earth, IRIG-B and fiber optic connections, as appropriate, from the rear of the device.

   There are two types of terminal block used on the equipment, medium and heavy duty, which are fastened to the rear panel using Pozidriv or PZ1 screws. The P24x/P34x/P64x ranges also includes an RTD/CLIO terminal block option. These block types are shown in the ***Commissioning*** chapter.

Important *The use of a magnetic bladed screwdriver is recommended to minimize the risk of the screws being left in the terminal block or lost.*

2. Without exerting excessive force or damaging the scheme wiring, pull the terminal blocks away from their internal connectors.
3. Remove the screws used to fasten the equipment to the panel, rack, etc. These are the screws with the larger diameter heads that are accessible when the access covers are fitted and open.

Warning **If the top and bottom access covers have been removed, do not remove the screws with the smaller diameter heads which are accessible. These screws secure the front panel to the equipment.**

4. Withdraw the equipment carefully from the panel, rack, etc. because it will be heavy due to the internal transformers.

To reinstall the repaired or replacement equipment, follow the above instructions in reverse, ensuring that each terminal block is relocated in the correct position and the case earth, IRIG-B and fiber optic connections are replaced. To facilitate easy identification of each terminal block, they are labeled alphabetically with 'A' on the left-hand side when viewed from the rear.

Once reinstallation is complete, the equipment should be re-commissioned using the instructions in the Commissioning chapter.

3.2 Replacing a PCB

Replacing PCBs and other internal components must be undertaken only by Service Centers approved by Schneider Electric. Failure to obtain the authorization of Schneider Electric after sales engineers prior to commencing work may invalidate the product warranty.

Warning **Before removing the front panel to replace a PCB, remove the auxiliary supply and wait at least 30 seconds for the capacitors to discharge.**
We strongly recommend that the voltage and current transformer connections and trip circuit are isolated.

Schneider Electric support teams are available world-wide. We strongly recommend that any repairs be entrusted to those trained personnel. For this reason, details on product disassembly and re-assembly are not included here.

4 RE-CALIBRATION

Re-calibration is not required when a PCB is replaced **unless it happens to be one of the boards in the input module;** the replacement of either directly affects the calibration.

Warning **Although it is possible to carry out re-calibration on site, this requires test equipment with suitable accuracy and a special calibration program to run on a PC. It is therefore recommended that the work be carried out by the manufacturer, or entrusted to an approved service center.**

5 CHANGING THE BATTERY

Each relay/IED has a battery to maintain status data and the correct time when the auxiliary supply voltage fails. The data maintained includes event, fault and disturbance records and the thermal state at the time of failure.

This battery will periodically need changing, although an alarm will be given as part of the relay's/IED's continuous self-monitoring in the event of a low battery condition.

If the battery-backed facilities are not required to be maintained during an interruption of the auxiliary supply, the steps below can be followed to remove the battery, but do not replace with a new battery.

Warning **Before carrying out any work on the equipment, you should be familiar with the contents of the Safety Information chapter/Safety Guide SFTY/5L M/L11 or later issue, the Technical Data chapter and the ratings on the equipment rating label.**

5.1 Instructions for Replacing the Battery

1. Open the bottom access cover on the front of the equipment.
2. Gently extract the battery from its socket. If necessary, use a small, insulated screwdriver to prize the battery free.
3. Ensure that the metal terminals in the battery socket are free from corrosion, grease and dust.
4. The replacement battery should be removed from its packaging and placed into the battery holder, taking care to ensure that the polarity markings on the battery agree with those adjacent to the socket.

Note *Only use a type ½AA Lithium battery with a nominal voltage of 3.6 V and safety approvals such as UL (Underwriters Laboratory), CSA (Canadian Standards Association) or VDE (Vereinigung Deutscher Elektrizitätswerke).*

5. Ensure that the battery is securely held in its socket and that the battery terminals are making good contact with the metal terminals of the socket.
6. Close the bottom access cover.

5.2 Post Modification Tests

To ensure that the replacement battery will maintain the time and status data if the auxiliary supply fails, check cell [0806: DATE and TIME, Battery Status] reads 'Healthy'. If further confirmation that the replacement battery is installed correctly is required, the commissioning test is described in the Commissioning chapter, 'Date and Time', can be performed.

5.3 Battery Disposal

The battery that has been removed should be disposed of in accordance with the disposal procedure for Lithium batteries in the country in which the equipment is installed.

6 CLEANING

Warning **Before cleaning the equipment ensure that all ac and dc supplies, current transformer and voltage transformer connections are isolated to prevent any chance of an electric shock whilst cleaning.**

The equipment may be cleaned using a lint-free cloth moistened with clean water. The use of detergents, solvents or abrasive cleaners is not recommended as they may damage the relay's surface and leave a conductive residue.

TROUBLESHOOTING

CHAPTER 14

Date:	09/2016	
Products covered by this chapter:	This chapter covers the specific versions of the MiCOM products listed below. This includes ***only*** the following combinations of Software Version and Hardware Suffix.	
Hardware Suffix:	All MiCOM Px4x products	
Software Version:	All MiCOM Px4x products	
Connection Diagrams:	P14x (P141, P142, P143 & P145): 10P141xx (xx = 01 to 02) 10P142xx (xx = 01 to 05) 10P143xx (xx = 01 to 11) 10P145xx (xx = 01 to 11) P24x (P241, P242 & P243): 10P241xx (xx = 01 to 02) 10P242xx (xx = 01) 10P243xx (xx = 01) P34x (P342, P343, P344, P345 & P391): 10P342xx (xx = 01 to 17) 10P343xx (xx = 01 to 19) 10P344xx (xx = 01 to 12) 10P345xx (xx = 01 to 07) 10P391xx (xx = 01 to 02) P445: 10P445xx (xx = 01 to 04) P44x(P442 & P444): 10P44101 (SH 1 & 2) 10P44201 (SH 1 & 2) 10P44202 (SH 1) 10P44203 (SH 1 & 2) 10P44401 (SH 1) 10P44402 (SH 1) 10P44403 (SH 1 & 2) 10P44404 (SH 1) 10P44405 (SH 1) 10P44407 (SH 1 & 2) P44y (P443 & P446): 10P44303 (SH 01 and 03) 10P44304 (SH 01 and 03) 10P44305 (SH 01 and 03) 10P44306 (SH 01 and 03) 10P44600 10P44601 (SH 1 to 2) 10P44602 (SH 1 to 2) 10P44603 (SH 1 to 2)	P54x (P543, P544, P545 & P546): 10P54302 (SH 1 to 2) 10P54303 (SH 1 to 2) 10P54400 10P54404 (SH 1 to 2) 10P54405 (SH 1 to 2) 10P54502 (SH 1 to 2) 10P54503 (SH 1 to 2) 10P54600 10P54604 (SH 1 to 2) 10P54605 (SH 1 to 2) 10P54606 (SH 1 to 2) P547: 10P54702xx (xx = 01 to 02) 10P54703xx (xx = 01 to 02) 10P54704xx (xx = 01 to 02) 10P54705xx (xx = 01 to 02) P64x (P642, P643 & P645): 10P642xx (xx = 1 to 10) 10P643xx (xx = 1 to 6) 10P645xx (xx = 1 to 9) P74x (P741, P742 & P743): 10P740xx (xx = 01 to 07) P746: 10P746xx (xx = 00 to 21) P841: 10P84100 10P84101 (SH 1 to 2) 10P84102 (SH 1 to 2) 10P84103 (SH 1 to 2) 10P84104 (SH 1 to 2) 10P84105 (SH 1 to 2) P849: 10P849xx (xx = 01 to 06)

CONTENTS

TABLES

Notes:

1 INTRODUCTION

Warning **Before carrying out any work on the equipment, you should be familiar with the contents of the Safety Information chapter/Safety Guide SFTY/5L M/L11 or later issue, the Technical Data chapter and the ratings on the equipment rating label.**

The purpose of this chapter of the service manual is to allow an error condition on the relay to be identified so that appropriate corrective action can be taken.

If the relay has developed a fault, it should be possible in most cases to identify which relay module requires attention. The *Maintenance* chapter advises on the recommended method of repair where faulty modules need replacing. It is not possible to perform an on-site repair to a faulted module.

In cases where a faulty relay/module is being returned to the manufacturer or one of their approved service centers, completed copy of the Repair/Modification Return Authorization Form located at the end of this chapter should be included.

2 INITIAL PROBLEM IDENTIFICATION

Consult the following table to find the description that best matches the problem experienced, then consult the section referenced to perform a more detailed analysis of the problem.

Symptom	Refer To
Relay fails to power up	Power-Up Errors section
Relay powers up - but indicates error and halts during power-up sequence	Error Message/Code On Power-Up section
Relay Powers up but Out of Service LED is illuminated	Out of Service LED illuminated on Power Up section
Error during normal operation	Error Code During Operation section
Mal-operation of the relay during testing	Mal-Operation of the Relay during Testing section

Table 1 - Problem identification

3 POWER UP ERRORS

If the relay does not appear to power up then the following procedure can be used to determine whether the fault is in the external wiring, auxiliary fuse, power supply module of the relay or the relay front panel.

Test	Check	Action
1	Measure auxiliary voltage on terminals 1 and 2; verify voltage level and polarity against rating the label on front. Terminal 1 is –dc, 2 is +dc	If auxiliary voltage is present and correct, then proceed to test 2. Otherwise the wiring/fuses in auxiliary supply should be checked.
2	Do LEDs/and LCD backlight illuminate on power-up, also check the N/O watchdog contact for closing.	If they illuminate or the contact closes and no error code is displayed then error is probably in the main processor board (front panel). If they do not illuminate and the contact does not close then proceed to test 3.
3	Check Field voltage output (nominally 48V DC)	If field voltage is not present then the fault is probably in the relay power supply module.

Table 2 - Failure of relay to power up

4 ERROR MESSAGE/CODE ON POWER-UP

During the power-up sequence of the relay self-testing is performed as indicated by the messages displayed on the LCD. If an error is detected by the relay during these self-tests, an error message will be displayed and the power-up sequence will be halted. If the error occurs when the relay application software is executing, a maintenance record will be created and the relay will reboot.

Test	Check	Action
1	Is an error message or code permanently displayed during power up?	If relay locks up and displays an error code permanently then proceed to Test 2. If the relay prompts for input by the user proceed to Test 4. If the relay re-boots automatically then proceed to Test 5.
2	Record displayed error, then remove and re-apply relay auxiliary supply.	Record whether the same error code is displayed when the relay is rebooted. If no error code is displayed then contact the local service center stating the error code and relay information. If the same code is displayed proceed to Test 3.
3	Error code Identification Following text messages (in English) will be displayed if a fundamental problem is detected preventing the system from booting: Bus Fail address lines SRAM Fail data lines FLASH Fail format error FLASH Fail checksum Code Verify Fail These hex error codes relate to errors detected in specific relay modules: 0c140005/0c0d0000 0c140006/0c0e0000 Last 4 digits provide details on the actual error.	These messages indicate that a problem has been detected on the main processor board of the relay (located in the front panel). Input Module (inc. Opto-isolated inputs) Output Relay Cards Other error codes relate to problems within the main processor board hardware or software. It will be necessary to contact Schneider Electric with details of the problem for a full analysis.
4	Relay displays message for corrupt settings and prompts for restoration of defaults to the affected settings.	The power up tests have detected corrupted relay settings, it is possible to restore defaults to allow the power-up to be completed. It will then be necessary to re-apply the application-specific settings.
5	Relay resets on completion of power up - record error code displayed	Error 0x0E080000, Programmable Scheme Logic (PSL) error due to excessive execution time. Restore default settings by performing a power up with ◊ and ◊ keys depressed, confirm restoration of defaults at prompt using (↵) key. If relay powers up successfully, check PSL for feedback paths. Other error codes will relate to software errors on the main processor board, contact Schneider Electric.

Table 3 - Power-up self-test error

5 OUT OF SERVICE LED ILLUMINATED ON POWER UP

Test	Check	Action	
1	Using the relay menu confirm whether the Commission Test/Test Mode setting is Contact Blocked. Otherwise proceed to test 2.	If the setting is Contact Blocked then disable the test mode and, verify that the Out of Service LED is extinguished.	
2	Select and view the last maintenance record from the menu (in the View Records).	Check for H/W Verify Fail this indicates a discrepancy between the relay model number and the hardware; examine the "**Maint. Data**", this indicates the causes of the failure using bit fields:	
		Bit	**Meaning**
		0	The application type field in the model number does not match the software ID
		1	The application field in the model number does not match the software ID
		2	The variant 1 field in the model number does not match the software ID
		3	The variant 2 field in the model number does not match the software ID
		4	The protocol field in the model number does not match the software ID
		5	The language field in the model number does not match the software ID
		6	The VT type field in the model number is incorrect (110V VTs fitted)
		7	The VT type field in the model number is incorrect (440V VTs fitted)
		8	The VT type field in the model number is incorrect (no VTs fitted)

Table 4 - Out of service LED illuminated

6 ERROR CODE DURING OPERATION

The relay performs continuous self-checking, if an error is detected then an error message will be displayed, a maintenance record will be logged and the relay will reset (after a 1.6 second delay). A permanent problem (for example due to a hardware fault) will generally be detected on the power up sequence, following which the relay will display an error code and halt. If the problem was transient in nature then the relay should reboot correctly and continue in operation. The nature of the detected fault can be determined by examination of the maintenance record logged.

There are also two cases where a maintenance record will be logged due to a detected error where the relay will not reset. These are detection of a failure of either the field voltage or the lithium battery, in these cases the failure is indicated by an alarm message, however the relay will continue to operate.

If the field voltage is detected to have failed (the voltage level has dropped below threshold), then a scheme logic signal is also set. This allows the scheme logic to be adapted in the case of this failure (for example if a blocking scheme is being used).

In the case of a battery failure it is possible to prevent the relay from issuing an alarm using the setting under the Date and Time section of the menu. This setting '**Battery Alarm**' can be set to '**Disabled**' to allow the relay to be used without a battery, without an alarm message being displayed.

In the case of an RTD board failure, an alarm "RTD board fail" message is displayed, the RTD protection is disabled, but the operation of the rest of the relay functionality is unaffected.

7 MAL-OPERATION OF THE RELAY DURING TESTING

7.1 Failure of Output Contacts

An apparent failure of the relay output contacts may be caused by the relay configuration; the following tests should be performed to identify the real cause of the failure.

Note	*The relay self-tests verify that the coil of the contact has been energized, an error will be displayed if there is a fault in the output relay board.*

Test	Check	Action
1	Is the Out of Service LED illuminated?	Illumination of this LED may indicate that the relay is Contact Blocked or that the protection has been disabled due to a hardware verify error (see the *Out of service LED illuminated* table..
2	Examine the Contact status in the Commissioning section of the menu.	If the relevant bits of the contact status are operated, proceed to test 4, if not proceed to test 3.
3	Verify by examination of the fault record or by using the test port whether the protection element is operating correctly.	If the protection element does not operate verify whether the test is being correctly applied. If the protection element does operate, it will be necessary to check the PSL to ensure that the mapping of the protection element to the contacts is correct.
4	Using the Commissioning/Test mode function apply a test pattern to the relevant relay output contacts and verify whether they operate (note the correct external connection diagram should be consulted). A continuity tester can be used at the rear of the relay for this purpose.	If the output relay does operate, the problem must be in the external wiring to the relay. If the output relay does not operate this could indicate a failure of the output relay contacts (note that the self-tests verify that the relay coil is being energized). Ensure that the closed resistance is not too high for the continuity tester to detect.

Table 5 - Failure of output contacts

7.2 Failure of Opto-Isolated Inputs

The opto-isolated inputs are mapped onto the relay internal signals using the PSL. If an input does not appear to be recognized by the relay scheme logic the Commission Tests/Opto Status menu option can be used to verify whether the problem is in the opto-isolated input itself or the mapping of its signal to the scheme logic functions. If the opto-isolated input does appear to be read correctly then it will be necessary to examine its mapping within the PSL.

Ensure the voltage rating for the opto inputs has been configured correctly with applied voltage. If the opto-isolated input state is not being correctly read by the relay the applied signal should be tested. Verify the connections to the opto-isolated input using the correct wiring diagram and the correct nominal voltage settings in any standard or custom menu settings. Next, using a voltmeter verify that 80% opto setting voltage is present on the terminals of the opto-isolated input in the energized state. If the signal is being correctly applied to the relay then the failure may be on the input card itself. Depending on which opto-isolated input has failed this may require replacement of either the complete analog input module (the board within this module cannot be individually replaced without re-calibration of the relay) or a separate opto board.

7.3 Incorrect Analog Signals

The measurements may be configured in primary or secondary to assist. If it is suspected that the analog quantities being measured by the relay are not correct then the measurement function of the relay can be used to verify the nature of the problem. The measured values displayed by the relay should be compared with the actual magnitudes at the relay terminals. Verify that the correct terminals are being used (in particular the dual rated CT inputs) and that the CT and VT ratios set on the relay are correct. The correct 120 degree displacement of the phase measurements should be used to confirm that the inputs have been correctly connected.

7.4 PSL Editor Troubleshooting

A failure to open a connection could be because of one or more of the following:

- The relay address is not valid (note: this address is always 1 for the front port).
- Password is not valid
- Communication Set-up - COM port, Baud rate, or Framing - is not correct
- Transaction values are not suitable for the relay and/or the type of connection
- Modem configuration is not valid. Changes may be necessary when using a modem
- The connection cable is not wired correctly or broken. See MiCOM S1 connection configurations
- The option switches on any KITZ101/102 that is in use may be incorrectly set

7.4.1 Diagram Reconstruction after Recover from Relay

Although the extraction of a scheme from a relay is supported, the facility is provided as a way of recovering a scheme in the event that the original file is unobtainable.

The recovered scheme will be logically correct, but much of the original graphical information is lost. Many signals will be drawn in a vertical line down the left side of the canvas. Links are drawn orthogonally using the shortest path from A to B.

Any annotation added to the original diagram (titles, notes, etc.) are lost.

Sometimes a gate type may not be what was expected, e.g. a 1-input AND gate in the original scheme will appear as an OR gate when uploaded. Programmable gates with an inputs-to-trigger value of 1 will also appear as OR gates.

7.4.2 PSL Version Check

The PSL is saved with a version reference, time stamp and CRC check. This gives a visual check whether the default PSL is in place or whether a new application has been downloaded.

8 REPAIR AND MODIFICATION PROCEDURE

Please follow these steps to return an Automation product to us:

1. Get the Repair and Modification Authorization Form (RMA).

   A copy of the RMA form is shown at the end of this section.

2. Fill in the RMA form.

   Fill in only the white part of the form.

   Please ensure that all fields marked **(M)** are completed such as:

   - Equipment model
   - Model No. and Serial No.
   - Description of failure or modification required (please be specific)
   - Value for customs (in case the product requires export)
   - Delivery and invoice addresses
   - Contact details

3. Receive from local service contact, the information required to ship the product.

   Your local service contact will provide you with all the information:

   - Pricing details
   - RMA No
   - Repair center address

   If required, an acceptance of the quote must be delivered before going to next stage.

4. Send the product to the repair center.

   Address the shipment to the repair center specified by your local contact.

   Ensure all items are protected by appropriate packaging: anti-static bag and foam protection.

   Ensure a copy of the import invoice is attached with the unit being returned.

   Ensure a copy of the RMA form is attached with the unit being returned.

   E-mail or fax a copy of the import invoice and airway bill document to your local contact.

Notes:

REPAIR/MODIFICATION RETURN AUTHORIZATION FORM

FIELDS IN GREY TO BE FILLED IN BY SCHNEIDER ELECTRIC PERSONNEL ONLY

Reference **RMA:**		Date:
Repair Center Address (for shipping)	**Service Type** ☐ Retrofit ☐ Warranty ☐ Paid service ☐ Under repair contract ☐ Wrong supply	LSC PO No.:
Schneider Electric - Local Contact Details Name: Telephone No.: Fax No.: E-mail:		

IDENTIFICATION OF UNIT

Fields marked (M) are mandatory, delays in return will occur if not completed.

Model No./Part No.: **(M)**	Site Name/Project:
Manufacturer Reference: **(M)**	Commissioning Date:
Serial No.: **(M)**	Under Warranty: ☐ Yes ☐ No
Software Version:	Additional Information:
Quantity:	Customer P.O (if paid):

FAULT INFORMATION

Type of Failure		**Found Defective**	
Hardware fail	☐	During FAT/inspection	☐
Mechanical fail/visible defect	☐	On receipt	☐
Software fail	☐	During installation/commissioning	☐
Other:		During operation	☐
		Other:	

Fault Reproducibility

Fault persists after removing, checking on test bench	☐
Fault persists after re-energization	☐
Intermittent fault	☐

Description of Failure Observed or Modification Required - *Please be specific* **(M)**

FOR REPAIRS ONLY

Would you like us to install an updated firmware version after repair? ☐ Yes ☐ No

CUSTOMS & INVOICING INFORMATION

Required to allow return of repaired items

Value for Customs (M)	
Customer Invoice Address ((M) if paid)	**Customer Return Delivery Address (full street address) (M)** Part shipment accepted ☐ Yes ☐ No **OR** Full shipment required ☐ Yes ☐ No
Contact Name: Telephone No.: Fax No.: E-mail:	Contact Name: Telephone No.: Fax No.: E-mail:

REPAIR TERMS

1. **Please ensure that a copy of the import invoice is attached with the returned unit, together with the airway bill document.** Please fax/e-mail a copy of the appropriate documentation **(M)**.
2. Please ensure the Purchase Order is released, for paid service, to allow the unit to be shipped.
3. Submission of equipment to Schneider Electric is deemed as authorization to repair and acceptance of quote.
4. Please ensure all items returned are marked as Returned for 'Repair/Modification' and **protected by appropriate packaging** (anti-static bag for each board and foam protection).

SCADA COMMUNICATIONS

CHAPTER 15

Date:	07/2018
Products covered by this chapter:	This chapter covers the specific versions of the MiCOM products listed below. This includes ***only*** the following combinations of Software Version and Hardware Suffix.
Hardware Suffix:	L (P642) M (P643/P645)
Software Version:	B4 - P64x (P642, P643 & P645)
Connection Diagrams:	10P642xx (xx = 01 to 10) 10P643xx (xx = 01 to 06) 10P645xx (xx = 01 to 09)

CONTENTS

FIGURES

TABLES

Notes:

1 INTRODUCTION

This chapter describes the remote interfaces of the MiCOM relay in enough detail to allow integration in a substation communication network. The relay supports a choice of one of a number of protocols through the rear 2-wire EIA(RS)485 communication interface, selected using the model number when ordering. This is in addition to the front serial interface and second rear communications port, which supports the Courier protocol only. According to the protocol and hardware options selected, the interface may alternatively be presented over an optical fiber interface, or via an Ethernet connection.

The supported protocols include:

- Courier
- IEC-60870-5-103
- DNP3.0
- MODBUS
- IEC 61850 Ethernet Interface

Note	*The IEC 60870-5-103 standard may be abbreviated to IEC870-5-103, IEC 60870, or even -103. In some references, it may even be described as the 'VDEW' standard.*

Table 1 – Supported protocols

The implementation of both Courier and IEC 60870-5-103 on RP1 can also, optionally, be presented over fiber as well as EIA(RS)485.

The DNP3.0 implementation is available via the EIA(RS)485 port.

The rear EIA(RS)-485 interface is isolated and is suitable for permanent connection whichever protocol is selected. The advantage of this type of connection is that up to 32 relays can be daisy-chained together using a simple twisted-pair electrical connection.

Note	*The second rear Courier port and the fiber optic interface are mutually exclusive as they occupy the same physical slot.*

The rear EIA(RS)485 interface is isolated and is suitable for permanent connection whichever protocol is selected. The advantage of this type of connection is that up to 32 relays can be '**daisy chained**' together using a simple twisted pair electrical connection.

It should be noted that the descriptions contained within this section do not aim to fully detail the protocol itself. The relevant documentation for the protocol should be referred to for this information. This section serves to describe the specific implementation of the protocol in the relay.

2 CONNECTIONS TO THE COMMUNICATION PORTS

2.1 Front Port

The front communications port is not intended for permanent connection. The front communications port supports the Courier protocol and is implemented on an EIA(RS)232 connection. A 9-pin connector type, as described in the 'Getting Started' (GS) chapter of this manual, is used, and the cabling requirements are detailed in the 'Connection Diagrams' (CD) chapter of this manual.

2.2 Rear Communication Port EIA(RS)-485

The rear EIA(RS)-485 communication port is provided by a 3-terminal screw connector on the back of the relay. See the Connection Diagrams chapter for details of the connection terminals. The rear port provides K-Bus/EIA(RS)-485 serial data communication and is intended for use with a permanently-wired connection to a remote control center. Of the three connections, two are for the signal connection, and the other is for the earth shield of the cable.

If the IEC60870-5-103, or the DNP3.0 protocols are specified as the interface for the rear port, then connections conform entirely to the EIA(RS)485 standards outline below. If, however, the Courier protocol is specified as the rear port protocol, then the interface can be set either to EIA(RS)485 or K-Bus. The configuration of the port as either EIA(RS)485 or K-Bus is described later together with K-Bus details, but as connection to the port is affected by this choice, the following points should be noted:

- Connection to an EIA(RS)485 device is polarity sensitive, whereas K-Bus connection is not.
- Whilst connection to between an EIA(RS)485 port and an EIA(RS)232 port on, say, a PC might be implemented using a general purpose EIA(RS)485 to EIA(RS)232 converter, connection between an EIA(RS)232 port and K-Bus requires a KITZ101, KITZ102 or KITZ201

Unless the K-Bus option is chosen for the rear port, correct polarity must be observed for the signal connections. In all other respects (bus wiring, topology, connection, biasing and termination) K-Bus can be considered the same as EIA(RS)485.

All rear port communication interfaces are fully isolated and suitable for permanent connection. EIA(RS)485 (and K-Bus) connections allow up to 32 devices to be 'daisy-chained' together using a simple twisted pair electrical connection.

The protocol provided by the relay is shown in the relay menu in the **Communications** column. Using the keypad and LCD, first check that the **Comms. settings** cell in the **Configuration** column is set to **Visible**, then move to the **Communications** column. The first cell down the column shows the communication protocol being used by the rear port.

Note	*Unless the K-Bus option is chosen for the rear port, correct polarity must be observed for the signal connections. In all other respects (bus wiring, topology, connection, biasing and termination) K-Bus can be considered the same as EIA(RS)485.*

2.3 Second Rear Communications Port (RP2) (Courier)

Relays with Courier, MODBUS, IEC60870-5-103 or DNP3.0 protocol on the first rear communications port have the option of a second rear port, running the Courier language. The second port is intended typically for dial-up modem access by protection engineers or operators, when the main port is reserved for SCADA communication traffic. Communication is through one of three physical links: K-Bus, EIA(RS)-485 or EIA(RS)-232. The port supports full local or remote protection and control access using MiCOM S1 Studio.

When changing the port configuration between K-Bus, EIA(RS)-485 and EIA(RS)-232, reboot the relay to update the hardware configuration of the second rear port.

The EIA(RS)-485 and EIA(RS)-232 protocols can be configured to operate with a modem, using an IEC60870 10-bit frame.

If both rear communications ports are connected to the same bus, make sure their address settings are not the same to avoid message conflicts.

Port Configuration	Valid Communication Protocol
K-Bus	K-Bus
EIA(RS)-232	IEC60870 FT1.2, 11-bit frame IEC60870, 10-bit frame
EIA(RS)-485	IEC60870 FT1.2, 11-bit frame IEC60870, 10-bit frame

Table 2 - Port configurations and communication protocols

2.3.1 Courier Protocol

The second rear communications port is functionally the same as described in the previous section for a Courier rear communications port, with the following exceptions:

2.3.1.1 Event Extraction

Automatic event extraction is not supported when the first rear port protocol is Courier, MODBUS or CS103. It is supported when the first rear port protocol is DNP3.0.

2.3.1.2 Disturbance Record Extraction

Automatic disturbance record extraction is not supported when the first rear port protocol is Courier, MODBUS or CS103. It is supported when the first rear port protocol is DNP3.0.

2.3.1.3 Connection to the Second Rear Port

The second rear Courier port connects using the 9-way female D-type connector (SK4) in the middle of the card end plate (between the IRIG-B connector and lower D-type). The connection complies with EIA(RS)-574.

For IEC60870-5-2 over EIA(RS)-232			For K-bus or IEC60870-5-2 over EIA(RS)-485	
Pin	Connection		Pin*	Connection
1	No Connection			
2	RxD			
3	TxD			
4	DTR#		4	EIA(RS)-485 - 1 (+ ve)
5	Ground			
6	No Connection			
7	RTS#		7	EIA(RS)-485 - 2 (- ve)
8	CTS#			
9	No Connection			
# - These pins are control lines for use with a modem.			* - All other pins unconnected.	

Notes *Connector pins 4 and 7 are used by both the EIA(RS)-232and EIA(RS)-485 physical layers, but for different purposes. Therefore, the cables should be removed during configuration switches.*
When using the EIA(RS)-485 protocol, an EIA(RS)-485 to EIA(RS)-232 converter is needed to connect the relay to a modem or PC running Easergy Studio. A Schneider Electric CK222 is recommended.
EIA(RS)-485 is polarity sensitive, with pin 4 positive (+) and pin 7 negative (-).
The K-Bus protocol can be connected to a PC using a KITZ101 or 102.

Table 3 - Pin connections over EIA(RS)-232 and EIS(RS)-485

2.4 EIA(RS)-485 - Bus

The EIA(RS)-485 two-wire connection provides a half-duplex fully isolated serial connection to the product. The connection is polarized and while the product's connection diagrams show the polarization of the connection terminals, there is no agreed definition of which terminal is which. If the master is unable to communicate with the product and the communication parameters match, make sure the two-wire connection is not reversed.

EIA(RS)-485 provides the capability to connect multiple devices to the same two-wire bus. MODBUS is a master-slave protocol, so one device is the master, and the remaining devices are slaves. It is not possible to connect two masters to the same bus, unless they negotiate bus access.

2.4.1 EIA(RS)-485 - Bus Termination

The EIA(RS)-485 bus must have 120 Ω (Ohm) ½ Watt terminating resistors fitted at either end across the signal wires, see the *EIA(RS)-485 bus connection arrangements* diagram below. Some devices may be able to provide the bus terminating resistors by different connection or configuration arrangements, in which case separate external components are not needed. However, this product does not provide such a facility, so if it is located at the bus terminus, an external termination resistor is needed.

2.4.2 EIA(RS)-485 - Bus Connections & Topologies

The EIA(RS)-485 standard requires each device to be directly connected to the physical cable that is the communications bus. Stubs and tees are expressly forbidden, as are star topologies. Loop bus topologies are not part of the EIA(RS)-485 standard and are forbidden by it.

Two-core screened cable is recommended. The specification of the cable depends on the application, although a multi-strand 0.5 mm^2 per core is normally adequate. Total cable length must not exceed 1000 m. The screen must be continuous and connected at one end, normally at the master connection point. It is important to avoid circulating currents, especially when the cable runs between buildings, for both safety and noise reasons.

This product does not provide a signal ground connection. If the bus cable has a signal ground connection, it must be ignored. However, the signal ground must have continuity for the benefit of other devices connected to the bus. For both safety and noise reasons, the signal ground must never be connected to the cable's screen or to the product's chassis.

2.4.3 EIA(RS)-485 - Biasing

It may also be necessary to bias the signal wires to prevent jabber. Jabber occurs when the signal level has an indeterminate state because the bus is not being actively driven. This can occur when all the slaves are in receive mode and the master is slow to switch from receive mode to transmit mode. This may be because the master purposefully waits in receive mode, or even in a high impedance state, until it has something to transmit. Jabber causes the receiving device(s) to miss the first bits of the first character in the packet, which results in the slave rejecting the message and consequentially not responding. Symptoms of this are poor response times (due to retries), increasing message error counters, erratic communications, and even a complete failure to communicate.

Biasing requires that the signal lines are weakly pulled to a defined voltage level of about 1 V. There should only be one bias point on the bus, which is best situated at the master connection point. The DC source used for the bias must be clean, otherwise noise is injected. Some devices may (optionally) be able to provide the bus bias, in which case external components are not required.

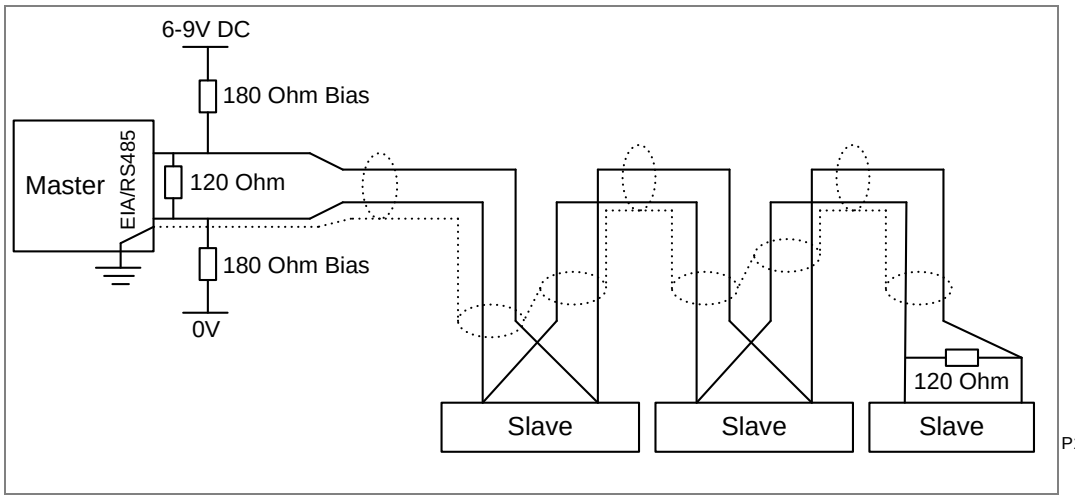


Figure 1 - EIA(RS)-485 bus connection arrangements

It is possible to use the product's field voltage output (48 V DC) to bias the bus using values of 2.2 k Ω (½W) as bias resistors instead of the 180 Ω resistors shown in the *EIA(RS)-485 bus connection arrangements* diagram. Note these warnings apply:

Warnings

It is extremely important that the 120 Ω termination resistors are fitted. Otherwise the bias voltage may be excessive and may damage the devices connected to the bus.

As the field voltage is much higher than that required, Schneider Electric cannot assume responsibility for any damage that may occur to a device connected to the network as a result of incorrect application of this voltage.

Ensure the field voltage is not used for other purposes, such as powering logic inputs, because noise may be passed to the communication network.

2.4.4 Courier Communication

Courier is the communication language developed to allow remote interrogation of its range of protection relays. Courier uses a master and slave. EIA(RS)-232 on the front panel allows only one slave but EIA(RS)-485 on the back panel allows up to 32 daisy-chained slaves. Each slave unit has a database of information and responds with information from its database when requested by the master unit.

The relay is a slave unit that is designed to be used with a Courier master unit such as MiCOM S1 Studio, MiCOM S10, PAS&T or a SCADA system. MiCOM S1 Studio is compatible with Windows™ 2000, XP or Vista and is specifically designed for setting changes with the relay.

To use the rear port to communicate with a PC-based master station using Courier, a KITZ K-Bus to EIA(RS)-232 protocol converter is needed. This unit (and information on how to use it) is available from Schneider Electric. A typical connection arrangement is shown in the *K-bus remote communication connection arrangements* diagram below. For more detailed information on other possible connection arrangements, refer to the manual for the Courier master station software and the manual for the KITZ protocol converter. Each spur of the K-Bus twisted pair wiring can be up to 1000 m in length and have up to 32 relays connected to it.

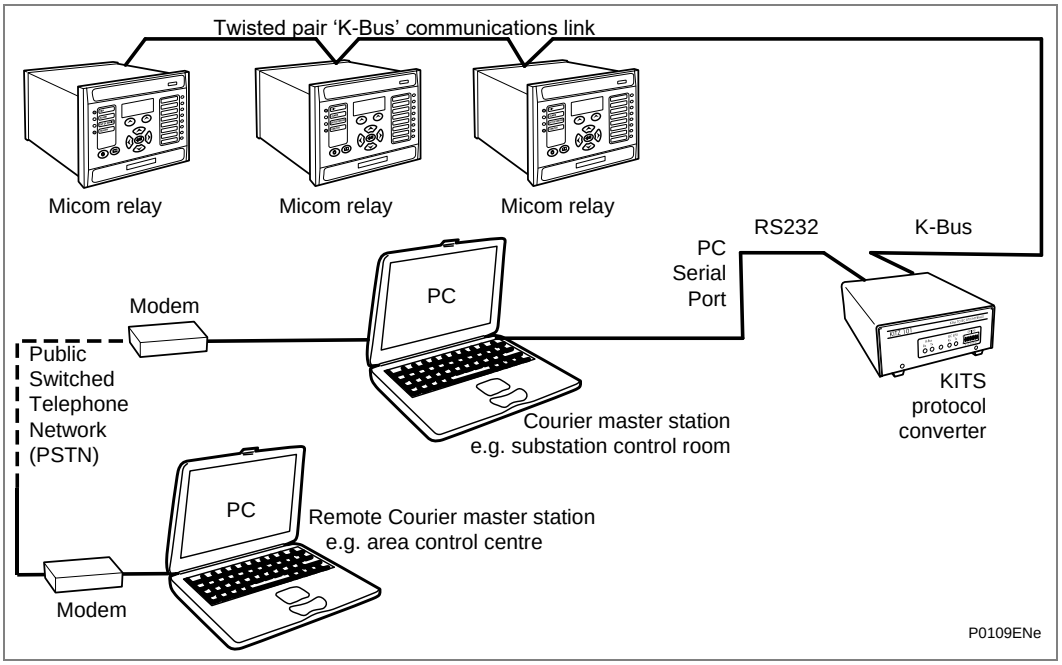


Figure 2 - Remote communication connection arrangements

Once the physical connection is made to the relay, configure the relay's communication settings using the keypad and LCD user interface.

3 CONFIGURING THE COMMUNICATION PORTS

3.1 Introduction

Courier works on a master/slave basis where the slave units contain information in the form of a database, and respond with information from the database when it is requested by a master unit.

The relay is a slave unit that is designed to be used with a Courier master unit such as Easergy Studio, PAS&T or a SCADA system.

3.2 Configuring the Front Courier Port

The front EIA(RS)232 9-pin port supports the Courier protocol for one-to-one communication. It is designed for use during installation, commissioning and maintenance and is not suitable for permanent connection. Since this interface is not intended to link the relay to a substation communication system, not all of the features of the Courier interface are supported; the port is not configurable and the following parameters apply:

- Physical presentation EIA(RS)232 via 9-pin connector
- Frame format IEC60870-5 FT1.2 = 11-bit (8 Even 1)
- Address 1
- Baud rate 19200 bps

Note	*As part of the limited implementation of Courier on the front port, neither automatic extraction of event and disturbance records, nor busy response are supported.)*

3.3 Configuring the First Rear Courier Port (RP1)

Once the physical connection is made to the relay, configure the relay's communication settings using the keypad and LCD user interface.

1. In the relay menu, select the **Configuration** column, then check that the **Comms. settings** cell is set to **Visible**.
2. Select the **Communications** column. Only two settings apply to the rear port using Courier, the relay's address and the inactivity timer. Synchronous communication uses a fixed baud rate of 64 kbits/s.
3. Move down the **Communications** column from the column heading to the first cell down. This shows the communication protocol.

```
Protocol
Courier
```

4. The next cell down the column controls the address of the relay. As up to 32 relays can be connected to one K-Bus spur, each relay must have a unique address so messages from the master control station are accepted by one relay only. Courier uses an integer (from 0 to 254) for the relay address that is set with this cell. Important: no two relays should have the same Courier address. The master station uses the Courier address to communicate with the relay.

```
Address
1
```

5. The next cell down controls the inactivity timer.

```
Inactiv timer
10.00 mins.
```

The inactivity timer controls how long the relay waits without receiving any messages on the rear port before it reverts to its default state, including revoking any password access that was enabled. For the rear port this can be set between 1 and 30 minutes.

Note	*Protection and disturbance recorder settings that are modified using an on-line editor such as PAS&T must be confirmed with a write to the 'Save changes' cell of the 'Configuration' column. Off-line editors such as Easergy Studio do not need this action for the setting changes to take effect.*

The next cell down controls the physical media used for the communication.

```
Physical link
Copper
```

The default setting is to select the electrical (copper) connection. If the optional fiber optic interface is fitted to the relay, then this setting can be changed to '**Fiber optic**'. This cell is invisible if a second rear communications port or an Ethernet card is fitted, as they are mutually exclusive and occupy the same physical location.

6. If the Physical link selection is copper, the next cell down becomes visible to further define the configuration:

```
Port Config
KBus
```

The setting choice is between K-Bus and EIA(RS)485. Selecting K-Bus allows connection with K-series devices, but means that a KITZ converter must be used to make a connection. If the EIA(RS)485 selection is made, direct connections can be made to proprietary equipment such as MODEMs. If the EIA(RS)485 selection is made, then two further cells become visible to control the frame format and the communication speed:

7. The frame format is selected in the RP1 Comms mode setting:

```
Comms Mode
IEC60870 FT1.2
```

The standard default is the IEC 60870-FT1.2. This is an 11-bit framing. Alternatively, a 10-bit framing may be selected for use with MODEMs that do not support 11-bit framing.

8. The final RP1 cell controls the communication speed or baud rate:

```
Baud Rate
19200 bits/s
```

Courier communications is asynchronous and three baud rate selections are available to allow the relay communication rate to be matched to that of the connected equipment. Three baud rates are supported by the relay, '9600 bits/s', '19200 bits/s' and '38400 bits/s'.

Important	**If you modify protection and disturbance recorder settings using an on-line editor such as PAS&T, you must confirm them. To do this, from the Configuration column select the Save changes cell. Off-line editors such as Easergy Studio do not need this action for the setting changes to take effect.**

3.4 Configuring the MODBUS Communication

Important	**MODBUS is not available for all MiCOM products. MODBUS availability is shown in the *Supported Protocols* table.**

MODBUS is a master/slave communication protocol that can be used for network control. In a similar way to Courier, the master device initiates all actions and the slave devices (the relays) respond to the master by supplying the requested data or by taking the requested action. MODBUS communication uses a twisted pair connection to the rear port and can be used over a distance of 1000 m with up to 32 slave devices.

To use the rear port with MODBUS communication, configure the relay's communication settings using the keypad and LCD user interface.

1. In the relay menu firstly check that the '**Comms. settings**' cell in the '**Configuration**' column is set to '**Visible**'.
2. Select the '**Communications**' column. Four settings apply to the rear port using MODBUS, which are described below.
3. Move down the **Communications** column from the column heading to the first cell down which indicates the communication protocol.

   ```
   Protocol
   MODBUS
   ```

4. The next cell down controls the MODBUS address of the relay:

   ```
   MODBUS address
   23
   ```

   Up to 32 relays can be connected to one MODBUS spur, and therefore it is necessary for each relay to have a unique address so that messages from the master control station are accepted by one relay only. MODBUS uses an integer number between 1 and 247 for the relay address. It is important that no two relays have the same MODBUS address. The MODBUS address is then used by the master station to communicate with the relay.
5. The next cell down controls the inactivity timer:

   ```
   Inactivity timer
   10.00 mins.
   ```

   The inactivity timer controls how long the relay will wait without receiving any messages on the rear port before it reverts to its default state, including revoking any password access that was enabled. For the rear port this can be set between 1 and 30 minutes.
6. The next cell down the column controls the baud rate to be used:

   ```
   Baud rate
   9600 bits/s
   ```

7. MODBUS communication is asynchronous. Three baud rates are supported by the relay, '**9600 bits/s**', '**19200 bits/s**' and '**38400 bits/s**'. It is important that whatever baud rate is selected on the relay is the same as that set on the MODBUS master station.
8. The next cell down controls the parity format used in the data frames:

   ```
   Parity
   None
   ```

   The parity can be set to be one of '**None**', '**Odd**' or '**Even**'. It is important that whatever parity format is selected on the relay is the same as that set on the MODBUS master station.
9. The next cell down controls the IEC time format used in the data frames:

```
MODBUS IEC time
Standard
```

10. The MODBUS IEC time can be set to '**Standard**' or '**Reverse**'. For a complete definition see the Relay Menu Database (P14x/EN MD), datatype G12.

3.5 Configuring the IEC 60870-5 CS 103 Communication

The IEC specification IEC 60870-5-103: Telecontrol Equipment and Systems, Part 5: Transmission Protocols Section 103 defines the use of standards IEC 60870-5-1 to IEC 60870-5-5 to perform communication with protection equipment. The standard configuration for the IEC 60870-5-103 protocol is to use a twisted pair connection over distances up to 1000 m. As an option for IEC 60870-5-103, the rear port can be specified to use a fiber optic connection for direct connection to a master station. The relay operates as a slave in the system, responding to commands from a master station. The method of communication uses standardized messages which are based on the VDEW communication protocol.

To use the rear port with IEC 60870-5-103 communication, configure the relay's communication settings using the keypad and LCD user interface.

1. In the relay menu, select the **Configuration** column, then check that the **Comms. settings** cell is set to **Visible**.
2. Select the **Communications** column. Four settings apply to the rear port using IEC 60870-5-103 that are described below.

   Move down the 'COMMUNICATIONS' column from the column heading to the first cell to confirm the communication protocol:

   ```
   Protocol
   IEC60870-5-103
   ```

3. The next cell sets the address of the relay on the IEC 60870-5-103 network:

   ```
   Remote Address
   162
   ```

   Up to 32 relays can be connected to one IEC 60870-5-103 spur, and therefore it is necessary for each relay to have a unique address so that messages from the master control station are accepted by one relay only. IEC 60870-5-103 uses an integer number between 0 and 254 for the relay address. It is important that no two relays have the same address. The address is then used by the master station to communicate with the relay.
4. The next cell down the column controls the baud rate to be used:

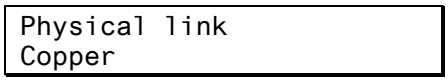
   ```
   Baud rate
   9600 bits/s
   ```

   IEC 60870-5-103 communication is asynchronous. Two baud rates are supported by the relay, '9600 bits/s' and '19200 bits/s'. It is important that whatever baud rate is selected on the relay is the same as that set on the IEC 60870-5-103 master station.
5. The next cell down controls the period between IEC 60870-5-103 measurements:

   ```
   Measure't period
   30.00 s
   ```

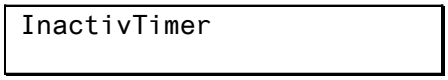
   The IEC 60870-5-103 protocol allows the relay to supply measurements at regular intervals. The interval between measurements is controlled by this cell, and can be set between 1 and 60 seconds.

6. An optional fiber optic card is available in the relay to allow optical connection to the IEC 60870-5-103 communication to be made over an optical connection. When fitted, it converts between EIA(RS)485 signals and fiber optic signals and the following cell is visible in the menu column:

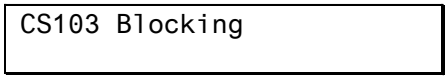


The default setting is to select the electrical (copper) connection. If the optional fiber optic interface is fitted to the relay, then this setting can be changed to 'Fiber optic'. This cell is invisible if a second rear communications port or an Ethernet card is fitted, as they are mutually exclusive and occupy the same physical location.

7. The following cell which may be displayed, is not currently used but is available for future expansion.



8. The next cell down can be used for monitor or command blocking:



There are three settings associated with this cell; these are:

- **Disabled**
  No blocking selected.
- **Monitor Blocking**
  When the monitor blocking DDB Signal is active high, either by energizing an opto input or control input, reading of the status information and disturbance records is not permitted. When in this mode the relay returns a "Termination of general interrogation" message to the master station.
- **Command Blocking**
  When the command blocking DDB signal is active high, either by energizing an opto input or control input, all remote commands are ignored, such as CB Trip/Close or change setting group. When in this mode the relay returns a **negative acknowledgement of command** message to the master station.

3.6 Configuring the DNP3.0 Communication Rear Port, RP1

The DNP3.0 protocol is defined and administered by the DNP User Group. Information about the user group, DNP3.0 in general and protocol specifications can be found on their website: www.dnp.org

The relay operates as a DNP3.0 slave and supports subset level 2 of the protocol plus some of the features from level 3. DNP3.0 communication is achieved using a twisted pair connection to the rear port and can be used over a distance of 1000 m with up to 32 slave devices.

1. To use the rear port with DNP3.0 communication, configure the relay's communication settings using the keypad and LCD user interface.
2. In the relay menu, select the **Configuration** column, then check that the **Comms. settings** cell is set to **Visible**.
3. Four settings apply to the rear port using DNP 3.0 that are described below.
4. Move down the 'COMMUNICATIONS' column from the column heading to the first cell that indicates the communications protocol:

```
Protocol
DNP 3.0
```

5. The next cell sets the device address on the DNP3.0 network:

```
DNP 3.0 Address
232
```

Up to 32 devices can be connected to one DNP3.0 spur, and therefore it is necessary for each device to have a unique address so that messages from the master control station are accepted by only one device. DNP3.0 uses a decimal number between 1 and 65519 for the device address. It is important that no two devices have the same address. The address is then used by the DNP3.0 master station to communicate with the relay.

6. The next cell sets the baud rate to be used:

```
Baud Rate
9600 bits/s
```

DNP3.0 communication is asynchronous. Six baud rates are supported by the relay '1200bits/s', '2400bits/s', '4800bits/s', '9600bits/s', '19200bits/s' and '38400bits/s'. It is important that whatever baud rate is selected on the relay is the same as that set on the DNP3.0 master station.

7. The next cell controls the parity format used in the data frames:

```
Parity
None
```

The parity can be set to be one of **None**, **Odd** or **Even.** It is important that whatever parity format is selected on the relay is the same as that set on the DNP3.0 master station.

An optional fiber optic card is available in the relay to allow optical connection to the IEC 60870-5-103 communication to be made over an optical connection. When fitted, it converts between EIA(RS)485 signals and fiber optic signals and the following cell is visible in the menu column.

8. The next cell down the column controls the physical media used for the communication.

```
Physical link
Copper
```

The default setting is to select the electrical (copper) connection. If the optional fiber optic interface is fitted to the relay, then this setting can be changed to **Fiber optic**. This cell is invisible if a second rear communications port or an Ethernet card is fitted, as they are mutually exclusive and occupy the same physical location.

9. The next cell down the column sets the time synchronization request from the master by the relay:

```
Time Sync.
Enabled
```

The time synchronization can be set to either enabled or disabled. If enabled it allows the DNP3.0 master to synchronize the time.

10. Analogue values can be set to be reported in terms of primary, secondary or normalized (with respect to the CT/VT ratio setting) values:

```
Meas Scaling
Primary
```

11. A message gap setting is provided:

```
Message Gap
ϕ
```

This allows a gap between message frames to be set to enable compatibility with different master stations.

The setting for enabling/disabling DNP3.0 time synchronization is described above. When DNP3.0 time sync is enabled, the required rate of synchronization, known as the “need time”, needs to be set.

12. A setting allows different “need time” to be set with setting range from 1 - 30 minutes, step of 1 minute and default at 10 minutes:

```
DNP Need Time
10mins
```

The transmitted application fragment size can be set to ensure that a Master Station cannot be held too long before a complete reply is received and allow it to move on to next IED in a token ring polling setup.

13. The maximum overall response message length can be configured:

```
DNP App Fragment
2048
```

A single fragment size is 249. Depending on circumstances, a user may set the fragment size as a multiple of 249 in order to optimize segment packing efficiency in fragments. However it can also be useful to allow "odd" sizes for users to choose under specific circumstances, such as if sending data inside SMS frames, through packet radios, etc. In such cases it can be useful to select the fragment size such that each packet occupies a single "transmission media frame".

In some cases, communication to the outstation is made over slow, packet-switched networks which can add seconds to the communication latency.

14. A setting is provided to allow the application layer timeout to be set:

```
DNP App Timeout
2s
```

15. Select Before Operate (SBO) timeouts can be set.
If the DNP3.0 “Select a trip command” causes the relay’s internal logic to block automatic tripping, then a corruption of the DNP3.0 “Operate” message could delay the trip. The delay of tripping can be set:

```
DNP SBO Timeout
10s
```

16. The DNP link timeout can be set:

```
DNP Link Timeout
10s
```

3.7 Configuring the Second Rear Communication Port (RP2)

For relays with Courier, MODBUS, IEC60870-5-103 or DNP3.0 protocol on the first rear communications port there is the hardware option of a second rear communications port, which will run the Courier language. This can be used over one of three physical links: twisted pair K-Bus (non-polarity sensitive), twisted pair EIA(RS)485 (connection polarity sensitive) or EIA(RS)232.
The settings for this port are located immediately below the ones for the first port as described in the *Introduction* chapter.

1. Move down the settings until the following sub heading is displayed.

```
Rear Port 2
(RP2)
```

2. The next cell defines the protocol, which is fixed at Courier for RP2.

```
RP2 protocol
Courier
```

3. The following cell indicates the status of the hardware.

```
RP2 card status
EIA(RS)232 OK
```

4. The following cell allows for selection of the port configuration.

```
RP2 port config.
EIA(RS)232
```

5. The port can be configured for EIA(RS)232, EIA(RS)485 or K-Bus.
As in the case of the first rear Courier port, if K-Bus is not selected certain other cells to control the communication mode and speed become visible. If either EIA(RS)232 or EIA(RS)485 is selected for the port configuration, the next cell is visible and selects the communication mode.

```
RP2 comms.  Mode
IEC60870 FT1.2
```

6. The standard default is the IEC 60870 FT1.2 for normal operation with 11-bit modems. Alternatively, a 10-bit framing with no parity bit can be selected for special cases.
7. The next cell down sets the communications port address.

```
RP2 address
255
```

Since up to 32 devices can be connected to one K-bus spur, it is necessary for each device to have a unique address so that messages from the master control station are accepted by one device only. Courier uses an integer number between 0 and 254 for the device address that is set with this cell. It is important that no two devices have the same Courier address. The Courier address is then used by the master station to communicate with the device. The default value is 255 and must be changed to a value in the range 0 to 254 before use.

8. The following cell controls the inactivity timer.

```
RP2 InactivTimer
15 mins.
```

9. The inactivity timer controls how long the relay will wait without receiving any messages on the rear port before it reverts to its default state. This includes revoking any password access that was enabled. The inactivity timer can be set between 1 and 30 minutes.
10. In the case of EIA(RS)232 and EIA(RS)485 the next cell down controls the baud rate. For K-Bus the baud rate is fixed at 64kbit/second between the relay and the KITZ interface at the end of the relay spur.

```
RP2 baud rate
19200
```

Courier communications is asynchronous and three selections are available to allow the relay communication rate to be matched to that of the connected equipment. The three baud rates supported by the relay are: '9600 bits/s', '19200 bits/s' and '38400 bits/s'.

3.8 Fiber Optic Converter (option)

An optional fiber optic card is available in this product. This converts the EIA(RS)485 protocols into a fiber optic output. This communication card is available for use on Courier, MODBUS (for products listed in the *Supported Protocols* table), IEC60870-5-103 and DNP3.0 it adds the following setting to the communication column.

This controls the physical media used for the communication:

```
Physical link
Copper
```

The default setting is to select the electrical EIA(RS)485 connection. If the optional fiber optic connectors are fitted to the relay, then this setting can be changed to '**Fiber optic**'. This cell is also invisible if a second rear comms. port, or Ethernet card is fitted, as it is mutually exclusive with the fiber optic connectors, and occupies the same physical location.

Where this is used, connection should be made using either 50/125µm or 62.5/125µm multi-mode optical fibers terminated with BFOC/2.5 (ST) connectors.

3.9 Second Rear Port K-Bus Application

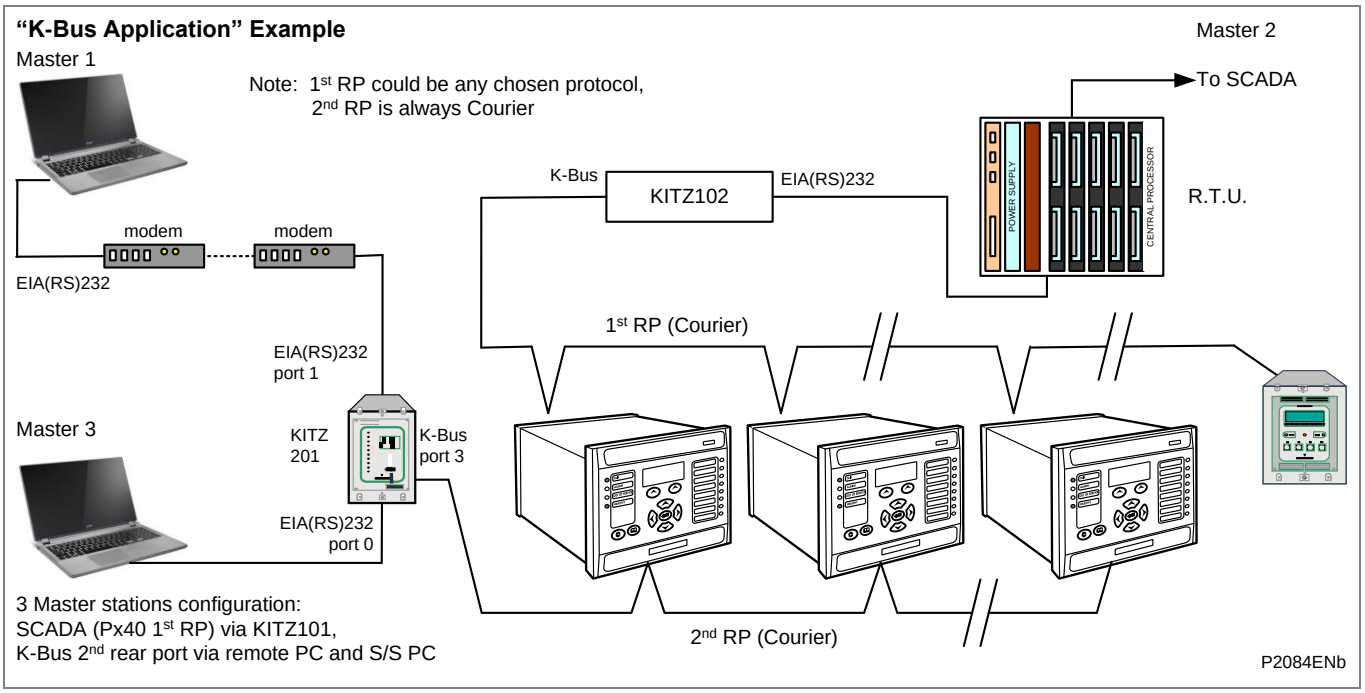


Figure 3 - Second rear port K-Bus application

3.10 Second Rear Port EIA(RS)485 Example

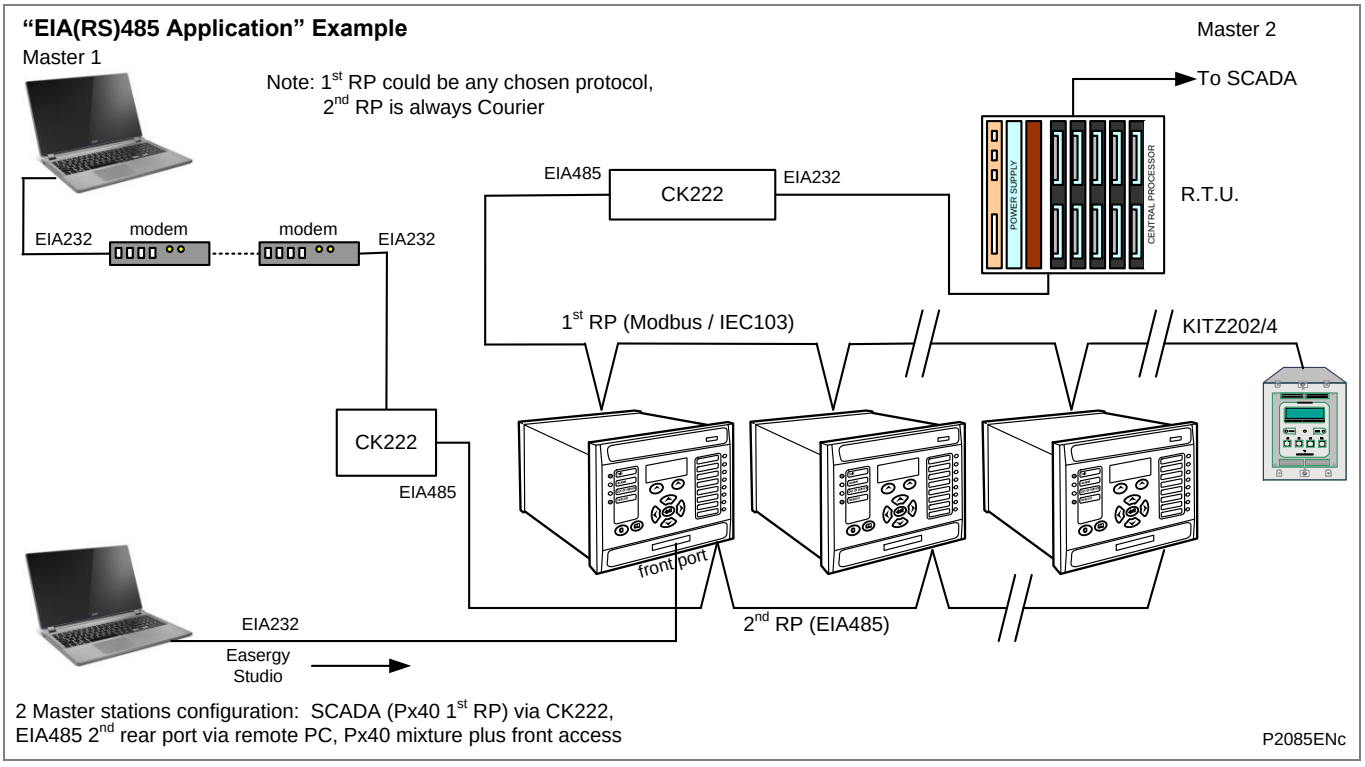


Figure 4 - Second rear port EIA(RS)-485 example

3.11 Second Rear Port EIA(RS)232 Example

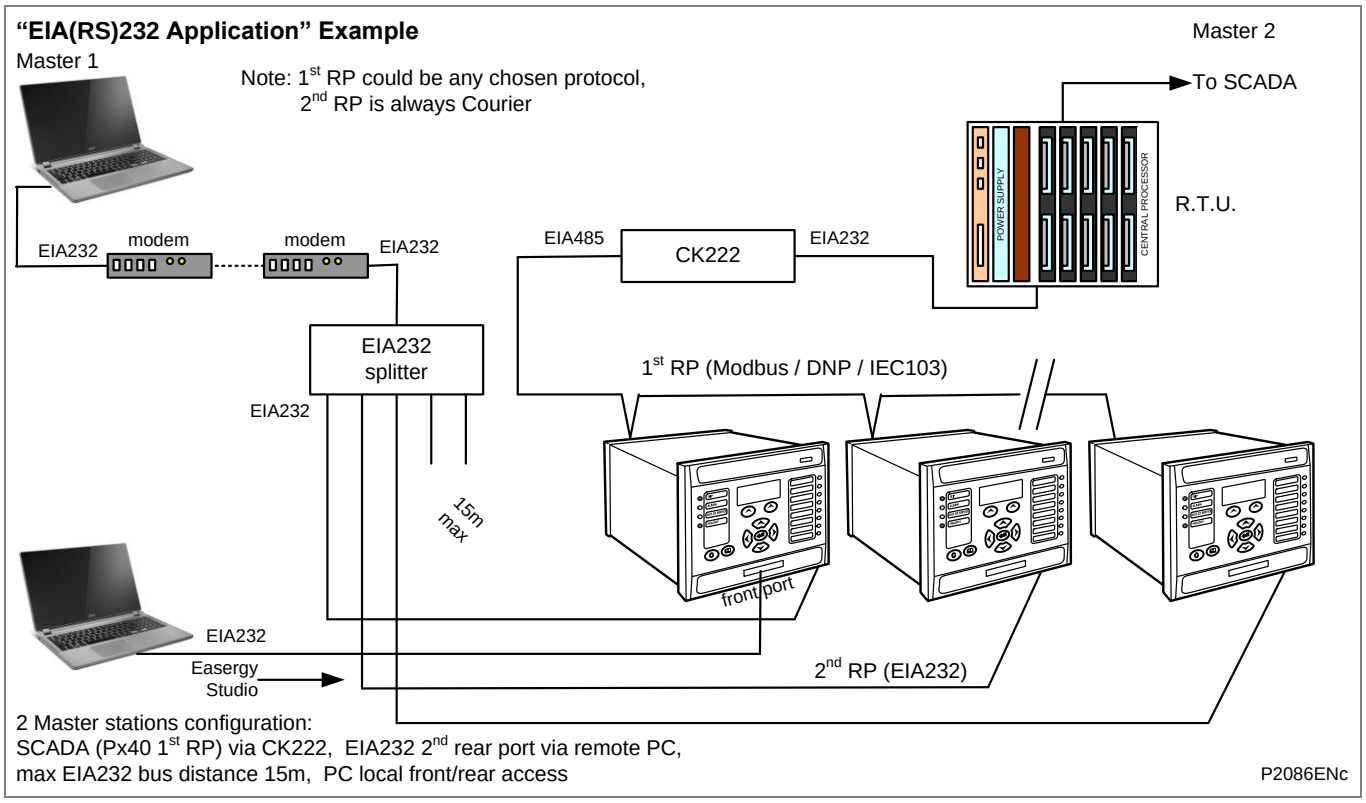


Figure 5 - Second rear port EIA(RS)-232 example

3.12 SK5 Port Connection

The lower 9-way D-type connector (SK5) is currently unsupported.
Do not connect to this port.

4 COURIER INTERFACE

4.1 Courier Protocol

Courier is a Schneider Electric communication protocol. The concept of the protocol is that a standard set of commands is used to access a database of settings and data in the relay. This allows a generic master to be able to communicate with different slave devices. The application-specific aspects are contained in the database rather than the commands used to interrogate it, so the master station does not need to be preconfigured.

The same protocol can be used through two physical links K-Bus or EIA(RS)-232.

K-Bus is based on EIA(RS)-485 voltage levels with HDLC FM0 encoded synchronous signaling and its own frame format. The K-Bus twisted pair connection is unpolarized, whereas the EIA(RS)-485 and EIA(RS)-232 interfaces are polarized.

The EIA(RS)-232 interface uses the IEC60870-5 FT1.2 frame format.

The relay supports an IEC60870-5 FT1.2 connection on the front-port. This is intended for temporary local connection and is not suitable for permanent connection. This interface uses a fixed baud rate, 11-bit frame, and a fixed device address.

The rear interface is used to provide a permanent connection for K-Bus and allows multi-drop connection. Although K-Bus is based on EIA(RS)-485 voltage levels, it is a synchronous HDLC protocol using FM0 encoding. It is not possible to use a standard EIA(RS)-232 to EIA(RS)-485 converter to convert IEC60870-5 FT1.2 frames to K-Bus. Also it is not possible to connect K-Bus to an EIA(RS)-485 computer port. A protocol converter, such as the KITZ101, should be used for this purpose.

For a detailed description of the Courier protocol, command-set and link description, see the following documentation:

R6509	K-Bus Interface Guide
R6510	IEC60870 Interface Guide
R6511	Courier Protocol
R6512	Courier User Guide

Alternatively for direct connections, the fiber optic converter card may be used to convert the rear EIA(RS)485 port into a fiber optic (ST) port. See the *Fiber Optic Converter (option)* section for more information.

4.2 Front Courier Port

The front EIA(RS)-232 9 pin port supports the Courier protocol for one-to-one communication. This port complies with EIA(RS)-574; the 9-pin version of EIA(RS)-232, see www.tiaonline.org. It is designed for use during installation and commissioning/maintenance and is not suitable for permanent connection. Since this interface is not used to link the relay to a substation communication system, some of the features of Courier are not implemented. These are as follows:

- Automatic extraction of Event Records:
  - Courier Status byte does not support the Event flag.
  - Send Event/Accept Event commands are not implemented.
- Automatic extraction of Disturbance records:
  - Courier Status byte does not support the Disturbance flag.
- Busy Response Layer:
  - Courier Status byte does not support the Busy flag, the only response to a request is the final data.
- Fixed Address:
  - The address of the front Courier port is always 1; the Change Device address command is not supported.
- Fixed Baud Rate:
  - 19200 bps.
  - Although automatic extraction of event and disturbance records is not supported, it is possible to manually access this data through the front port.

4.3 Supported Command Set

The following Courier commands are supported by the relay:

Protocol Layer:
- Reset Remote Link
- Poll Status
- Poll Buffer*

Low Level Commands:
- Send Event*
- Accept Event*
- Send Block
- Store Block Identifier
- Store Block Footer

Menu Browsing:
- Get Column Headings
- Get Column Text
- Get Column Values
- Get Strings
- Get Text
- Get Value
- Get Column Setting Limits

Setting Changes:
- Enter Setting Mode
- Preload Setting
- Abort Setting
- Execute Setting
- Reset Menu Cell
- Set Value

Control Commands:
- Select Setting Group
- Change Device Address*
- Set Real Time

Note	*Commands marked with an asterisk (*) are not supported through the front Courier port.*

4.4 Courier Database

The Courier database is two-dimensional. Each cell in the database is referenced by a row and column address. Both the column and the row can take a range from 0 to 255. Addresses in the database are specified as hexadecimal values, for example, 0A02 is column 0A (10 decimal) row 02. Associated settings or data are part of the same column. Row zero of the column has a text string to identify the contents of the column and to act as a column heading.

The *Relay Menu Database document* contains the complete database definition for the relay. For each cell location the following information is stated:

- Cell Text
- Cell Data type
- Cell value
- Whether the cell is settable, if so
  - Minimum value
  - Maximum value
  - Step size
- Password Level required to allow setting changes
- String information (for Indexed String or Binary flag cells)

4.5 Setting Changes

(See R6512, Courier User Guide - Chapter 9)
Courier provides two mechanisms for making setting changes, both of these are supported by the relay. Either method can be used for editing any of the settings in the relay database.

4.5.1 Method 1

This uses a combination of three commands to perform a settings change:

Enter Setting Mode	Checks that the cell is settable and returns the limits.
Preload Setting	Places a new value to the cell. This value is echoed to ensure that setting corruption has not taken place. The validity of the setting is not checked by this action.
Execute Setting	Confirms the setting change. If the change is valid, a positive response is returned. If the setting change fails, an error response is returned.
Abort Setting	This command can be used to abandon the setting change.

This is the most secure method. It is ideally suited to on-line editors because the setting limits are taken from the relay before the setting change is made. However, this method can be slow if many settings are being changed because three commands are required for each change.

4.5.2 Method 2

The **Set Value** command can be used to directly change a setting, the response to this command is either a positive confirm or an error code to indicate the nature of a failure. This command can be used to implement a setting more rapidly than the previous method, however the limits are not extracted from the relay. This method is most suitable for off-line setting editors such as Easergy Studio, or for issuing preconfigured (SCADA) control commands.

4.5.3 Relay Settings

There are three categories of settings in the relay database:

- Control and support
- Disturbance recorder
- Protection settings group

Setting changes made to the control and support settings are implemented immediately and stored in non-volatile memory. Changes made to either the Disturbance recorder settings or the Protection Settings Groups are stored in a 'scratchpad' memory and are not immediately implemented by the relay.

To action setting changes stored in the scratchpad the Save **Changes cell** in the **Configuration** column must be written to. This allows the changes to either be confirmed and stored in non-volatile memory, or the setting changes to be aborted.

4.5.4 Setting Transfer Mode

If it is necessary to transfer all of the relay settings to or from the relay, a cell in the **Communication System Data** column can be used. This cell (location BF03) when set to 1 makes all of the relay settings visible. Any setting changes made with the relay set in this mode are stored in scratchpad memory, including control and support settings. When the value of BF03 is set back to 0, any setting changes are verified and stored in non-volatile memory.

4.6 Event Extraction

Events can be extracted either automatically (rear port only) or manually (either Courier port). For automatic extraction all events are extracted in sequential order using the standard Courier event mechanism, this includes fault/maintenance data if appropriate. The manual approach allows the user to select events, faults, or maintenance data at random from the stored records.

4.6.1 Automatic Event Extraction

(See Chapter 7 Courier User Guide, publication R6512).

This method is intended for continuous extraction of event and fault information as it is produced. It is only supported through the rear Courier port.

When new event information is created, the Event bit is set in the Status byte. This indicates to the Master device that event information is available. The oldest, unextracted event can be extracted from the relay using the Send Event command. The relay responds with the event data, which is either a Courier Type 0 or Type 3 event. The Type 3 event is used for fault records and maintenance records.

Once an event has been extracted from the relay, the Accept Event can be used to confirm that the event has been successfully extracted. If all events have been extracted, the event bit is reset. If there are more events still to be extracted, the next event can be accessed using the **Send Event** command as before.

4.6.2 Event Types

Events are created by the relay under these circumstances:

- Change of state of output contact
- Change of state of opto input
- Protection element operation
- Alarm condition
- Setting change
- Password entered/timed-out
- Fault record (Type 3 Courier Event)
- Maintenance record (Type 3 Courier Event)

4.6.3 Event Format

The Send Event command results in these fields being returned by the relay:

- Cell reference
- Time stamp
- Cell text
- Cell value

The *Relay Menu Database* document for the relevant product, contains a table of the events created by the relay and indicates how the contents of the above fields are interpreted. Fault records and Maintenance records return a Courier Type 3 event, which contains the above fields with two additional fields:

- Event extraction column
- Event number

These events contain additional information that is extracted from the relay using the referenced extraction column. Row 01 of the extraction column contains a setting that allows the fault/maintenance record to be selected. This setting should be set to the event number value returned in the record. The extended data can be extracted from the relay by uploading the text and data from the column.

4.6.4 Manual Event Record Extraction

Column 01 of the database can be used for manual viewing of event, fault, and maintenance records. The contents of this column depend on the nature of the record selected. It is possible to select events by event number and to directly select a fault record or maintenance record by number.

Event Record selection (Row 01)

This cell can be set to a value between 0 to 249 to select from 250 stored events. 0 selects the most recent record and 249 the oldest stored record. For simple event records, (Type 0) cells 0102 to 0105 contain the event details. A single cell is used to represent each of the event fields. If the event selected is a fault or maintenance record (Type 3), the remainder of the column contains the additional information.

Fault Record Selection (Row 05)

This cell can be used to select a fault record directly, using a value between 0 and 4 to select one of up to five stored fault records. (0 is the most recent fault and 4 is the oldest). The column then contains the details of the fault record selected.

Maintenance Record Selection (Row F0)

This cell can be used to select a maintenance record using a value between 0 and 4. This cell operates in a similar way to the fault record selection.

If this column is used to extract event information from the relay, the number associated with a particular record changes when a new event or fault occurs.

4.7 Disturbance Record Extraction

The stored disturbance records in the relay are accessible in a compressed format through the Courier interface. The records are extracted using column B4. Cells required for extraction of uncompressed disturbance records are not supported.

Select Record Number (Row 01)

This cell can be used to select the record to be extracted. Record 0 is the oldest unextracted record, already extracted older records are assigned positive values, and negative values are used for more recent records. To help automatic extraction through the rear port, the Disturbance bit of the Status byte is set by the relay whenever there are unextracted disturbance records.

Once a record has been selected, using the above cell, the time and date of the record can be read from cell 02. The disturbance record can be extracted using the block transfer mechanism from cell B00B. The file extracted from the relay is in a compressed format. Use Easergy Studio to decompress this file and save the disturbance record in the COMTRADE format.

As has been stated, the rear Courier port can be used to extract disturbance records automatically as they occur. This operates using the standard Courier mechanism, see *Chapter 8 of the Courier User Guide*. The front Courier port does not support automatic extraction although disturbance record data can be extracted manually from this port.

4.8 Programmable Scheme Logic (PSL) Settings

The Programmable Scheme Logic (PSL) settings can be uploaded from and downloaded to the relay using the block transfer mechanism defined in the Courier User Guide.

These cells are used to perform the extraction:

- B204 Domain — Used to select either PSL settings (upload or download) or PSL configuration data (upload only)
- B208 Sub-Domain — Used to select the Protection Setting Group to be uploaded or downloaded.
- B20C Version — Used on a download to check the compatibility of the file to be downloaded with the relay.
- B21C Transfer Mode — Used to set up the transfer process.
- B120 Data Transfer Cell — Used to perform upload or download.

The PSL settings can be uploaded and downloaded to and from the relay using this mechanism. If it is necessary to edit the settings, Easergy Studio must be used because the data is compressed. Easergy Studio also performs checks on the validity of the settings before they are downloaded to the relay.

5 MODBUS INTERFACE

The MODBUS interface is a master/slave protocol and is defined by: www.modbus.org
MODBUS Serial Protocol Reference Guide: PI-MBUS-300 Rev. E

5.1 Communication Link (Serial Interface)

This interface also uses the rear EIA(RS)485 port (or converted fiber optic port) for communication using '**RTU**' mode communication rather than '**ASCII**' mode as this provides more efficient use of the communication bandwidth. This mode of communication is defined by the MODBUS standard.

5.1.1 Character Framing

The character framing is 1 start bit, 7 data bits (least significant bit sent first), 1 bit for even/odd parity or no bit for no parity, 1 stop bit if parity is used or 2 bits if no parity, plus 1 error checking bit. This gives 11 bits per character.

5.1.2 Maximum MODBUS Query and Response Frame Size

The maximum query and response frame size is limited to 260 bytes in total. (This includes the frame header and CRC footer, as defined by the MODBUS protocol.).

5.1.3 User Configurable Communications Parameters

The following parameters can be configured for this port using the product's front panel user interface (in the communications sub-menu):

- Baud rate: 9600, 19200, 38400 bps
- Device address: 1 - 247
- Parity: Odd, even, none.
- Inactivity time: 1 - 30 minutes

The MODBUS interface communication parameters are not part of the product's setting file and cannot be configured with MiCOM S1 Studio.

5.2 Supported MODBUS Query Functions

The MODBUS protocol provides numerous query functions, of which the product supports the subset in the following table. The product responds with exception code 01 if any other query function is received by it.

Query Function Code	MODBUS Query Name	Application / Interpretation
01	Read Coil Status	Read status of output contacts (0x addresses)
02	Read Input Status	Read status of opto-isolated status inputs (1x addresses)
03	Read Holding Registers	Read setting values (4x addresses)
04	Read Input Registers	Read measurement values (3x addresses)
06	Preset Single Register	Write single setting value (4x addresses)
07	Read Exception Status	Read relay status, same value as register 3x1
08	Diagnostics	Application defined by the MODBUS protocol specification
11	Fetch Communication Event Counter	
12	Fetch Communication Event Log	
16	Preset Multiple Registers (127 max)	Write multiple setting values (4x addresses)

Table 4 - MODBUS query functions supported by the product

5.3 MODBUS Response Code Interpretation

Code	MODBUS response name	Product interpretation
01	Illegal Function Code	The function code transmitted is not supported.
02	Illegal Data Address	The start data address in the request is not an allowable value. If any of the addresses in the range cannot be accessed due to password protection, all changes in the request are discarded and this error response is returned. Note If the start address is correct but the range includes non-implemented addresses, this response is not produced.
03	Illegal Value	A value referenced in the data field transmitted by the master is not in range. Other values transmitted in the same packet are executed if they are in the range.
04	Slave Device Failure	An exception arose during the processing of the received query that is not covered by any of the other exception codes in this table.
05	Acknowledge	Not used.
06	Slave Device Busy	The write command cannot be implemented due to the product's internal database being locked by another interface. This response is also produced if the product is busy executing a previous request.

Table 5 - MODBUS response code interpretation

5.4 Maximum Query and Response Parameters

The following table shows the maximum amount of data that the product can process for each of the supported query functions (see the Supported MODBUS Query Functions section) and the maximum amount of data that can be sent in a corresponding response frame. The principal constraint is the maximum query and response frame size, as noted in the *Maximum MODBUS Query and Response Frame Size* section. Maximum MODBUS query and response frame size.

Query function code	MODBUS query name	Maximum query data request size	Maximum response data size
01	Read Coil Status	32 coils	32 coils
02	Read Input Status	32 inputs	32 inputs
03	Read Holding Registers	127 registers	127 registers
04	Read Input Registers	127 registers	127 registers
06	Preset Single Register	1 register	1 register
07	Read Exception Status	-	8 coils
08	Diagnostics	-	-
11	Fetch Communication Event Counter	-	-
12	Fetch Communication Event Log	-	70 bytes
16	Preset Multiple Registers	127 registers	127 registers

Table 6 - Maximum query and response parameters for supported queries

5.5 Register Mapping

5.5.1 Conventions

5.5.1.1 Memory Pages

The MODBUS specification associates a specific register address space to each query that has a data address field. The address spaces are often called memory pages because they are analogous to separate memory devices. A simplistic view of the queries in MODBUS is that a specified location in a specified memory device is being read from or written to. However, the product's implementation of such queries is not as a memory access but as a translation to an internal database query (see Note).

Note	*One consequence of this is that the granularity of the register address space (in the 3x and 4x memory pages) is governed by the size of the data item being requested from the internal database. Since this is often more than the 16 bits of an individual register, not all register addresses are valid. See the Register Data Types section for more details.*

Each MODBUS memory page has a name and an ID. The *MODBUS "memory" pages reference and application* table provides a summary of the memory pages, their Ids, and their application in the product.

It is common practice to prefix a decimal register address with the page ID and generally this is the style used in this document.

Memory page ID	MODBUS memory page name	Product application
0xxxx	Coil Status	Read and write access of the Output Relays.
1xxxx	Input Status	Read only access of the Opto-Isolated Status Inputs.
3xxxx	Input Registers	Read-only data access, such as measurements and records.
4xxxx	Holding Registers	Read and write data access, such as product configurations settings and control commands.
6xxxx	Extended Memory File	Not used or supported.
Note	*xxxx represents the addresses available in the page (0 to 9999).*	

Table 7 - MODBUS "memory" pages reference and application

5.5.1.2 MODBUS Register Identification

The MODBUS convention is to document register identifiers with ordinal values (first, second, third…) whereas the actual protocol uses memory-page based register addresses that begin with address zero. Therefore the first register in a memory page is register address zero, the second register is register address 1 and so on. In general, one must be subtracted from a register's identifier to find its equivalent address. The page number notation is not part of the address.

Example:

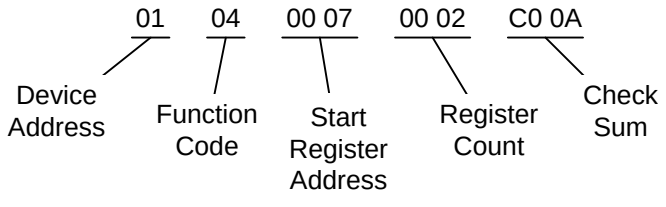
Task:

Obtain the status of the output contacts from the Schneider Electric MiCOM Pxxx device at address 1.

The output contact status is a 32-bit binary string held in input registers 3x8 and 3x9 (see the *Binary Status Information* section).

Select MODBUS function code 4 “Read input registers” and request two registers starting at input register address 7. Note the register address is one less than the required register ordinal.

The MODBUS query frame is:

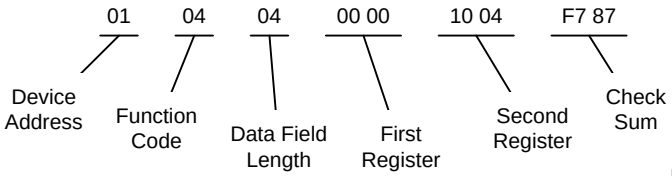


P2700ENa

Note that the following frame data is shown in hexadecimal 8-bit bytes.

The frame is transmitted from left to right by the master device. The start register address, register count and check sum are all 16-bit numbers that are transmitted in a high byte - low byte order.

The query may elicit the following response: [4]



P2701ENb

The frame was transmitted from left to right by the slave device. The response frame is valid because the eighth bit of the function code field is not set. The data field length is 4 bytes since the query was a read from two 16-bit registers. The data field consists of two pairs of bytes in a high byte - low byte order with the first requested register’s data coming first. Therefore the request for the 32-bit output contact status starting at register 3x8 is 00001004h (1000000000100b), which shows that outputs 3 and 13 are energized and the remaining outputs are de-energized.

5.6 Register Map

For a complete map of the MODBUS addresses supported by the product, see the *Relay Menu Database document*.

The register map tables in this document include an Equivalent Courier Cell column. The cell identifiers relate to the product’s internal Courier database and may be used in cross-reference with the Courier Protocol documentation or the product’s front panel user interface documentation.

The Data Format column specifies the format of the data presented by the associated MODBUS register or registers. The *Register Data Types* section describes the formats used.

The right-hand columns in the tables show whether the register is used in a particular product model. An asterisk indicates that the model uses the register.

5.7 Measurement Values

This table presents all of the product's available measurements: analog values and counters. An asterisk indicates that the model uses the register. Their values are refreshed approximately every second.

Measurement name	Measurement unit	Equivalent courier cell		Start register	End register	Data format	Data size registers	Cell type	P642	P643	P645
Measurements 1		02	00								
IA-1 Magnitude	Amps	02	01	3x11200	3x11201	G24	2	Data	*	*	*
IA-1 Phase Angle	Degrees	02	02	3x11202		G30	1	Data	*	*	*
IB-1 Magnitude	Amps	02	03	3x11203	3x11204	G24	2	Data	*	*	*
IB-1 Phase Angle	Degrees	02	04	3x11205		G30	1	Data	*	*	*
IC-1 Magnitude	Amps	02	05	3x11206	3x11207	G24	2	Data	*	*	*
IC-1 Phase Angle	Degrees	02	06	3x11208		G30	1	Data	*	*	*
IA-2 Magnitude	Amps	02	07	3x11209	3x11210	G24	2	Data	*	*	*
IA-2 Phase Angle	Degrees	02	08	3x11211		G30	1	Data	*	*	*
IB-2 Magnitude	Amps	02	09	3x11212	3x11213	G24	2	Data	*	*	*
IB-2 Phase Angle	Degrees	02	0A	3x11214		G30	1	Data	*	*	*
IC-2 Magnitude	Amps	02	0B	3x11215	3x11216	G24	2	Data	*	*	*
IC-2 Phase Angle	Degrees	02	0C	3x11217		G30	1	Data	*	*	*
IA-3 Magnitude	Amps	02	0D	3x11218	3x11219	G24	2	Data		*	*
IA-3 Phase Angle	Degrees	02	0E	3x11220		G30	1	Data		*	*
IB-3 Magnitude	Amps	02	0F	3x11221	3x11222	G24	2	Data		*	*
IB-3 Phase Angle	Degrees	02	10	3x11223		G30	1	Data		*	*
IC-3 Magnitude	Amps	02	11	3x11224	3x11225	G24	2	Data		*	*
IC-3 Phase Angle	Degrees	02	12	3x11226		G30	1	Data		*	*
IA-4 Magnitude	Amps	02	13	3x11227	3x11228	G24	2	Data			*
IA-4 Phase Angle	Degrees	02	14	3x11229		G30	1	Data			*
IB-4 Magnitude	Amps	02	15	3x11230	3x11231	G24	2	Data			*
IB-4 Phase Angle	Degrees	02	16	3x11232		G30	1	Data			*
IC-4 Magnitude	Amps	02	17	3x11233	3x11234	G24	2	Data			*
IC-4 Phase Angle	Degrees	02	18	3x11235		G30	1	Data			*
IA-5 Magnitude	Amps	02	19	3x11236	3x11237	G24	2	Data			*
IA-5 Phase Angle	Degrees	02	1A	3x11238		G30	1	Data			*
IB-5 Magnitude	Amps	02	1B	3x11239	3x11240	G24	2	Data			*
IB-5 Phase Angle	Degrees	02	1C	3x11241		G30	1	Data			*
IC-5 Magnitude	Amps	02	1D	3x11242	3x11243	G24	2	Data			*
IC-5 Phase Angle	Degrees	02	1E	3x11244		G30	1	Data			*
IA-HV Magnitude	Amps	02	50	3x11308	3x11309	G24	2	Data	*	*	*
IA-HV Phase Ang	Degrees	02	51	3x11310		G30	1	Data	*	*	*
IB-HV Magnitude	Amps	02	52	3x11311	3x11312	G24	2	Data	*	*	*
IB-HV Phase Ang	Degrees	02	53	3x11313		G30	1	Data	*	*	*
IC-HV Magnitude	Amps	02	54	3x11314	3x11315	G24	2	Data	*	*	*
IC-HV Phase Ang	Degrees	02	55	3x11316		G30	1	Data	*	*	*
IA-LV Magnitude	Amps	02	56	3x11317	3x11318	G24	2	Data	*	*	*
IA-LV Phase Ang	Degrees	02	57	3x11319		G30	1	Data	*	*	*
IB-LV Magnitude	Amps	02	58	3x11320	3x11321	G24	2	Data	*	*	*

Measurement name	Measurement unit	Equivalent courier cell		Start register	End register	Data format	Data size registers	Cell type	P642	P643	P645
IB-LV Phase Ang	Degrees	02	59	3x11322		G30	1	Data	*	*	*
IC-LV Magnitude	Amps	02	5A	3x11323	3x11324	G24	2	Data	*	*	*
IC-LV Phase Ang	Degrees	02	5B	3x11325		G30	1	Data	*	*	*
IA-TV Magnitude	Amps	02	5C	3x11326	3x11327	G24	2	Data		*	*
IA-TV Phase Ang	Degrees	02	5D	3x11328		G30	1	Data		*	*
IB-TV Magnitude	Amps	02	5E	3x11329	3x11330	G24	2	Data		*	*
IB-TV Phase Ang	Degrees	02	5F	3x11331		G30	1	Data		*	*
IC-TV Magnitude	Amps	02	60	3x11332	3x11333	G24	2	Data		*	*
IC-TV Phase Ang	Degrees	02	61	3x11334		G30	1	Data		*	*
I0-1 Magnitude	Amps	02	62	3x11335	3x11336	G24	2	Data	*	*	*
I1-1 Magnitude	Amps	02	63	3x11337	3x11338	G24	2	Data	*	*	*
I2-1 Magnitude	Amps	02	64	3x11339	3x11340	G24	2	Data	*	*	*
IN-HV Mea Mag	Amps	02	65	3x11341	3x11342	G24	2	Data	*	*	*
IN-HV Mea Ang	Degrees	02	66	3x11343		G30	1	Data	*	*	*
IN-HV Deriv Mag IN-1 Derived Mag	Amps	02	67	3x11344	3x11345	G24	2	Data	*	*	*
IN-HV Deriv Ang IN-1 Derived Ang	Degrees	02	68	3x11346		G30	1	Data	*	*	*
I0-2 Magnitude	Amps	02	69	3x11347	3x11348	G24	2	Data	*	*	*
I1-2 Magnitude	Amps	02	6A	3x11349	3x11350	G24	2	Data	*	*	*
I2-2 Magnitude	Amps	02	6B	3x11351	3x11352	G24	2	Data	*	*	*
IN-LV Mea Mag	Amps	02	6C	3x11353	3x11354	G24	2	Data	*	*	*
IN-LV Mea Ang	Degrees	02	6D	3x11355		G30	1	Data	*	*	*
IN-LV Deriv Mag IN-2 Derived Mag	Amps	02	6E	3x11356	3x11357	G24	2	Data	*	*	*
IN-LV Deriv Ang IN-2 Derived Ang	Degrees	02	6F	3x11358		G30	1	Data	*	*	*
I0-3 Magnitude	Amps	02	70	3x11359	3x11360	G24	2	Data		*	*
I1-3 Magnitude	Amps	02	71	3x11361	3x11362	G24	2	Data		*	*
I2-3 Magnitude	Amps	02	72	3x11363	3x11364	G24	2	Data		*	*
IN-TV Mea Mag	Amps	02	73	3x11365	3x11366	G24	2	Data		*	*
IN-TV Mea Ang	Degrees	02	74	3x11367		G30	1	Data		*	*
IN-TV Deriv Mag IN-3 Derived Mag	Amps	02	75	3x11368	3x11369	G24	2	Data		*	*
IN-TV Deriv Ang IN-3 Derived Ang	Degrees	02	76	3x11370		G30	1	Data		*	*
I0-4 Magnitude	Amps	02	77	3x11371	3x11372	G24	2	Data			*
I1-4 Magnitude	Amps	02	78	3x11373	3x11374	G24	2	Data			*
I2-4 Magnitude	Amps	02	79	3x11375	3x11376	G24	2	Data			*
I0-5 Magnitude	Amps	02	7C	3x11380	3x11381	G24	2	Data			*
I1-5 Magnitude	Amps	02	7D	3x11382	3x11383	G24	2	Data			*
I2-5 Magnitude	Amps	02	7E	3x11384	3x11385	G24	2	Data			*
IA-HV RMS	Amps	02	86	3x11398	3x11399	G24	2	Data	*	*	*
IB-HV RMS	Amps	02	87	3x11400	3x11401	G24	2	Data	*	*	*
IC-HV RMS	Amps	02	88	3x11402	3x11403	G24	2	Data	*	*	*

Measurement name	Measurement unit	Equivalent courier cell		Start register	End register	Data format	Data size registers	Cell type	P642	P643	P645
IA-LV RMS	Amps	02	89	3x11404	3x11405	G24	2	Data	*	*	*
IB-LV RMS	Amps	02	8A	3x11406	3x11407	G24	2	Data	*	*	*
IC-LV RMS	Amps	02	8B	3x11408	3x11409	G24	2	Data	*	*	*
IA-TV RMS	Amps	02	8C	3x11410	3x11411	G24	2	Data		*	*
IB-TV RMS	Amps	02	8D	3x11412	3x11413	G24	2	Data		*	*
IC-TV RMS	Amps	02	8E	3x11414	3x11415	G24	2	Data		*	*
VAN Magnitude	Volts	02	8F	3x11416	3x11417	G24	2	Data		*	*
VAN Phase Angle	Degrees	02	90	3x11418		G30	1	Data		*	*
VBN Magnitude	Volts	02	91	3x11419	3x11420	G24	2	Data		*	*
VBN Phase Angle	Degrees	02	92	3x11421		G30	1	Data		*	*
VCN Magnitude	Volts	02	93	3x11422	3x11423	G24	2	Data		*	*
VCN Phase Angle	Degrees	02	94	3x11424		G30	1	Data		*	*
Vx Magnitude	Volts	02	95	3x11425	3x11426	G24	2	Data	*	*	*
Vx Phase Angle	Degrees	02	96	3x11427		G30	1	Data	*	*	*
V1 Magnitude	Volts	02	97	3x11428	3x11429	G24	2	Data		*	*
V2 Magnitude	Volts	02	98	3x11430	3x11431	G24	2	Data		*	*
V0 Magnitude	Volts	02	99	3x11432	3x11433	G24	2	Data		*	*
VN Derived Mag	Volts	02	9A	3x11434	3x11435	G24	2	Data		*	*
VN Derived Angle	Degrees	02	9B	3x11436		G30	1	Data		*	*
VAB Magnitude	Volts	02	9C	3x11437	3x11438	G24	2	Data		*	*
VAB Phase Angle	Degrees	02	9D	3x11439		G30	1	Data		*	*
VBC Magnitude	Volts	02	9E	3x11440	3x11441	G24	2	Data		*	*
VBC Phase Angle	Degrees	02	9F	3x11442		G30	1	Data		*	*
VCA Magnitude	Volts	02	A0	3x11443	3x11444	G24	2	Data		*	*
VCA Phase Angle	Degrees	02	A1	3x11445		G30	1	Data		*	*
VAN RMS	Volts	02	A2	3x11446	3x11447	G24	2	Data		*	*
VBN RMS	Volts	02	A3	3x11448	3x11449	G24	2	Data		*	*
VCN RMS	Volts	02	A4	3x11450	3x11451	G24	2	Data		*	*
Frequency	Hz	02	AA	3x11452		G30	1	Data	*	*	*
A Phase Watts	Watts	03	01	3x11500	3x11502	G29	3	Data		*	*
A Phase Watts	Watts	03	02	3x11503	3x11505	G29	3	Data		*	*
A Phase Watts	Watts	03	03	3x11506	3x11508	G29	3	Data		*	*
B Phase Watts	Watts	03	04	3x11509	3x11511	G29	3	Data		*	*
B Phase Watts	Watts	03	05	3x11512	3x11514	G29	3	Data		*	*
B Phase Watts	Watts	03	06	3x11515	3x11517	G29	3	Data		*	*
C Phase Watts	Watts	03	07	3x11518	3x11520	G29	3	Data		*	*
C Phase Watts	Watts	03	08	3x11521	3x11523	G29	3	Data		*	*
C Phase Watts	Watts	03	09	3x11524	3x11526	G29	3	Data		*	*
A Phase VArs	VAr	03	0A	3x11527	3x11529	G29	3	Data		*	*
A Phase VArs	VAr	03	0B	3x11530	3x11532	G29	3	Data		*	*
A Phase VArs	VAr	03	0C	3x11533	3x11535	G29	3	Data		*	*
B Phase VArs	VAr	03	0D	3x11536	3x11538	G29	3	Data		*	*
B Phase VArs	VAr	03	0E	3x11539	3x11541	G29	3	Data		*	*

Measurement name	Measurement unit	Equivalent courier cell		Start register	End register	Data format	Data size registers	Cell type	P642	P643	P645
B Phase VArs	VAr	03	0F	3x11542	3x11544	G29	3	Data		*	*
C Phase VArs	VAr	03	10	3x11545	3x11547	G29	3	Data		*	*
C Phase VArs	VAr	03	11	3x11548	3x11550	G29	3	Data		*	*
C Phase VArs	VAr	03	12	3x11551	3x11553	G29	3	Data		*	*
A Phase VA	VA	03	13	3x11554	3x11556	G29	3	Data		*	*
A Phase VA	VA	03	14	3x11557	3x11559	G29	3	Data		*	*
A Phase VA	VA	03	15	3x11560	3x11562	G29	3	Data		*	*
B Phase VA	VA	03	16	3x11563	3x11565	G29	3	Data		*	*
B Phase VA	VA	03	17	3x11566	3x11568	G29	3	Data		*	*
B Phase VA	VA	03	18	3x11569	3x11571	G29	3	Data		*	*
C Phase VA	VA	03	19	3x11572	3x11574	G29	3	Data		*	*
C Phase VA	VA	03	1A	3x11575	3x11577	G29	3	Data		*	*
C Phase VA	VA	03	1B	3x11578	3x11580	G29	3	Data		*	*
3 Phase Watts	Watts	03	1C	3x11581	3x11583	G29	3	Data		*	*
3 Phase Watts	Watts	03	1D	3x11584	3x11586	G29	3	Data		*	*
3 Phase Watts	Watts	03	1E	3x11587	3x11589	G29	3	Data		*	*
3 Phase VArs	VAr	03	1F	3x11590	3x11592	G29	3	Data		*	*
3 Phase VArs	VAr	03	20	3x11593	3x11595	G29	3	Data		*	*
3 Phase VArs	VAr	03	21	3x11596	3x11598	G29	3	Data		*	*
3 Phase VA	VA	03	22	3x11599	3x11601	G29	3	Data		*	*
3 Phase VA	VA	03	23	3x11602	3x11604	G29	3	Data		*	*
3 Phase VA	VA	03	24	3x11605	3x11607	G29	3	Data		*	*
3Ph Power Factor	% pf	03	25	3x11608		G30	1	Data		*	*
APh Power Factor	% pf	03	26	3x11609		G30	1	Data		*	*
BPh Power Factor	% pf	03	27	3x11610		G30	1	Data		*	*
CPh Power Factor	% pf	03	28	3x11611		G30	1	Data		*	*
3Ph WHours Fwd	Wh	03	29	3x11612	3x11614	G29	3	Data		*	*
3Ph WHours Rev	Wh	03	2A	3x11615	3x11617	G29	3	Data		*	*
3Ph VArHours Fwd	VArh	03	2B	3x11618	3x11620	G29	3	Data		*	*
3Ph VArHours Rev	VArh	03	2C	3x11621	3x11623	G29	3	Data		*	*
3Ph W Fix Demand	Watts	03	2D	3x11624	3x11626	G29	3	Data		*	*
3Ph VArs Fix Demand	VArs	03	2E	3x11627	3x11629	G29	3	Data		*	*
3 Ph W Roll Dem	Watts	03	2F	3x11630	3x11632	G29	3	Data		*	*
3 Ph VArs Roll Dem	VAr	03	30	3x11633	3x11635	G29	3	Data		*	*
3Ph W Peak Dem	Watts	03	31	3x11636	3x11638	G29	3	Data		*	*
3Ph VAr Peak Dem	VAr	03	32	3x11639	3x11641	G29	3	Data		*	*
Reset Demand	Indexed String	03	50	4x00103		G11	1	Data		*	*
IA Differential IA Z1 Diff	Amps	04	01	3x11750	3x11751	G24	2	Data	*	*	*
IB Differential IB Z1 Diff	Amps	04	02	3x11752	3x11753	G24	2	Data	*	*	*
IC Differential IC Z1 Diff	Amps	04	03	3x11754	3x11755	G24	2	Data	*	*	*
IA Bias IA Z1 Bias	Amps	04	04	3x11756	3x11757	G24	2	Data	*	*	*

Measurement name	Measurement unit	Equivalent courier cell		Start register	End register	Data format	Data size registers	Cell type	P642	P643	P645
IB Bias IB Z1 Bias	Amps	04	05	3x11758	3x11759	G24	2	Data	*	*	*
IC Bias IC Z1 Bias	Amps	04	06	3x11760	3x11761	G24	2	Data	*	*	*
IA Diff 2H IA Z1 Diff 2H	Amps	04	07	3x11762	3x11763	G24	2	Data	*	*	*
IB Diff 2H IB Z1 Diff 2H	Amps	04	08	3x11764	3x11765	G24	2	Data	*	*	*
IC Diff 2H IC Z1 Diff 2H	Amps	04	09	3x11766	3x11767	G24	2	Data	*	*	*
IA Diff 5H IA Z2 Diff	Amps	04	0A	3x11768	3x11769	G24	2	Data	*	*	*
IB Diff 5H IB Z2 Diff	Amps	04	0B	3x11770	3x11771	G24	2	Data	*	*	*
IC Diff 5H IC Z2 Diff	Amps	04	0C	3x11772	3x11773	G24	2	Data	*	*	*
IREF HV LoZ Diff IA Z2 Bias	Amps	04	0D	3x11774	3x11775	G24	2	Data	*	*	*
IREF HV LoZ Bias IB Z2 Bias	Amps	04	0E	3x11776	3x11777	G24	2	Data	*	*	*
IREF LV LoZ Diff	Amps	04	0F	3x11778	3x11779	G24	2	Data	*	*	*
IREF LV LoZ Bias IA Z2 Diff 2H	Amps	04	10	3x11780	3x11781	G24	2	Data	*	*	*
IREF TV LoZ Diff IB Z2 Diff 2H	Amps	04	11	3x11782	3x11783	G24	2	Data		*	*
IREF TV LoZ Bias IC Z2 Diff 2H	Amps	04	12	3x11784	3x11785	G24	2	Data		*	*
Hot Spot T	°C	04	28	3x11798		G10	1	Data	*	*	*
Top Oil T	°C	04	2A	3x11799		G10	1	Data	*	*	*
Ambient T	°C	04	2C	3x11800		G10	1	Data	*	*	*
TOL Pretrip left	Courier Number (decimal)	04	2D	3x11801	3x11802	G24	2	Data	*	*	*
LOL status	Courier Number (decimal)	04	2F	3x11803	3x11804	G27	2	Data	*	*	*
Rate of LOL	Courier Number (decimal)	04	31	3x11805		G24	2	Data	*	*	*
LOL Aging Factor	Courier Number (decimal)	04	32	3x11807	3x11808	G27	2	Data	*	*	*
Lres at designed	Courier Number (decimal)	04	33	3x11809	3x11810	G27	2	Data	*	*	*
FAA,m	Courier Number (decimal)	04	34	3x11811	3x11812	G27	2	Data	*	*	*
Lres at FAA,m	Courier Number (decimal)	04	35	3x11813	3x11814	G24	2	Data	*	*	*
Volts/Hz	(Sub Heading)	04	38						*	*	*
Volts/Hz W1	Volts/Hz	04	39	3x11815		G24	2	Data		*	*
V/Hz W1 tPretrip	Courier Number (time)	04	3A	3x11817	3x11818	G24	2	Data		*	*

Measurement name	Measurement unit	Equivalent courier cell		Start register	End register	Data format	Data size registers	Cell type	P642	P643	P645
V/Hz W1 Thermal	Courier Number (time)	04	3B	3x11819	3x11820	G24	2	Data		*	*
Volts/Hz W2	Volts/Hz	04	3D	3x11821		G24	2	Data	*	*	*
V/Hz W2 tPretrip	Courier Number (time)	04	3E	3x11823	3x11824	G24	2	Data	*	*	*
V/Hz W2 Thermal	Courier Number (time)	04	3F	3x11825	3x11826	G24	2	Data	*	*	*
RTD 1 label	Courier Number (decimal)	04	60	3x11827		G10	1	Data	*	*	*
RTD 2 label	Courier Number (decimal)	04	61	3x11828		G10	1	Data	*	*	*
RTD 3 label	Courier Number (decimal)	04	62	3x11829		G10	1	Data	*	*	*
RTD 4 label	Courier Number (decimal)	04	63	3x11830		G10	1	Data	*	*	*
RTD 5 label	Courier Number (decimal)	04	64	3x11831		G10	1	Data	*	*	*
RTD 6 label	Courier Number (decimal)	04	65	3x11832		G10	1	Data	*	*	*
RTD 7 label	Courier Number (decimal)	04	66	3x11833		G10	1	Data	*	*	*
RTD 8 label	Courier Number (decimal)	04	67	3x11834		G10	1	Data	*	*	*
RTD 9 label	Courier Number (decimal)	04	68	3x11835		G10	1	Data	*	*	*
RTD 10 label	Courier Number (decimal)	04	69	3x11836		G10	1	Data	*	*	*
RTD Open Cct	Binary Flag (10 bits)	04	6A	3x11837		G108	1	Data	*	*	*
RTD Short Cct	Binary Flag (10 bits)	04	6B	3x11838		G109	1	Data	*	*	*
RTD Data Error	Binary Flag (10 bits)	04	6C	3x11839		G110	1	Data	*	*	*
CLIO Input 1	Courier Number (Decimal)	04	70	3x11840	3x11841	G125	2	Data	*	*	*
CLIO Input 2	Courier Number (Decimal)	04	71	3x11842	3x11843	G125	2	Data	*	*	*
CLIO Input 3	Courier Number (Decimal)	04	72	3x11844	3x11845	G125	2	Data	*	*	*
CLIO Input 4	Courier Number (Decimal)	04	73	3x11846	3x11847	G125	2	Data	*	*	*

Table 8 - Measurement data available in the P64x product range

5.8 Binary Status Information

Binary status information is available for the product's optically-isolated status inputs (optos), relay contact outputs, alarm flags, control inputs, internal Digital Data Bus (DDB), and the front panel 25-pin test port (see Note).

> *Note* *The test port allows the product to be configured to map up to eight of its DDB signals (see the Relay Menu Database document) to eight output pins. The usual application is to control test equipment. However, since the test port output status is available on the MODBUS interface, it could be used to efficiently collect up to eight DDB signals.*

The product's internal DDB consists of 1023 binary-status flags. The allocation of the points in the DDB are largely product and version specific. See the *Relay Menu Database document*, for a definition of the product's DDB.

The relay-contact status information is available from the 0x "Coil Status" MODBUS page and from the 3x "Input Register" MODBUS page. For legacy reasons the information is duplicated in the 3x page with explicit registers (8 & 9) and in the DDB status register area (723 & 724).

The current state of the optically isolated status inputs is available from the 1x "Input Status" MODBUS page and from the 3x "Input Register" MODBUS page. The principal 3x registers are part of the DDB status register area (725 & 726). For legacy reasons, a single register at 3x00007 provides the status of the first 16 inputs.

The 0x "Coil Status" and 1x "Input Status" pages allow individual or blocks of binary status flags to be read. The resultant data is left aligned and transmitted in a big-endian (high-order to low-order) format in the response frame. Relay contact 1 is mapped to coil 1, contact 2 to coil 2 and so on. Similarly, opto input 1 is mapped to input 1, opto input 2 to input 2 and so on.

The following table shows the available 3x and 4x binary status information.

Name	Equivalent courier cell	Start register	End register	Data format	Data size (registers)	P64 2	P64 3	P64 5
Opto I/P Status	0030	3x11027	3x11028	G8	2	*	*	*
Relay O/P Status	0040	3x00008	3x00009	G9	2	*	*	*
Alarm Status 1	0050	3x00011	3x00012	G96	2	*	*	*
Alarm Status 2	0051	3x00013	3x00014	G128	2	*	*	*
Alarm Status 3	0052	3x00015	3x00016	G228	2	*	*	*
Ctrl I/P Status	1201	4x00950	4x00951	G202	2	*	*	*
Relay Test Port Status	0F03	3x00722		G1	1	*	*	*
DDB 31 - 0	0F20	3x11023	3x11024	G27	2	*	*	*
DDB 63 - 32	0F21	3x11025	3x11026	G27	2	*	*	*
DDB 95 - 64	0F22	3x11027	3x11028	G27	2	*	*	*
DDB 127 - 96	0F23	3x11029	3x11030	G27	2	*	*	*
DDB 159 - 128	0F24	3x11031	3x11032	G27	2	*	*	*
DDB 191 - 160	0F25	3x11033	3x11034	G27	2	*	*	*
DDB 223 - 192	0F26	3x11035	3x11036	G27	2	*	*	*
DDB 255 - 224	0F27	3x11037	3x11038	G27	2	*	*	*
DDB 287 - 256	0F28	3x11039	3x11040	G27	2	*	*	*
DDB 319 - 288	0F29	3x11041	3x11042	G27	2	*	*	*
DDB 351 - 320	0F2A	3x11043	3x11044	G27	2	*	*	*
DDB 383 - 352	0F2B	3x11045	3x11046	G27	2	*	*	*
DDB 415 - 384	0F2C	3x11047	3x11048	G27	2	*	*	*
DDB 447 - 416	0F2D	3x11049	3x11050	G27	2	*	*	*
DDB 479 - 448	0F2E	3x11051	3x11052	G27	2	*	*	*
DDB 511 - 480	0F2F	3x11053	3x11054	G27	2	*	*	*
DDB 543 - 512	0F30	3x11055	3x11056	G27	2	*	*	*
DDB 575 - 544	0F31	3x11057	3x11058	G27	2	*	*	*
DDB 607 - 576	0F32	3x11059	3x11060	G27	2	*	*	*
DDB 639 - 608	0F33	3x11061	3x11062	G27	2	*	*	*

Name	Equivalent courier cell	Start register	End register	Data format	Data size (registers)	P64 2	P64 3	P64 5
DDB 671 - 640	0F34	3x11063	3x11064	G27	2	*	*	*
DDB 703 - 672	0F35	3x11065	3x11066	G27	2	*	*	*
DDB 735 - 704	0F36	3x11067	3x11068	G27	2	*	*	*
DDB 767 - 736	0F37	3x11069	3x11070	G27	2	*	*	*
DDB 799 - 768	0F38	3x11071	3x11072	G27	2	*	*	*
DDB 831 - 800	0F39	3x11073	3x11074	G27	2	*	*	*
DDB 863 - 832	0F3A	3x11075	3x11076	G27	2	*	*	*
DDB 895 - 864	0F3B	3x11077	3x11078	G27	2	*	*	*
DDB 927 - 896	0F3C	3x11079	3x11080	G27	2	*	*	*
DDB 959 - 928	0F3D	3x11081	3x11082	G27	2	*	*	*
DDB 991 - 960	0F3E	3x11083	3x11084	G27	2	*	*	*
DDB 1023 - 992	0F3F	3x11085	3x11086	G27	2	*	*	*
DDB 1055-1024	0F40	3x11087	3x11088	G27	2	*	*	*
DDB 1087-1056	0F41	3x11089	3x11090	G27	2	*	*	*
DDB 1119-1088	0F42	3x11091	3x11092	G27	2	*	*	*
DDB 1151-1120	0F43	3x11093	3x11094	G27	2	*	*	*
DDB 1183-1152	0F44	3x11095	3x11096	G27	2	*	*	*
DDB 1215-1184	0F45	3x11097	3x11098	G27	2	*	*	*
DDB 1247-1216	0F46	3x11099	3x11100	G27	2	*	*	*
DDB 1279-1248	0F47	3x11101	3x11102	G27	2	*	*	*
DDB 1311-1280	0F48	3x11103	3x11104	G27	2	*	*	*
DDB 1343-1312	0F49	3x11105	3x11106	G27	2	*	*	*
DDB 1375-1344	0F4A	3x11107	3x11108	G27	2	*	*	*
DDB 1407-1376	0F4B	3x11109	3x11110	G27	2	*	*	*
DDB 1439-1408	0F4C	4x10493	4x10494	G27	2	*	*	*
DDB 1471-1440	0F4D	4x10493	4x10494	G27	2	*	*	*
DDB 1503-1472	0F4E	4x10493	4x10494	G27	2	*	*	*
DDB 1535-1504	0F4F	4x10493	4x10494	G27	2	*	*	*
DDB 1567-1536	0F50	4x10493	4x10494	G27	2	*	*	*
DDB 1599-1568	0F51	4x10493	4x10494	G27	2	*	*	*
DDB 1631-1600	0F52	4x10493	4x10494	G27	2	*	*	*
DDB 1663-1632	0F53	4x10493	4x10494	G27	2	*	*	*
DDB 1695-1664	0F54	4x10493	4x10494	G27	2	*	*	*
DDB 1727-1696	0F55	4x10493	4x10494	G27	2	*	*	*
DDB 1759-1728	0F56	4x10493	4x10494	G27	2	*	*	*
DDB 1791-1760	0F57	4x10493	4x10494	G27	2	*	*	*
DDB 1823-1792	0F58	4x10493	4x10494	G27	2	*	*	*
DDB 1855-1824	0F59	4x10493	4x10494	G27	2	*	*	*
DDB 1887-1856	0F5A	4x10493	4x10494	G27	2	*	*	*
DDB 1919-1888	0F5B	4x10493	4x10494	G27	2	*	*	*
DDB 1951-1920	0F5C	4x10493	4x10494	G27	2	*	*	*
DDB 1983-1952	0F5D	4x10493	4x10494	G27	2	*	*	*
DDB 2015-1984	0F5E	4x10493	4x10494	G27	2	*	*	*
DDB 2047-2016	0F5F	4x10493	4x10494	G27	2	*	*	*

Table 9 - Binary status information available in the P64x product range

5.9 Measurement and Binary Status 3x Register Sets

The data available from the 3x input registers is arranged into register sets. A register set is a fixed collection of values in a contiguous block of register addresses. The advantage of this is that multiple values may be read with a single MODBUS query, function code 4 “Read Input Registers”, up to the maximum data limits of the query, see the *Maximum Query and Response Parameters* section.

The definition of a register-set is specified by the selection of a start and end address, which can span multiple contiguous values in the 3x Register, see the *Relay Menu Database document*. The only rule is that a register set must not result in an attempt to read only part of a multi-register data type, see the *Register Data Types* section. A register set can span unused register locations, in which case a value of zero is returned for each such register location.

Some examples of useful register sets are:

- For P64x:
  - 3x701 to 3x786 provide a selection of measurement and binary-status values. Some of these registers are duplicates of other register values.
  - 3x723 to 3x786 provide the DDB status.
  - 3x391 to 3x408 provide the per phase power measurements in floating point format.
  - 3x409 to 3x414 provide the three-phase power measurements in floating point format.
  - 3x184 to 3x193 provide the ten RTD measurement values (P642/P643 only).

There are many other possibilities depending on your application and an appraisal of the 3x Register Map in the *Relay Menu Database document.* The capabilities of the MODBUS master device, performance targets, and communications latencies may also influence the degree to which multiple values are read as register sets, as opposed to individually.

5.10 Controls

The *Control (commands) available in the product range* table shows MODBUS 4x “Holding Registers” that allow the external system to control aspects of the product’s behavior, configuration, records, or items of plant connected to the product such as circuit breakers.

The **Command or setting** column indicates whether the control is a self-resetting “Command” or a state based “Setting”.

“Command” controls automatically return to their default value when the control action has been completed. This may cause problems with masters that try to verify write requests by reading back the value that was written.

“Setting” controls maintain the written value, assuming that it was accepted. For example, the **Active Settings** register reports the current active group on reads. The Active Setting Group register also accepts writes with a valid setting group number to change the active group to the one specified. This assumes that the setting group selection by optically isolated status inputs has not been enabled and that the specified group is enabled.

Entries without a defined setting range, as for the **min.**, **max.** and **step** columns, are binary-string values whose pattern is defined by its stated data type.

5.11 Event Extraction

The product can store up to 512 event records in battery backed-up memory. An event record consists of a time stamp, a record type, and a set of information fields. The record type and the information fields record the event that occurred at the time captured by the time stamp.

The product has several classes of event record:

- Alarm events
- Opto-isolated status input events
- Relay contact output events
- Protection/DDB operation events
- Fault data capture events
- General events

The *Relay Menu Database document* specifies the available events. The product provides an "event filtering" feature that may be used to prevent specific events from being logged. The event filter is configured in the **Record Control** section of the product's menu database in the MiCOM S1 Studio configuration tool.

The product supports two methods of event extraction providing either automatic or manual extraction of the stored event, fault, and maintenance records.

The product stores event, fault, and maintenance records in three separate queues. As entries are added to the fault and maintenance queues, a corresponding event is added to the event queue. Each queue is of different length and each queue may be individually cleared – see the *Event Record Delection* section. It is therefore possible to have a fault event or a maintenance event entry in the event queue with no corresponding entry in the associated queue because it has been overwritten or deleted.

The manual extraction procedure (see the *Manual Extraction Procedure section*) allows each of these three queues to be read independently.

The automatic extraction procedure (sss the *Automatic Extraction Procedure* s*ection*) reads records from the event queue. If the event record is a fault or a maintenance record, the record's extended data is read also, if it is available from their queues.

5.11.1 Manual Extraction Procedure

There are three registers used to manually select stored records. For each of these registers, zero represents the most-recent stored record. For example:

- 4x00100 - Select Event, 0 to 511.
  511 was 249 in P24x software version 57, P34x/P64x software versions 01, 02, 03, 04, 05, 06, & 07, since they only stored 250 event records.
- 4x00101 - Select Fault, 0 to 4
- 4x00102 - Select Maintenance Record, 0 to 4

There are also three read-only registers used to determine the number of various types of stored records. For example:

- 3x10000 - Number of stored event records
- 3x10001 - Number of stored fault records
- 3x10002 - Number of stored maintenance records

Each fault or maintenance record logged causes an event record to be created by the product. If this event record is selected, the additional registers showing the fault or maintenance record details are also populated.

5.11.2 Automatic Extraction Procedure

Automatic event-record extraction allows records to be extracted as they occur. Event records are extracted in sequential order, including any fault or maintenance data that may be associated with an event.

The MODBUS master can determine whether the product has any events stored that have not yet been extracted. This is done by reading the product's status register 3x00001 (G26 data type). If the event bit of this register is set, the product contains event records that have not yet been extracted.

To select the next event for sequential extraction, the master station writes a value of one to the record selection register 4x00400 (G18 data type). The event data, plus any fault or maintenance data, can be read from the registers specified in the *Record Data* section. Once the data has been read, the event record is marked. This is done by writing a value of 2 to register 4x00400. The G18 data type consists of bit fields. Therefore it is also possible to both mark the current record as read and automatically select the next unread record. This is done by writing a value of 3 to the register.

When the last (most recent) record is accepted, the event flag in the status register (3x00001) resets. If the last record is accepted by writing a value of 3 to the record selection register (4x00400), a dummy record appears in the event-record registers with an "Event Type" value of 255. Selecting another record when none are available gives a MODBUS exception code 3, "Invalid value" (see the *MODBUS Response Code Interpretation* section).

One possible event record extraction procedure is shown in the following *Automatic event extraction procedure* diagram.

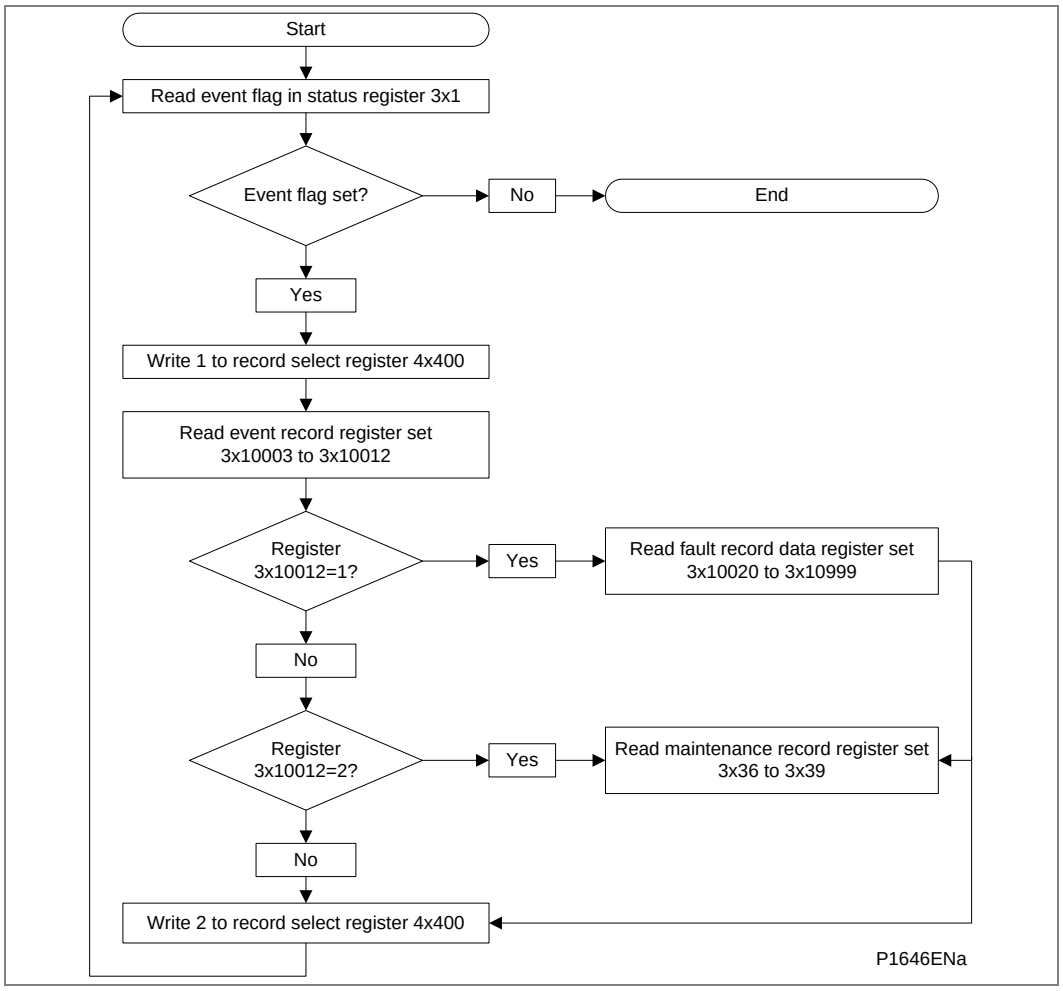


Figure 6 - Automatic event extraction procedure

5.11.3 Record Data

The location and format of the registers used to access the record data is the same whether they have been selected using manual or automatic extraction mechanisms, see the *Manual Extraction Procedure* and *Automatic Extraction Procedure* sections.

Description	Register	Length (registers)	Comments
Time Stamp	3x10003	4	See G12 data type in the Relay Menu Database document, P64x/EN MD.
Event Type	3x10007	1	Indicates the type of the event record. See G13 data type in the Relay Menu Database document, P64x/EN MD (a value of 255 indicates that the end of the event log has been reached).
Event Value	3x10008	2	Contains the associated status register value as a string of binary flags for relay-contact, opto-input, alarm, and protection events. Otherwise it has a value of zero. When a status value is supplied, the value represents the recorded value of the event types associated register pair, as indicated by the Event Origin value (see Note 1).
Event Origin	3x10010	1	The Event Original value indicates the MODBUS Register pair where the change occurred (see Note 2). Possible values are: 30011: Alarm Status 1 event 30013: Alarm Status 2 event 30015: Alarm Status 3 event 30723: Relay contact event (2 registers: DDB 0-31 status) 30725: Status input event (2 registers: DDB 32-63 status) 30727 to 30785: Protection events (Indicates the 32-bit DDB status word that was the origin of the event) For General events, Fault events, and Maintenance events, a value of zero is returned.
Event Index	3x10011	1	The Event Index value is used to distinguish between events with the same Event Type and Event Origin. The registers value depends on the type of the event: For protection events, the value is the ID of the DDB that caused the event. For alarm events, the value is the ID of the alarm that caused the event. In both cases, the value includes the direction of the state transition in the Most Significant Bit. This direction bit is 1 for a 0-1 (low to high) change, and 0 for a 1-0 (high to low) change. For all other types of events, it has a value of zero.
Additional Data Present	3x10012	1	Indicates whether the record has additional data. 0: Indicates that there is no additional data. 1: Indicates that fault record data can be read from 3x10020 to 3x10999 (see Note 3). 2: Indicates that maintenance record data can be read from registers 3x36 to 3x39.

Note 1 *The protection-event status information is the value of the DDB status word that contains the protection DDB that caused the event.*

Note 2 *Subtracting 3000 from the Event Origin value results in the MODBUS 3x memory-page register ID, subtracting one from this results in the MODBUS register address - see section 5.5.1.2. The resultant register address can be used in a function code 4 MODBUS query.*

Note 3 *The exact number of fault record registers depends on the individual product - see Relay Menu Database, P64x/EN GC.*

Table 10 - Event record extraction registers

If a fault record or maintenance record is directly selected using the manual mechanism, the data can be read from the fault or maintenance data register ranges specified in the *Maintenance record types* table. The event record data in registers 3x10003 to 3x10012 is not valid.

See the *Relay Menu Database document* for the record values for each event.

The general procedure for decoding an event record is to use the value of the **Event Type** field combined with the value of the **Event Index** field to uniquely identify the event. The exceptions to this are event types 4, 5, 7, 8, & 9.

Event types 4 **Relay Contact Output Events** and 5 **Opto-Isolated Status Input Events** only provide the value of the input or output status register (as indicated by the Event Origin value) when the event occurred. If event transition information for each input or output is required, it must be deduced by comparing the event value with the previous event value (for identically-typed events records).

Event type 7 **General Event** events are solely identified by their **Event Value**.

Event types 8 **Fault Record** and 9 **Maintenance Record** require additional registers to be read when the associated additional data is available (see Note). The Fault record registers in the range 3x10020 to 3x10999 (the exact number of registers depends on the individual product) are documented in the 3x register-map in the *Relay Menu Database document*. The two additional 32-bit maintenance record register-pairs consist of a maintenance record type (register pair 3x36/7) and a type-specific error code (register pair 3x38/9). The *Maintenance record types* table lists the different types of maintenance record available from the product.

Note	*As noted at the beginning of the Event Extraction section, it should not be assumed that the additional data is available for fault and maintenance record events.*

Maintenance record	Front panel text	Record type 3x00036
Power on test errors (non-fatal)		
Watchdog 1 failure (fast)	Fast W'Dog Error	0
Battery fail	Battery Failure	1
Battery-backed RAM failure	BBRAM Failure	2
Field voltage failure	Field Volt Fail	3
Ribbon bus check failure	Bus Reset Error	4
Watchdog 2 failure (slow)	Slow W'Dog Error	5
Continuous self-test errors		
SRAM bus failure	SRAM Failure Bus	6
SRAM cell failure	SRAM Failure Blk.	7
Flash EPROM checksum failure	FLASH Failure	8
Program code verify failure	Code Verify Fail	9
Battery-backed RAM failure	BBRAM Failure	10
Battery fail	Battery Failure	11
Field Voltage failure	Field Volt Fail	12
EEPROM failure	EEPROM Failure	13
Fatal software exception	Software Failure	14
Incorrect hardware configuration	H/W Verify Fail	15
Software exception (typically non-fatal)	Non Standard	16
Analog module failure	Ana. Sample Fail	17
Ethernet card error	NIC Soft Error	18

Table 11 - Maintenance record types

5.11.4 Event Record Deletion

It is possible to independently delete (“clear”) the stored event, fault, and maintenance record queues. This is done by writing a value of 1, 2, or 3 to register 4x401 (G6 data type), respectively.

Register 4x401 also provides an option to reset the product’s front panel indications, which has the same effect as pressing the front panel “Clear” key when viewing alarm indications using the front panel user interface. This is done by writing a value of 4 to register 4x401.

See also the *Disturbance Record Deletion* section for details about deleting disturbance records.

5.11.5 Legacy Event Record Support

Version 57 of P24x and Version 31 of P34x product introduced a new set of 3x registers for the presentation of the event and fault record data. For legacy compatibility, the original registers are supported and are described in this section. They should not be used for new installations and they are correspondingly described as previous MODBUS address in the 3x-register table in the *Relay Menu Database document*.

The *Correspondence of obsolete event record 3x registers with their counterparts* table provides a mapping between the obsolete event record 3x-registers and the registers used in the event record discussions in the previous sub-sections.

The obsolete fault record data between registers 3x113 and 3x199, and 3x490 and 3x499, now exists between registers 3x10020 and 3x10999. In comparison with the obsolete fault record data, the data between registers 3x10020 and 3x10999 is ordered slightly differently and it contains new data values. These new values are not available in the obsolete fault-record register sets.

The maintenance-record registers 3x36 to 3x39 remain unaffected by this evolution.

Description	Obsolete register	Length (registers)	Corresponds to register
Number of stored event records	3x00100	1	3x10100
Number of stored fault records	3x00101	1	3x10101
Number of stored maintenance records	3x00102	1	3x10102
Time Stamp	3x00103	4	3x10103
Event Type	3x00107	1	3x10107
Event Value	3x00108	2	3x10108
Event Origin	3x00110	1	3x10110
Event Index	3x00111	1	3x10111
Additional Data Present	3x00112	1	3x10112

Table 12 - Correspondence of obsolete event record 3x registers with their counterparts

5.12 Disturbance Record Extraction

The product provides facilities for both manual and automatic extraction of disturbance records. The two methods differ only in the mechanism for selecting a disturbance record; the method for extracting the data and the format of the data are identical.

Records extracted are presented in IEEE COMTRADE format. This involves extracting two files: an ASCII text configuration file, and a binary data file.

Each file is extracted by repeatedly reading a data-page until all of the file’s data has been transferred. The data-page is made up of 127 registers; providing a maximum of 254 bytes for each register block request.

5.12.1 Interface Registers

The following set of registers is presented to the master station to support the extraction of uncompressed disturbance records:

Register	Name	Description
3x00001	Status register	Provides the status of the product as bit flags: b0 Out of service b1 Minor self test failure b2 Event b3 Time synchronization b4 Disturbance b5 Fault b6 Trip b7 Alarm b8 to b15 Unused A '1' in bit "b4" indicates the presence of one or more disturbance records.
3x00800	Number of stored disturbances	Indicates the total number of disturbance records currently stored in the product, both extracted and unextracted.
3x00801	Unique identifier of the oldest disturbance record	Indicates the unique identifier value for the oldest disturbance record stored in the product. This is an integer value used in conjunction with the 'Number of stored disturbances' value to calculate a value for manually selecting records.
4x00250	Manual disturbance record selection register	This register is used to manually select disturbance records. The values written to this cell are an offset of the unique identifier value for the oldest record. The offset value, which ranges from 0 to the No of stored disturbances - 1, is added to the identifier of the oldest record to generate the identifier of the required record.
4x00400	Record selection command register	This register is used during the extraction process and has a number of commands. These are: b0 Select next event b1 Accept event b2 Select next disturbance record b3 Accept disturbance record b4 Select next page of disturbance data b5 Select data file
3x00930 to 3x00933	Record time stamp	These registers return the timestamp of the disturbance record.
3x00802	Number of registers in data page	This register informs the master station of the number of registers in the data page that are populated.
3x00803 to 3x00929	Data page registers	These 127 registers are used to transfer data from the product to the master station.
3x00934	Disturbance record status register	The disturbance record status register is used during the extraction process to indicate to the master station when data is ready for extraction. See next table.
4x00251	Data file format selection	This is used to select the required data file format. This is reserved for future use.

Table 13 - Disturbance record extraction registers

The Disturbance Record status register will report one of the following values:

State		Description
Idle		This will be the state reported when no record is selected; such as after power on or after a record has been marked as extracted.
Busy		The product is currently processing data.
Page ready		The data page has been populated and the master can now safely read the data.
Configuration complete		All of the configuration data has been read without error.
Record complete	4	All of the disturbance data has been extracted.
Disturbance overwritten	5	An error occurred during the extraction process where the disturbance being extracted was overwritten by a new record.
No unextracted disturbances	6	An attempt was made by the master station to automatically select the next oldest unextracted disturbance when all records have been extracted.
Not a valid disturbance	7	An attempt was made by the master station to manually select a record that did not exist in the product.
Command out of sequence	8	The master station issued a command to the product that was not expected during the extraction process.

Table 14 - Disturbance record status register (3x934) values

5.12.2 Extraction Procedure

The following procedure must be used to extract disturbance records from the product. The procedure is split into four sections:

1. Selection of a disturbance, either manually or automatically.
2. Extraction of the configuration file.
3. Extraction of the data file.
4. Accepting the extracted record (automatic extraction only).

5.12.2.1 Manual Extraction Procedure

The procedure used to extract a disturbance manually is shown in the following *Manual selection of a disturbance record* diagram. The manual method of extraction does not allow for the acceptance of disturbance records.

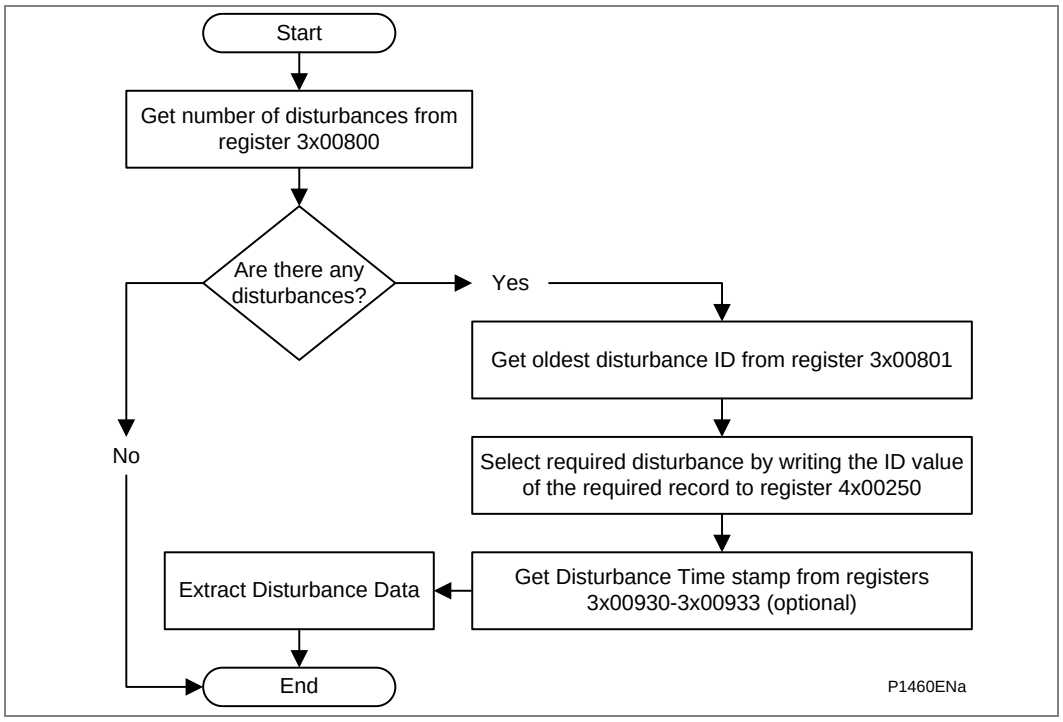


Figure 7 - Manual selection of a disturbance record

5.12.2.2 Automatic Extraction Procedure

There are two methods that can be used for automatically extracting disturbances.

- Option 1 is simpler and is better at extracting single disturbance records, i.e. when the disturbance recorder is polled regularly.
- Option 2, however, is more complex to implement but is more efficient at extracting large quantities of disturbance records. This may be useful when the disturbance recorder is polled only occasionally and hence may have many stored records.

5.12.2.3 Automatic Extraction Procedure - Option 1

There are two methods that can be used for automatically extracting disturbances. The procedure for the first method is shown in the *Automatic selection of a disturbance - option 1* diagram. This also shows the acceptance of the disturbance record once the extraction is complete.

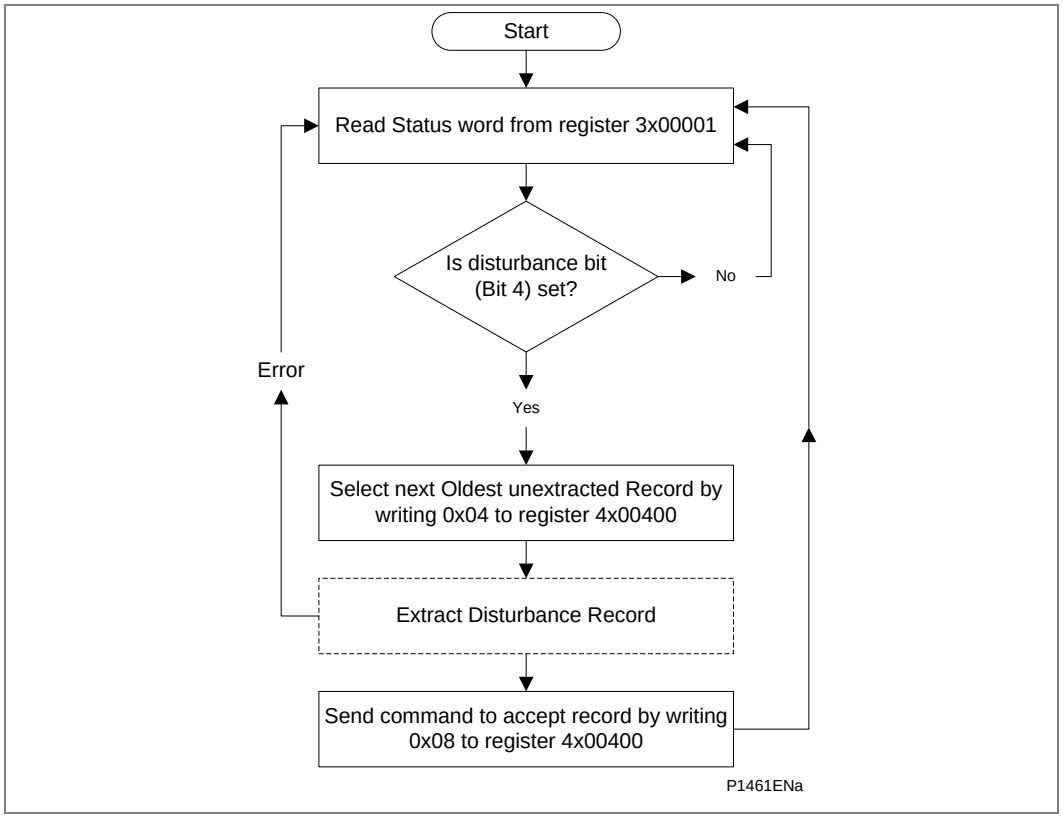


Figure 8 - Automatic selection of a disturbance - option 1

5.12.2.4 Automatic Extraction Procedure - Option 2

The second method that can be used for automatic extraction is shown in the *Automatic selection of a disturbance - option 2* diagram. This also shows the acceptance of the disturbance record once the extraction is complete.

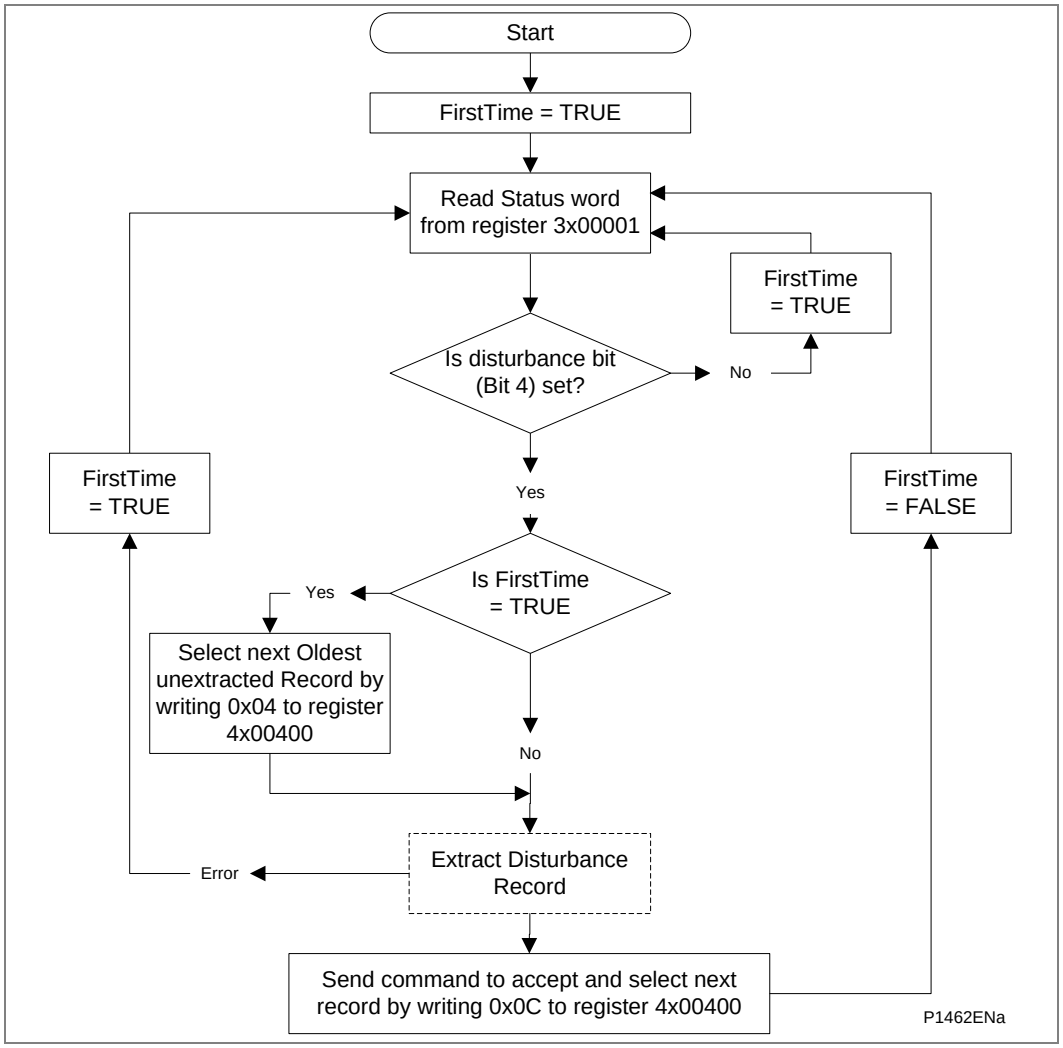


Figure 9 - Automatic selection of a disturbance - option 2

5.12.2.5 Extracting the Disturbance Data

Extraction of a selected disturbance record is a two-stage process. This involves first reading the configuration file, then the data file. The *Extracting the COMTRADE configuration file* diagram shows how the configuration file is read and *the Extracting the COMTRADE binary data file* diagram shows how the data file is extracted.

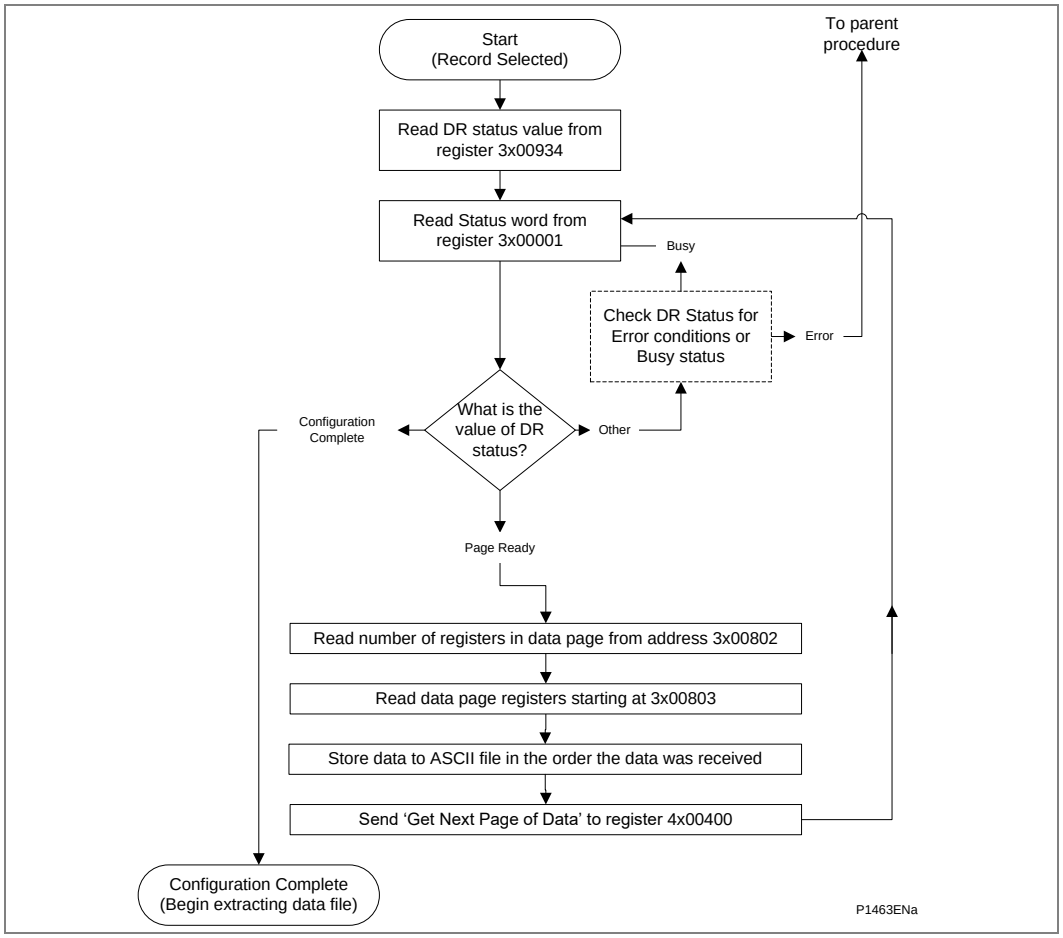


Figure 10 - Extracting the COMTRADE configuration file

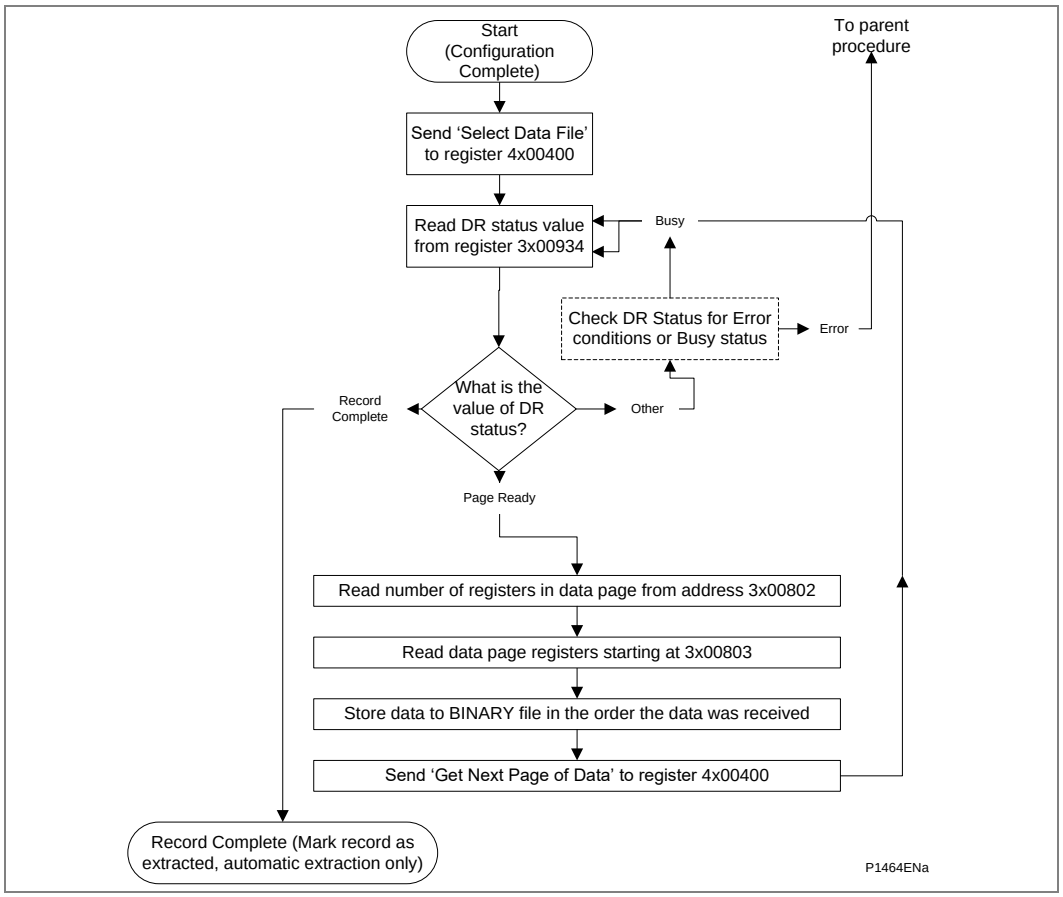


Figure 11 - Extracting the COMTRADE binary data file

During the extraction of a COMTRADE file, an error may occur that is reported in the disturbance record status register, 3x934. This can be caused by the product overwriting the record that is being extracted. It can also be caused by the master issuing a command that is not in the bounds of the extraction procedure.

5.12.3 Storage of Extracted Data

The extracted data needs to be written to two separate files. The first is the configuration file, which is in ASCII text format, and the second is the data file, which is in a binary format.

5.12.3.1 Storing the Configuration File

As the configuration data is extracted from the product, it should be stored to an ASCII text file with a '.cfg' file extension. Each register in the page is a G1 format 16-bit unsigned integer that is transmitted in big-endian byte order. The master must write the configuration file page-data to the file in ascending register order with each register's high order byte written before its low order byte, until all the pages have been processed.

5.12.3.2 Storing the Binary Data File

As the binary data is extracted from the product, it should be stored to a binary file with the same name as the configuration file, but with a '.dat' file extension instead of the '.cfg' extension. Each register in the page is a G1-format 16-bit unsigned integer that is transmitted in big-endian byte order. The master must write the page data to a file in ascending register order with each register's high order byte written before its low order byte until all the pages have been processed.

5.12.4 Disturbance Record Deletion

All of the disturbance records stored in the product can be deleted ("cleared") by writing 5 to the record control register 4x401 (G6 data type). See the *Event Record Deletion* section for details on event record deletion.

5.13 Setting Changes

The relay settings can be split into two categories:

- Control and support settings
- Disturbance record settings and protection setting groups

Changes to settings in the control and support area are executed immediately. Changes to the protection setting groups or the disturbance recorder settings are stored in a temporary 'scratchpad' area and must be confirmed before they are implemented. All the product settings are 4xxxx page registers; see the *Relay Menu Database document*. The following points should be noted when changing settings:

- Settings implemented using multiple registers must be written to using a multi-register write operation. The product does not support write access to sub-parts of multi-register data types.
- The first address for a multi-register write must be a valid address. If there are unmapped addresses in the range that is written to, the data associated with these addresses are discarded.
- If a write operation is performed with values that are out of range, an "illegal data" response code is produced. Valid setting values in the same write operation are executed.
- If a write operation is performed attempting to change registers that require a higher level of password access than is currently enabled, all setting changes in the write operation are discarded.

5.13.1 Password Protection

Access to the product's settings is subject to authentication of a user who has the correct role. The authentication needed to change a setting is shown in the 4x register-map table in the *Relay Menu Database document, P64x/EN MD*.

5.13.2 Control and Support Settings

Control and support settings are committed immediately when a value is written to such a register. The MODBUS registers in this category are:

- 4x00000-4x00599
- 4x00700-4x00999
- 4x02049-4x02052
- 4x10000-4x10999

5.13.2.1 Time Synchronization

The value of the product's real time clock can be set by writing the desired time (see the *Date and Time Format (Data Type G12)* section) to registers 4x02049 through 4x02052. These registers are standard to Schneider Electric MiCOM products, which makes it easier to broadcast a time synchronization packet, being a block write to the time setting registers sent to slave address zero.

When the product's time has been set using these registers, the Time Synchronized flag in the MODBUS Status Register (3x1: type G26) is set. The product automatically clears this flag if more than five minutes has elapsed since these registers were last written to.

A "Time synchronization" event is logged if the new time value is more than two seconds different to the current value.

5.13.3 Disturbance Recorder Configuration Settings

Disturbance recorder configuration-settings are written to a scratchpad memory area. A confirmation procedure is required to commit the contents of the scratchpad to the disturbance recorder's set-up, which ensures that the recorders configuration is consistent at all times. The contents of the scratchpad memory can be discarded with the abort procedure. The scratchpad confirmation and abort procedures are described in the *Scratchpad Management* section.

The disturbance recorder configuration registers are in the range:

- 4x00600-4x00699

5.13.4 Protection Settings

Protection configuration-settings are written to a scratchpad memory area. A confirmation procedure is required to commit the contents of the scratchpad to the product's protection functions, which ensures that their configuration is consistent at all times. The contents of the scratchpad memory can be discarded with the abort procedure. The scratchpad confirmation and abort procedures are described in the *Scratchpad Management* section.

The product supports four groups of protection settings. One protection-group is active and the other three are either dormant or disabled. The active protection-group can be selected by writing to register 4x00404. An illegal data response is returned if an attempt is made to set the active group to one that has been disabled.

The MODBUS registers for each of the four groups are repeated in the following ranges:

- Group 1 4x01000-4x02999, (see note) 4x11000-4x12999
- Group 2 4x03000-4x04999, 4x13000-4x14999
- Group 3 4x05000-4x06999, 4x15000-4x16999
- Group 4 4x07000-4x08999, 4x17000-4x18999

Note	*Registers 4x02049 to 4x02052 are not part of protection setting group #1 so they do not repeat in any of the other protection setting groups. These registers are for time synchronization purposes and are standard for most Schneider Electric products. See the Time Synchronization section.*

5.13.5 Scratchpad Management

Register 4x00405 can be used to either confirm or abort the setting changes in the scratchpad area. In addition to the basic editing of the protection setting groups, these functions are provided:

- Default values can be restored to a setting group or to all of the product settings by writing to register 4x00402.
- It is possible to copy the contents of one setting group to another by writing the source group to register 4x00406 and the target group to 4x00407.
- The setting changes performed by either of these two operations are made to the scratchpad area. These changes must be confirmed by writing to register 4x00405.

5.14 Register Data Types

The product maps one or more MODBUS registers to data-typed information contained in an internal database. These data-types are referred to as G-Types since they have a 'G' prefixed identifier. The *Relay Menu Database document* gives a complete definition of the all of the G-Types used in the product.

Generally the data types are transmitted in high byte to low byte order, also known as "Big Endian format". This may require the MODBUS master to reorder the received bytes into a format that complies with its byte order and register order (for multi-register G-Types) conventions. Most MODBUS masters provide byte-swap and register-swap device (or data point) configuration to cope with the wide range of implementations.

The product's data types cannot be broken into smaller parts. Therefore multi-register data types cannot be read from or written to on an individual register basis. All of the registers for a multi-register data-typed item must be read from or written to with a single block read or write command. The following subsections provide some additional notes for a few of the more complex G-Types.

5.15 Numeric Setting (Data Types G2 & G35)

Numeric settings are integer representations of real (non-integer) values. The register value is the number of setting increments (or steps) that the real value is away from the real minimum value. This is expressed by this formula:

$S_{real} = S_{min.} + (S_{inc.} \times S_{numeric})$

Where:

S_{real} Setting real value

$S_{min.}$ Setting real minimum value

$S_{inc.}$ Setting real increment (step) value

$S_{numeric}$ Setting numeric (register) value

For example, a setting with a real value setting range of 0.01 to 10 in steps of 0.01 would have the following numeric setting values:

Real value (S_{real})	Numeric value ($S_{numeric}$)
0.01	0
0.02	1
1.00	99

Table 15 - Real and numeric values

The G2 numeric data type uses 1 register as an unsigned 16-bit integer, whereas the G35 numeric data type uses 2 registers as an unsigned 32-bit integer. The G2 data type therefore provides a maximum setting range of $2^{16} \times S_{inc}$. Similarly the G35 data type provides a maximum setting range of $2^{32} \times S_{inc}$.

5.16 Date and Time Format (Data Type G12)

The date-time data type G12 allows real date and time information to be conveyed down to a resolution of 1 ms. The data-type is used for record time-stamps and for time synchronization (see the *Time Synchronization* section).

The structure of the data type is shown in the following table and complies with the IEC60870-5-4 Binary Time 2a format.

Byte	Bit Position							
	7	6	5	4	3	2	1	0
1	m^7	m^6	m^5	m^4	m^3	m^2	m^1	m^0
2	m^{15}	m^{14}	m^{13}	m^{12}	m^{11}	m^{10}	m^9	m^8
3	IV	R	I^5	I^4	I^3	I^2	I^1	I^0
4	SU	R	R	H^4	H^3	H^2	H^1	H^0
5	W^2	W^1	W^0	D^4	D^3	D^2	D^1	D^0
6	R	R	R	R	M^3	M^2	M^1	M^0
7	R	Y^6	Y^5	Y^4	Y^3	Y^2	Y^1	Y^0

Where:					
m	=	0…59,999ms	Y	=	0…99 Years (year of century)
I	=	0…59 minutes	R	=	Reserved bit = 0
H	=	0…23 Hours	SU	=	Summertime:
W	=	1…7 Day of week;			0=standard time,
		Monday to Sunday,			1=summer time
		0 for not calculated	IV	=	Invalid value:
D	=	1…31 Day of Month			0=valid,
M	=	1…12 Month of year;			1=invalid
		January to December	range	=	0ms…99 years

Table 16 - G12 date & time data type structure

The seven bytes of the structure are packed into four 16-bit registers. Two packing formats are provided: standard and reverse. The prevailing format is selected by the G238 setting in the **Date and Time** menu column or by register 4x306 (Modbus IEC Time).

The standard packing format is the default and complies with the IEC60870-5-4 requirement that byte 1 is transmitted first. This is followed by byte 2 through to byte 7, followed by a null (zero) byte to make eight bytes in total. Since register data is usually transmitted in big-endian format (high-order byte followed by low-order byte), byte 1 is in the high-order byte position followed by byte 2 in the low-order position for the first register. The last register contains just byte 7 in the high-order position and the low-order byte has a value of zero.

The reverse packing format is the exact byte transmission order reverse of the standard format. The null (zero) byte is sent as the high-order byte of the first register and byte 7 as the register's low-order byte. The second register's high-order byte contains byte 6 and byte 5 in its low order byte.

Both packing formats are fully documented in the *Relay Menu Database document* for the G12 type.

The principal application of the reverse format is for date-time packet format consistency when a mixture of MiCOM Px20, Px30, and Px40 series products are being used. This is especially true when there is a requirement for broadcast time synchronization with a mixture of such MiCOM products.

The data type provides only the value for the year of the century. The century must be deduced. The century could be imposed as 20 for applications not dealing with dates stored in this format from the previous (20th) century. Alternatively, the century can be calculated as the one that produces the nearest time value to the current date. For example: 30-12-99 is 30-12-1999 when received in 1999 & 2000, but is 30-12-2099 when received in 2050. This technique allows 2-digit years to be accurately converted to 4 digits in a ±50 year window around the current datum.

The invalid bit has two applications:

- It can indicate that the date-time information is considered inaccurate, but is the best information available.
- Date-time information is not available.

The summertime bit is used to indicate that summertime (day light saving) is being used and, more importantly, to resolve the alias and time discontinuity which occurs when summertime starts and ends. This is important for the correct time correlation of time stamped records.

Note	*The value of the summertime bit does not affect the time displayed by the product.*

The day of the week field is optional and if not calculated is set to zero.

This data type (and therefore the product) does not cater for time zones so the end user must determine the time zone used by the product. UTC (universal co-ordinated time) is commonly used and avoids the complications of daylight saving timestamps.

5.17 Power and Energy Measurement Data Formats (G29 & G125)

The power and energy measurements are available in two data formats, G29 integer format and G125 IEEE754 floating point format. The G125 format is preferred over the older G29 format.

For historical reasons the registers listed in the main part of the "**Measurements 2**" column of the *Menu Database* are of the G29 format. The floating point, G125, versions appear at the end of the column.

5.17.1 Data Type G29

Data type G29 consists of three registers. The first register is the per-unit power or energy measurement and is of type G28, which is a signed 16-bit quantity. The second and third registers contain a multiplier to convert the per-unit value to a real value.

The multiplier is of type G27, which is an unsigned 32-bit quantity. Therefore the overall value conveyed by the G29 data type must be calculated as G29 = G28 × G27.

The product calculates the G28 per unit power or energy value as

G28 = ((measured secondary quantity) / (CT secondary) × (110 V / (VT secondary)).

Since data type G28 is a signed 16-bit integer, its dynamic range is constrained to ±32768. This limitation should be borne in mind for the energy measurements, as the G29 value saturates a long time before the equivalent G125.

The associated G27 multiplier is calculated as

G27 = (CT primary) × (VT primary / 110 V)
when primary value measurements are selected,
and as
G27 = (CT secondary) × (VT secondary / 110 V)
when secondary value measurements are selected.

Due to the required truncations from floating point values to integer values in the calculations of the G29 component parts and its limited dynamic range, the use of the G29 values is only recommended when the MODBUS master cannot deal with the G125 IEEE754 floating point equivalents.

Note	*The G29 values must be read in whole multiples of three registers. It is not possible to read the G28 and G27 parts with separate read commands.*

Example:

For A-Phase Power (Watts) (registers 3x00300 - 3x00302) for a 110 V nominal, In = 1 A, VT ratio = 110 V:110 V and CT ratio = 1 A : 1 A.

Applying A-phase 1A @ 63.51V

A-phase Watts = ((63.51 V × 1 A) / In=1 A) × (110/Vn=110 V) = 63.51 Watts

The G28 part of the value is the truncated per unit quantity, which is equal to 64 (40h).

The multiplier is derived from the VT and CT ratios set in the product, with the equation ((CT Primary) × (VT Primary) / 110 V)). Therefore the G27 part of the value equals 1 and the overall value of the G29 register set is 64×1 = 64 W.

The registers would contain:

3x00300 - 0040h
3x00301 - 0000h
3x00302 - 0001h

Using the previous example with a VT ratio = 110,000 V:110 V and CT ratio = 10,000 A : 1 A the G27 multiplier would be 10,000 A × 110,000 V / 110 = 10,000,000. The overall value of the G29 register set is 64 × 10,000,000 = 640 MW. (Note that there is an actual error of 49 MW in this calculation due to loss of resolution).

The registers would contain:

3x00300 - 0040h
3x00301 - 0098h
3x00302 - 9680h

5.17.2 Data Type G125

Data type G125 is a short float IEEE754 floating point format, which occupies 32 bits in two consecutive registers. The most significant 16 bits of the format are in the first (low order) register and the least significant 16 bits in the second register.

The value of the G125 measurement is as accurate as the product's ability to resolve the measurement after it has applied the secondary or primary scaling factors as required. It does not suffer from the truncation errors or dynamic range limitations associated with the G29 data format.

6 IEC60870-5-103 INTERFACE

The IEC60870-5-103 interface is a master/slave interface with the relay as the slave device. The relay conforms to compatibility level 2; compatibility level 3 is not supported.

These IEC60870-5-103 facilities are supported by this interface:

- Initialization (Reset)
- Time Synchronization
- Event Record Extraction
- General Interrogation
- Cyclic Measurements
- General Commands
- Disturbance Record Extraction
- Private Codes

6.1 Physical Connection and Link Layer

Two connection options are available for IEC60870-5-103, either the rear EIA(RS)-485 port or an optional rear fiber optic port. If the fiber optic port is fitted, the active port can be selected using the front panel menu or the front Courier port. However the selection is only effective following the next relay power up.

For either of the two connection modes, both the relay address and baud rate can be selected using the front panel menu or the front Courier port. Following a change to either of these two settings a reset command is required to re-establish communications, see the description of the reset command in the *Initialization* section.

6.2 Initialization

Whenever the relay has been powered up, or if the communication parameters have been changed, a reset command is required to initialize the communications. The relay responds to either of the two reset commands (Reset CU or Reset FCB). However, the Reset CU clears any unsent messages in the relay's transmit buffer.

The relay responds to the reset command with an identification message ASDU 5. The Cause Of Transmission (COT) of this response is either Reset CU or Reset FCB depending on the nature of the reset command. For information on the content of ASDU 5 see *section IEC60870-5-103 in the Relay Menu Database document*.

In addition to the ASDU 5 identification message, if the relay has been powered up it also produces a power-up event.

6.3 Time Synchronization

The relay time and date can be set using the time synchronization feature of the IEC60870-5-103 protocol. The relay corrects for the transmission delay as specified in IEC60870-5-103. If the time synchronization message is sent as a send / confirm message, the relay responds with a confirm. Whether the time-synchronization message is sent as a send / confirm or a broadcast (send / no reply) message, a time synchronization Class 1 event is generated.

If the relay clock is synchronised using the IRIG-B input, it is not possible to set the relay time using the IEC60870-5-103 interface. If the time is set using the interface, the relay creates an event using the current date and time from the internal clock, which is synchronised to IRIG-B.

6.4 Spontaneous Events

Events are categorized using the following information:

- Function Type
- Information Number

The IEC60870-5-103 profile in the *Relay Menu Database document*, contains a complete listing of all events produced by the relay.

6.5 General Interrogation

The General Interrogation (GI) request can be used to read the status of the relay, the function numbers, and information numbers that are returned during the GI cycle. See the IEC60870-5-103 profile in the *Relay Menu Database document*.

6.6 Cyclic Measurements

The relay produces measured values using ASDU 9 cyclically. This can be read from the relay using a Class 2 poll (note ADSU 3 is not used). The rate at which the relay produces new measured values can be controlled using the Measurement Period setting. This setting can be edited from the front panel menu or the front Courier port and is active immediately following a change.

The measurands transmitted by the relay are sent as a proportion of 2.4 times the rated value of the analog value.

6.7 Commands

A list of the supported commands is contained in the *Relay Menu Database document*. The relay responds to other commands with an ASDU 1, with a Cause of Transmission (COT) indicating ‘negative acknowledgement’.

6.8 Test Mode

The **Test Mode** menu cell (in the **COMMISSION TESTS** column) is used to allow secondary injection testing to be performed on the relay.

To select test mode set the Test Mode menu cell to '**Test Mode**'. It causes an alarm condition to be recorded, the yellow ALARM LED to light and an alarm message '**Test Mode Alm**' to be generated.

Test Mode freezes any information stored in the **CB CONDITION** column and (in IEC60870-5-103 builds) changes the Cause Of Transmission (COT) to Test Mode. For relays supporting IEC 61850 Edition 2, the test bit for data quality attribute shall set to TRUE, and the Logical Device Mode will set to test.

Test mode can also be enabled by energizing an opto mapped to the **Test Mode** signal.

To enable testing of output contacts set the **Test Mode** cell to **Contacts Blocked**. It causes an alarm condition to be recorded, the yellow ALARM LED to light and an alarm message '**Contacts Blk Alm**' to be generated.

In **Contact Blocked** mode, the protection function still works but the contacts will not operate. Also the **test pattern** and contact test functions are visible, which can be used to manually operate the output contacts. For relays supporting IEC 61850 Edition 2, the test bit for data quality attribute shall set to TRUE, and the Logical Device Mode will set to test/blocked.

Contacts Blocked can also be enabled by energizing an opto mapped to the **Contacts Blocked** signal.

Once testing is complete the cell must be set back to '**Disabled**' to restore the relay back to service.

WARNING **If you use or enable Test Mode, you must disable Test Mode before putting the relay back into active service. IT IS POTENTIALLY EXTREMELY UNSAFE TO ATTEMPT TO USE ANY RELAY WHICH IS STILL IN TEST MODE IN ACTIVE SERVICE.**

6.9 Disturbance Records

The disturbance records are stored in uncompressed format and can be extracted using the standard mechanisms described in IEC60870-5-103.

Note	*IEC60870-5-103 only supports up to 8 records.*

6.10 Blocking of Monitor Direction

The relay supports a facility to block messages in the Monitor direction and in the Command direction. Messages can be blocked in the Monitor and Command directions using the menu commands, Communications - CS103 Blocking - Disabled / Monitor Blocking / Command Blocking or DDB signals Monitor Blocked and Command Blocked.

7 DNP3.0 INTERFACE

7.1 DNP3.0 Protocol

The DNP3.0 protocol is defined and administered by the DNP Users Group. For information on the user group, DNP3.0 in general and the protocol specifications, see www.dnp.org

The descriptions given there are intended to accompany the device profile document that is included in the *Relay Menu Database document.* The DNP3.0 protocol is not described here, please refer to the documentation available from the user group. The device profile document specifies the full details of the DNP3.0 implementation for the relay. This is the standard format DNP3.0 document that specifies which objects; variations and qualifiers are supported. The device profile document also specifies what data is available from the relay using DNP3.0. The relay operates as a DNP3.0 slave and supports subset level 2 of the protocol, plus some of the features from level 3.

DNP3.0 communication uses the EIA(RS)-485 communication port at the rear of the relay. The data format is 1 start bit, 8 data bits, an optional parity bit and 1 stop bit. Parity is configurable (see menu settings below).

7.2 DNP3.0 Menu Setting

The following settings are in the DNP3.0 menu in the ***Communications*** column.

Settings	Range	Description
Remote Address	0 - 65519	DNP3.0 address of relay (decimal)
Baud Rate	1200, 2400, 4800, 9600, 19200, 38400	Selectable baud rate for DNP3.0 serial communication
Parity	None, Odd, Even	Parity setting
DNP Time Sync	Disabled, Enabled	If set to 'Enabled' the DNP3.0 master station can be used to synchronize the time on the IED. If set to 'Disabled' either the internet free running clock, or IRIG-B input are used.
Meas Scaling	Primary, Secondary or Normalised	Setting to report analog values in terms of primary, secondary or normalized (with respect to the CT/VT ratio setting) values.
Message Gap (ms)	0-50	DNP3.0 versions only. This setting allows the master station to have an interframe gap.
DNP Need Time	1 - 30 mins	The length of time waited before requesting another time sync from the master.
DNP App Fragment	100 - 2048 bytes	The maximum message length (application fragment size) transmitted by the relay.
DNP App Timeout	1 - 120 s	The length of time waited after sending a message fragment and waiting for a confirmation from the master.
DNP SBO Timeout	1 - 10 s	The length of time waited after receiving a select command and waiting for an operate confirmation from the master.
DNP Link Timeout	0 - 120 s	The length of time the relay waits for a Data Link Confirm from the master. A value of 0 means data link support disabled and 1 to 120 seconds is the timeout setting.

Table 17 - DNP3.0 Menu Settings

7.3 Object 1 Binary Inputs

Object 1, binary inputs, contains information describing the state of signals in the relay, which mostly form part of the Digital Data Bus (DDB). In general, these include the state of the output contacts and input optos, alarm signals and protection start and trip signals. The 'DDB number' column in the device profile document provides the DDB numbers for the DNP3.0 point data. These can be used to cross-reference to the DDB definition list. See the *Relay Menu Database document*. The binary input points can also be read as change events using object 2 and object 60 for class 1-3 event data.

7.4 Object 10 Binary Outputs

Object 10, binary outputs, contains commands that can be operated using DNP3.0. Therefore the points accept commands of type pulse on [null, trip, close] and latch on/off as detailed in the device profile in the *Relay Menu Database document* and execute the command once for either command. The other fields are ignored (queue, clear, trip/close, in time and off time).

There is an additional image of the control inputs. Described as alias control inputs, they reflect the state of the control input, but with a dynamic nature.

- If the Control Input DDB signal is already SET and a new DNP SET command is sent to the Control Input, the Control Input DDB signal goes momentarily to RESET and then back to SET.
- If the Control Input DDB signal is already RESET and a new DNP RESET command is sent to the Control Input, the Control Input DDB signal goes momentarily to SET and then back to RESET.

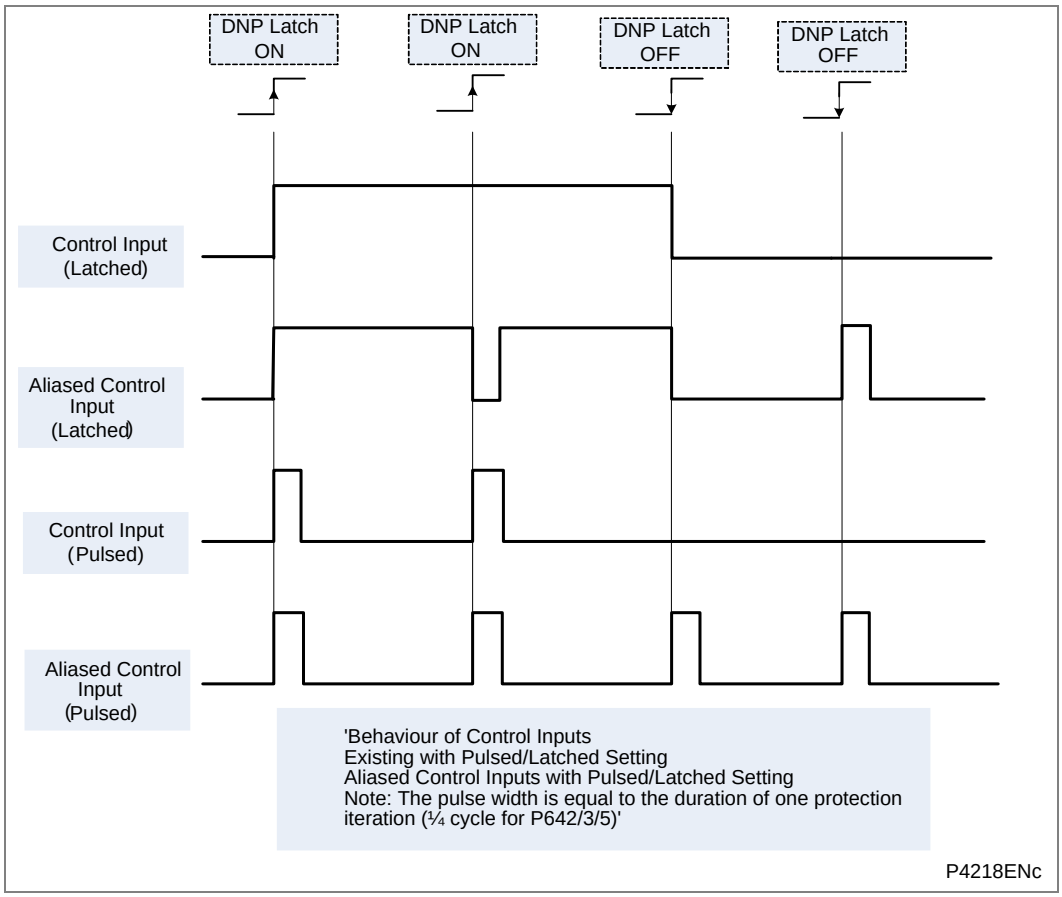


Figure 12 - Behavior when control input is set to pulsed or latched

Many of the relay's functions are configurable so some of the object 10 commands described in the following sections may not be available. A read from object 10 reports the point as off-line and an operate command to object 12 generates an error response.

Examples of object 10 points that maybe reported as off-line are:

- Activate setting groups — Ensure setting groups are enabled
- CB trip/close — Ensure remote CB control is enabled
- Reset NPS thermal — Ensure NPS thermal protection is enabled
- Reset thermal O/L — Ensure thermal overload protection is enabled
- Reset RTD flags — Ensure RTD Inputs is enabled
- Control inputs — Ensure control inputs are enabled

7.5 Object 20 Binary Counters

Object 20, binary counters, contains cumulative counters and measurements. The binary counters can be read as their present 'running' value from object 20, or as a 'frozen' value from object 21. The running counters of object 20 accept the read, freeze and clear functions. The freeze function takes the current value of the object 20 running counter and stores it in the corresponding object 21 frozen counter. The freeze and clear function resets the object 20 running counter to zero after freezing its value.

Binary counter and frozen counter change event values are available for reporting from object 22 and object 23 respectively. Counter change events (object 22) only report the most recent change, so the maximum number of events supported is the same as the total number of counters. Frozen counter change events (object 23) are generated whenever a freeze operation is performed and a change has occurred since the previous freeze command. The frozen counter event queues store the points for up to two freeze operations.

7.6 Object 30 Analog Input

Object 30, analog inputs, contains information from the relay's measurements columns in the menu. All Object 30 points can be reported as 16 or 32-bit integer values with flag, 16 or 32-bit integer values without flag, as well as short floating point values.

Analogue values can be reported to the master station as primary, secondary or normalized values (which takes into account the relay's CT and VT ratios) and this is settable in the DNP3.0 Communications Column in the relay. Corresponding deadband settings can be displayed in terms of a primary, secondary or normalized value. Deadband point values can be reported and written using Object 34 variations.

The deadband is the setting used to determine whether a change event should be generated for each point. The change events can be read using Object 32 or Object 60. These events are generated for any point which has a value changed by more than the deadband setting since the last time the data value was reported.

Any analog measurement that is unavailable when it is read is reported as offline. For example, the frequency when the current and voltage frequency is outside the tracking range of the relay or the thermal state when the thermal protection is disabled in the configuration column. All Object 30 points are reported as secondary values in DNP3.0 (with respect to CT and VT ratios).

Beside the measurements described above, the latest fault record can also be retrieved over DNP3.0. The fault data defined in Object 30 table are:

- Fault voltages, Fault currents and Fault Location
- Operating time of relay and Operating time of breaker
- Fault time, Fault data, etc...

The following fault data can be mapped in DNP3.0 protocol in serial and Ethernet connections:

- Fault voltages
- Fault currents
- Fault location
- Operating time of relay
- Operating time of breaker
- Fault time
- Fault date

The latest fault records only will be retrieved over DNP3.0.

7.7 Object 40 Analog Output

The conversion to fixed-point format requires the use of a scaling factor, which is configurable for the various types of data within the relay such as current, voltage, and phase angle. All Object 40 points report the integer scaling values and Object 41 is available to configure integer scaling quantities.

7.8 DNP3.0 Configuration using Easergy Studio

DNP3.0 over Ethernet includes support for unsolicited responses. For the Unsolicited Responses configuration of DNP over Ethernet, please refer to this table:

Setting Name	Explanation
unsolAllowed	Determines whether unsolicited responses are allowed. If unsolAllowed is set to disabled, no unsolicited responses will be generated. Requests to enable or disable unsolicited responses will fail and the master station will reply indicating bad function information. If it is configured to allow unsolicited mode (enabled), the relay will be able to send event data in an unsolicited response after it receives a request from the master station containing function code ENABLE_UNSOLICITED(0x14) that enables some or all points to initiate unsolicited responses.
unsolMaxRetries	Specify the maximum number of unsolicited retries before changing to the 'offline' retry period (30 seconds).
unsolRetryDelay	Specifies the time, in seconds, to delay after an unsolicited confirm timeout before retrying the unsolicited response.
unsolClass1MaxDelay	If unsolicited responses are enabled, unsolClassXMaxDelay specifies the maximum amount of time in seconds after an event in the corresponding class is received before an unsolicited response will be generated. A configured value of 0 indicates that responses are not delayed.
unsolClass2MaxDelay	
unsolClass3MaxDelay	
unsolClass1MaxEvents	If unsolicited responses are enabled, unsolClassXMaxEvents specifies the maximum number of events in the corresponding class to be allowed before an unsolicited response will be generated.
unsolClass2MaxEvents	
unsolClass3MaxEvents	

Important	***At most 8 clients are supported to connect to device at the same time in DNP3.0 over Ethernet protocol.***

7.8.1 DNP3.0 over Ethernet runs concurrently with IEC61850

DNP3.0 over Ethernet can run concurrently with IEC61850 if DNP3.0 over Ethernet plus IEC61850 option is chosen. Below table describes the different cases of the usage of DNP3.0 over Ethernet service and IEC61850 service. IEC61850 service will always run under this situation, but DNPoE service only runs when certain requirements are met.

Board Type	Dual or PRP/HSR	Configuration file	Interface 1		Interface 2		Invalid DNPoE IP Alarm
			IP address	DNP3oE	IP address	DNP3oE	
Q or R	Doesn't matter	Default IEC61850 configuration No DNP setting or IP_DNP is 0.0.0.0	DEF_IP_1	Disabled	DEF_IP_2	Disabled	No
	Dual	Default IEC61850 configuration	IP_DNP	Run	DEF_IP_2	N/A	No
	PRP/HSR	Customized DNP setting with valid IP_DNP	DEF_IP_1	N/A	IP_DNP	Run	No
	Doesn't matter	Customized IEC61850 configuration No DNPoE setting or IP_DNP is 0.0.0.0	IP_1	Disabled	IP_2	Disabled	No
	Doesn't matter	Customized IEC61850 configuration Customized DNPoE setting where IP_DNP = IP_1	IP_1	Run	IP_2	N/A	No
	Doesn't matter	Customized IEC61850 configuration Customized DNPoE setting where IP_DNP = IP_2	IP_1	N/A	IP_2	Run	No
	Doesn't matter	Customized IEC61850 configuration Customized DNPoE setting where IP_DNP ≠ IP_1 and IP_DNP ≠ IP_2	IP_1	Disabled	IP_2	Disabled	Yes
S	N/A	Default IEC61850 configuration No DNPoE setting or IP_DNP is 0.0.0.0	DEF_IP_1	Disabled	N/A	N/A	No
	N/A	Default IEC61850 configuration Customized DNPoE setting with valid IP_DNP	IP_DNP	Run	N/A	N/A	No
	N/A	Customized IEC61850 configuration No DNPoE setting or IP_DNP is 0.0.0.0	IP_1	Disabled	N/A	N/A	No
	N/A	Customized IEC61850 configuration Customized DNPoE setting where IP_DNP = IP_1	IP_1	Run	N/A	N/A	No
	N/A	Customized IEC61850 configuration Customized DNPoE setting where IP_DNP ≠ IP_1	IP_1	Disabled	N/A	N/A	Yes

Note *For detailed information about different interfaces please refer to the **Dual IP in MiCOM** section in the Dual Redundant Ethernet Board (DREB) chapter.*

Table 18 – Protocol running options for different board types

For these IP abbreviations please refer to this table:

Abbreviation	Description
DEF_IP_1	Default IP of interface 1 with default IEC61850 configuration
DEF_IP_2	Default IP of interface 2 with default IEC61850 configuration
IP_1	IP of interface 1 configured in a IEC61850 configuration file
IP_2	IP of interface 2 configured in a IEC61850 configuration file
IP_DNP	IP configured in DNP over Ethernet setting

Table 19 – Abbreviations of Different IP

Note *Running DNP3.0 serial and DNP3.0 over Ethernet concurrently is not recommended.*

8 IEC 61850 ETHERNET INTERFACE

8.1 Introduction

IEC 61850 is the international standard for Ethernet-based communication in substations. It enables integration of all protection, control, measurement and monitoring functions in a substation, and provides the means for interlocking and inter-tripping. It combines the convenience of Ethernet with the security which is essential in substations today.

The MiCOM protection relays can integrate with the PACiS substation control systems, to complete Schneider Electric's offer of a full IEC 61850 solution for the substation. The majority of MiCOM Px3x and Px4x relay types can be supplied with Ethernet, in addition to traditional serial protocols. Relays which have already been delivered with UCA2.0 on Ethernet can be easily upgraded to IEC 61850.

8.2 What is IEC 61850?

IEC 61850 is a 14-part international standard, which defines a communication architecture for substations. It is more than just a protocol and provides:

- Standardized models for IEDs and other equipment in the substation
- Standardized communication services (the methods used to access and exchange data)
- Standardized formats for configuration files
- Peer-to-peer (for example, relay to relay) communication

The standard includes mapping of data onto Ethernet. Using Ethernet in the substation offers many advantages, most significantly including:

- High-speed data rates (currently 100 Mbits/s, rather than tens of kbits/s or less used by most serial protocols)
- Multiple masters (called “clients”)
- Ethernet is an open standard in every-day use

Schneider Electric has been involved in the Working Groups which formed the standard, building on experience gained with UCA2.0, the predecessor of IEC 61850.

8.2.1 Interoperability

A major benefit of IEC 61850 is interoperability. IEC 61850 standardizes the data model of substation IEDs which simplifies integration of different vendors’ products. Data is accessed in the same way in all IEDs, regardless of the vendor, even though the protection algorithms of different vendors’ relays may be different.

IEC 61850-compliant devices are not interchangeable, you cannot replace one device with another (although they are interoperable). However, the terminology is predefined and anyone with knowledge of IEC 61850 can quickly integrate a new device without mapping all of the new data. IEC 61850 improves substation communications and interoperability at a lower cost to the end user.

8.2.2 The Data Model

To ease understanding, the data model of any IEC 61850 IED can be viewed as a hierarchy of information. The categories and naming of this information is standardized in the IEC 61850 specification.

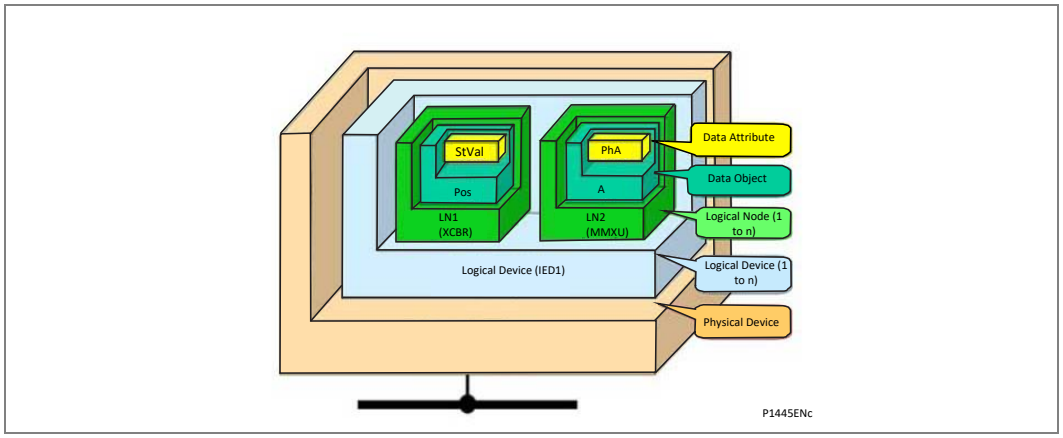


Figure 13 - Data model layers in IEC 61850

The levels of this hierarchy can be described as follows:

- Physical Device — Identifies the actual IED in a system. Typically the device's name or IP address can be used (for example **Feeder_1** or **10.0.0.2**).
- Logical Device — Identifies groups of related Logical Nodes inthe Physical Device. For the MiCOM relays, five Logical Devices exist: **Control, Measurements, Protection, Records, System**.
- Wrapper/Logical Node Instance — Identifies the major functional areas in the IEC 61850 data model. Either 3 or 6 characters are used as a prefix to define the functional group (wrapper) while the actual functionality is identified by a 4 character Logical Node name, suffixed by an instance number. For example, XCBR1 (circuit breaker), MMXU1 (measurements), FrqPTOF2 (overfrequency protection, stage 2).
- Data Object — This next layer is used to identify the type of data presented. For example, **Pos** (position) of Logical Node type **XCBR**.
- Data Attribute — This is the actual data (such as measurement value, status, and description). For example, **stVal** (status value) indicates the actual position of the circuit breaker for Data Object type **Pos** of Logical Node type **XCBR**.

8.3 IEC 61850 in MiCOM Relays

IEC 61850 is implemented in MiCOM relays by use of a separate Ethernet card. This card manages the majority of the IEC 61850 implementation and data transfer to avoid any impact on the performance of the protection.

To communicate with an IEC 61850 IED on Ethernet, it is necessary only to know its IP address. This can then be configured into either:

- An IEC 61850 **client** (or **master**), for example a PACiS computer (MiCOM C264) or HMI, or
- An **MMS browser**, with which the full data model can be retrieved from the IED, without any prior knowledge

8.3.1 Capability

The IEC 61850 interface provides these capabilities:

- Read access to measurements

  All measurands are presented using the measurement Logical Nodes, in the **Measurements** Logical Device. Reported measurement values are refreshed by the relay once per second, in line with the relay user interface.

The following fault data have been mapped in LN RFLO1 of LD Records of IEC61850 data model:

- Fault voltages, Fault currents and Fault location
- Operating time of relay and Operating time of breaker
- Fault time, Fault date, etc…

Only the latest fault record can be retrieved over IEC61850.

- Generation of unbuffered reports on change of status/measurement

  Unbuffered reports, when enabled, report any change of state in statuses and measurements (according to deadband settings).
- Support for time synchronization over an Ethernet link

  Time synchronization is supported using SNTP (Simple Network Time Protocol). This protocol is used to synchronize the internal real time clock of the relays.
- GOOSE peer-to-peer communication
  GOOSE communications of statuses are included as part of the IEC 61850 implementation. See *Peer-to-Peer (GSE) Communications* for more details.
- Disturbance record extraction
  Disturbance records can be extracted from MiCOM relays by file transfer, as ASCII format COMTRADE files.
- Controls
  The following control services are available:
  - Direct Control
  - Direct Control with enhanced security
  - Select Before Operate (SBO) with enhanced security
  - Controls are applied to open and close circuit breakers using XCBR.Pos and DDB signals ‘Control Trip’ and ‘Control Close’.
  - System/LLN0. LLN0.LEDRs are used to reset any trip LED indications.

- Reports
  Reports only include data objects that have changed and not the complete dataset. The exceptions to this are a General Interrogation request and integrity reports.
- Buffered Reports
  Eight Buffered Report Control Blocks, (BRCB), are provided in SYSTEM/LLN0 in Logical Device 'System'.
  Buffered reports are configurable to use any configurable dataset located in the same Logical device as the BRCB (SYSTEM/LLN0).
- Unbuffered Reports
  Sixteen Unbuffered Report Control Blocks (URCB) are provided in SYSTEM/LLN0 in Logical Device 'System'.
  Unbuffered reports are configurable to use any configurable dataset located in the same Logical device as the URCB (SYSTEM/LLN0).
- Configurable Data Sets
  It is possible to create and configure datasets in any Logical Node using the IED Configurator. The maximum number of datasets will be specified in an IED's ICD file. An IED is capable of handling 100 datasets.
- Published GOOSE message
  Eight GOCBs are provided in SYSTEM/LLN0.
- Uniqueness of control
  The Uniqueness of control mechanism is implemented to be consistent with the PACiS mechanism. This requires the relay to subscribe to the OrdRun signal from all devices in the system and be able to publish such a signal in a GOOSE message.
- Select Active Setting Group
  Functional protection groups can be enabled or disabled using private mod/beh attributes in the Protection/LLN0.OcpMod object. Setting groups are selectable using the Setting Group Control Block class, (SGCB). The Active Setting Group can be selected using the System/LLN0.SP.SGCB.ActSG data attribute in Logical Device 'System'.
- Quality for GOOSE
  It is possible to process the quality attributes of any Data Object in an incoming GOOSE message. Devices that do not support IEC61850 quality flags send quality attributes as all zeros. The supported quality attributes for outgoing GOOSE messages are described in the Protocol Implementation eXtra Information for Testing (PIXIT) document.
- Address List
  An Address List document (to be titled ADL) is produced for each IED which shows the mapping between the IEC61850 data model and the internal data model of the IED. It includes a mapping in the reverse direction, which may be more useful. This document is separate from the PICS/MICS document.
- Originator of Control
  Originator of control mechanism is implemented for operate response message and in the data model on the ST of the related control object, consistent with the PACiS mechanism.

- Metering
  MMTR (metering) logical node is implemented in P14x products. All metered values in the MMTR logical node are of type BCR. The actVal attribute of the BCR class is of type INT128, but this type is not supported by the SISCO MMSLite library. Instead, an INT64 value will be encoded for transmission.
  A SPC data object named MTTRs has been included in the MMTR logical node. This control will reset the demand measurements. A SPC data object named MTTRs is also included in the PTTR logical node. This control will reset the thermal measurements.
- Scaled Measurements
  The Unit definition, as per IEC specifies an SI unit and an optional multiplier for each measurement. This allows a magnitude of measurement to be specified e.g. mA, A, kA, MA.

The multiplier will always be included in the Unit definition and will be configurable in SCL, but not settable at runtime. It will apply to the magnitude, rangeC.min & rangeC.max attributes. rangeC.min & rangeC.max will not be settable at runtime to be more consistent with Px30 and to reduce configuration problems regarding deadbands.

Setting changes, such as changes to protection settings, are done using Easergy Studio. These changes can also be done using the relay's front port serial connection or the relay's Ethernet link, and is known as "tunneling".

8.3.2 IEC 61850 Configuration

One of the main objectives of IEC 61850 is to allow IEDs to be directly configured from a configuration file generated at system configuration time. At the system configuration level, the capabilities of the IED are determined from an IED capability description file (ICD), which is provided with the product. Using a collection of these ICD files from different products, the entire protection of a substation can be designed, configured and tested (using simulation tools) before the product is even installed into the substation.

To help this process, the Easergy Studio Support Software provides an IEC61850 IED Configurator tool. Select **Tools > IEC61850 IED Configurator**. This tool allows the preconfigured IEC 61850 configuration file (SCD or CID) to be imported and transferred to the IED. The configuration files for MiCOM relays can also be created manually, based on their original IED Capability Description (ICD) file.

Other features include the extraction of configuration data for viewing and editing, and a sophisticated error-checking sequence. The error checking ensures the configuration data is valid for sending to the IED and ensures the IED functions correctly in the substation.

To help the user, some configuration data is available in the **IED CONFIGURATOR** column of the relay user interface, allowing read-only access to basic configuration data.

8.3.2.1 Configuration Banks

To promote version management and minimize down-time during system upgrades and maintenance, the MiCOM relays have incorporated a mechanism consisting of multiple configuration banks. These configuration banks are categorized as:

- Active Configuration Bank
- Inactive Configuration Bank

Any new configuration sent to the relay is automatically stored in the inactive configuration bank, therefore not immediately affecting the current configuration. Both active and inactive configuration banks can be extracted at any time.

When the upgrade or maintenance stage is complete, the IED Configurator tool can be used to transmit a command to a single IED. This command authorizes the activation of the new configuration contained in the inactive configuration bank, by switching the active and inactive configuration banks. This technique ensures that the system down-time is minimized to the start-up time of the new configuration. The capability to switch the configuration banks is also available using the **IED CONFIGURATOR** column.

For version management, data is available in the **IED CONFIGURATOR** column in the relay user interface, displaying the SCL Name and Revision attributes of both configuration banks.

8.3.2.2 Network Connectivity

Note	*This section presumes a prior knowledge of IP addressing and related topics. Further details on this topic may be found on the Internet (search for IP Configuration) and in numerous relevant books.*

Configuration of the relay IP parameters (IP Address, Subnet Mask, Gateway) and SNTP time synchronization parameters (SNTP Server 1, SNTP Server 2) is performed by the IED Configurator tool. If these parameters are not available using an SCL file, they must be configured manually.

If the assigned IP address is duplicated elsewhere on the same network, the remote communications do not operate in a fixed way. However, the relay checks for a conflict at power up and every time the IP configuration is changed. An alarm is raised if an IP conflict is detected.

Use the **Gateway** setting to configure the relay to accept data from networks other than the local network.

8.4 The Data Model of MiCOM Relays

The data model naming adopted in the Px30 and Px40 relays has been standardized for consistency. The Logical Nodes are allocated to one of the five Logical Devices, as appropriate, and the wrapper names used to instantiate Logical Nodes are consistent between Px30 and Px40 relays.

The data model is described in the Model Implementation Conformance Statement (MICS) document, which is available separately. The MICS document provides lists of Logical Device definitions, Logical Node definitions, Common Data Class and Attribute definitions, Enumeration definitions, and MMS data type conversions. It generally follows the format used in Parts 7-3 and 7-4 of the IEC 61850 standard.

8.5 The Communication Services of MiCOM Relays

The IEC 61850 communication services which are implemented in the Px30 and Px40 relays are described in the Protocol Implementation Conformance Statement (PICS) document, which is available separately. The PICS document provides the Abstract Communication Service Interface (ACSI) conformance statements as defined in Annex A of Part 7-2 of the IEC 61850 standard.

8.6 Peer-to-Peer (GSE) Communications

The implementation of IEC 61850 Generic Object Oriented Substation Event (GOOSE) sets the way for cheaper and faster inter-relay communications. The generic substation event model provides fast and reliable system-wide distribution of input and output data values. The generic substation event model is based on autonomous decentralization This provides an efficient method of allowing simultaneous delivery of the same generic substation event information to more than one physical device, by using multicast services.

The use of multicast messaging means that IEC 61850 GOOSE uses a publisher-subscriber system to transfer information around the network*. When a device detects a change in one of its monitored status points, it publishes (sends) a new message. Any device that is interested in the information subscribes (listens) to the data message.

*Note**	*Multicast messages cannot be routed across networks without specialized equipment.*

Each new message is retransmitted at user-configurable intervals until the maximum interval is reached, to overcome possible corruption due to interference and collisions. In practice, the parameters which control the message transmission cannot be calculated. Time must be allocated to the testing of GOOSE schemes before or during commissioning; in just the same way a hardwired scheme must be tested.

8.6.1 Scope

A maximum of 128 virtual inputs are available within the PSL which can be mapped directly to a published dataset in a GOOSE message (Configurable dataset is supported).

Each GOOSE signal contained in a subscribed GOOSE message can be mapped to any of the 128 virtual inputs within the PSL. The virtual inputs allow the mapping to internal logic functions for protection control, directly to output contacts or LEDs for monitoring.

The MiCOM relay can subscribe to all GOOSE messages but only these data types can be decoded and mapped to a virtual input:

- BOOLEAN
- BSTR2
- INT16
- INT32
- INT8
- UINT16
- UINT32
- UINT8

The MiCOM relay also can subscribe to analogue GOOSE messages with Float32 data type. The received analogue values can not apply to any application function, these values will be stored only on the IEC 61850 data mode.

8.6.2 Simulation GOOSE Configuration

From Easergy Studio select Tools > IEC 61850 IED Configurator (Ed.2). Make sure the configuration is correct as this ensures efficient GOOSE scheme operation.

The relay can be set to publish/subscribe simulation/test GOOSE; it is important that this setting is returned to publish/receive normal GOOSE messages after testing to permit normal operation of the application and GOOSE messaging.

The relay provides a single setting to receive Simulated GOOSE, however it manages each subscribed GOOSE signal independently when the setting is set to simulated GOOSE. Each subscription (virtual input) will continue to respond to GOOSE messages without the simulation flag set; however once the relay receives a GOOSE for a subscription with the simulation flag set, it will respond to this and ignore messages without the simulation flag set. Other subscriptions (virtual inputs) which have not received a GOOSE message with the simulation flag will continue to operate as before. When the setting is reset back to normal GOOSE messaging the relay will ignore all GOOSE messages with the simulation flag set and act on GOOSE messages without the simulation flag.

WARNING **If you set the GOOSE in Simulation Mode, you MUST set it back to normal GOOSE after testing.**
IT IS POTENTIALLY EXTREMELY UNSAFE TO ATTEMPT TO USE ANY RELAY WHICH IS STILL IN GOOSE SIMULATION MODE.

8.6.3 High Performance GOOSE

In addition, the Px40 device is designed to provide maximum performance through an optimized publishing mechanism. This optimized mechanism is enabled so that the published GOOSE message is mapped using only the data attributes rather than mapping a complete data object. If data objects are mapped, the GOOSE messaging will operate correctly; but without the benefit of the optimized mechanism.

A pre-configured dataset named as "HighPerformGOOSE" is available in Ed.2 ICD template, which include all data attributes of all virtual outputs.

8.7 Ethernet Functionality

Settings relating to a failed Ethernet link are available in the 'COMMUNICATIONS' column of the relay user interface.

8.7.1 Ethernet Disconnection

IEC 61850 'Associations' are unique and made to the relay between the client (master) and server (IEC 61850 device). If the Ethernet is disconnected, such associations are lost and must be re-established by the client. The TCP_KEEPALIVE function is implemented in the relay to monitor each association and terminate any which are no longer active.

8.7.2 Loss of Power

If the relay's power is removed, the relay allows the client to re-establish associations without a negative impact on the relay's operation. As the relay acts as a server in this process, the client must request the association. Uncommitted settings are cancelled when power is lost. Reports requested by connected clients are reset and must be re-enabled by the client when the client next creates the new association to the relay.

8.7.3 Courier Tunneling via Secure Ethernet Communications

8.7.3.1 Introduction

When the IED and Easergy Studio are connected via the Ethernet port they will communicate securely using TLS.
The benefits of secure communication are:

- Help in the prevention of unwanted eavesdropping between Easergy Studio and the IED
- Help in the prevention of modification of data between Easergy Studio and the IED
- Ensure integrity of data
- Prevent replay of data at a later data

Note	*The communication will be done using port 4422, ensure this port is left unblocked on your network.*

8.7.3.2 Setting up a Connection

As a quick guide, you need to do the following:

1. In Easergy Studio, click the Quick Connect… button
2. Select the relevant Device Type in the Quick Connect dialog box.
3. Select Ethernet port
4. Enter the relevant data i.e. IP address of IED
5. Click Finish
6. Easergy Studio will attempt to communicate with the device

Note	*When attempting to connect to the IED via Ethernet, Easergy Studio will first try to communicate with the IED via secure communication. If this is not possible, it will use open communication with no encryption.* *For secure communication, please ensure port 4422 is left unblocked on the firewalls on which Easergy Studio is running.*

Notes:

INSTALLATION

CHAPTER 16

Date (month/year):	11/2016			
Products covered by this chapter:	This chapter covers the specific versions of the MiCOM products listed below. This includes ***only*** the following combinations of Software Version and Hardware Suffix.			
Hardware suffix:	P141/P142/P143 P145 P241 P242/P243 P342 P343/P344/P345 P391 P445 P44x (P441/P442/P444) P44x (P442/P444)	J/L J/M J K J K A J/L J/K M	P44y (P443/P446) P547 P54x (P543/P544/P545/P546) P642 P643 P645 P74x (P741/P742/P743) P746 P841 P849	K/M K K/M J/L K/M K/M J/K K/M K/M K/M
Software version:	P14x (P141/P142/P143/P145) P24x (P241/P242/P243): P342/P343/P344/P345/P391 P445 P44x (P441/P442/P444) P44x (P442/P444)	43/44/46/ B0/B1/B2 57 36 35/36/J4 C7.x/D4.x/ D5.x/D6.x/ E0/E1	P44y (P443/P446) P547 P54x (P543/P544/P545/P546) P64x (P642/P643/P645) P74x (P741/P742/P743) P746 P841 P849	55/H4 57 45/55/H4 04/A0/B1/B2 51/A0/B1 A0/B1/B2/B3/ C1/C2/C3 45/55/G4/H4 A0/B1
Connection diagrams:	P14x (P141, P142, P143 & P145): 10P141xx (xx = 01 to 02) 10P142xx (xx = 01 to 05) 10P143xx (xx = 01 to 11) 10P145xx (xx = 01 to 11) P24x (P241, P242 & P243): 10P241xx (xx = 01 to 02) 10P242xx (xx = 01) 10P243xx (xx = 01) P34x (P342, P343, P344, P345 & P391): 10P342xx (xx = 01 to 17) 10P343xx (xx = 01 to 19) 10P344xx (xx = 01 to 12) 10P345xx (xx = 01 to 07) 10P391xx (xx = 01 to 02) P445: 10P445xx (xx = 01 to 04) P44x (P441, P442 & P444): 10P44101 (SH 1 & 2) 10P44201 (SH 1 & 2) 10P44202 (SH 1) 10P44203 (SH 1 & 2) 10P44401 (SH 1) 10P44402 (SH 1) 10P44403 (SH 1 & 2) 10P44404 (SH 1) 10P44405 (SH 1) 10P44407 (SH 1 & 2) P44y (P443 & P446): 10P44303 (SH 01 and 03) 10P44304 (SH 01 and 03) 10P44305 (SH 01 and 03) 10P44306 (SH 01 and 03) 10P44600 10P44601 (SH 1 to 2) 10P44602 (SH 1 to 2) 10P44603 (SH 1 to 2)		P54x (P543, P544, P545 & P546): 10P54302 (SH 1 to 2) 10P54303 (SH 1 to 2) 10P54400 10P54404 (SH 1 to 2) 10P54405 (SH 1 to 2) 10P54502 (SH 1 to 2) 10P54503 (SH 1 to 2) 10P54600 10P54604 (SH 1 to 2) 10P54605 (SH 1 to 2) 10P54606 (SH 1 to 2) P547: 10P54702xx (xx = 01 to 02) 10P54703xx (xx = 01 to 02) 10P54704xx (xx = 01 to 02) 10P54705xx (xx = 01 to 02) P64x (P642, P643 & P645): 10P642xx (xx = 1 to 10) 10P643xx (xx = 1 to 6) 10P645xx (xx = 1 to 9) P74x (P741, P742 & P743): 10P740xx (xx = 01 to 07) P746: 10P746xx (xx = 00 to 21) P841: 10P84100 10P84101 (SH 1 to 2) 10P84102 (SH 1 to 2) 10P84103 (SH 1 to 2) 10P84104 (SH 1 to 2) 10P84105 (SH 1 to 2) P849: 10P849xx (xx = 01 to 06)	

CONTENTS

Page (IN) 16-

TABLES

FIGURES

1 INTRODUCTION TO MICOM RANGE

About MiCOM Range

MiCOM is a comprehensive solution capable of meeting all electricity supply requirements. It comprises a range of components, systems and services from Schneider Electric.

Central to the MiCOM concept is flexibility. MiCOM provides the ability to define an application solution and, through extensive communication capabilities, integrate it with your power supply control system.

The components within MiCOM are:

- P range protection relays
- C range control products
- M range measurement products for accurate metering and monitoring
- S range versatile PC support and substation control packages

MiCOM products include extensive facilities for recording information on the state and behaviour of the power system using disturbance and fault records. They can also provide measurements of the system at regular intervals to a control centre enabling remote monitoring and control to take place.

For up-to-date information, please see:

www.schneider-electric.com

MiCOM Px4x Products

The MiCOM Px4x series of protection devices provide a wide range of protection and control functions and meet the requirements of a wide market segment.

Different parts of the Px4x range provide different functions. These include:

- **P14x** **Feeder Management** relay suitable for MV and HV systems
- **P24x** **Motors** and rotating machine management relay for use on a wide range of synchronous and induction machines
- **P34x** **Generator Protection** for small to sophisticated generator systems and interconnection protection
- **P445** Full scheme **Distance Protection** relays for MV, HV and EHV systems
- **P44x** Full scheme **Distance Protection** relays for MV, HV and EHV systems
- **P44y** Full scheme **Distance Protection** relays for MV, HV and EHV systems
- **P54x** **Line Differential** protection relays for HV/EHV systems with multiple communication options and phase comparison protection for use with PLC
- **P547** **Line Differential** protection relays for HV/EHV systems with multiple communication options and phase comparison protection for use with PLC
- **P64x** **Transformer Protection Relays**
- **P74x** **Numerical Busbar Protection** for use on MV, HV and EHV busbars
- **P746** **Numerical Busbar Protection** for use on MV, HV and EHV busbars
- **P84x** **Breaker Failure** protection relays

Note	*During 2011, the International Electrotechnical Commission classified the voltages into different levels (IEC 60038). The IEC defined LV, MV, HV and EHV as follows: LV is up to 1000V. MV is from 1000V up to 35 kV. HV is from 110 kV or 230 kV. EHV is above 230 KV.* *There is still ambiguity about where each band starts and ends. A voltage level defined as LV in one country or sector, may be described as MV in a different country or sector. Accordingly, LV, MV, HV and EHV suggests a possible range, rather than a fixed band. Please refer to your local Schneider Electric office for more guidance.*

2 RECEIPT, HANDLING, STORAGE AND UNPACKING RELAYS

2.1 Receipt of Relays

Protective relays, although generally of robust construction, require careful treatment prior to installation on site.
Upon receipt, relays should be examined immediately to ensure no external damage has been sustained in transit. If damage has been sustained, a claim should be made to the transport contractor and Schneider Electric should be promptly notified.
Relays that are supplied unmounted and not intended for immediate installation should be returned to their protective polythene bags and delivery carton. See the *Storage* section for more information about the storage of relays.

2.2 Handling of Electronic Equipment

Warning **Before carrying out any work on the equipment, you should be familiar with the contents of the Safety Information chapter/Safety Guide SFTY/5L M/L11 or later issue, the Technical Data chapter and the ratings on the equipment rating label.**

A person's normal movements can easily generate electrostatic potentials of several thousand volts. Discharge of these voltages into semiconductor devices when handling electronic circuits can cause serious damage which, although not always immediately apparent, will reduce the reliability of the circuit. This is particularly important to consider where the circuits use Complementary Metal Oxide Semiconductors (CMOS), as is the case with these relays.
The electronic circuits inside the relay are protected from electrostatic discharge when housed in the case. Do not expose them to risk by removing the front panel or Printed Circuit Boards (PCBs) unnecessarily.
Each PCB incorporates the highest practicable protection for its semiconductor devices. However, if it becomes necessary to remove a PCB, the following precautions should be taken to preserve the high reliability and long life for which the relay has been designed and manufactured.

- Before removing a PCB, ensure that you are at the same electrostatic potential as the equipment by touching the case.
- Handle analogue input modules by the front panel, frame or edges of the circuit boards. PCBs should only be handled by their edges. Avoid touching the electronic components, printed circuit tracks or connectors.
- Do not pass the module to another person without first ensuring you are both at the same electrostatic potential. Shaking hands achieves equipotential.
- Place the module on an anti-static surface, or on a conducting surface which is at the same potential as yourself.
- If it is necessary to store or transport printed circuit boards removed from the case, place them individually in electrically conducting anti-static bags.

In the unlikely event that you are making measurements on the internal electronic circuitry of a relay in service, it is preferable that you are earthed to the case with a conductive wrist strap. Wrist straps should have a resistance to ground between 500kΩ to 10MΩ. If a wrist strap is not available you should maintain regular contact with the case to prevent a build-up of electrostatic potential. Instrumentation which may be used for making measurements should also be earthed to the case whenever possible.

More information on safe working procedures for all electronic equipment can be found in IEC 61340-5-1. It is strongly recommended that detailed investigations on electronic circuitry or modification work should be carried out in a special handling area such as described in the aforementioned Standard document.

2.3 Storage

If relays are not to be installed immediately upon receipt, they should be stored in a place free from dust and moisture in their original cartons. Where de-humidifier bags have been included in the packing they should be retained. The action of the de-humidifier crystals will be impaired if the bag is exposed to ambient conditions and may be restored by gently heating the bag for about an hour prior to replacing it in the carton.
To prevent battery drain during transportation and storage a battery isolation strip is fitted during manufacture. With the lower access cover open, presence of the battery isolation strip can be checked by a red tab protruding from the positive side.
Care should be taken on subsequent unpacking that any dust which has collected on the carton does not fall inside. In locations of high humidity the carton and packing may become impregnated with moisture and the de-humidifier crystals will lose their efficiency.
Prior to installation, relays should be stored at a temperature of between -40°C to +70°C (-13°F to +158°F).

2.4 Unpacking

Care must be taken when unpacking and installing the relays so that none of the parts are damaged and additional components are not accidentally left in the packing or lost. Make sure that any user's CDROM or technical documentation is NOT discarded, and accompanies the relay to its destination substation.

Note	*With the lower access cover open, the red tab of the battery isolation strip will be seen protruding from the positive side of the battery compartment. Do not remove this strip because it prevents battery drain during transportation and storage and will be removed as part of the commissioning tests.*

Relays must only be handled by skilled persons.
The site should be well lit to facilitate inspection, clean, dry and reasonably free from dust and excessive vibration. This particularly applies to installations which are being carried out at the same time as construction work.

3 RELAY MOUNTING

MiCOM relays are dispatched either individually or as part of a panel/rack assembly. Individual relays are normally supplied with an outline diagram showing the dimensions for panel cut-outs and hole centres. This information can also be found in the product publication.
Secondary front covers can also be supplied as an option item to prevent unauthorised changing of settings and alarm status. They are available in sizes 40TE and 60TE. The 60TE cover also fits the 80TE case size of the relay.
The old GN0037/GN0038 part numbers are now obsolete.
They have been replaced by the GN0242/GN0243 versions as shown below.

Product	Size	Part No (obsolete)	Replacement Part No
P40	**40TE** **60TE / 80TE**	**GN0037 001** **GN0038 001**	**GN0242 001** **GN0243 001**
P14x	40TE 60TE / 80TE	GN0037 001 GN0038 001	GN0242 001 GN0243 001
P24xxxxxxxxxxA P24xxxxxxxxxxC	40TE 60TE / 80TE	GN0037 001 GN0038 001	GN0242 001 GN0243 001
P24xxxxxxxxxxJ P24xxxxxxxxxxK	40TE 60TE / 80TE		GN0242 001 GN0243 001
P34xxxxxxxxxxA P34xxxxxxxxxxC	40TE 60TE / 80TE	GN0037 001 GN0038 001	GN0242 001 GN0243 001
P34xxxxxxxxxxJ P34xxxxxxxxxxK	40TE 60TE / 80TE		GN0242 001 GN0243 001
P44x	40TE 60TE / 80TE	GN0037 001 GN0038 001	GN0242 001 GN0243 001
P44y	60TE / 80TE	GN0038 001	GN0243 001
P445	40TE 60TE / 80TE	GN0037 001 GN0038 001	GN0242 001 GN0243 001
P54x	60TE / 80TE	GN0038 001	GN0243 001
P547	60TE / 80TE	GN0038 001	GN0243 001
P64xxxxxxxxxxA/B/C	40TE 60TE / 80TE	GN0037 001 GN0038 001	GN0242 001 GN0243 001
P64xxxxxxxxxxJ/K	40TE 60TE / 80TE		GN0242 001 GN0243 001
P74x P74x	40TE 60TE	GN0037 001 GN0038 001	GN0242 001 GN0243 001
P746	80TE	GN0038 001	GN0243 001
P841	60TE / 80TE	GN0038 001	GN0243 001
P849	80TE	GN0038 001	GN0243 001

Note *Part Numbers suitable for rack-mounting have an "N" as the 10th digit.*
Part Numbers suitable for panel-mounting have an "M" as the 10th digit.
Size 40TE may be GN0242 001 and 60TE/80TE as GN0243 001.

Table 1 - Products, sizes and part numbers

The design of the relay is such that the fixing holes in the mounting flanges are only accessible when the access covers are open and hidden from sight when the covers are closed.
If a MiCOM P991 or Easergy test block is to be included with the relays, we recommend you position the test block on the right-hand side of the associated relays (when viewed from the front). This minimises the wiring between the relay and test block, and allows the correct test block to be easily identified during commissioning and maintenance tests.

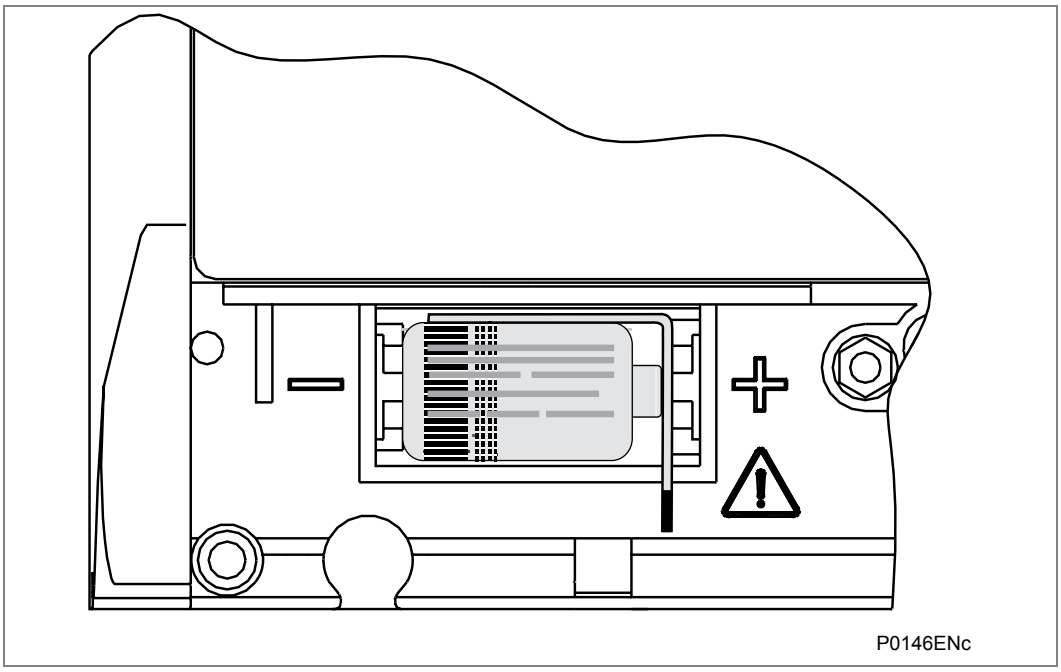


Figure 1 - Location of battery isolation strip

If you need to test correct relay operation during the installation, the battery isolation strip can be removed but should be replaced if commissioning of the scheme is not imminent. This will prevent unnecessary battery drain during transportation to site and installation. The red tab of the isolation strip can be seen protruding from the positive side of the battery compartment when the lower access cover is open. To remove the isolation strip, pull the red tab whilst lightly pressing the battery to prevent it falling out of the compartment. When replacing the battery isolation strip, ensure that the strip is refitted as shown in the *Location of battery isolation strip* diagram, i.e. with the strip behind the battery with the red tab protruding.

3.1 Rack Mounting

Virtually all MiCOM relays can be rack mounted using single tier rack frames (part number FX0021 101), see the ***Rack mounting of relays*** diagram below. These frames have dimensions in accordance with IEC 60297 and are supplied pre-assembled ready to use. On a standard 483 mm rack this enables combinations of case widths up to a total equivalent of size 80TE to be mounted side-by-side.
The two horizontal rails of the rack frame have holes drilled at approximately 26 mm intervals and the relays are attached via their mounting flanges using M4 Taptite self-tapping screws with captive 3 mm thick washers (also known as a SEMS unit). These fastenings are available in packs of 5 (part number ZA0005 104).

Warning	**Risk of damage to the front cover moulding. Do not use conventional self-tapping screws, including those supplied for mounting other relays because they have slightly larger heads.**

Once the tier is complete, the frames are fastened into the racks using mounting angles at each end of the tier.

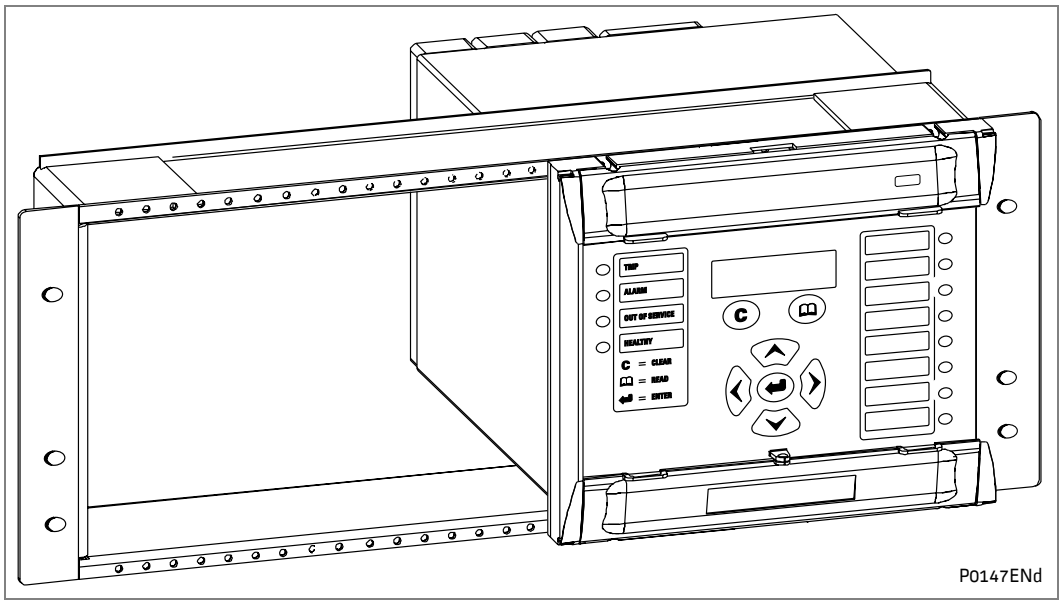


Figure 2 - Rack mounting of relays

Relays can be mechanically grouped into single tier (4U) or multi-tier arrangements by the rack frame. This enables schemes using MiCOM products to be pre-wired together prior to mounting.

Use blanking plates if there are empty spaces. The spaces may be for future installation of relays or because the total size is less than 80TE on any tier. Blanking plates can also be used to mount ancillary components. The following ***Blanking plates*** table shows the sizes that can be ordered.

Note	*Blanking plates are only available in grey.*

Case size summation	Blanking plate part number
10TE	GJ2028 102
20TE	GJ2028 104
30TE	GJ2028 106
40TE	GJ2028 108

Table 2 - Blanking plates

3.2 Panel Mounting

The relays can be flush mounted into panels using M4 SEMS Taptite self-tapping screws with captive 3 mm thick washers (also known as a SEMS unit). These fastenings are available in packs of 5 (part number ZA0005 104).

Warning **Risk of damage to the front cover moulding. Do not use conventional self-tapping screws, including those supplied for mounting other relays because they have slightly larger heads.**

Alternatively tapped holes can be used if the panel has a minimum thickness of 2.5 mm. If several relays are mounted in a single cut-out in the panel, mechanically group them together horizontally or vertically to form rigid assemblies prior to mounting in the panel.

Note *Fastening MiCOM relays with pop rivets is not advised because this does not allow easy removal if repair is necessary.*

Rack-mounting panel-mounted versions: it is possible to rack-mount some relay versions which have been designed to be panel-mounted. The relay is mounted on a single-tier rack frame, which occupies the full width of the rack. To make sure a panel-mounted relay assembly complies with BS EN60529 IP52, fit a metallic sealing strip between adjoining relays (Part No GN2044 001) and a sealing ring from the following ***IP52 sealing rings*** table around the complete assembly.

Width	Single tier	Double tier
40TE	GJ9018 008	GJ9018 024
45TE	GJ9018 009	GJ9018 025
50TE	GJ9018 010	GJ9018 026
55TE	GJ9018 011	GJ9018 027
60TE	GJ9018 012	GJ9018 028
65TE	GJ9018 013	GJ9018 029
70TE	GJ9018 014	GJ9018 030
75TE	GJ9018 015	GJ9018 031
80TE	GJ9018 016	GJ9018 032

Table 3 - IP52 sealing rings

4 RELAY WIRING

This section serves as a guide to selecting the appropriate cable and connector type for each terminal on the MiCOM relay.

Warning **Before carrying out any work on the equipment, you should be familiar with the contents of the Safety Information chapter/Safety Guide SFTY/5L M/L11 or later issue, the Technical Data chapter and the ratings on the equipment rating label.**

4.1 Medium and Heavy Duty Terminal Block Connections

Key:
Heavy duty terminal block: CT and VT circuits, terminals with "C","D","E" or "F" prefix (depending on the relay)
Medium duty: All other terminal blocks (grey color)
Loose relays are supplied with sufficient M4 screws for making connections to the rear mounted terminal blocks using ring terminals, with a recommended maximum of two ring terminals per relay terminal.
If required, Schneider Electric can supply M4 90° crimp ring terminals in three different sizes depending on wire size (see the *M4 90° crimp ring terminals* table). Each type is available in bags of 100.

Part number	Wire size	Insulation colour
ZB9124 901	0.25 – 1.65mm^2 (22 – 16AWG)	Red
ZB9124 900	1.04 – 2.63mm^2 (16 – 14AWG)	Blue
ZB9124 904	2.53 – 6.64mm^2 (12 – 10AWG)	Uninsulated*

Note ** To maintain the terminal block insulation requirements for safety, fit an insulating sleeve over the ring terminal after crimping.*

Table 4 - M4 90° crimp ring terminals

The following minimum wire sizes are recommended:

- Current Transformers 2.5mm^2
- Auxiliary Supply Vx 1.5mm^2
- RS485 Port See separate section
- Rotor winding to P391 1.0mm^2
- Other circuits 1.0mm^2

Due to the limitations of the ring terminal, the maximum wire size that can be used for any of the medium or heavy duty terminals is 6.0mm^2 using ring terminals that are not pre-insulated. Where it required to only use pre-insulated ring terminals, the maximum wire size that can be used is reduced to 2.63mm^2 per ring terminal. If a larger wire size is required, two wires should be used in parallel, each terminated in a separate ring terminal at the relay.
The wire used for all connections to the medium and heavy duty terminal blocks, except the RS485 port, should have a minimum voltage rating of 300Vrms.
It is recommended that the auxiliary supply wiring should be protected by a 16A maximum High Rupture Capacity (HRC) fuse of type NIT or TIA. For safety reasons, current transformer circuits must never be fused. Other circuits should be appropriately fused to protect the wire used.

Note *The high-break contacts optional fitted to P44y (P443/P446) and P54x relays are polarity sensitive. External wiring must respect the polarity requirements which are shown on the external connection diagram to ensure correct operation.*

Each opto input has selectable filtering. This allows use of a pre-set filter of ½ cycle which renders the input immune to induced noise on the wiring: although this method is secure it can be slow, particularly for intertripping. This can be improved by switching off the ½ cycle filter in which case one of the following methods to reduce ac noise should be considered. The first method is to use double pole switching on the input, the second is to use screened twisted cable on the input circuit. The recognition time of the opto inputs without the filtering is <2 ms and with the filtering is <12 ms.

4.2 EIA(RS)485 Port

Connections to the first rear EIA(RS)485 port use ring terminals. 2-core screened cable is recommended with a maximum total length of 1000m or 200nF total cable capacitance. A typical cable specification would be:

Each core:	16/0.2mm copper conductors. PVC insulated
Nominal conductor area:	0.5mm^2 per core
Screen:	Overall braid, PVC sheathed

See the SCADA Communications chapter for details of setting up an EIA(RS)485 bus.

4.3 Current Loop Input Output (CLIO) Connections (if applicable)

Where current loop inputs and outputs are available on a MiCOM relay, the connections are made using screw clamp connectors, as per the RTD inputs, on the rear of the relay which can accept wire sizes between 0.1 mm^2 and 1.5 mm^2. It is recommended that connections between the relay and the current loop inputs and outputs are made using a screened cable. The wire should have a minimum voltage rating of 300 Vrms.

4.4 IRIG-B Connections (if applicable)

The IRIG-B input and BNC connector have a characteristic impedance of 50Ω. It is recommended that connections between the IRIG-B equipment and the relay are made using coaxial cable of type RG59LSF with a halogen free, fire retardant sheath.

4.5 EIA(RS)232 Port

Short term connections to the RS232 port, located behind the bottom access cover, can be made using a screened multi-core communication cable up to 15m long, or a total capacitance of 2500pF. The cable should be terminated at the relay end with a 9-way, metal shelled, D-type male plug. The Getting Started chapter of this manual details the pin allocations.

4.6 Optical Fiber Connectors (when applicable)

Warning **LASER LIGHT RAYS: Where fibre optic communication devices are fitted, never look into the end of a fiber optic due to the risk of causing serious damage to the eye. Optical power meters should be used to determine the operation or signal level of the device. Non-observance of this rule could possibly result in personal injury.**

If electrical to optical converters are used, they must have management of character idle state capability (for when the fibre optic cable interface is "Light off").
Specific care should be taken with the bend radius of the fibres, and the use of optical shunts is not recommended as these can degrade the transmission path over time.
The relay uses 1310nm multi mode 100BaseFx and BFOC 2.5 - (ST/LC according to the MiCOM model) connectors (one Tx – optical emitter, one Rx – optical receiver).

4.7 Ethernet Port for IEC 61850 and/or DNP3.0 (where applicable)

4.7.1 Fiber Optic (FO) Port

The relays can have 100 Mbps Ethernet port. Fibre Optic (FO) connection is recommended for use in permanent connections in a substation environment. The 100 Mbit port uses a type LC connector (according to the MiCOM model), compatible with fiber multimode 50/125 µm or 62.5/125 µm to 1310 nm.

Note	*The new LC fiber optical connector can be used with the Px40 Enhanced Ethernet Board.*

4.7.2 RJ-45 Metallic Port

Due to possibility of noise and interference on this part, it is recommended that this connection type be used for short-term connections and over short distance. Ideally, where the relays and switches are located in the same cubicle.
The connector for the Ethernet port is a shielded RJ-45. The following ***Signals on the Ethernet connector*** table shows the signals and pins on the connector.

Pin	Signal name	Signal definition
1	TXP	Transmit (positive)
2	TXN	Transmit (negative)
3	RXP	Receive (positive)
4	-	Not used
5	-	Not used
6	RXN	Receive (negative)
7	-	Not used
8	-	Not used

Table 5 - Signals on the Ethernet connector

4.8 RTD Connections (if applicable)

Where RTD inputs are available on a MiCOM relay, the connections are made using screw clamp connectors on the rear of the relay that can accept wire sizes between 0.1 mm^2 and 1.5 mm^2. The connections between the relay and the RTDs must be made using a screened 3-core cable with a total resistance less than 10 Ω. The cable should have a minimum voltage rating of 300 Vrms.
A 3-core cable should be used even for 2-wire RTD applications, as it allows for the cable's resistance to be removed from the overall resistance measurement. In such cases the third wire is connected to the second wire at the point the cable is joined to the RTD.
The screen of each cable must only be earthed at one end, preferably at the relay end and must be continuous. Multiple earthing of the screen can cause circulating current to flow along the screen, which induces noise and is unsafe.
It is recommended to minimize noise pick-up in the RTD cables by keeping them close to earthed metal casings and avoiding areas of high electromagnetic and radio interference. The RTD cables should not be run adjacent to or in the same conduit as other high voltage or current cables.
A typical cable specification would be:

Each core: 7/0.2 mm copper conductors heat resistant PVC insulated
Nominal conductor area: 0.22 mm^2 per core
Screen: Nickel-plated copper wire braid heat resistant PVC sheathed

The extract below may be useful in defining cable recommendations for the RTDs:

Noise pick-up by cables can be categorized in to three types:

- Resistive
- Capacitive
- Inductive

Resistive coupling	requires there to be an electrical connection to the noise source. So assuming that the wire and cable insulation is sound and that the junctions are clean then this can be dismissed.
Capacitive coupling	requires there to be sufficient capacitance for the impedance path to the noise source to be small enough to allow for significant coupling. This is a function of the dielectric strength between the signal cable on the noise source and the potential (i.e. power) of the noise source.
Inductive coupling	occurs when the signal cable is adjacent to a cable/wire carrying the noise or it is exposed to a radiated EMF.

Standard screened cable is normally used to protect against capacitively coupled noise, but in order for it to be effective the screen must only be bonded to the system ground at one point, otherwise a current could flow and the noise would be coupled in to the signal wires of the cable. There are different types of screening available, but basically there are two types: aluminum foil wrap and tin-copper braid.
Foil screens are good for low to medium frequencies and braid is good for high frequencies. High-fidelity screen cables provide both types.
Protection against magnetic inductive coupling requires very careful cable routing and magnetic shielding. The latter can be achieved with steel-armored cable and the use of steel cable trays. It is important that the armor of the cable is grounded at both ends so that the EMF of the induced current cancels the field of the noise source and hence shields the cables conductors from it. (However, the design of the system ground must be considered and care taken to not bridge two isolated ground systems since this could be hazardous and defeat the objectives of the original ground design). The cable should be laid in the cable trays as close as possible to the metal of the tray and under no circumstance should any power cable be in or near to the tray. (Power cables should only cross the signal cables at 90 degrees and never be adjacent to them).
Both the capacitive and inductive screens must be contiguous from the RTD probes to the relay terminals.
The best types of cable are those provided by the RTD manufactures. These tend to be three conductors (a so-called "triad") which are screened with foil. Such triad cables are available in armored forms as well as multi-triad armored forms.

4.9 Download/Monitor Port

Short term connections to the download/monitor port, located behind the bottom access cover, can be made using a screened 25-core communication cable up to 4m long. The cable should be terminated at the relay end with a 25-way, metal shelled, D-type male plug.
The Getting Started and Commissioning chapters this manual details the pin allocations.

4.10 Second EIA(RS)232/485 Port

Relays with Courier, MODBUS, IEC 60870-5-103 or DNP3 protocol on the first rear communications port have the option of a second rear port, running Courier protocol. The second rear communications port can be used over one of three physical links:

- twisted pair K-Bus (non-polarity sensitive),
- twisted pair EIA(RS)485 (connection polarity sensitive) or
- EIA(RS)232. This EIA(RS)232 port is actually compliant to EIA(RS)574; the 9-pin version of EIA(RS)232, see www.tiaonline.org.

4.10.1 Connection to the Second Rear Port

The second rear Courier port connects via a 9-way female D-type connector (SK4) in the middle of the card end plate (in between IRIG-B connector and lower D-type). The connection is compliant to EIA(RS)574.

4.10.1.1 For IEC 60870-5-2 over EIA(RS)232/574

Pin	Connection
1	No Connection
2	RxD
3	TxD
4	DTR#
5	Ground
6	No Connection
7	RTS #
8	CTS #
9	No Connection
# - These pins are control lines for use with a modem.	

Table 6 - Pin connections for IEC 60870-5-2 over EIA(RS)232/574

Connections to the second rear port configured for EIA(RS)232 operation can be made using a screened multi-core communication cable up to 15 m long, or a total capacitance of 2500 pF. The cable should be terminated at the relay end with a 9-way, metal shelled, D-type male plug. The table above details the pin allocations.

4.10.1.2 For K-bus or IEC 60870-5-2 over EIA(RS)485

Pin*	Connection
4	EIA(RS)485 - 1 (+ ve)
7	EIA(RS)485 - 2 (- ve)
* - All other pins unconnected.	

Note *Connector pins 4 and 7 are used by both the EIA(RS)232/574 and EIA(RS)485 physical layers, but for different purposes. Therefore, the cables should be removed during configuration switches.*
For the EIA(RS)485 protocol an EIA(RS)485 to EIA(RS)232/574 converter will be required to connect a modem or PC running MiCOM S1 Studio, to the relay. A Schneider Electric CK222 is recommended.
EIA(RS)485 is polarity sensitive, with pin 4 positive (+) and pin 7 negative (-).
The K-Bus protocol can be connected to a PC via a KITZ101 or 102.
It is recommended that a 2-core screened cable be used. To avoid exceeding the second communications port flash clearances it is recommended that the length of cable between the port and the communications equipment should be less than 300 m. This length can be increased to 1000 m or 200nF total cable capacitance if the communications cable is not laid in close proximity to high current carrying conductors. The cable screen should be earthed at one end only.

Table 7 - Pin connections for K-bus or IEC 60870-5-2 over EIA(RS)485

A typical cable specification would be:

Each core:	16/0.2mm copper conductors. PVC insulated
Nominal conductor area:	0.5mm^2 per core
Screen:	Overall braid, PVC sheathed

4.11 Earth Connection (Protective Conductor)

Every relay must be connected to the local earth bar using the M4 earth studs in the bottom left hand corner of the relay case. The minimum recommended wire size is 2.5mm^2 and should have a ring terminal at the relay end.
Due to the limitations of the ring terminal, the maximum wire size that can be used for any of the medium or heavy duty terminals is 6.0mm^2 per wire. If a greater cross-sectional area is required, two parallel connected wires, each terminated in a separate ring terminal at the relay, or a metal earth bar could be used.

Note	*To prevent any possibility of electrolytic action between brass or copper earth conductors and the rear panel of the relay, precautions should be taken to isolate them from one another. This could be achieved in a number of ways, including placing a nickel-plated or insulating washer between the conductor and the relay case, or using tinned ring terminals.*

Warning	**Before carrying out any work on the equipment, you should be familiar with the contents of the Safety Information chapter/Safety Guide SFTY/5L M/L11 or later issue, the Technical Data chapter and the ratings on the equipment rating label.**

4.12 P391 Rotor Earth Fault Unit (REFU) Mounting

Under rotor earth fault conditions, DC currents of up to 29mA can appear in the earth circuit. Accordingly, the P391 must be permanently connected to the local earth via the protective conductor terminal provided.
This section serves as a guide to selecting the appropriate cable and connector type for each terminal on the P391 unit.

Caution	**You must be familiar with all safety statements listed in the Commissioning chapter and the Safety Information section SFTY/4LM/G11 (or later issue) before undertaking any work on the P391.**

Caution	**Under no circumstances should the high voltage DC rotor winding supply be connected via Easergy or P99x test blocks. Both Easergy and P990 test blocks are not rated for continuous working voltages greater than 300 Vrms. These test blocks are not designed to withstand the inductive EMF voltages which will be experienced on disconnection or de-energization of the DC rotor winding supply.**

4.12.1 Medium Duty Terminal Block Connections

Information about the medium duty terminal block connections is described in the ***Medium and Heavy Duty Terminal Block Connections*** section.

Caution **Wiring between the DC rotor winding and the P391 must be suitably rated to withstand at least twice the rotor winding supply voltage to earth. This is to ensure that the wiring insulation can withstand the inductive Electro Motive Force (EMF) voltage which will be experienced on disconnection or de-energization of the DC rotor winding supply.**

Due to the limitations of the ring terminal, the maximum wire size that can be used for any of the medium terminals is 6.0 mm^2 using ring terminals that are not pre-insulated (protective conductor terminal (PCT) only). All P391 terminals, except PCT shall be pre-insulated ring terminals, the maximum wire size that can be used is reduced to 2.63 mm^2 per ring terminal.

Wiring between the DC rotor winding and the P391 shall be suitably rated to withstand at least twice the rotor winding supply voltage to earth. The wire used for other P391 connections to the medium duty terminal blocks should have a minimum voltage rating of 300 Vrms.

The dielectric withstand of P391 injection resistor connections (A16, B16, A8, B8) to earth is 5.8 kV rms, 1 minute.

It is recommended that the auxiliary supply wiring should be protected by a High Rupture Capacity (HRC) fuse of type NIT or TIA, rated between 2 A and 16 A. Other circuits should be appropriately fused to protect the wire used.

5 CASE DIMENSIONS

The MiCOM range of products are available in a series of different case sizes.
The case sizes available for each product are shown here:

Range	Case Size		
	40TE	60TE	80TE
P14x	P141, P142	P143, P145	P143
P24x	P241	P242	P243
P34x	P341, P342	P341, P342, P343	P343, P344, P345
P441	P441		
P44x		P442	P444
P44y			P443, P446
P445	P445	P445	
P541	P541		
P542		P542	
P54x		P543, P544	P545, P546
P547			P547
P64x	P642	P643, P645	P645
P74x	P742	P743	P741
P746			P746
P841		P841	P841
P849			P849

Table 8 - Products and case sizes

5.1 40TE Case Dimensions

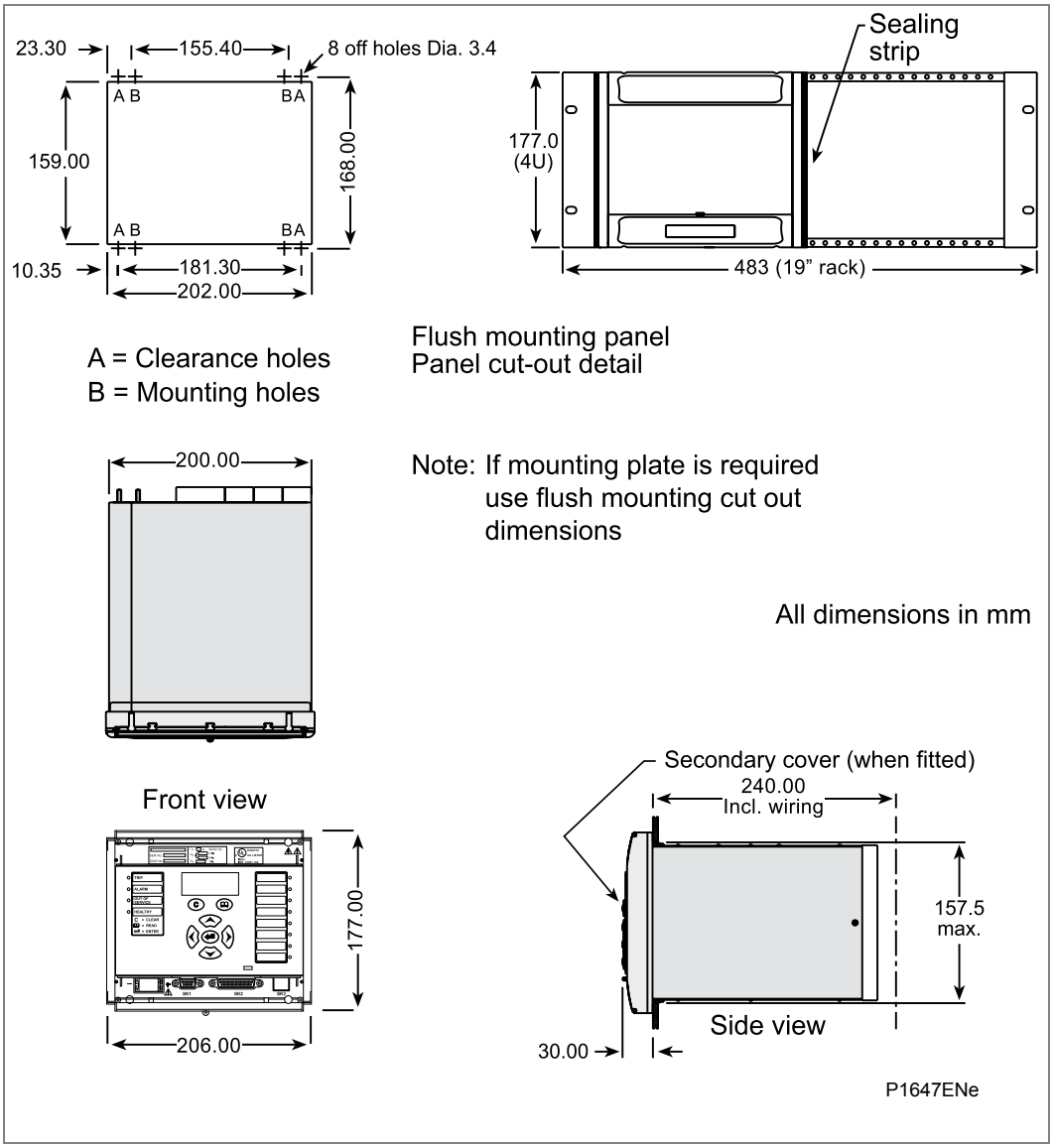


Figure 3 - 40TE Case Dimensions

5.2 60TE Case Dimensions

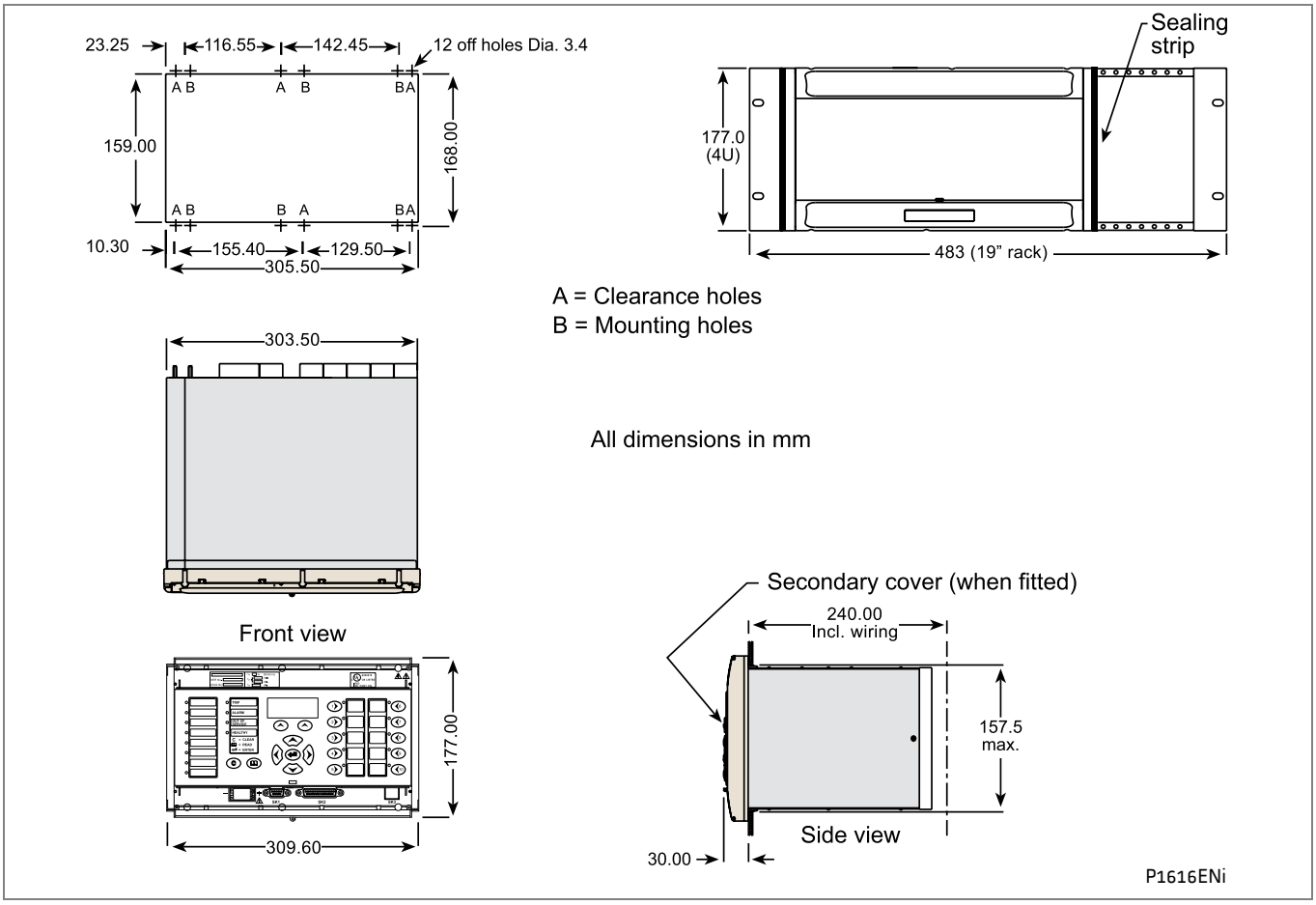


Figure 4 - 60TE Case Dimensions

5.3 80TE Case Dimensions

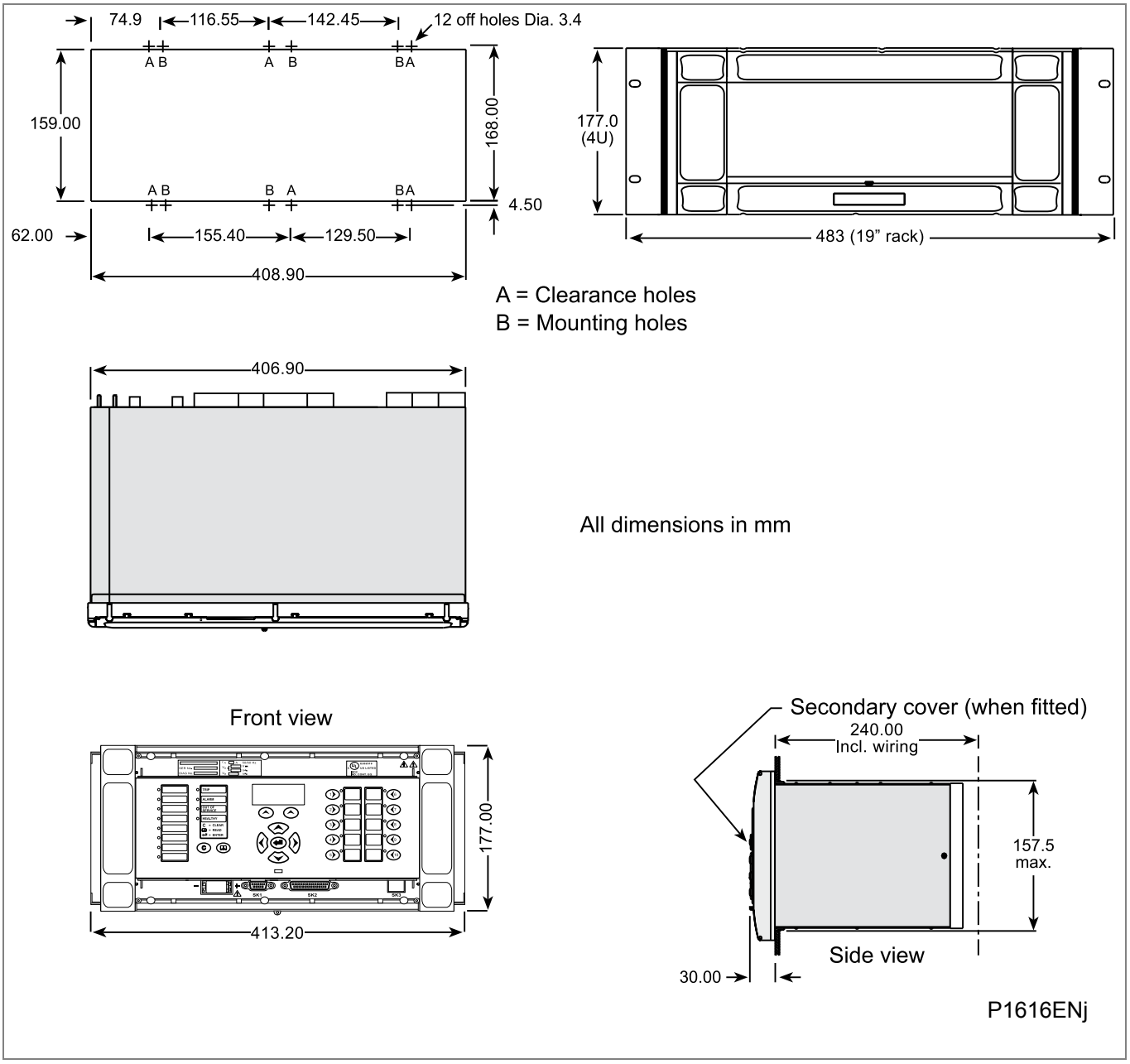


Figure 5 - 80TE Case Dimensions

CONNECTION DIAGRAMS

CHAPTER 17

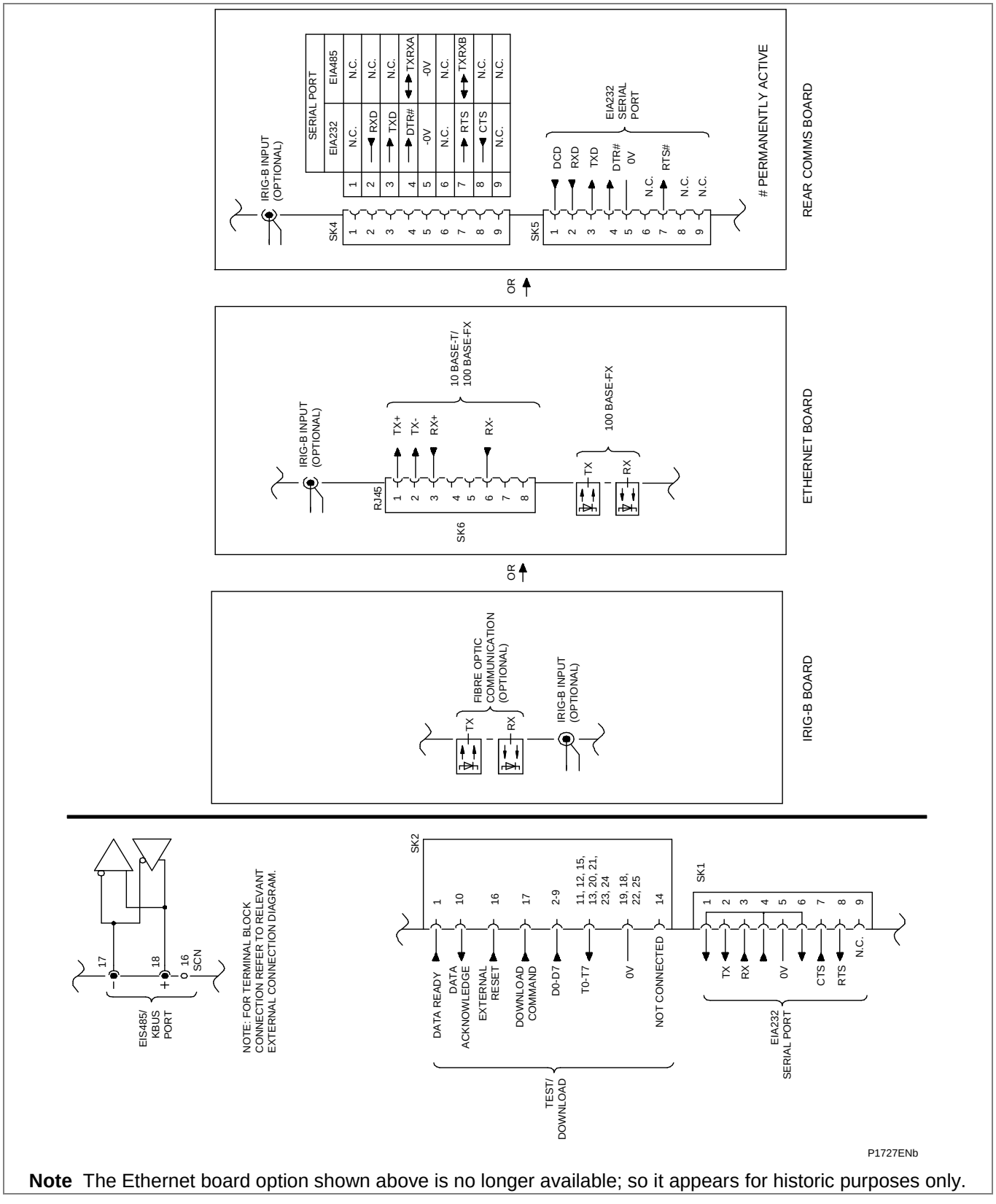
Date (month/year):	07/2018
Products covered by this chapter:	This chapter covers the specific versions of the MiCOM products listed below. This includes ***only*** the following combinations of Software Version and Hardware Suffix.
Hardware suffix:	L (P642) & M (P643/P645)
Software version:	B4 - P64x (P642, P643 & P645)
Connection diagrams:	10P642xx (xx = 01 to 10) 10P643xx (xx = 01 to 06) 10P645xx (xx = 01 to 09)

CONTENTS

FIGURES

Note	*In the following captions, ITD = Input Transformer Differential, I/P = Input, O/P = Output, 1P = 1-Pole, 2P = 2-Pole*

P64X EXTERNAL CONNECTION DIAGRAMS



Note The Ethernet board option shown above is no longer available; so it appears for historic purposes only.

Figure 1 - Serial Communications Options MiCOM Px40 platform

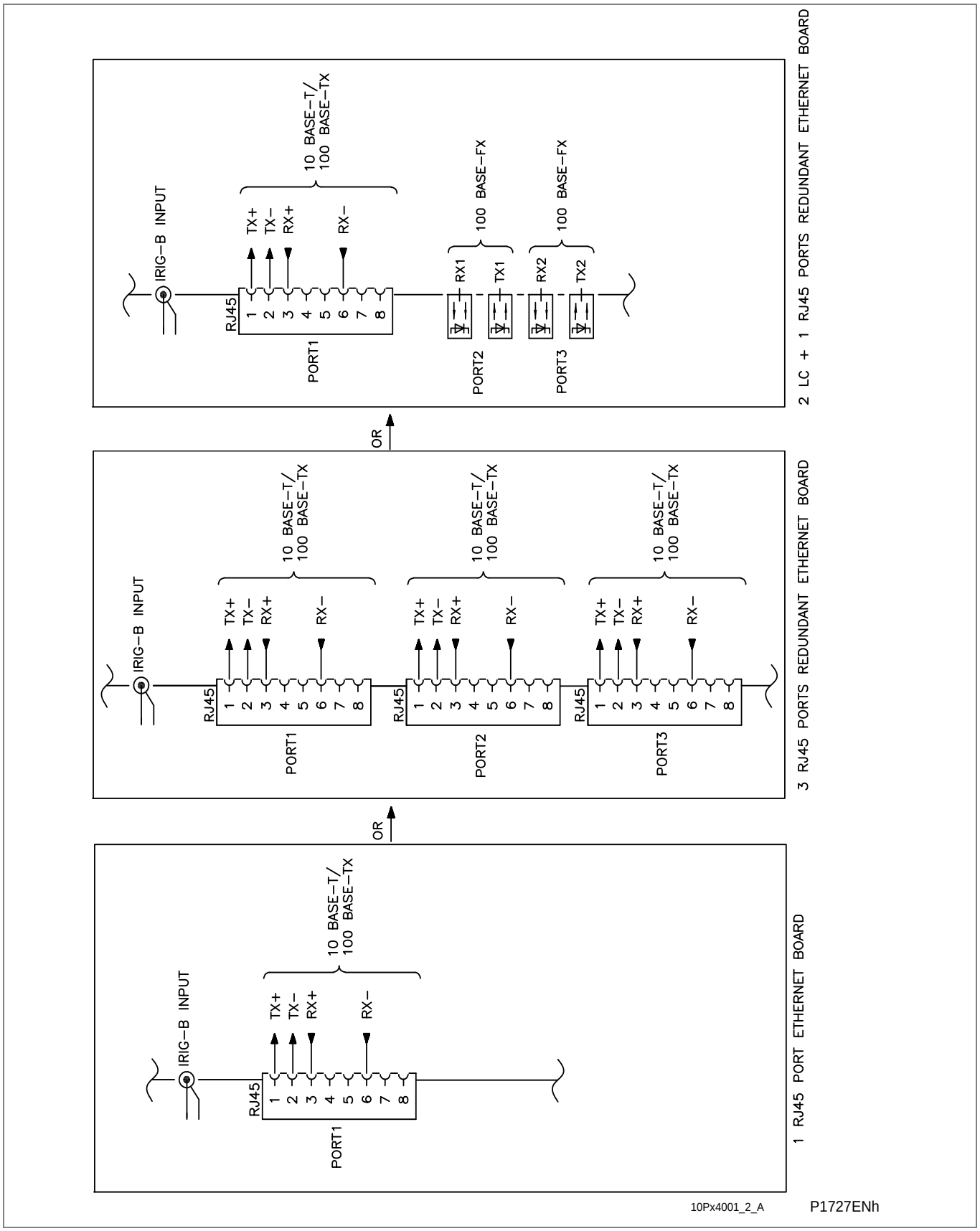


Figure 2 - Ethernet Communications Options MiCOM Px40 platform

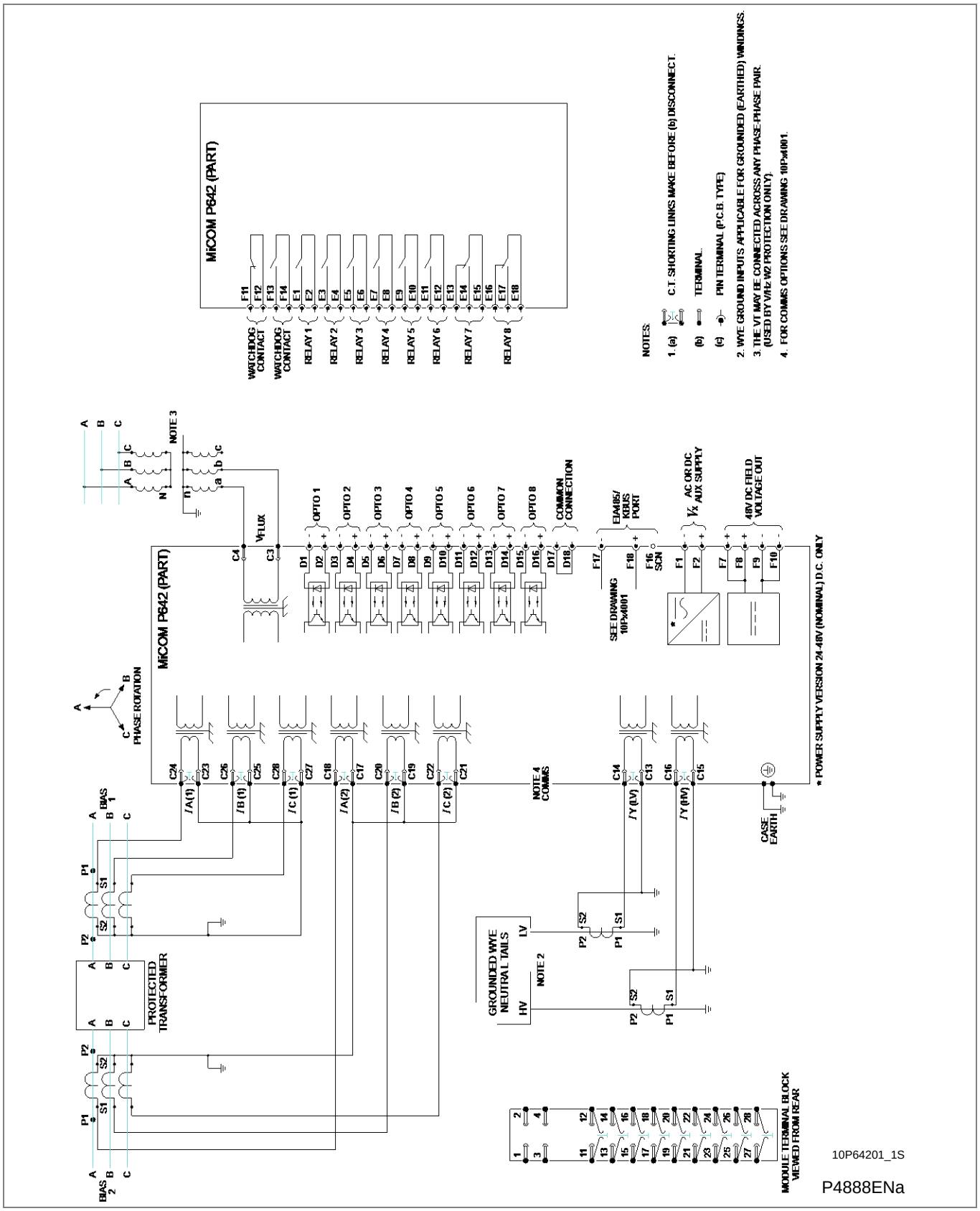


Figure 3 - Two bias ITD (8 I/P & 8 O/P) with 1P VT input (40TE)

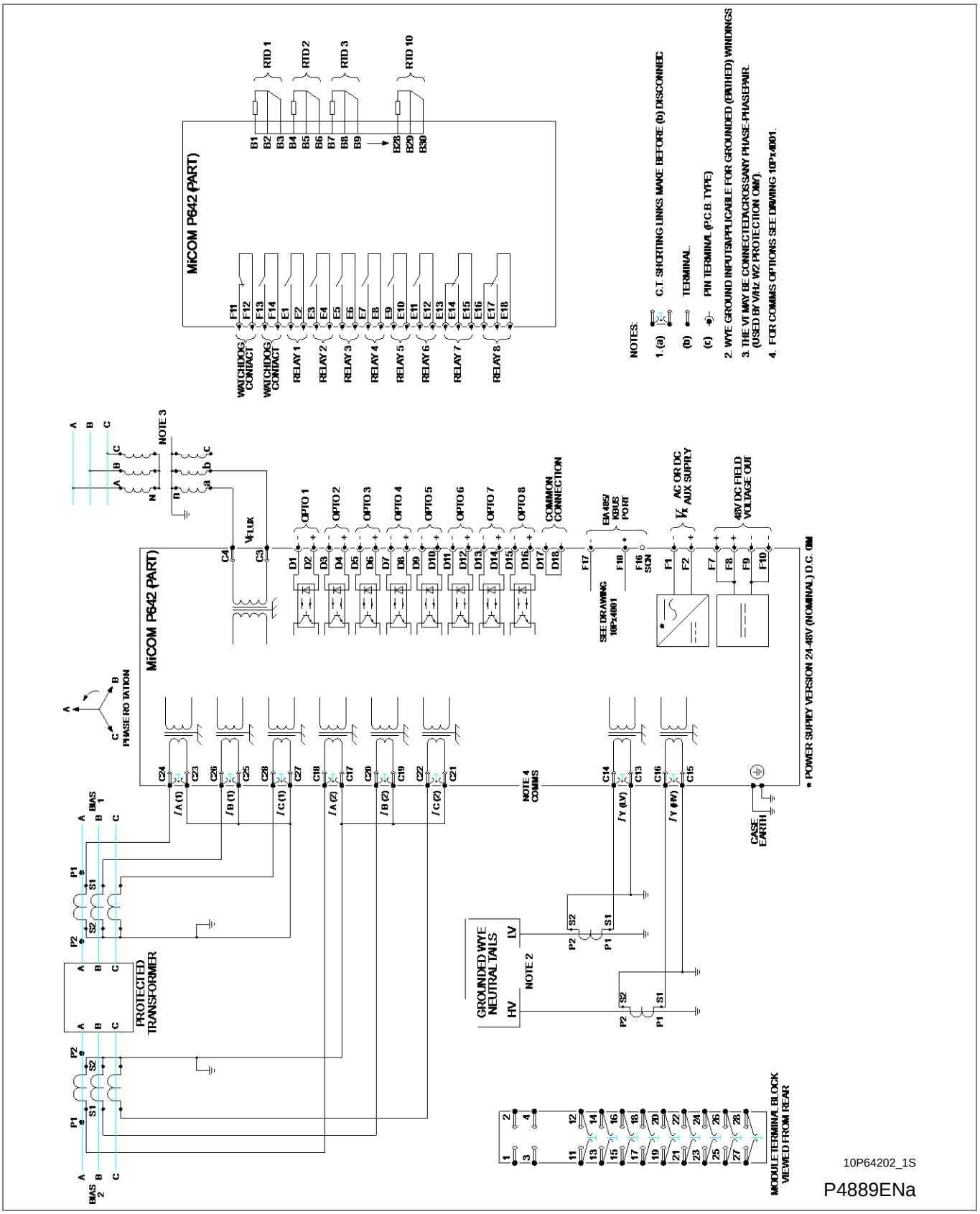


Figure 4 - Two bias ITD (8 I/P & 8 O/P + RTD) with 1P VT input (40TE)

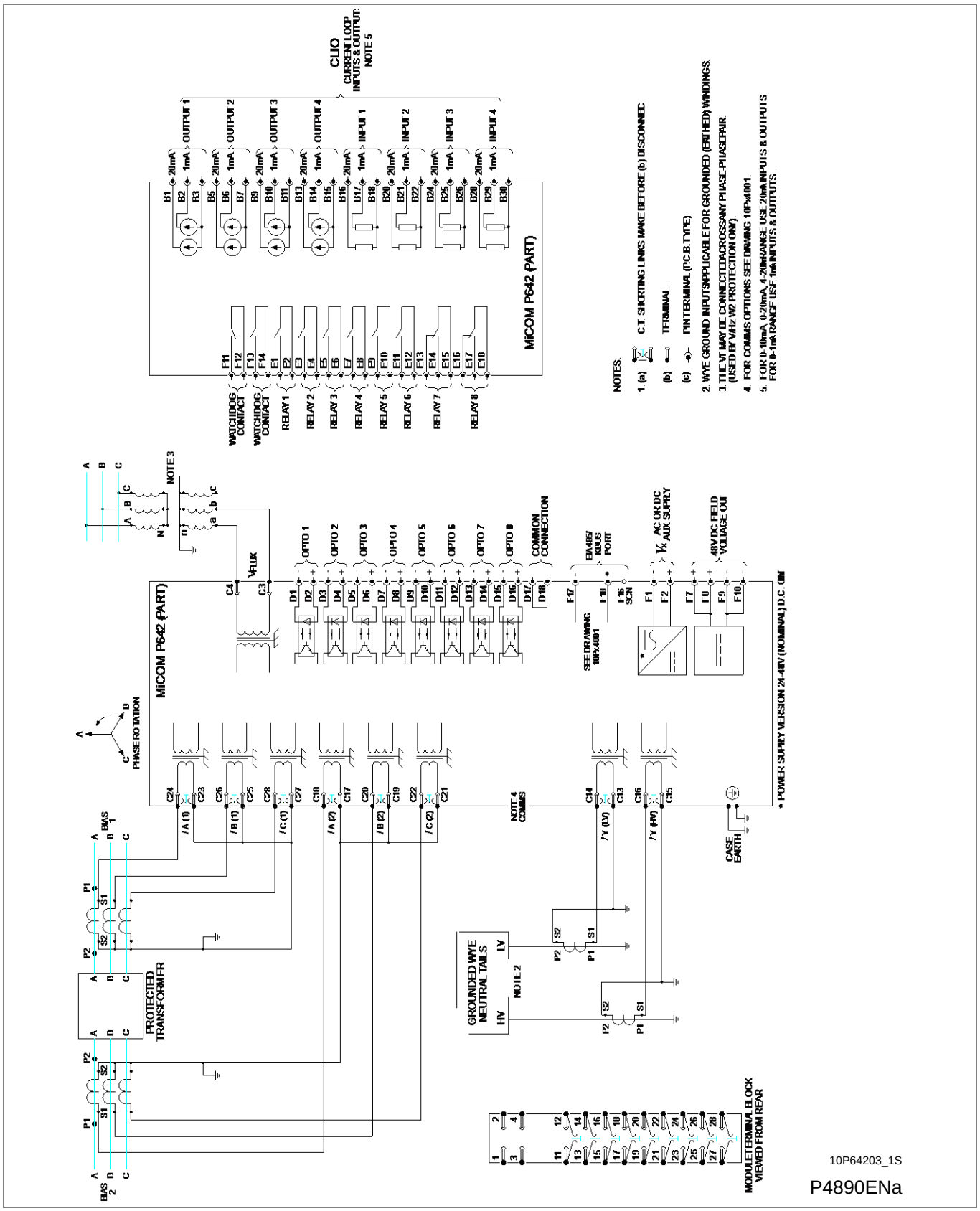


Figure 5 - Two bias ITD (8 I/P & 8 O/P + CLIO) with 1P VT input (40TE)

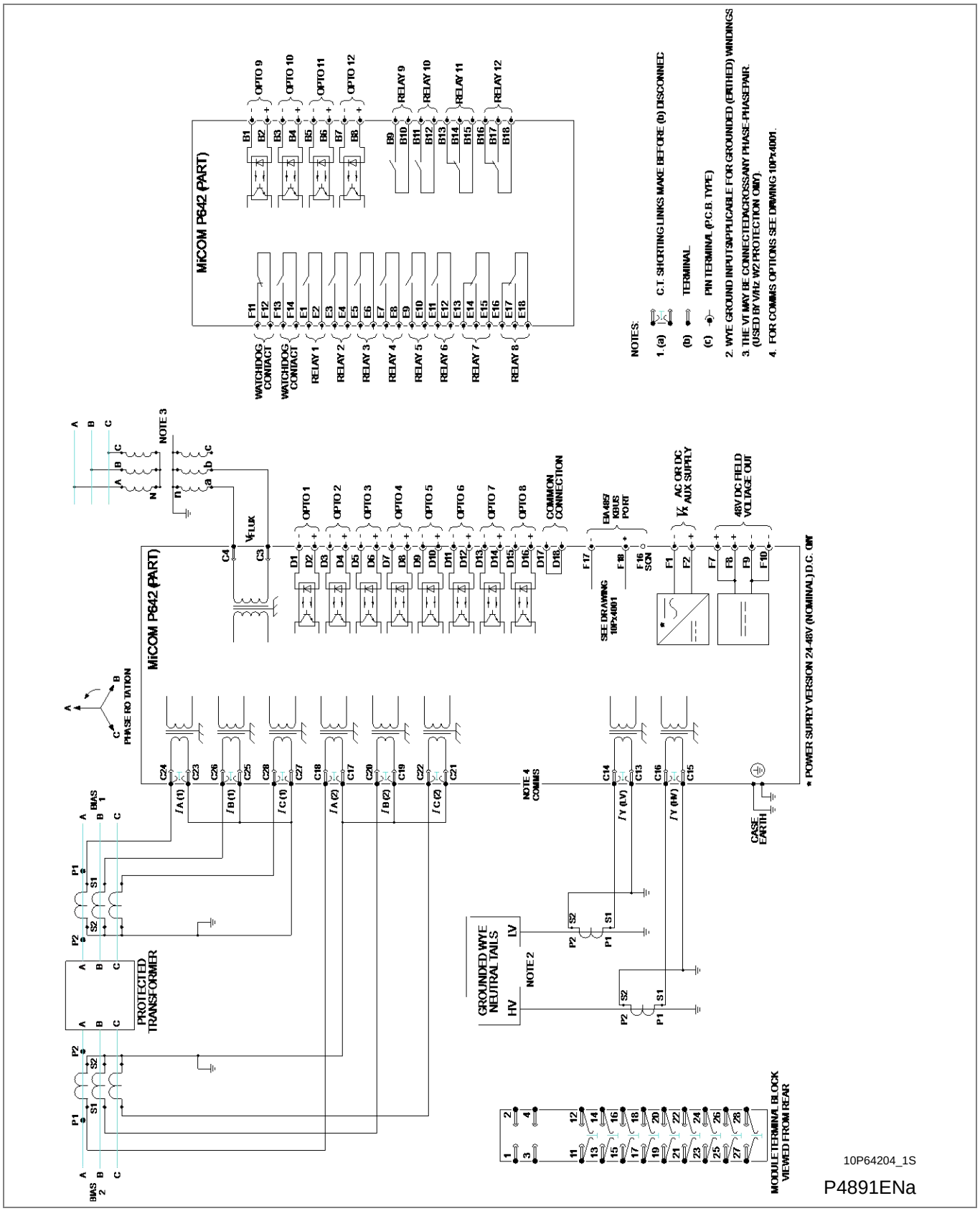


Figure 6 - Two bias ITD (12 I/P & 12 O/P) with 1P VT input (40TE)

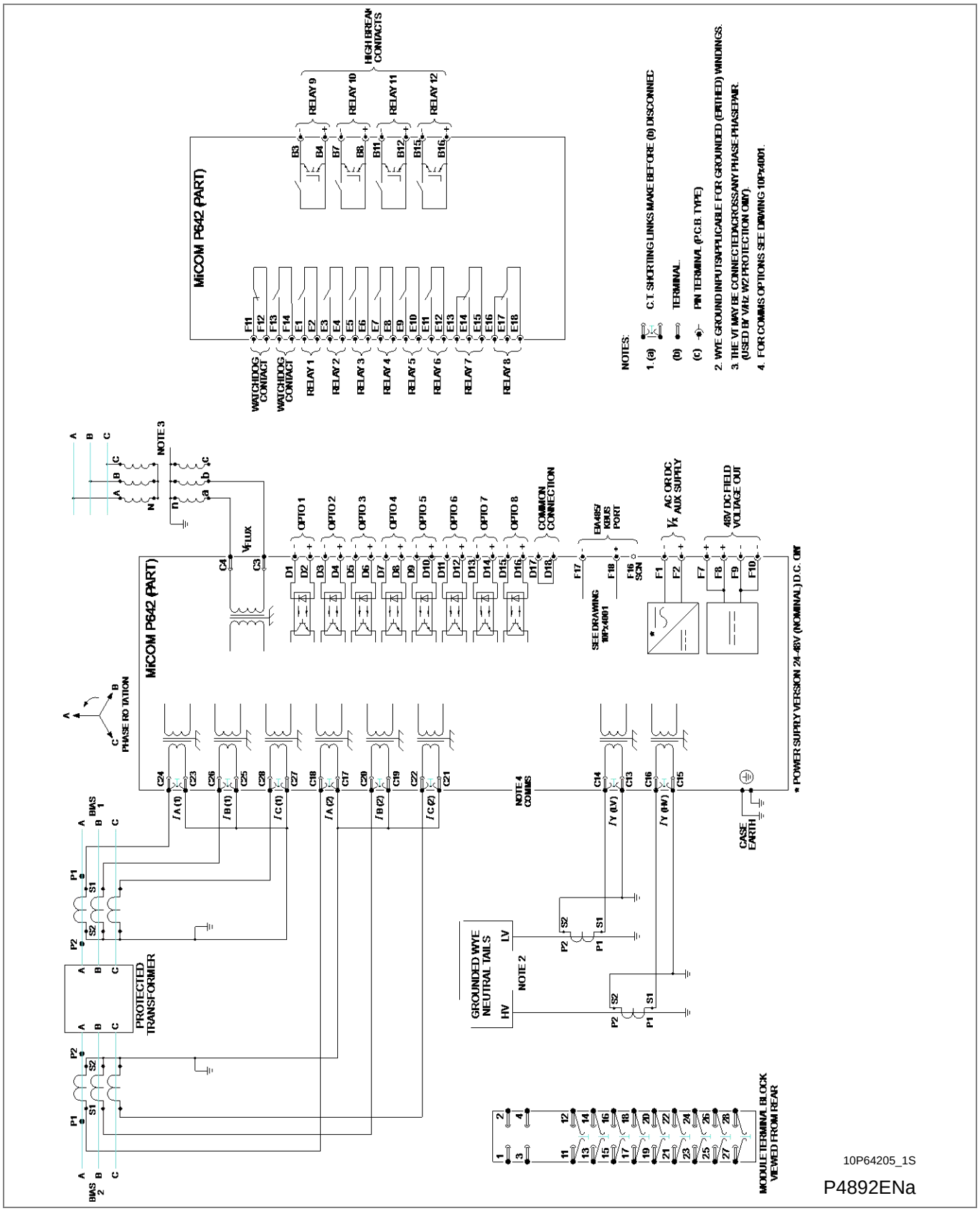


Figure 7 - Two bias ITD (8 I/P & 12 O/P) with 1P input (40TE)

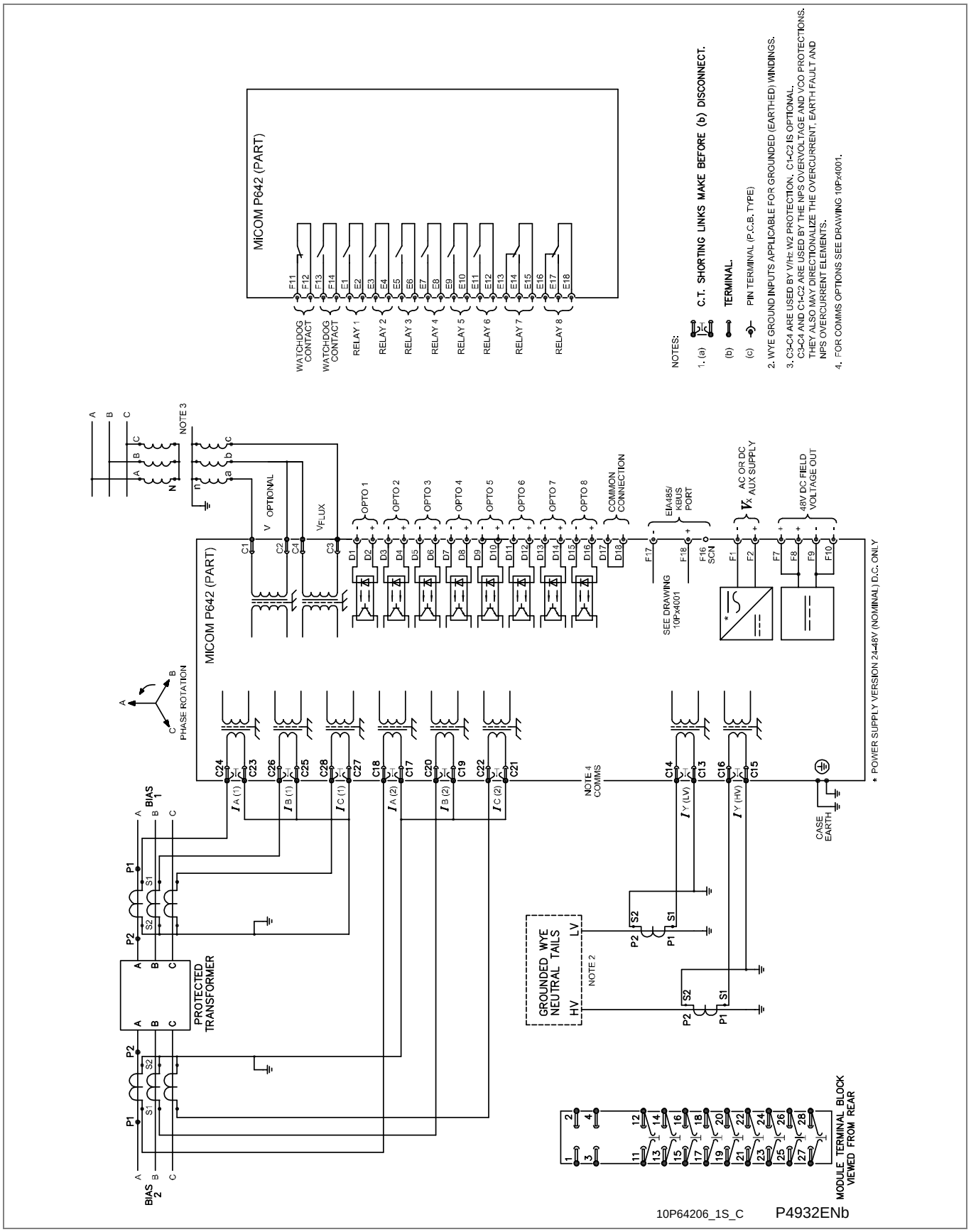


Figure 8 - Two bias ITD (8 I/P & 8 O/P) with 2P VT inputs (40TE)

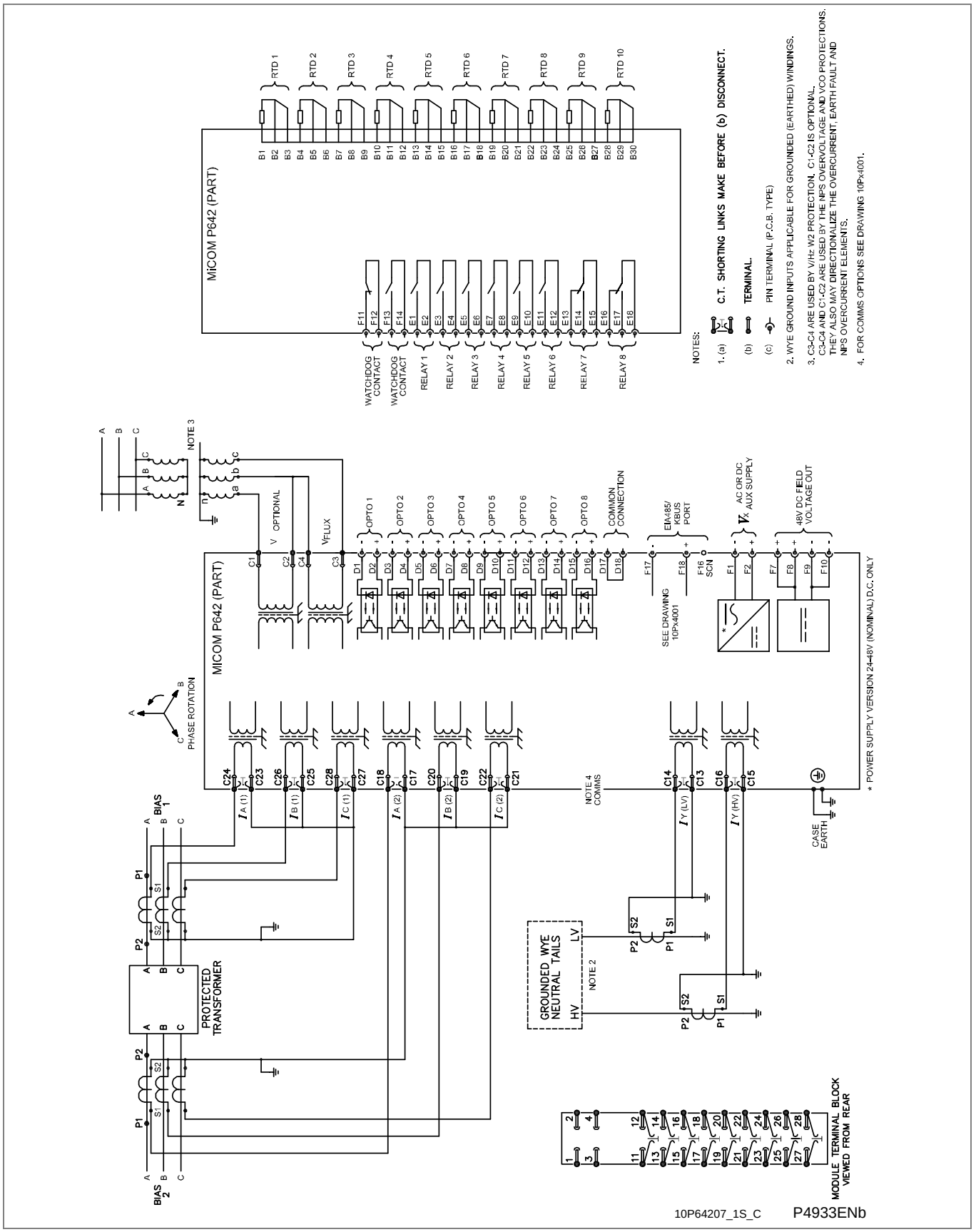


Figure 9 - Two bias ITD (8 I/P & 8 O/P + RTD) with 2P VT inputs (40TE)

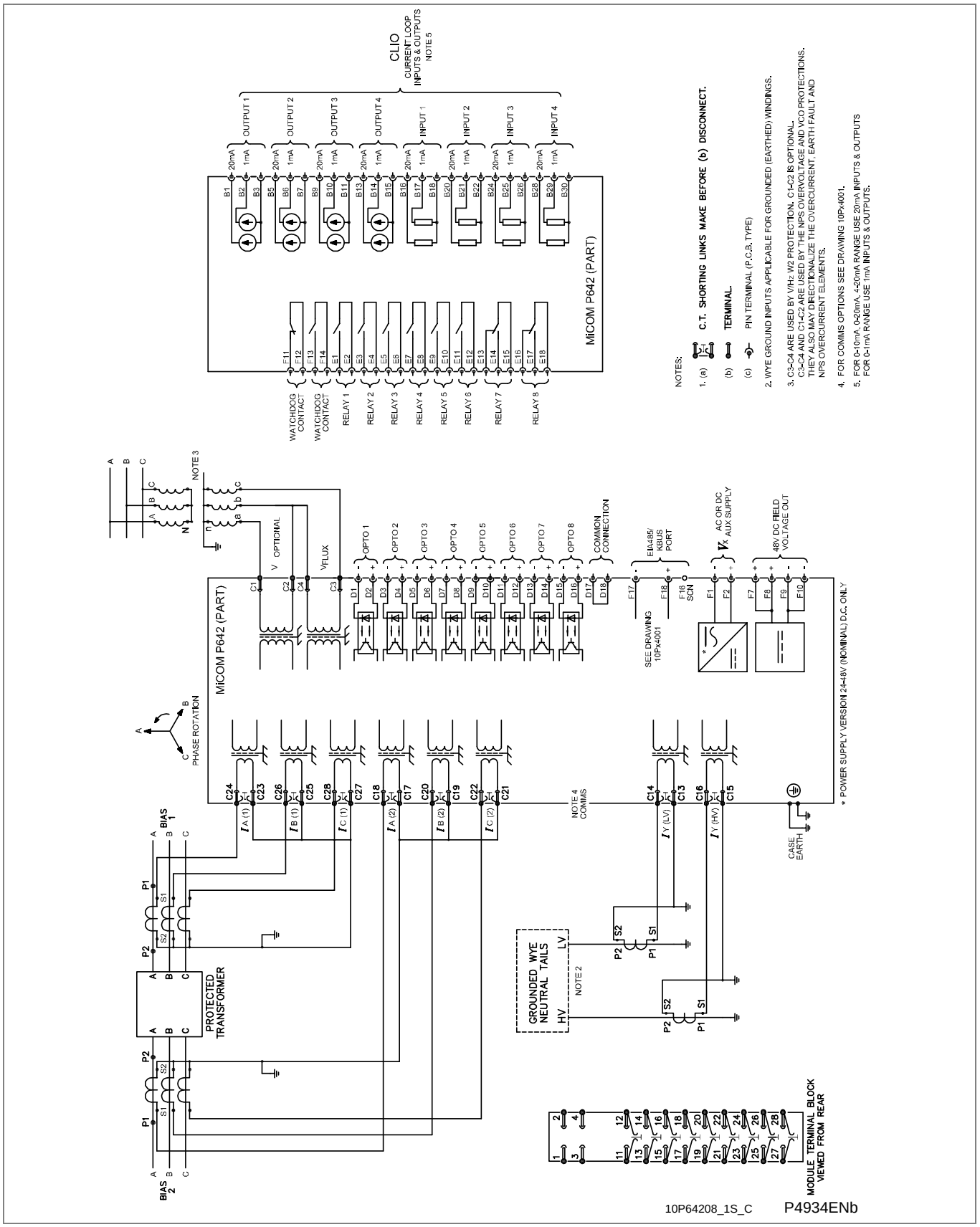


Figure 10 - Two bias ITD (8 I/P & 8 O/P + CLIO) with 2P VT inputs (40TE)

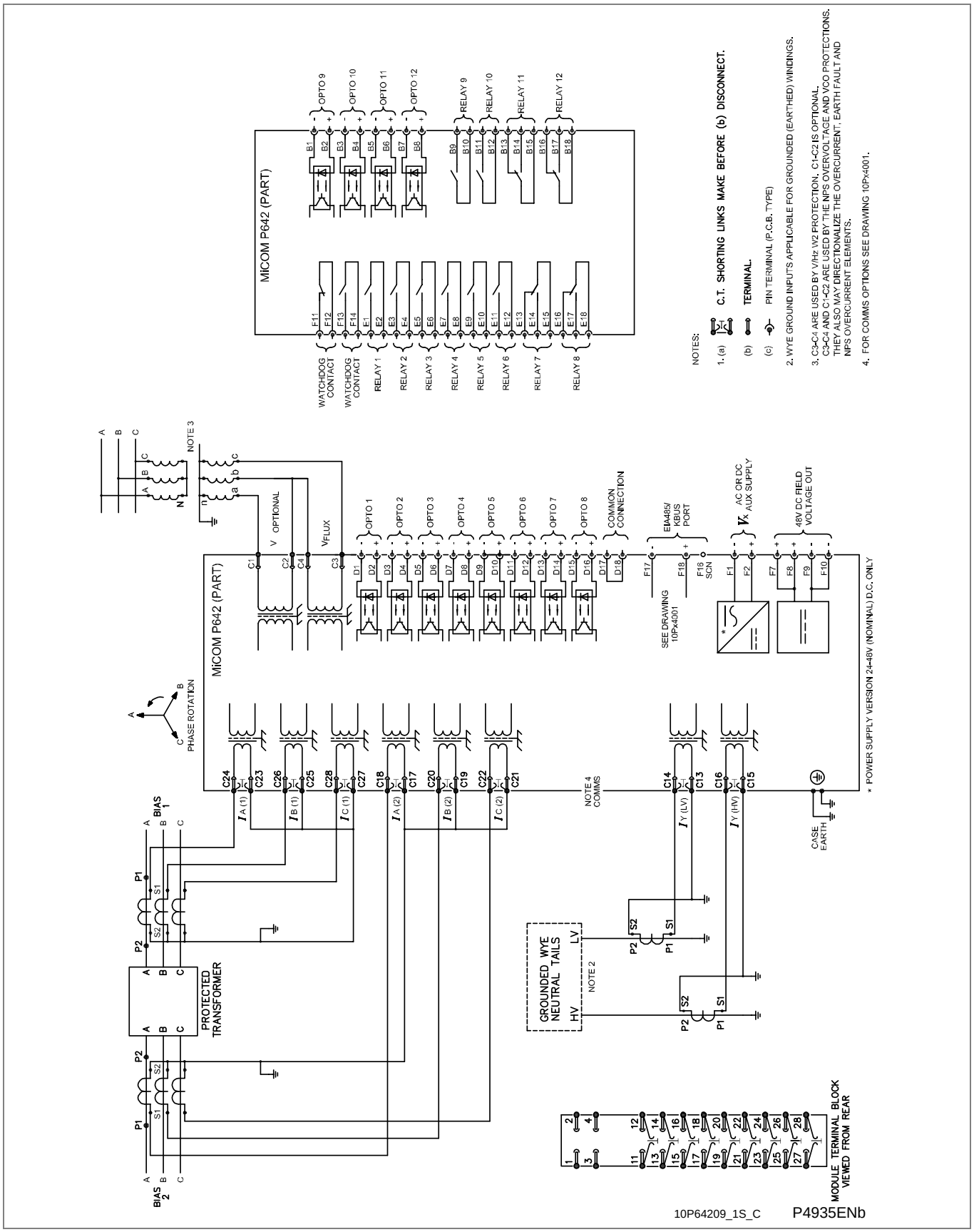


Figure 11 - Two bias ITD (12 I/P & 12 O/P) with 2P VT inputs (40TE)

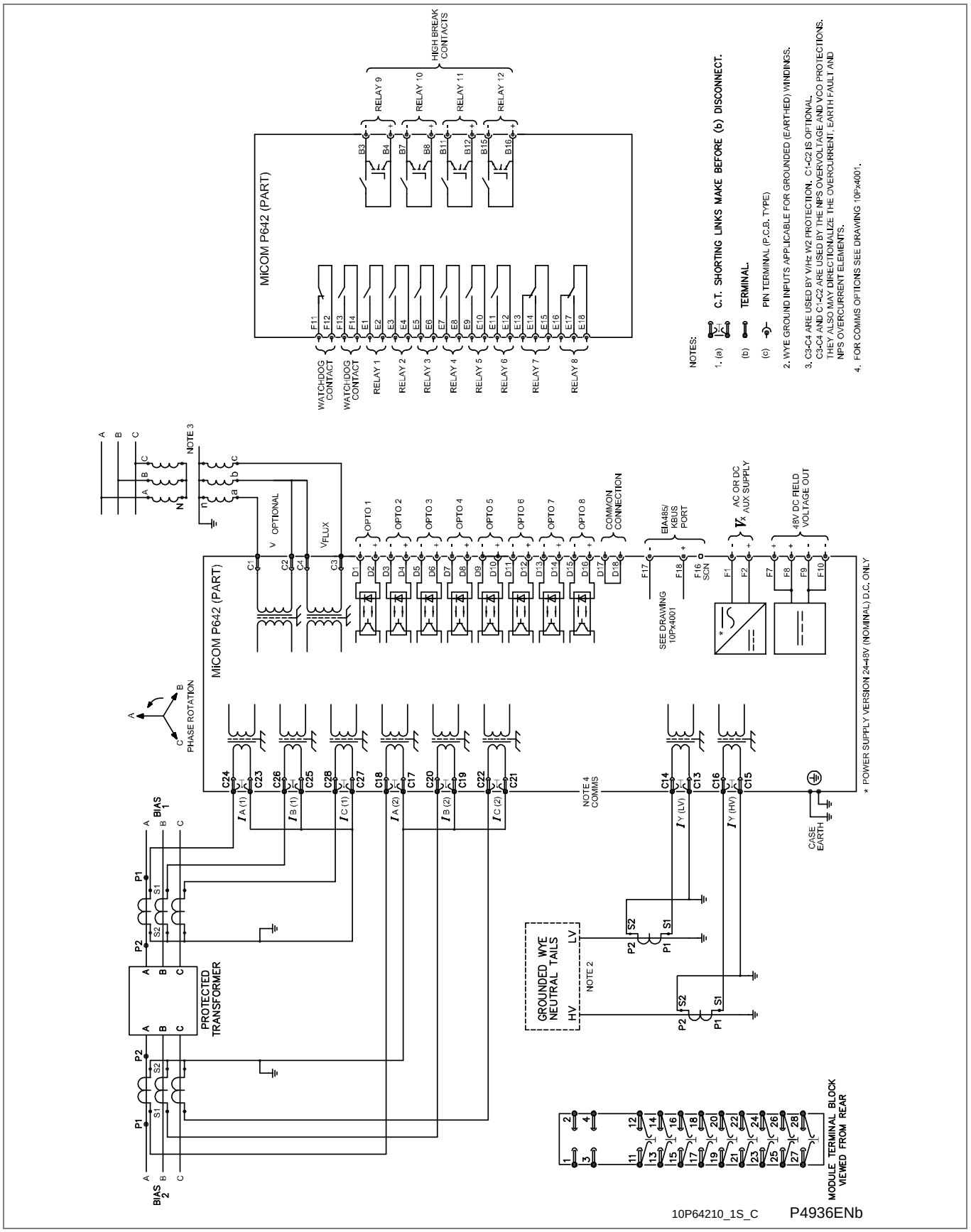


Figure 12 - Two bias ITD (8 I/P & 12 O/P) with 2P inputs (40TE)

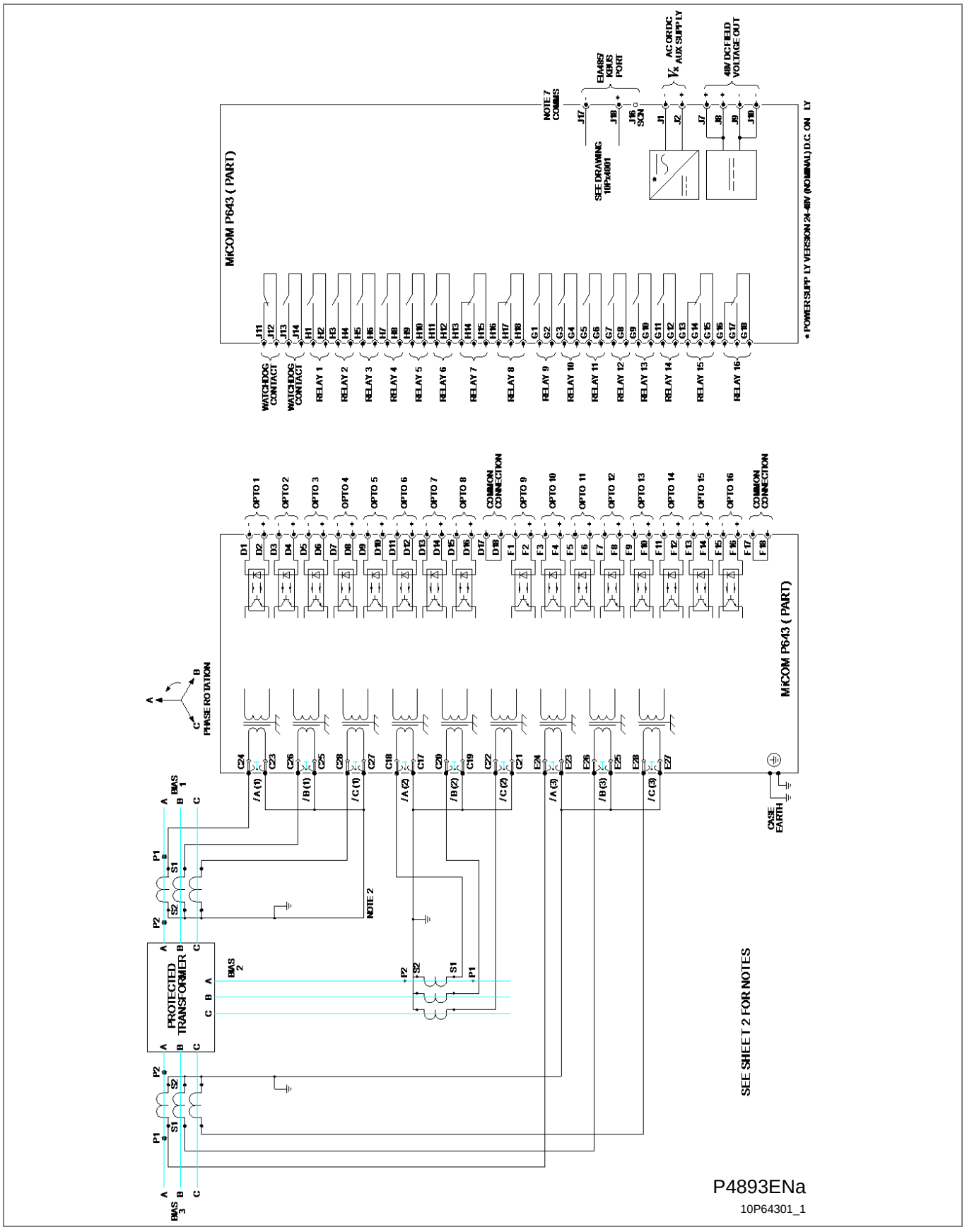


Figure 13 - Three bias ITD (16 I/P & 16 O/P) with 4P VT inputs (60TE)

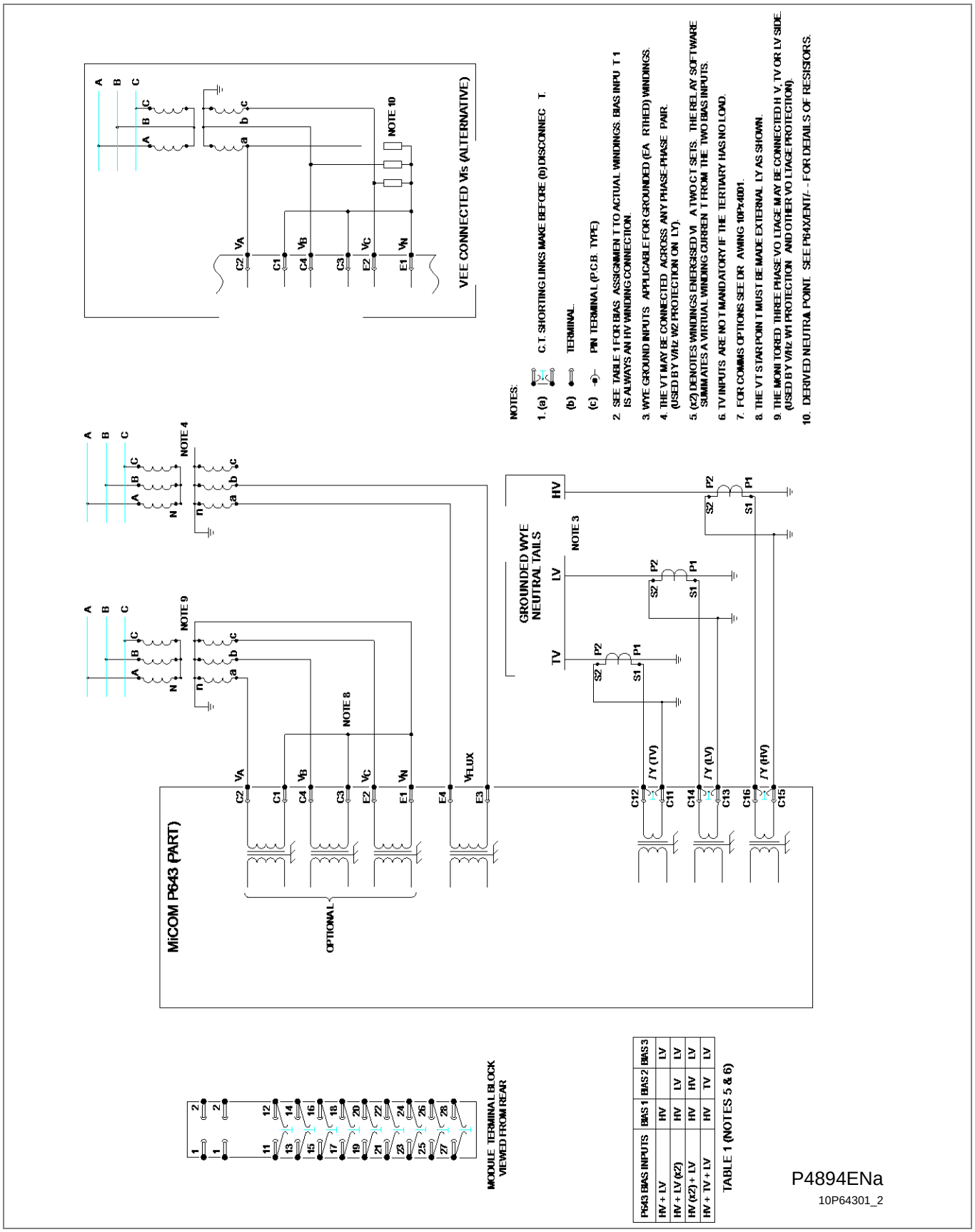


Figure 14 - Three bias ITD (16 I/P & 16 O/P) with 4P VT inputs (60TE)

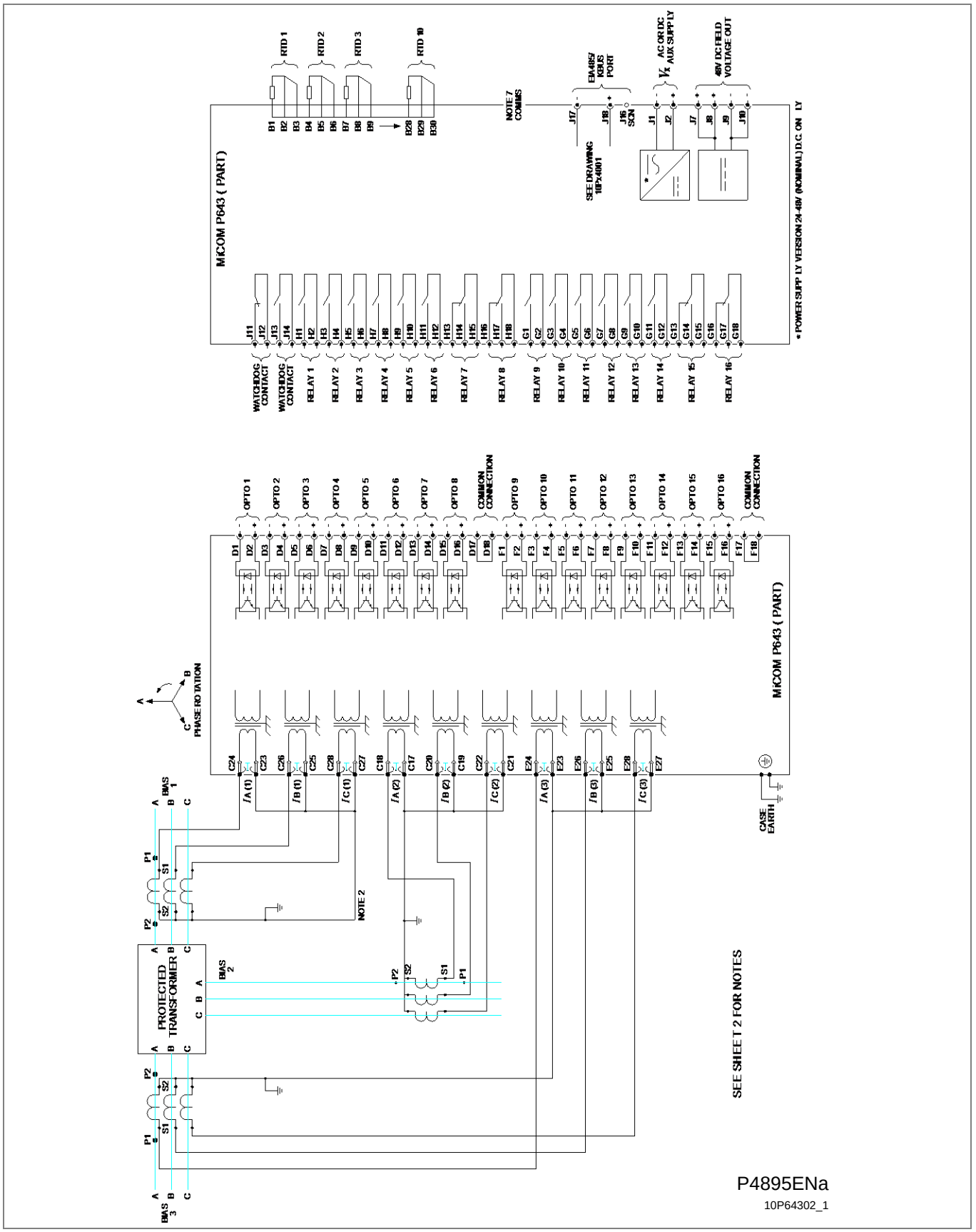


Figure 15 - Three bias ITD (16 I/P & 16 O/P + RTD) with 4P VT inputs (60TE)

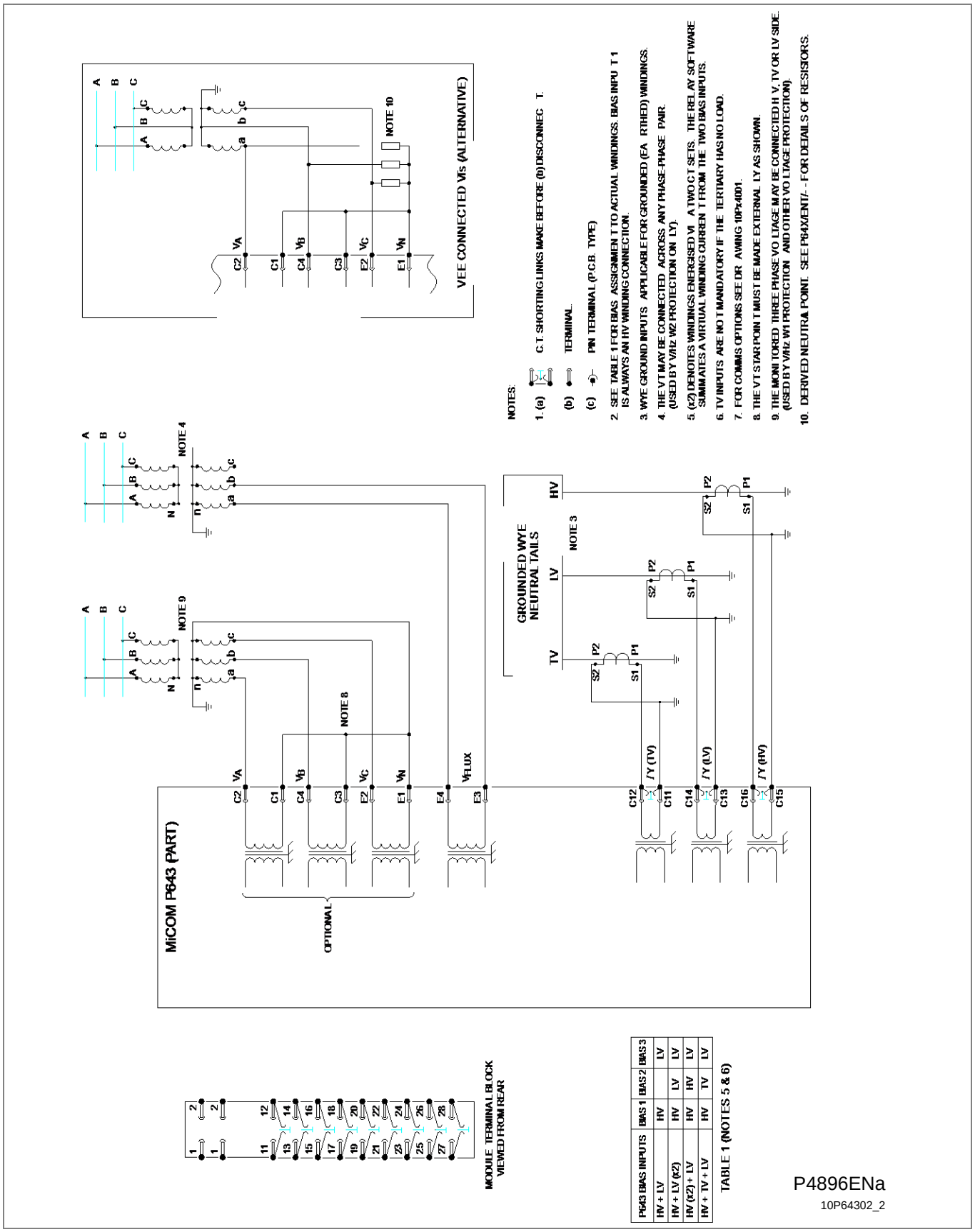


Figure 16 - Three bias ITD (16 I/P & 16 O/P + RTD) with 4P VT inputs (60TE)

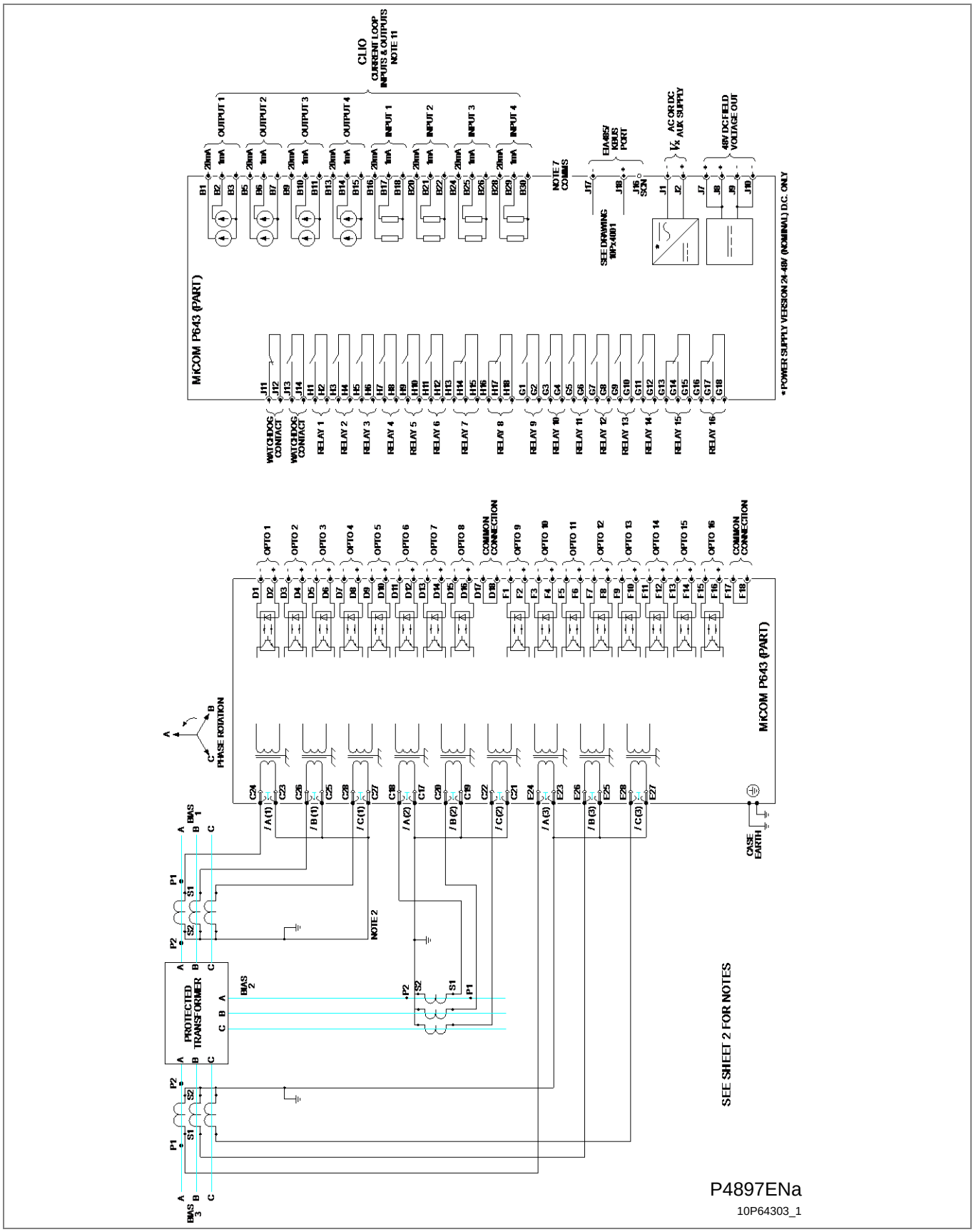


Figure 17 - Three bias ITD (16 I/P & 16 O/P + CLIO) with 4P VT inputs (60TE)

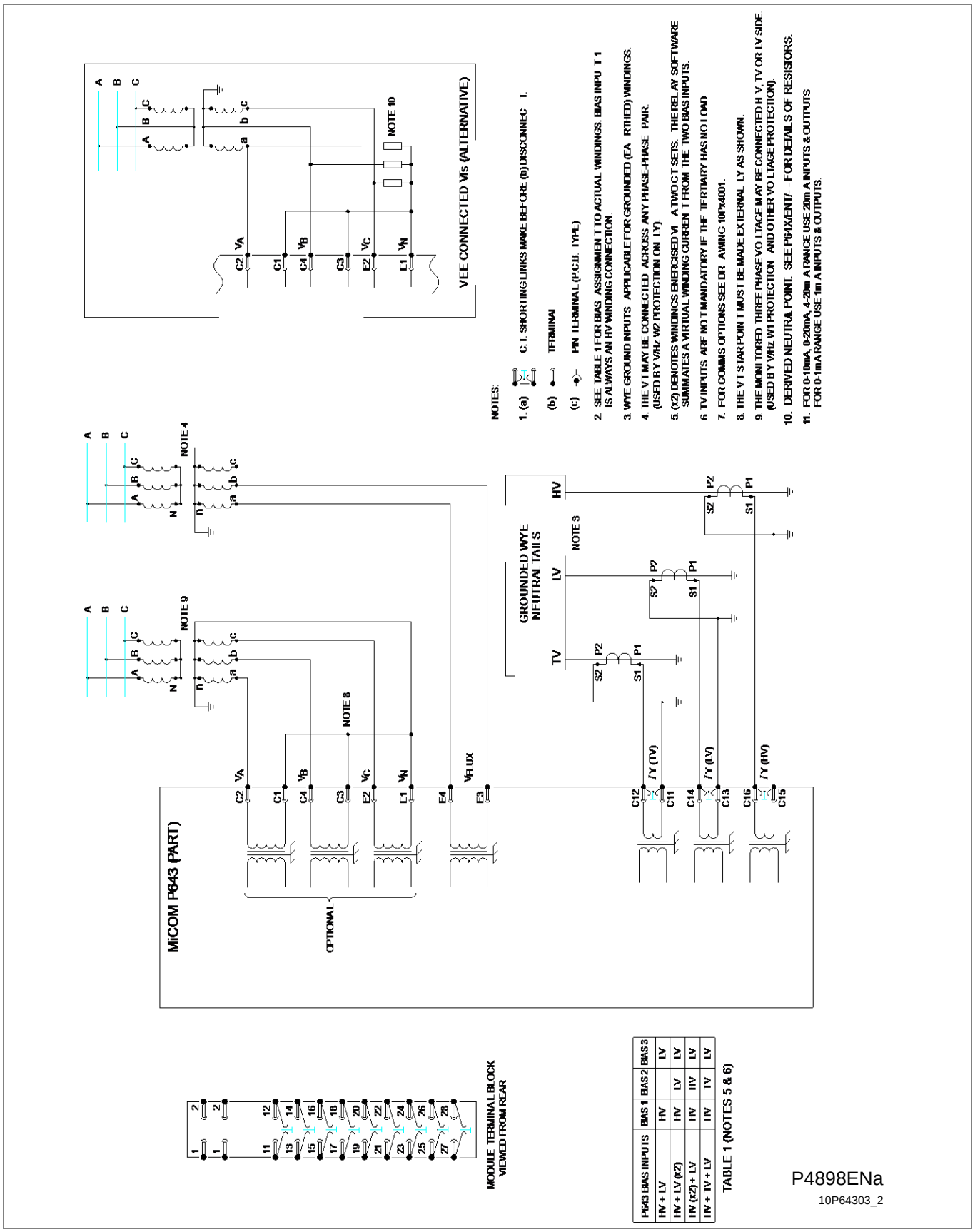


Figure 18 - Three bias ITD (16 I/P & 16 O/P + CLIO) with 4P VT inputs (60TE)

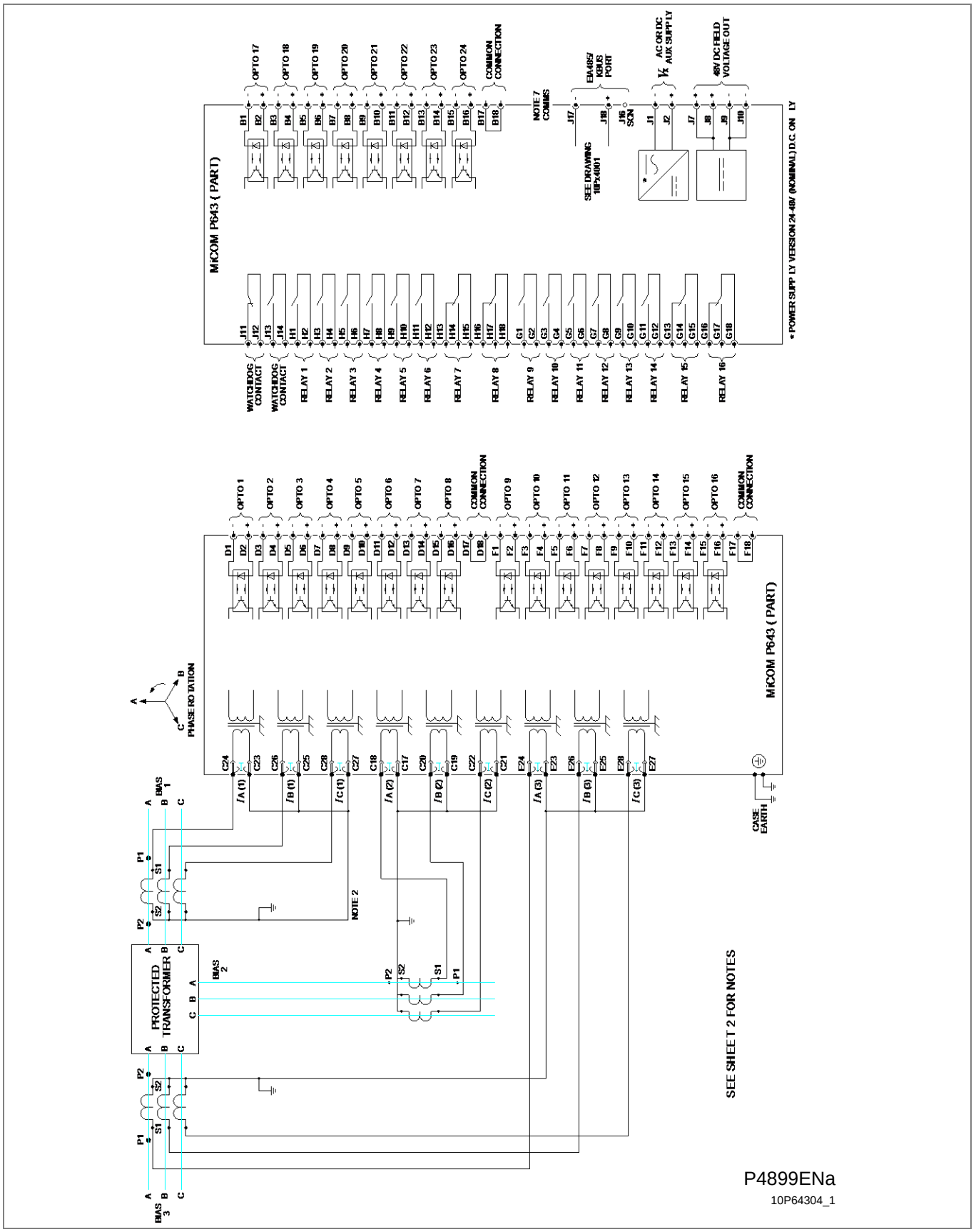


Figure 19 - Three bias ITD (24 I/P & 16 O/P) with 4P VT inputs (60TE)

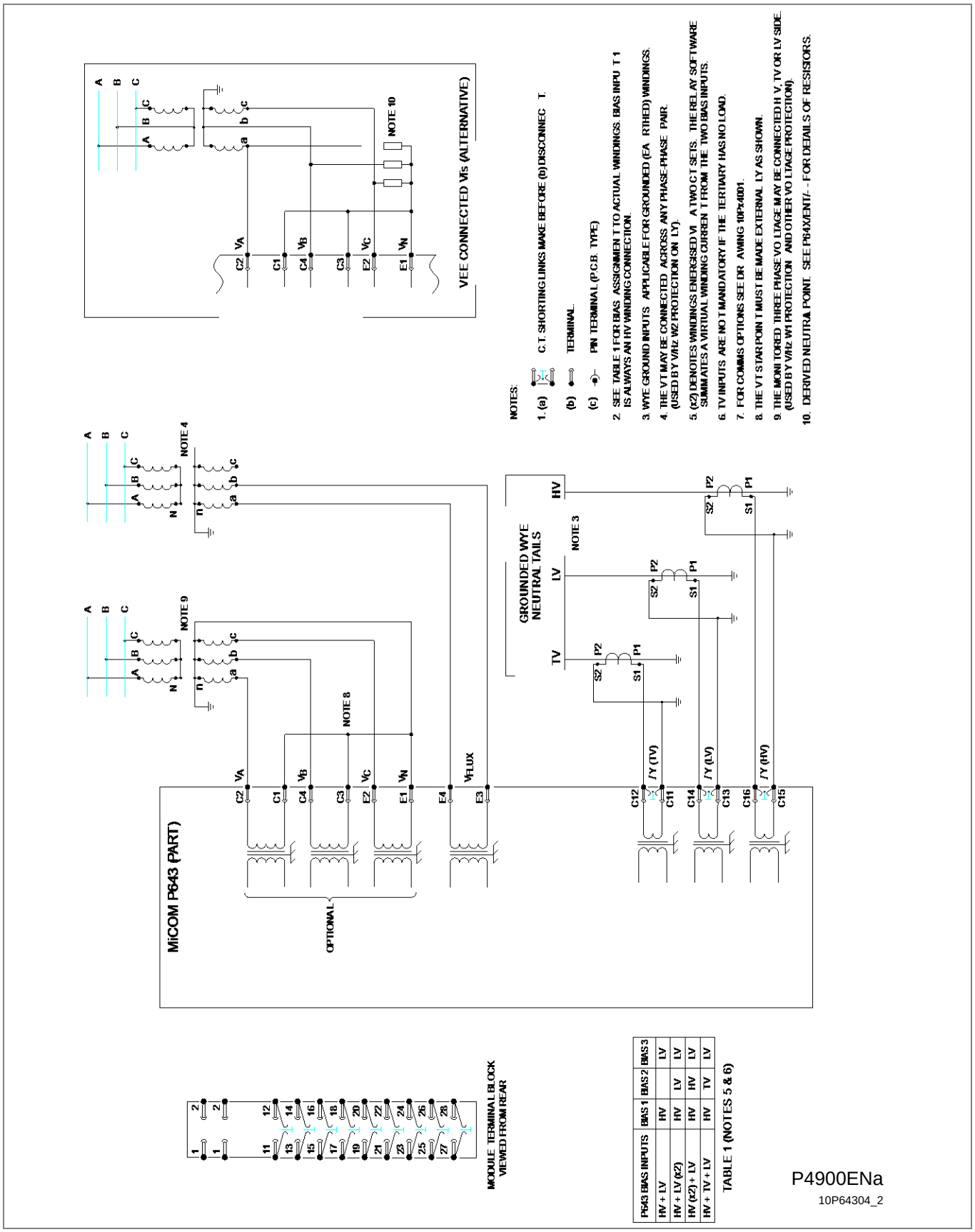


Figure 20 - Three bias ITD (24 I/P & 16 O/P) with 4P VT inputs (60TE)

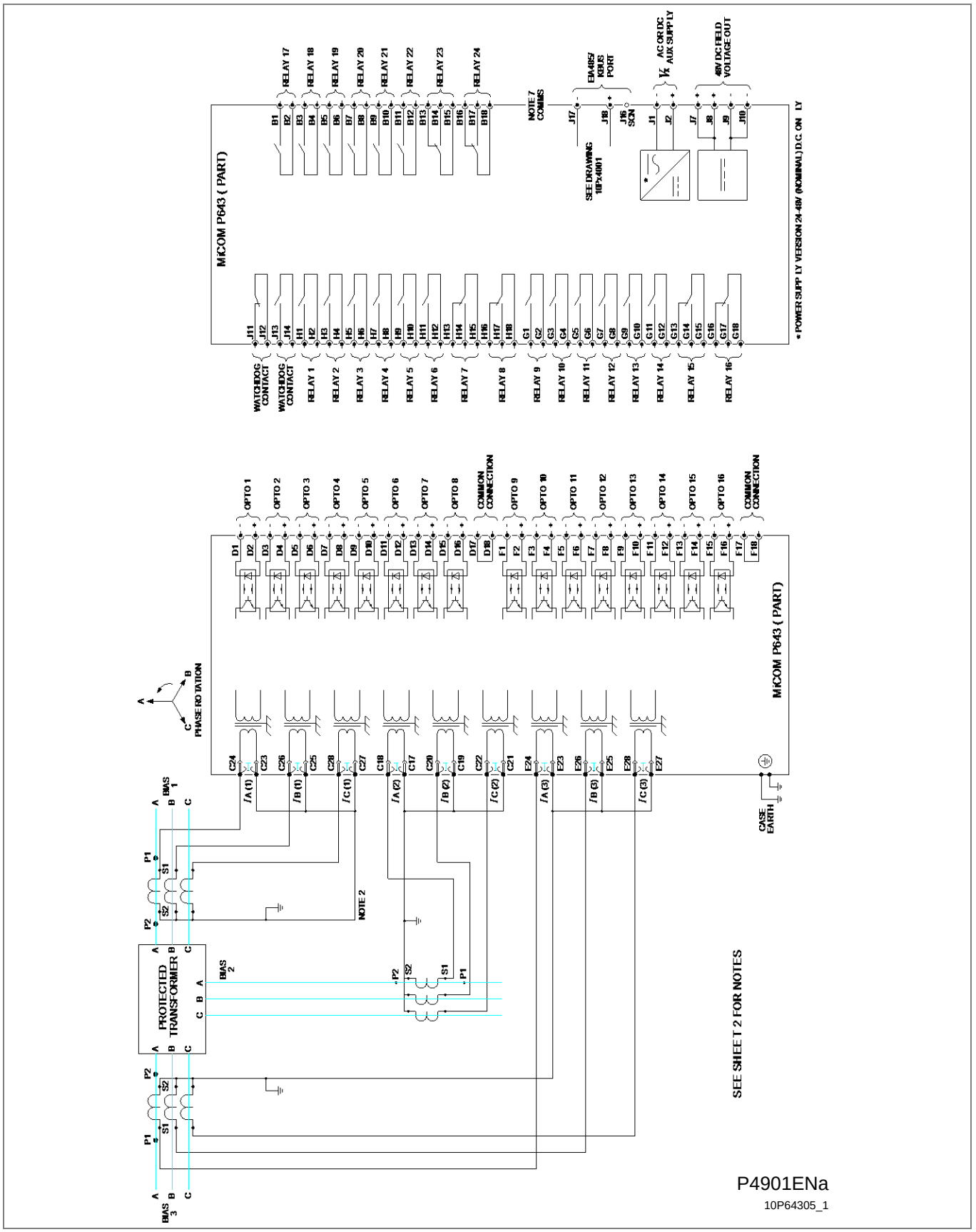


Figure 21 - Three bias ITD (16 I/P & 24 O/P) with 4P VT inputs (60TE)

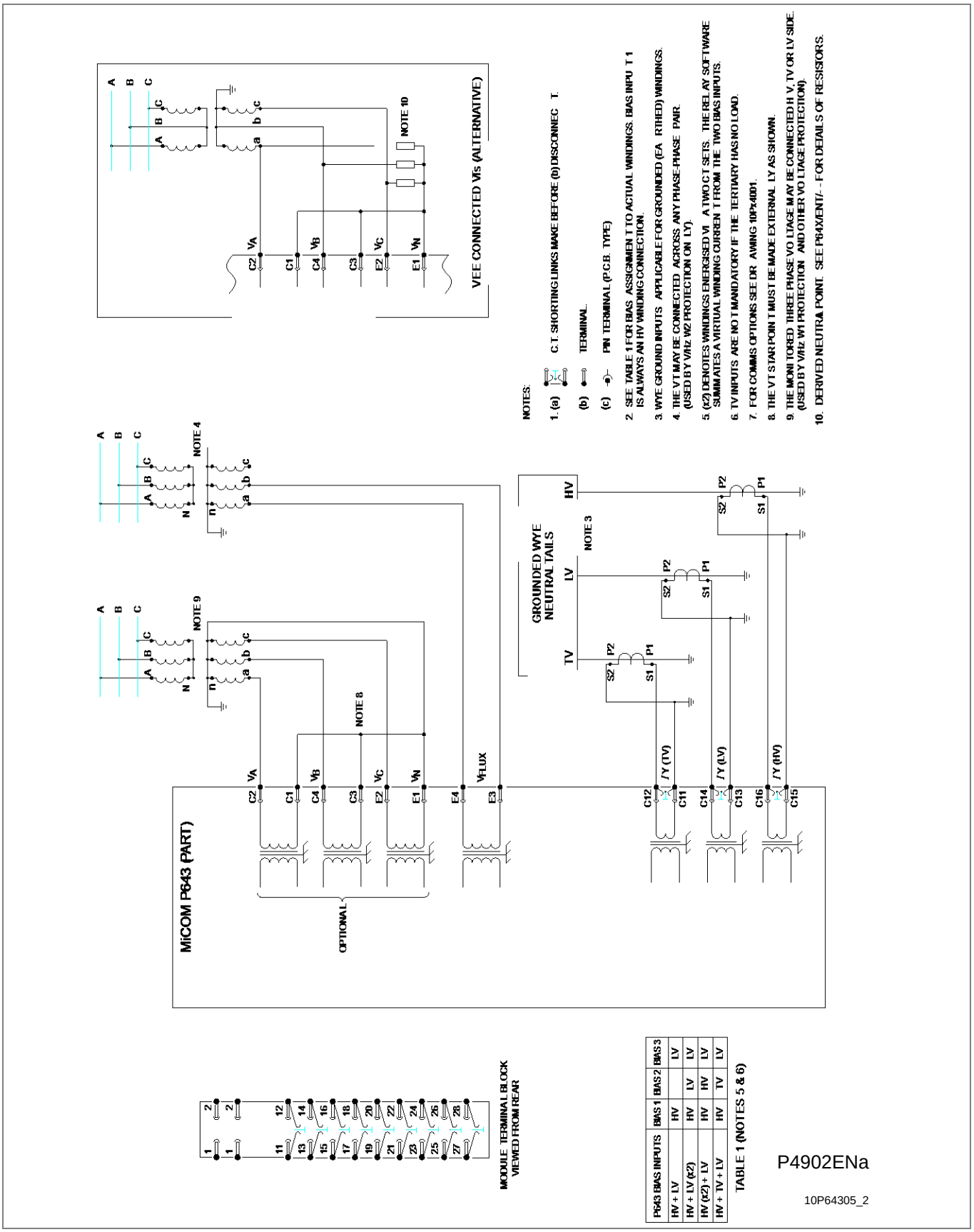


Figure 22 - Three bias ITD (16 I/P & 24 O/P) with 4P VT inputs (60TE)

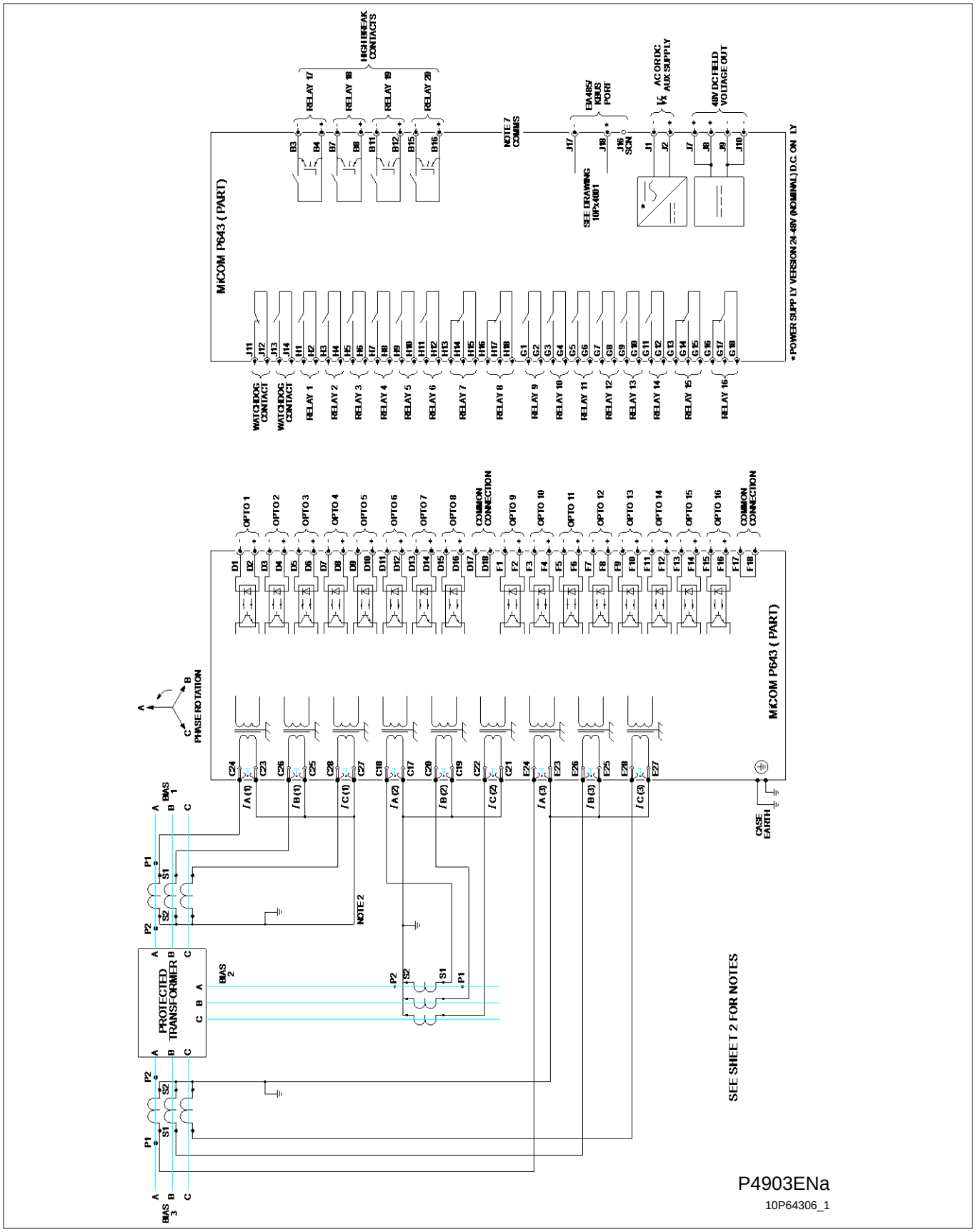


Figure 23 - Three bias ITD (16 I/P & 20 O/P) with 4P VT input (60TE)

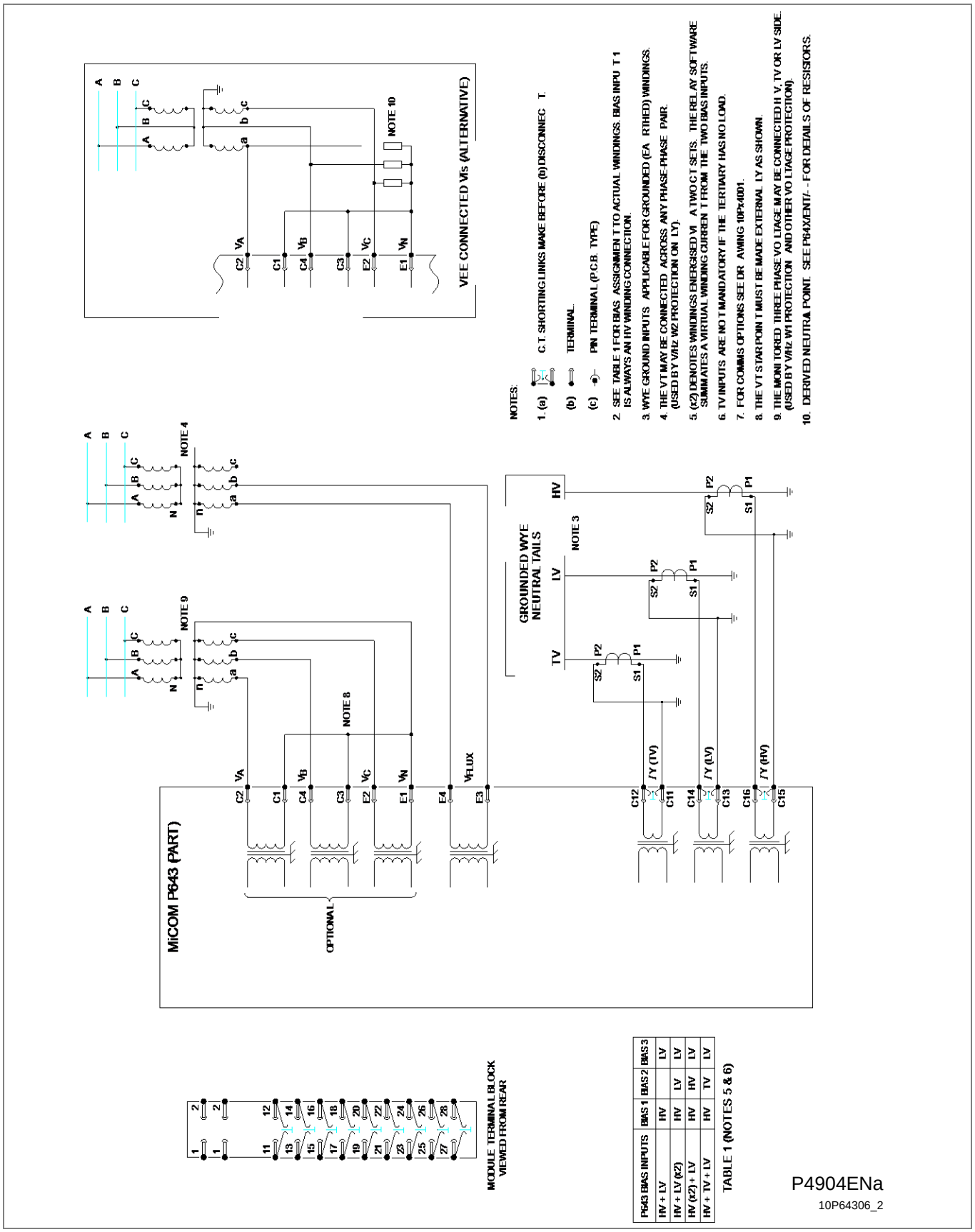


Figure 24 - Three bias ITD (16 I/P & 20 O/P) with 4P VT input (60TE)

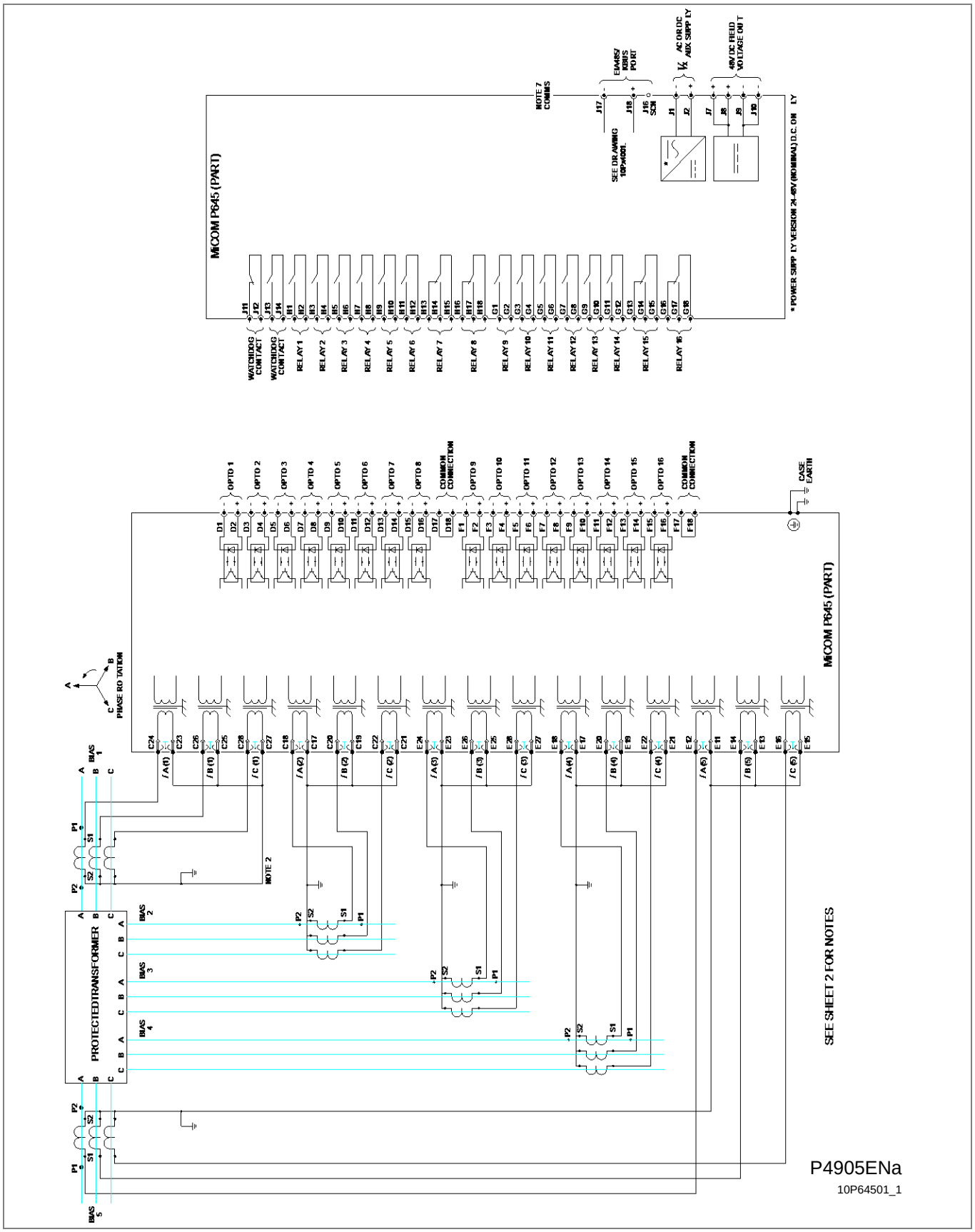
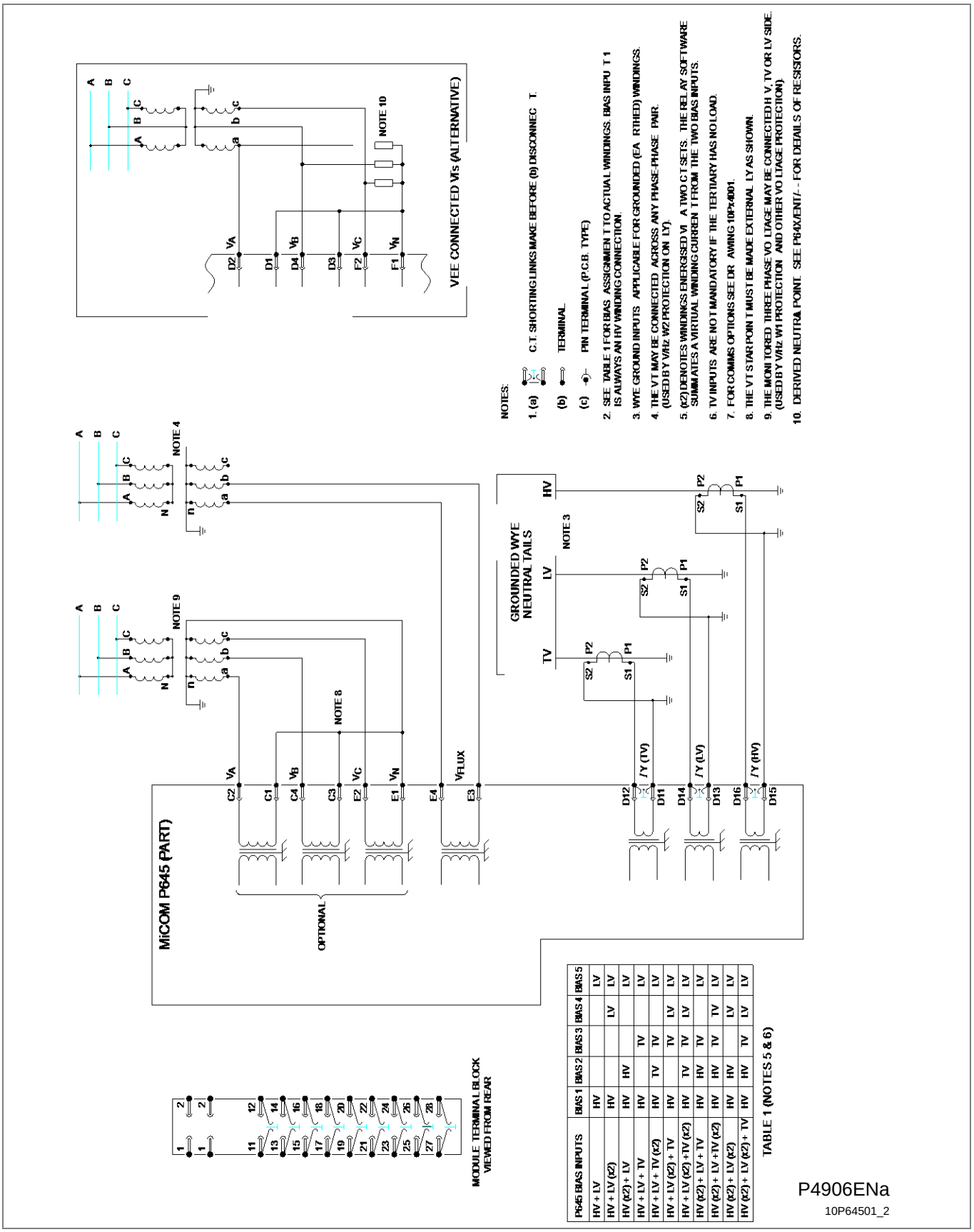


Figure 25 - Five bias ITD (16 I/P & 16 O/P) with 4P VT inputs (60TE)



P645 BIAS INPUTS	BIAS 1	BIAS 2	BIAS 3	BIAS 4	BIAS 5
HV + LV	HV				LV
HV + LV (x2)	HV			LV	LV
HV (x2) + LV	HV	HV			LV
HV + LV + TV	HV		TV		LV
HV + LV + TV (x2)	HV	TV	TV		LV
HV + LV (x2) + TV	HV		TV	LV	LV
HV + LV (x2) +TV (x2)	HV	TV	TV	LV	LV
HV (x2) + LV + TV	HV	HV	TV		LV
HV (x2) + LV +TV (x2)	HV	HV	TV	TV	LV
HV (x2) + LV (x2)	HV	HV		LV	LV
HV (x2) + LV (x2) + TV	HV	HV	TV	LV	LV

Figure 26 - Five bias ITD (16 I/P & 16 O/P) with 4P VT inputs (60TE)

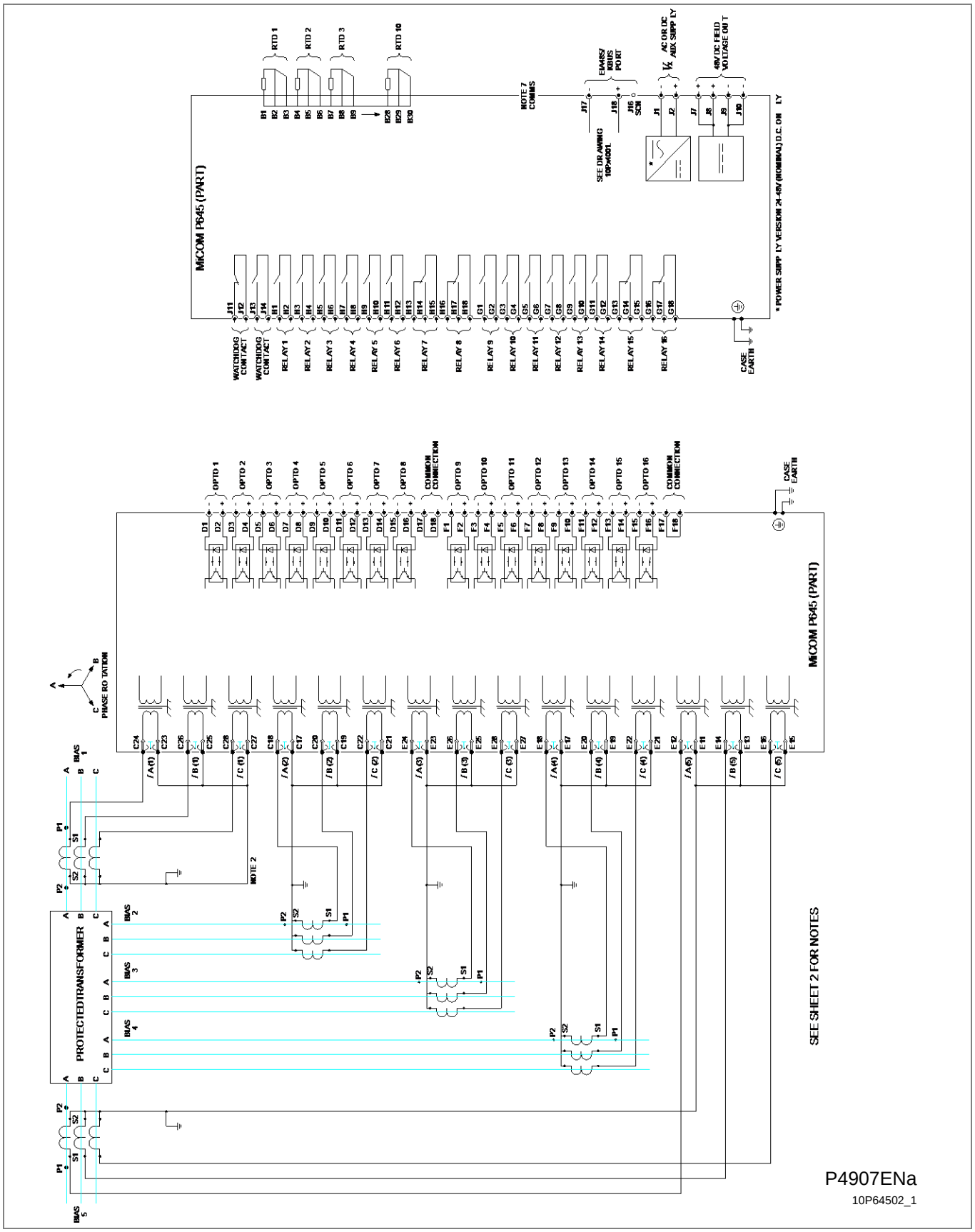
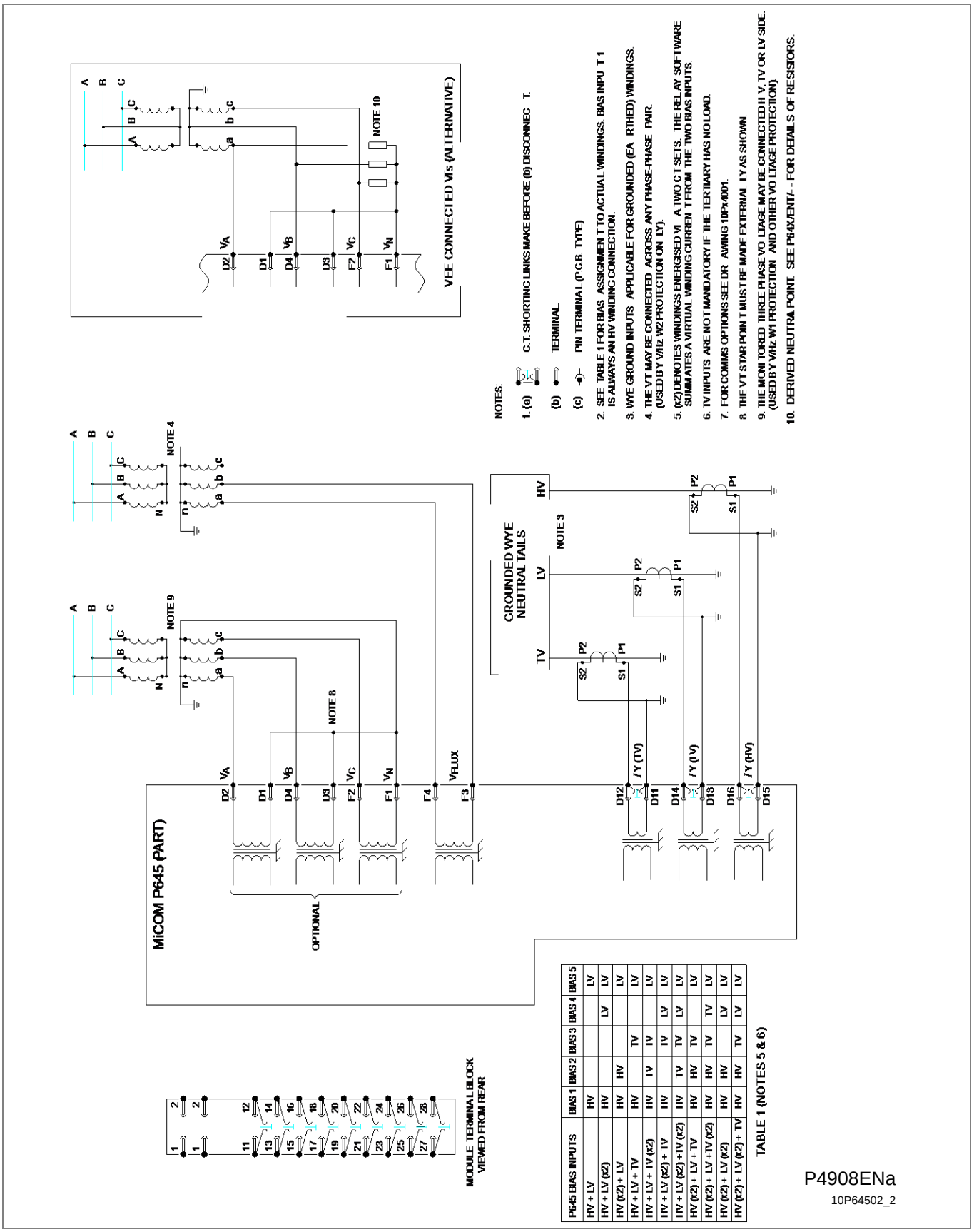


Figure 27 - Five bias ITD (16 I/P & 16 O/P + RTD) with 4P VT inputs (60TE)



P645 BIAS INPUTS	BIAS 1	BIAS 2	BIAS 3	BIAS 4	BIAS 5
HV + LV	HV				LV
HV + LV (x2)	HV			LV	LV
HV (x2) + LV	HV	HV			LV
HV + LV + TV	HV		TV		LV
HV + LV + TV (x2)	HV	TV	TV		LV
HV + LV (x2) + TV	HV		TV	LV	LV
HV + LV (x2) +TV (x2)	HV	TV	TV	LV	LV
HV (x2) + LV + TV	HV	HV	TV		LV
HV (x2) + LV +TV (x2)	HV	HV	TV	TV	LV
HV (x2) + LV (x2)	HV	HV		LV	LV
HV (x2) + LV (x2) + TV	HV	HV	TV	LV	LV

Figure 28 - Five bias ITD (16 I/P & 16 O/P + RTD) with 4P VT inputs (60TE)

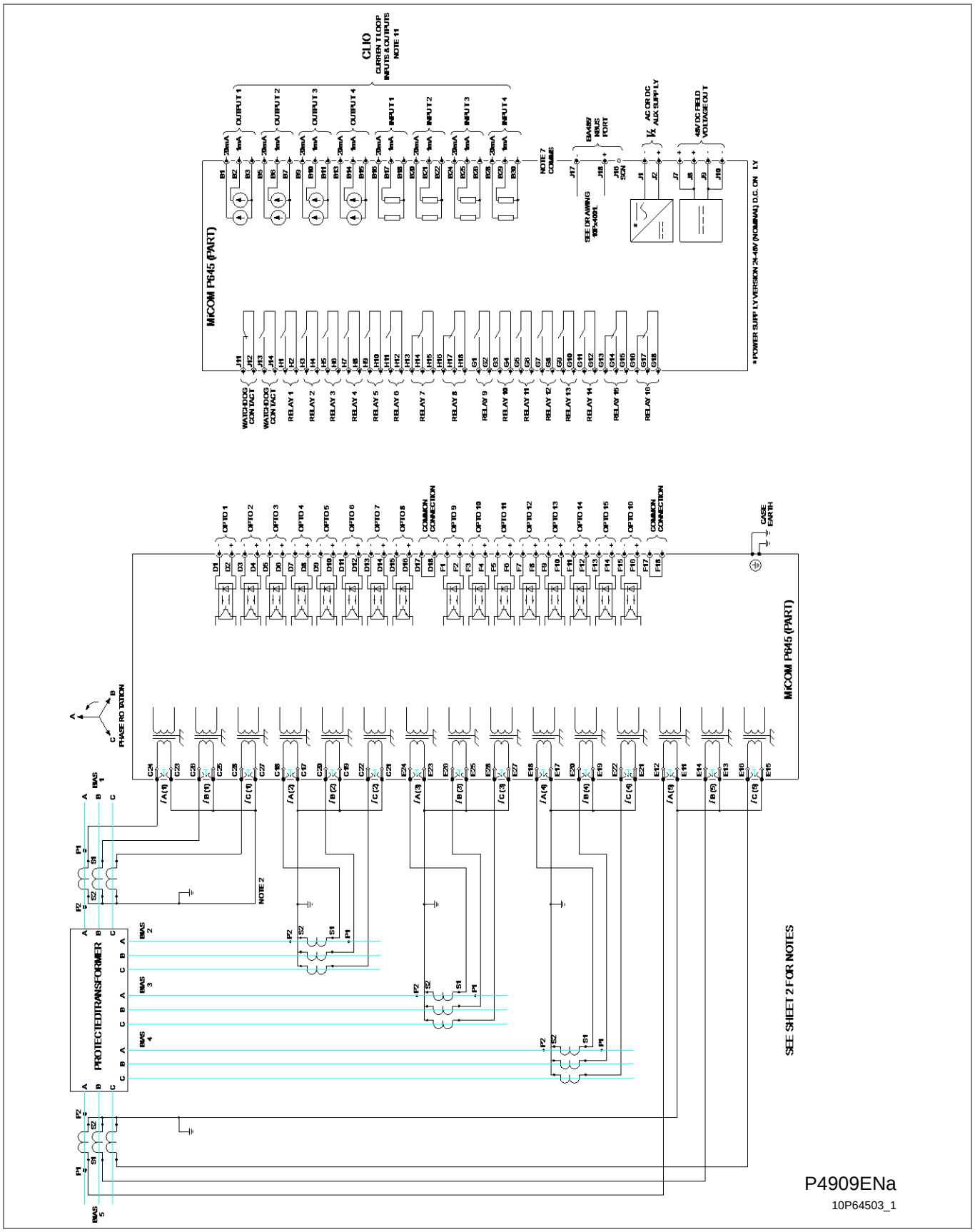
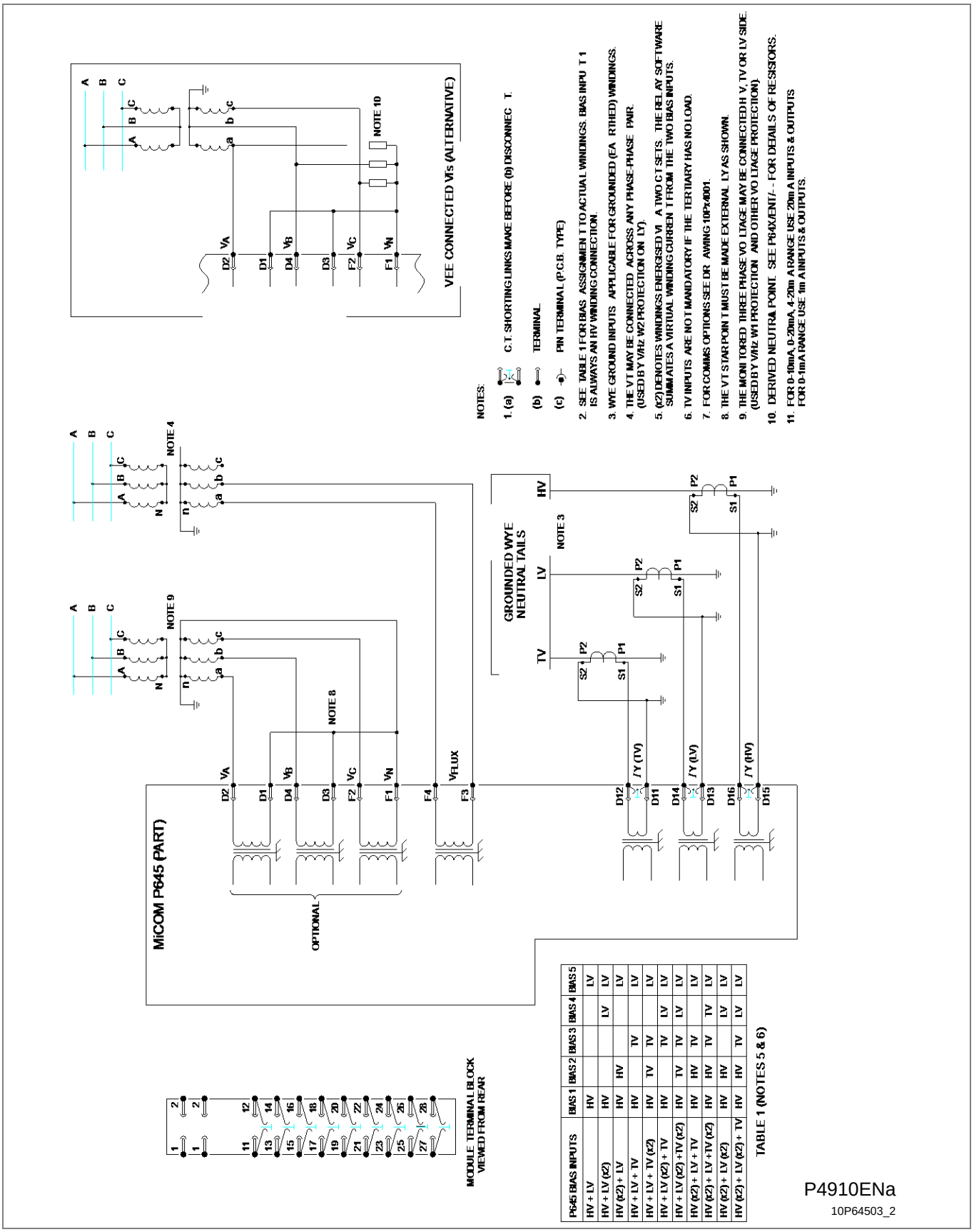


Figure 29 - Five bias ITD (16 I/P & 16 O/P + CLIO) with 4P VT inputs (60TE)



P645 BIAS INPUTS	BIAS 1	BIAS 2	BIAS 3	BIAS 4	BIAS 5
HV + LV	HV				LV
HV + LV (x2)	HV			LV	LV
HV (x2) + LV	HV	HV			LV
HV + LV + TV	HV		TV		LV
HV + LV + TV (x2)	HV	TV	TV		LV
HV + LV (x2) + TV	HV		TV	LV	LV
HV + LV (x2) +TV (x2)	HV	TV	TV	LV	LV
HV (x2) + LV + TV	HV	HV	TV		LV
HV (x2) + LV +TV (x2)	HV	HV	TV	TV	LV
HV (x2) + LV (x2)	HV	HV		LV	LV
HV (x2) + LV (x2) + TV	HV	HV	TV	LV	LV

Figure 30 - Five bias ITD (16 I/P & 16 O/P + CLIO) with 4P VT inputs (60TE)

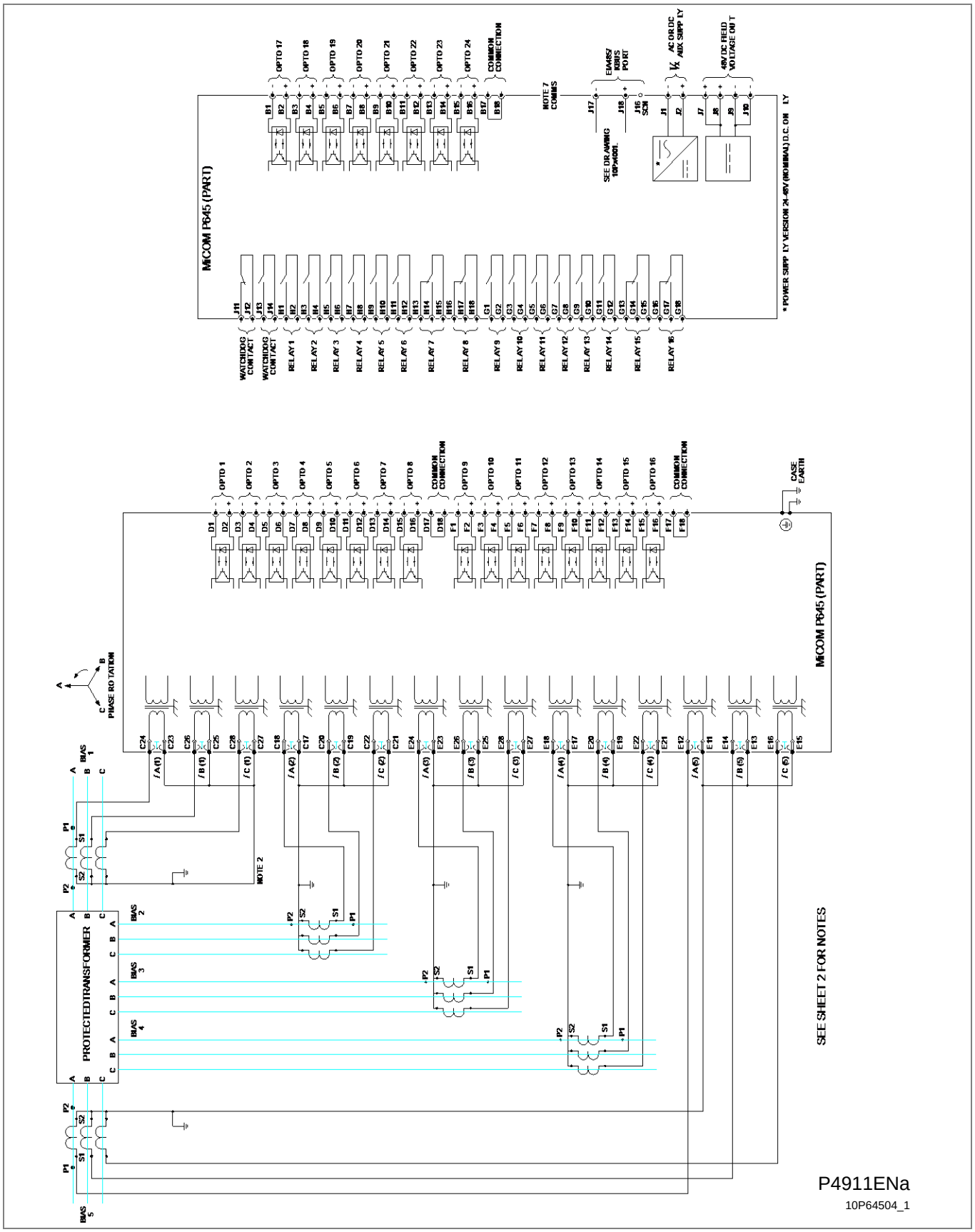
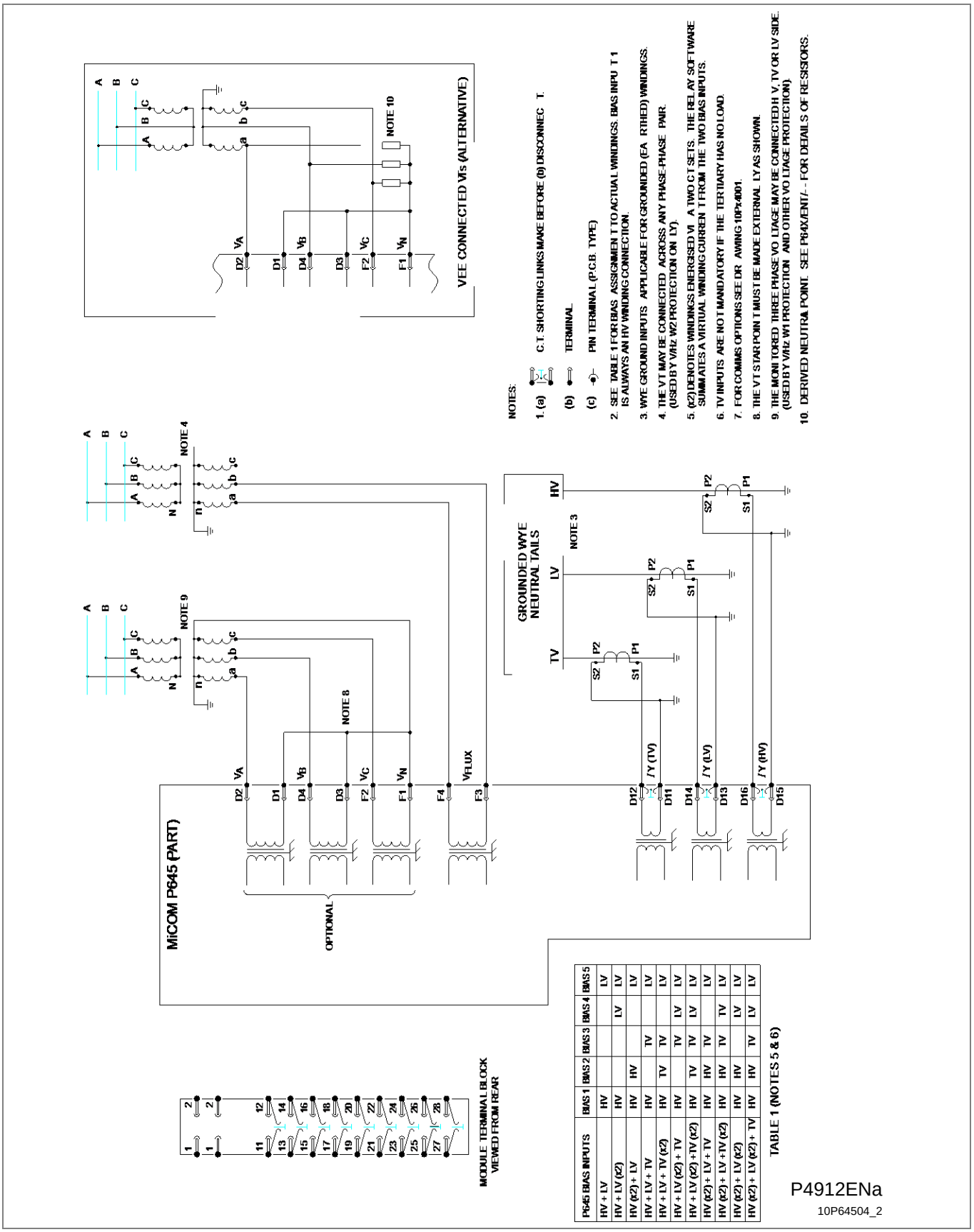


Figure 31 - Five bias ITD (24 I/P & 16 O/P) with 4P VT inputs (60TE)



P645 BIAS INPUTS	BIAS 1	BIAS 2	BIAS 3	BIAS 4	BIAS 5
HV + LV	HV				LV
HV + LV (x2)	HV			LV	LV
HV (x2) + LV	HV	HV			LV
HV + LV + TV	HV		TV		LV
HV + LV + TV (x2)	HV	TV	TV		LV
HV + LV (x2) + TV	HV		TV	LV	LV
HV + LV (x2) +IV (x2)	HV	TV	TV	LV	LV
HV (x2) + LV + TV	HV	HV	TV		LV
HV (x2) + LV +IV (x2)	HV	HV	TV	TV	LV
HV (x2) + LV (x2)	HV	HV		LV	LV
HV (x2) + LV (x2) + TV	HV	HV	TV	LV	LV

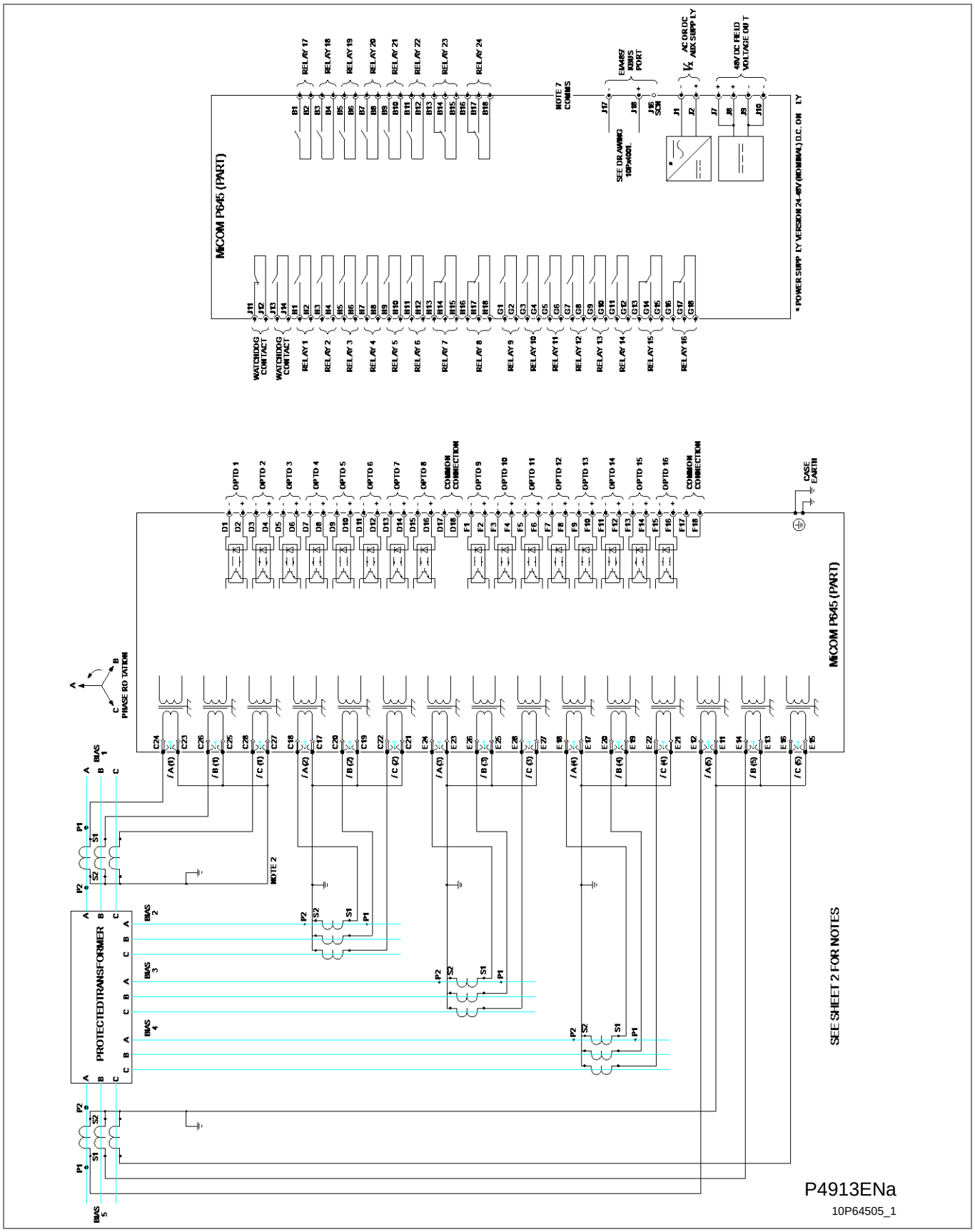
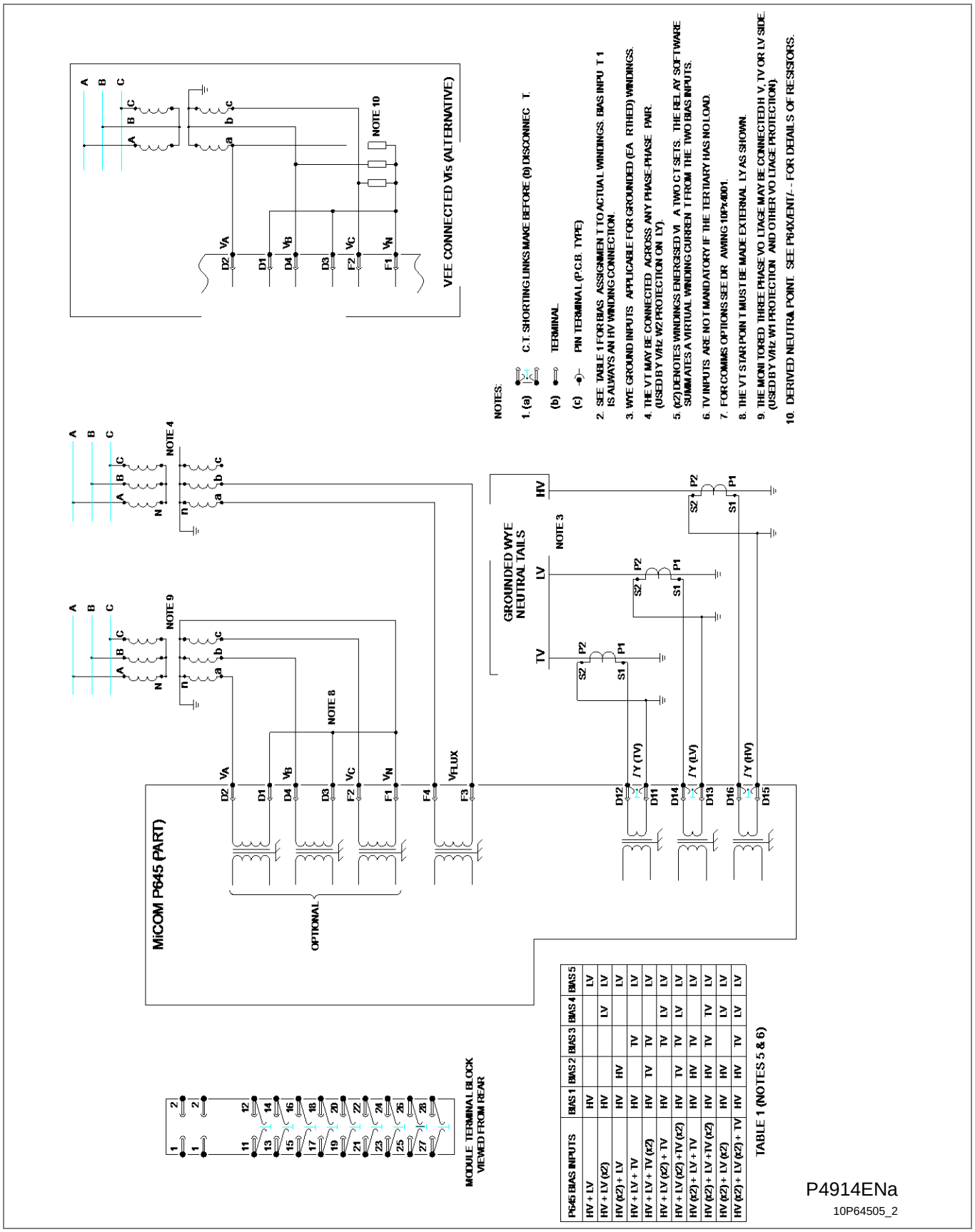


Figure 33 - Five bias ITD (16 I/O & 24 O/P) with 4P VT inputs (60TE)



P645 BIAS INPUTS	BIAS 1	BIAS 2	BIAS 3	BIAS 4	BIAS 5
HV + LV	HV				LV
HV + LV (x2)	HV			LV	LV
HV (x2) + LV	HV	HV			LV
HV + LV + TV	HV		TV		LV
HV + LV + TV (x2)	HV	TV	TV		LV
HV + LV (x2) + TV	HV		TV	LV	LV
HV + LV (x2) +TV (x2)	HV	TV	TV	LV	LV
HV (x2) + LV + TV	HV	HV	TV		LV
HV (x2) + LV +TV (x2)	HV	HV	TV	TV	LV
HV (x2) + LV (x2)	HV	HV		LV	LV
HV (x2) + LV (x2) + TV	HV	HV	TV	LV	LV

Figure 34 - Five bias ITD (16 I/P & 24 O/P) with 4P VT inputs (60TE)

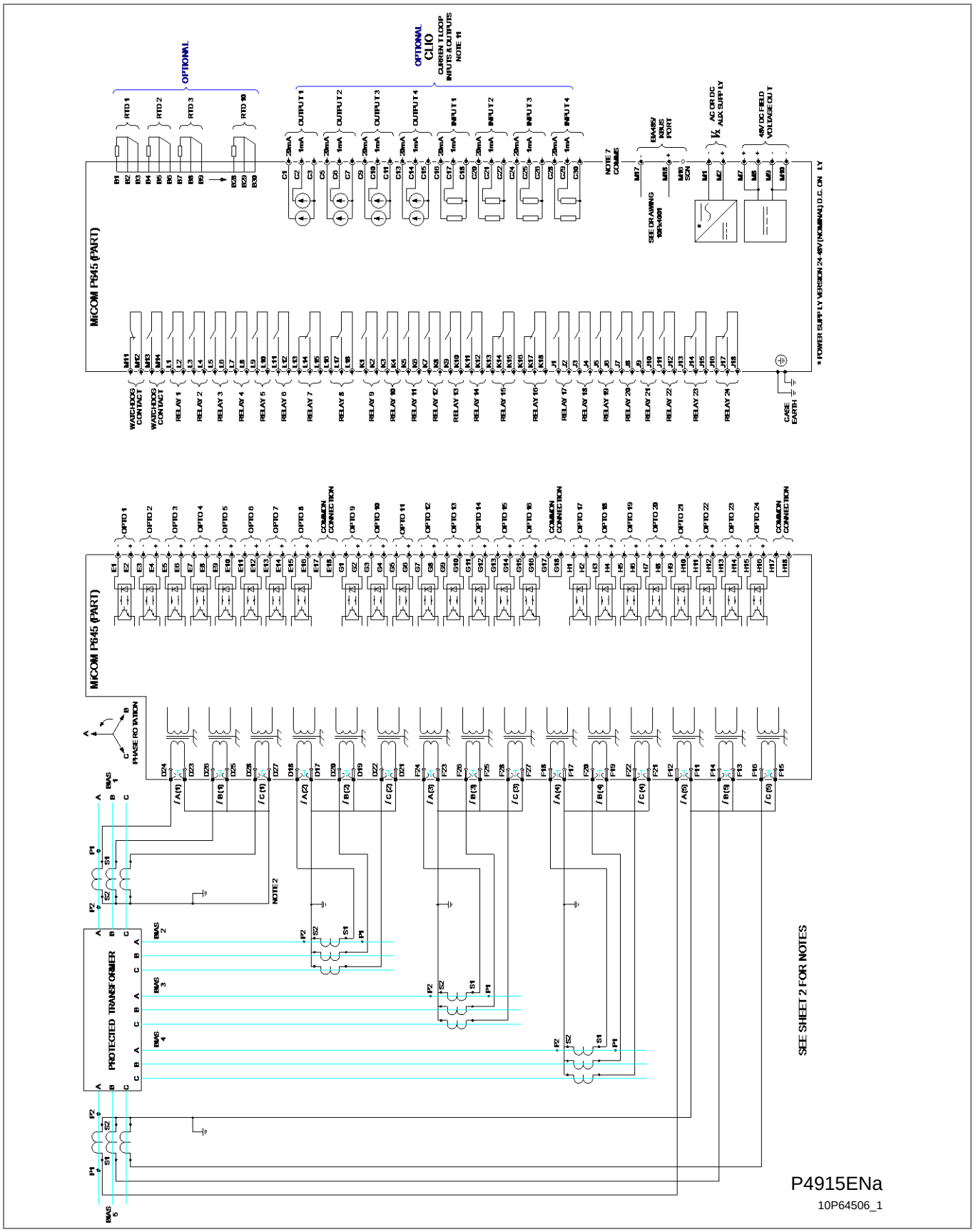
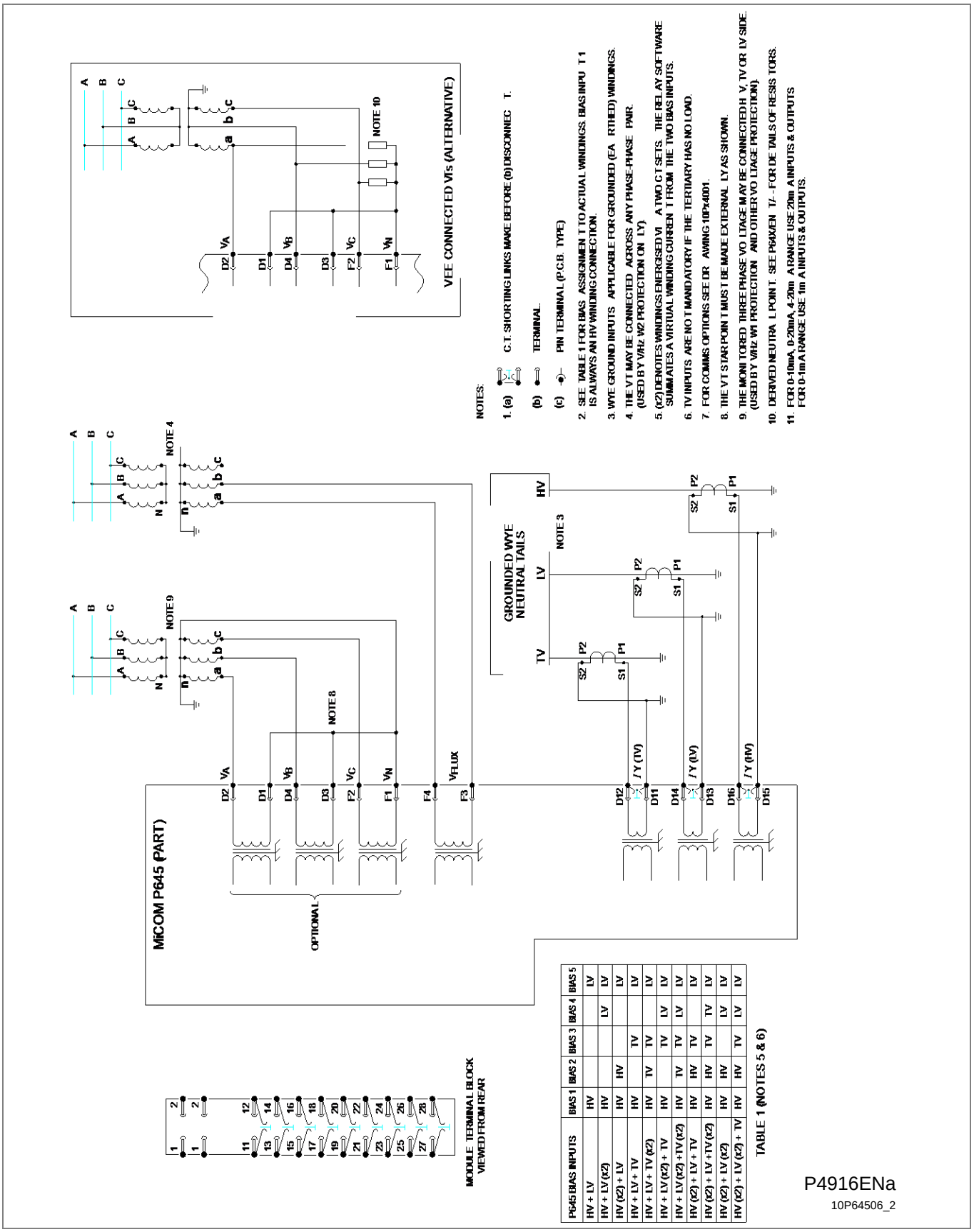


Figure 35 - Five bias ITD (24 I/P & 24 O/P + CLIO & RTD) with 4P VT inputs (80TE)



NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNEC T.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. SEE TABLE 1 FOR BIAS ASSIGNMEN T TO ACTUAL WINDINGS. BIAS INPU T 1 IS ALWAYS AN HV WINDING CONNECTION.
3. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EA RTHED) WINDINGS.
4. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY VAN W2 PROTECTION ON LV).
5. (x2) DENOTES WINDINGS ENERGISED VI A TWO CT SETS. THE RELAY SOFTWARE SUMMATES A VIRTUAL WINDING CURREN T FROM THE TWO BIAS INPUTS.
6. TV INPUTS ARE NOT MANDATORY IF THE TERTIARY HAS NO LOAD.
7. FOR COMMS OPTIONS SEE DR AWING 10P40D1.
8. THE VT STAR POIN T MUST BE MADE EXTERNAL LY AS SHOWN.
9. THE MONI TORED THREE PHASE VO LTAGE MAY BE CONNECTED H V, TV OR LV SIDE (USED BY VAN W1 PROTECTION AND OTHER VO LTAGE PROTECTION).
10. DERIVED NEUTRA L POINT T. SEE P642/EN TI - FOR DE TAILS OF RESIS TORS.
11. FOR 0-10mA, 0-20mA, 4-20m A RANGE USE 20m A INPUTS & OUTPUTS FOR 0-1m A RANGE USE 1m A INPUTS & OUTPUTS.

TABLE 1 (NOTES 5 & 6)

P645 BIAS INPUTS	BIAS 1	BIAS 2	BIAS 3	BIAS 4	BIAS 5
HV + LV	HV				LV
HV + LV(x2)	HV			LV	LV
HV (x2) + LV	HV	HV			LV
HV + LV + TV	HV		TV		LV
HV + LV+ TV (x2)	HV	TV	TV		LV
HV + LV(x2) + TV	HV		TV	LV	LV
HV + LV(x2) +TV(x2)	HV	TV	TV	LV	LV
HV (x2) + LV + TV	HV	HV	TV		LV
HV (x2) + LV +TV(x2)	HV	HV	TV	TV	LV
HV (x2) + LV (x2)	HV	HV		LV	LV
HV (x2) + LV (x2) + TV	HV	HV	TV	LV	LV

Figure 36 - Five bias ITD (24 I/O & 24 O/P + CLIO & RTD) with 4P VT inputs (80TE)

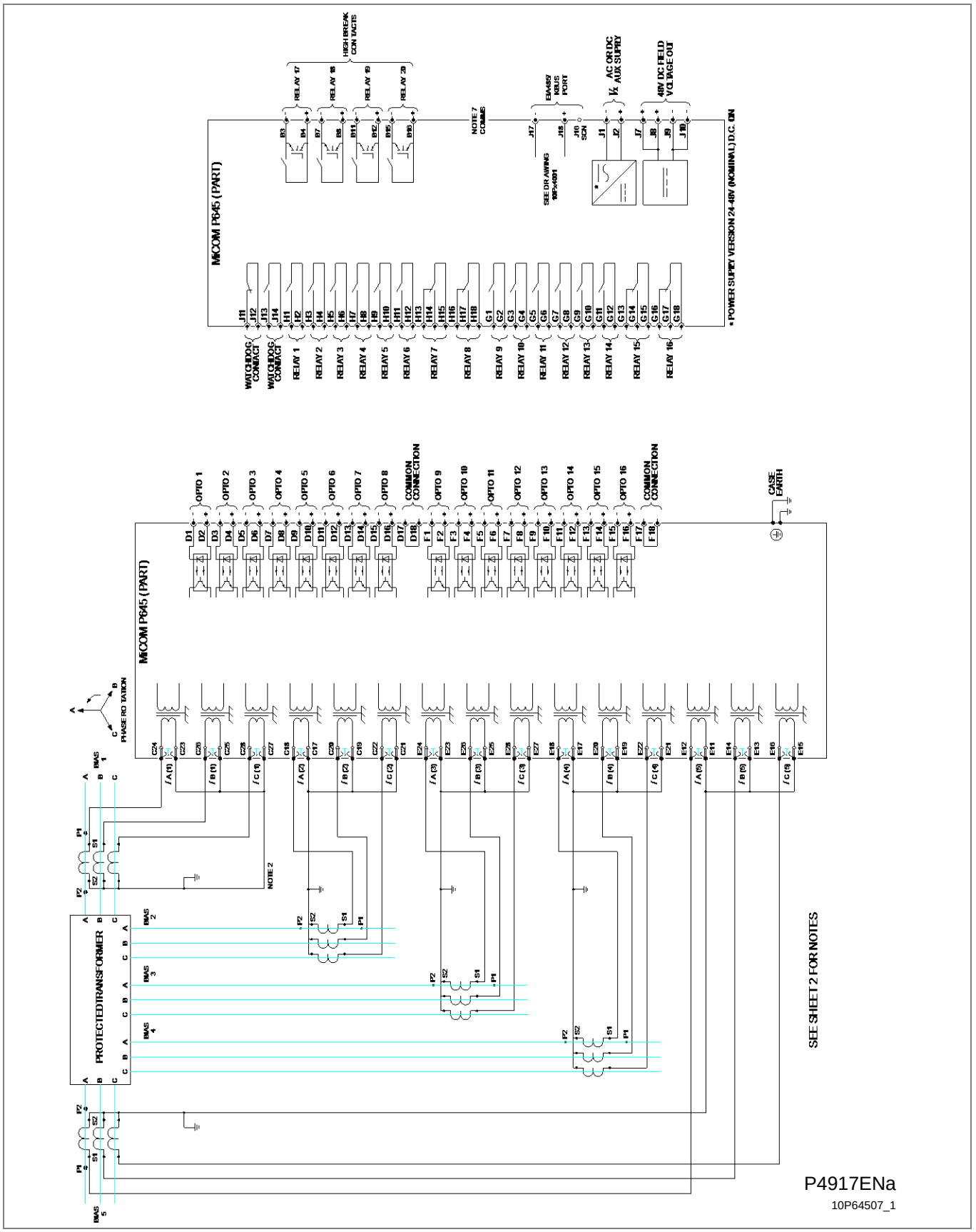
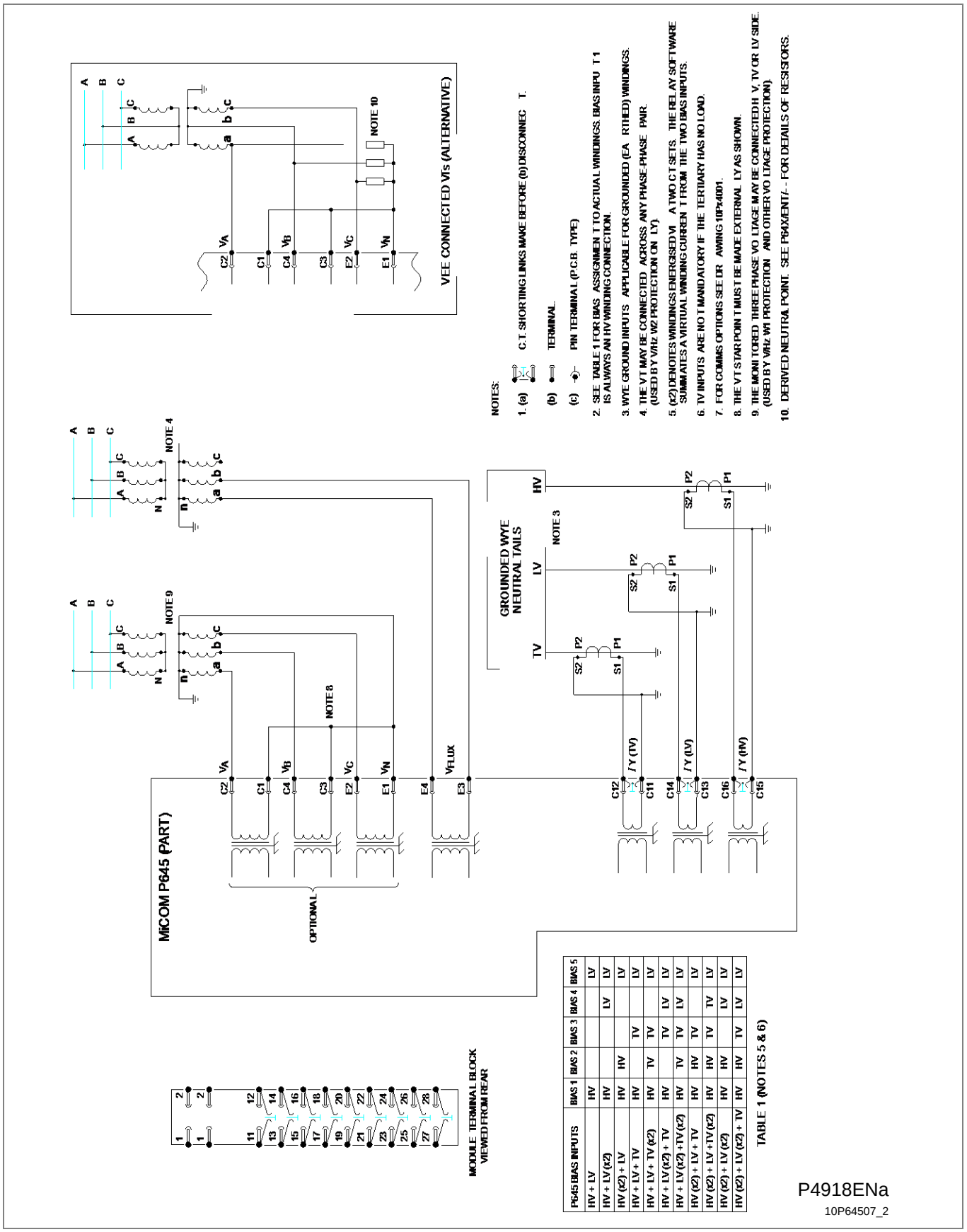


Figure 37 - Five bias ITD (24 I/P & 20 O/P) with 4P VT input (60TE)



P645 BIAS INPUTS	BIAS 1	BIAS 2	BIAS 3	BIAS 4	BIAS 5
HV + LV	HV				LV
HV + LV (x2)	HV			LV	LV
HV (x2) + LV	HV	HV			LV
HV + LV + TV	HV		TV		LV
HV + LV + TV (x2)	HV	TV	TV		LV
HV + LV (x2) + TV	HV		TV	LV	LV
HV + LV (x2) +TV(x2)	HV	TV	TV	LV	LV
HV (x2) + LV + TV	HV	HV	TV		LV
HV (x2) + LV +TV(x2)	HV	HV	TV	TV	LV
HV (x2) + LV (x2)	HV	HV		LV	LV
HV (x2) + LV (x2) + TV	HV	HV	TV	LV	LV

Figure 38 - Five bias ITD (24 I/P & 20 O/P) with 4P VT input (60TE)

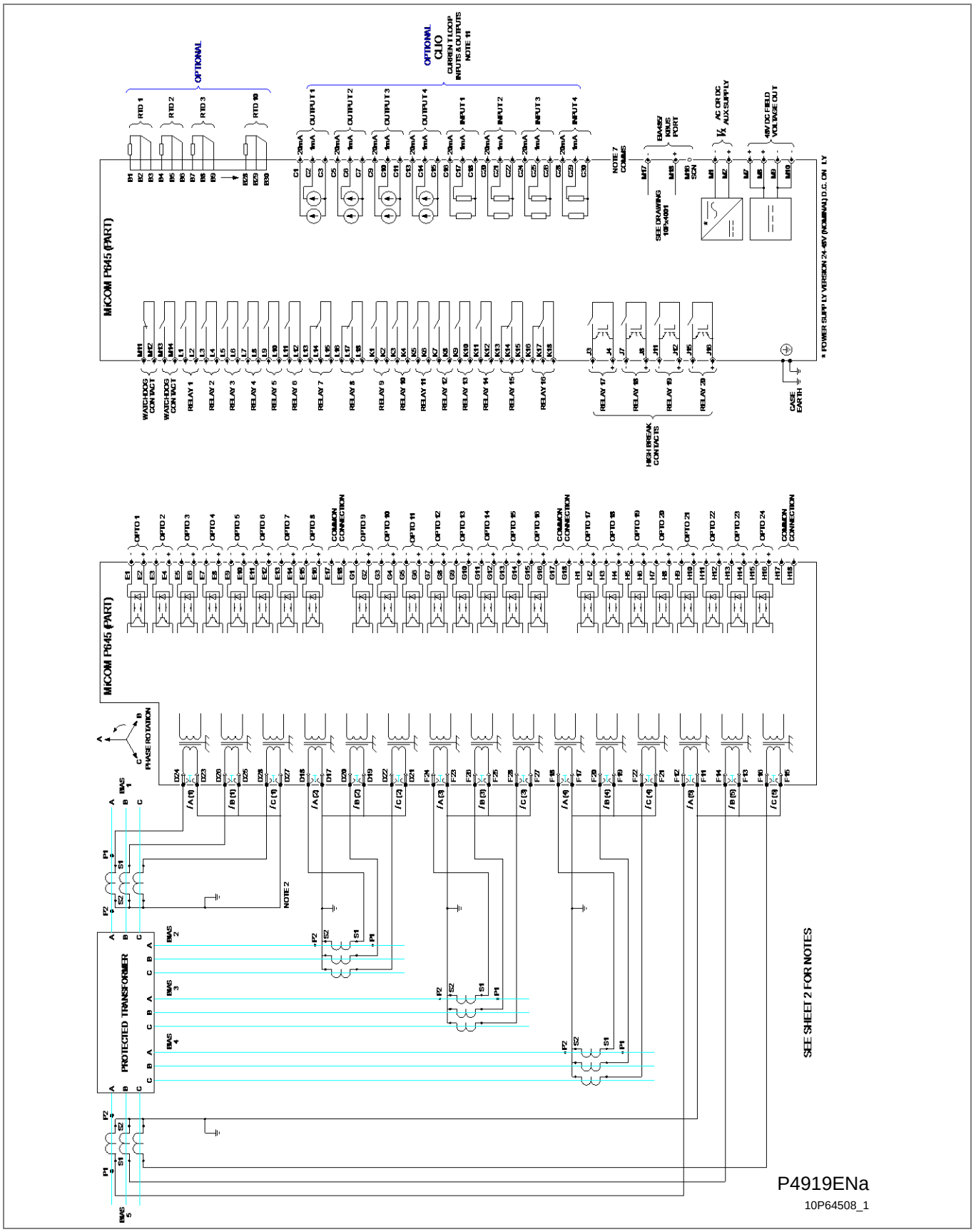
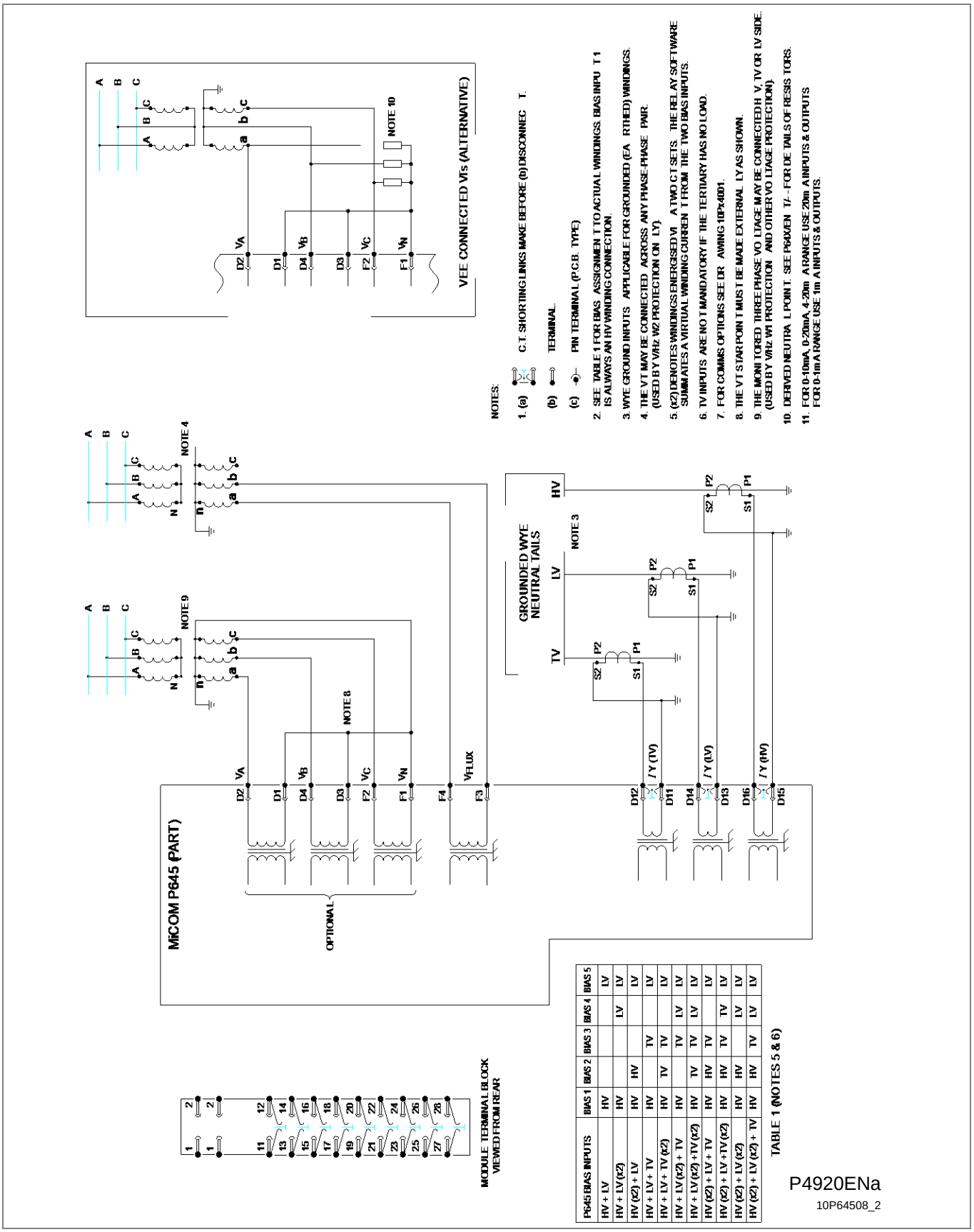


Figure 39 - Five bias ITD (24 I/P & 20 O/P + CLIO & RTD) with 4P VT input (80TE)



P645 BIAS INPUTS	BIAS 1	BIAS 2	BIAS 3	BIAS 4	BIAS 5
HV + LV	HV				LV
HV + LV (x2)	HV			LV	LV
HV (x2) + LV	HV	HV			LV
HV + LV + TV	HV		TV		LV
HV + LV + TV (x2)	HV	TV	TV		LV
HV + LV (x2) + TV	HV		TV	LV	LV
HV + LV (x2) +TV(x2)	HV	TV	TV	LV	LV
HV (x2) + LV + TV	HV	HV	TV		LV
HV (x2) + LV +TV (x2)	HV	HV	TV	TV	LV
HV (x2) + LV (x2)	HV	HV		LV	LV
HV (x2) + LV (x2) + TV	HV	HV	TV	LV	LV

Figure 40 - Five bias ITD (24 I/P & 20 O/P + CLIO & RTD) with 4P VT input (80TE)

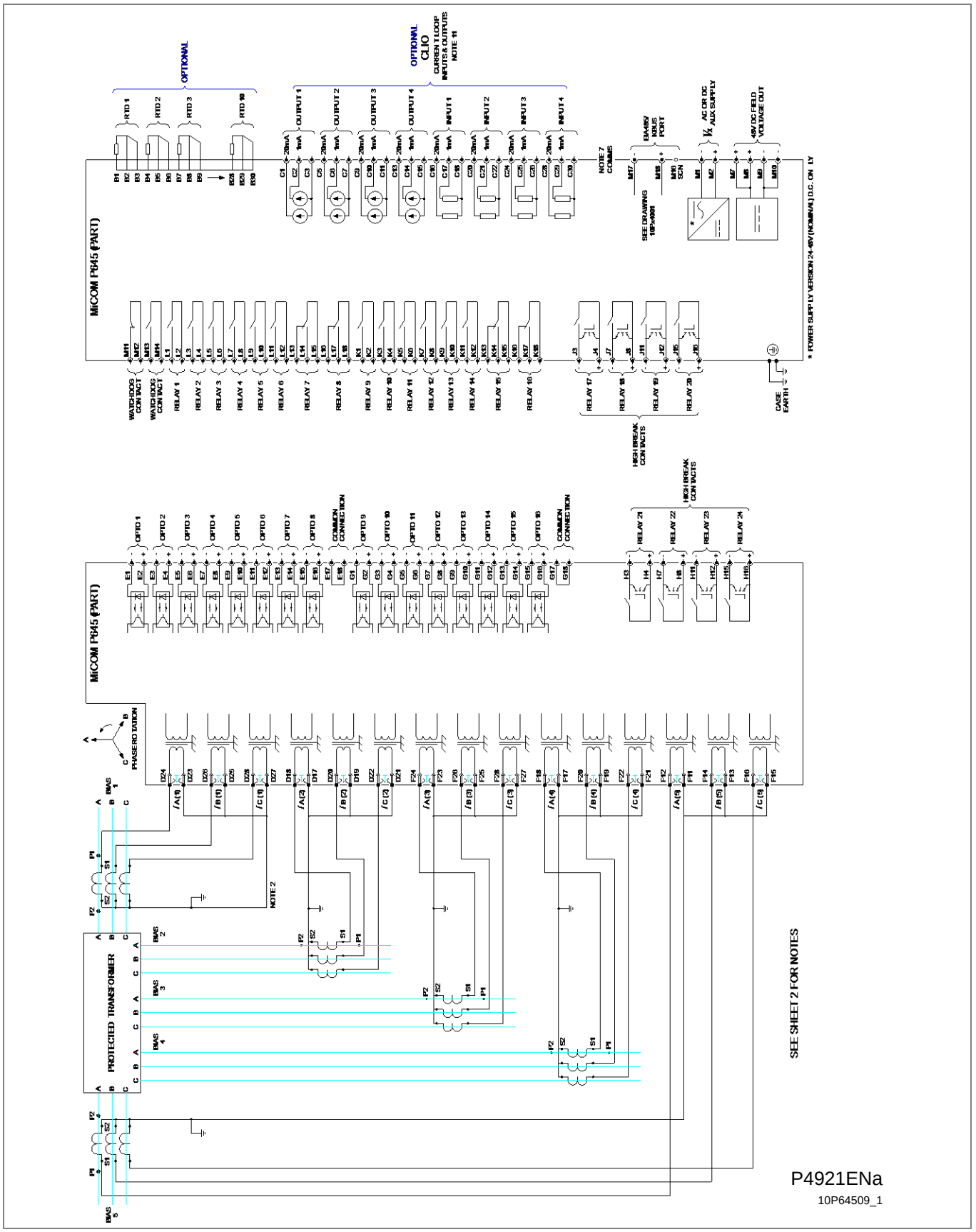


Figure 41 - Five bias ITD (16 I/P & 24 O/P + CLIO & RTD) with 4P VT input (80TE)

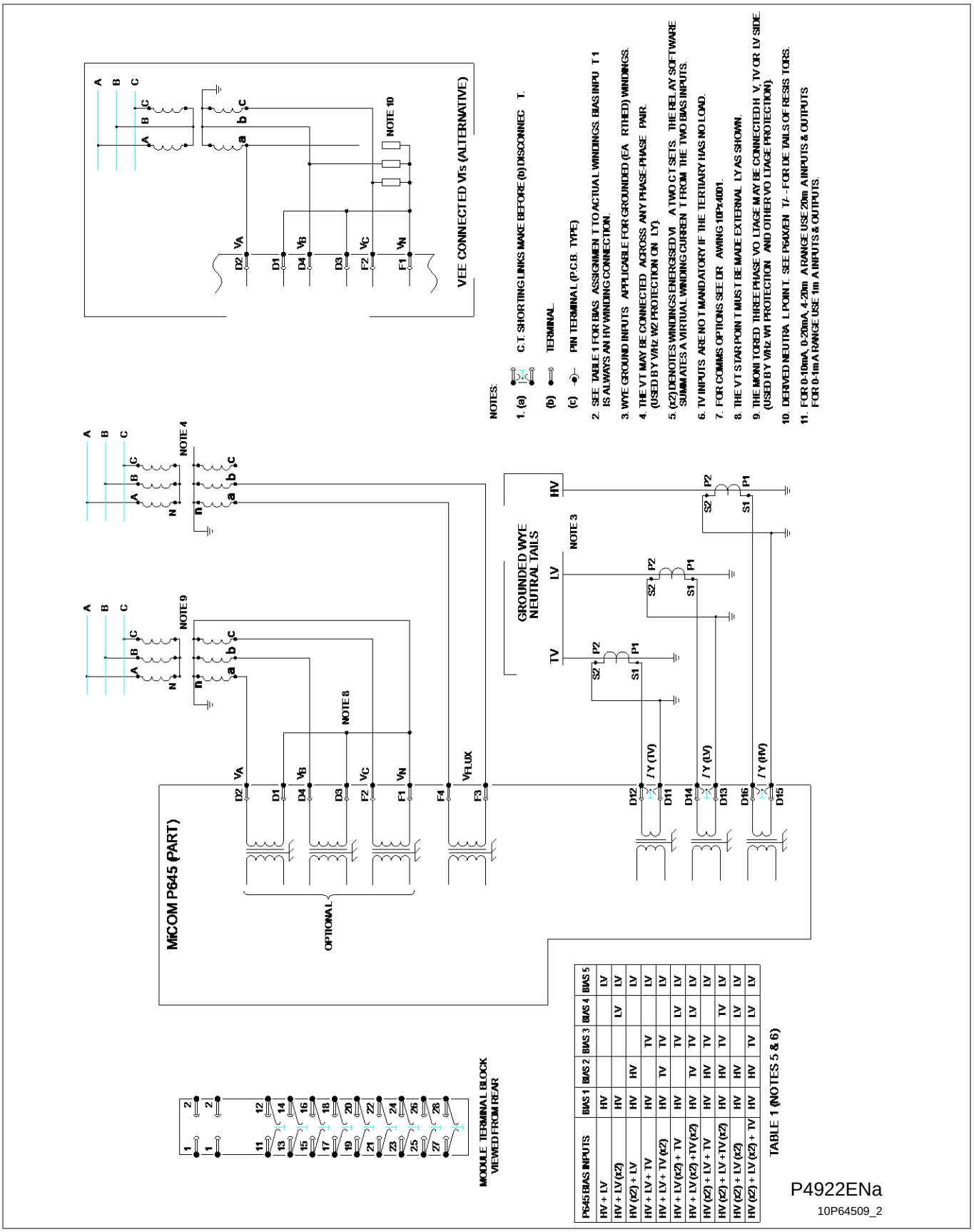


Figure 42 - Five bias ITD (16 I/P & 24 O/P + CLIO & RTD) with 4P VT input (80TE)

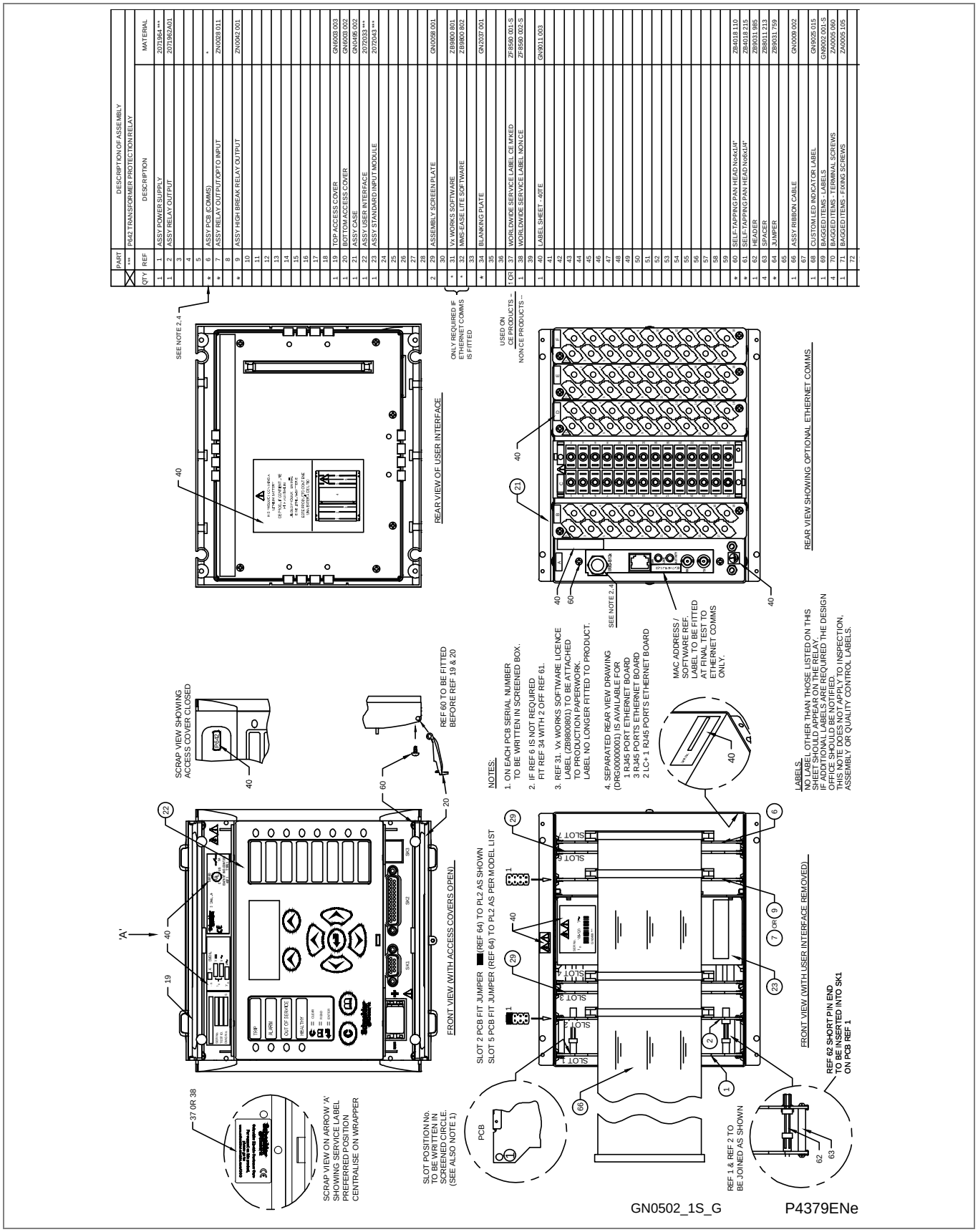


Figure 43 - P642 assembly relay (40TE)

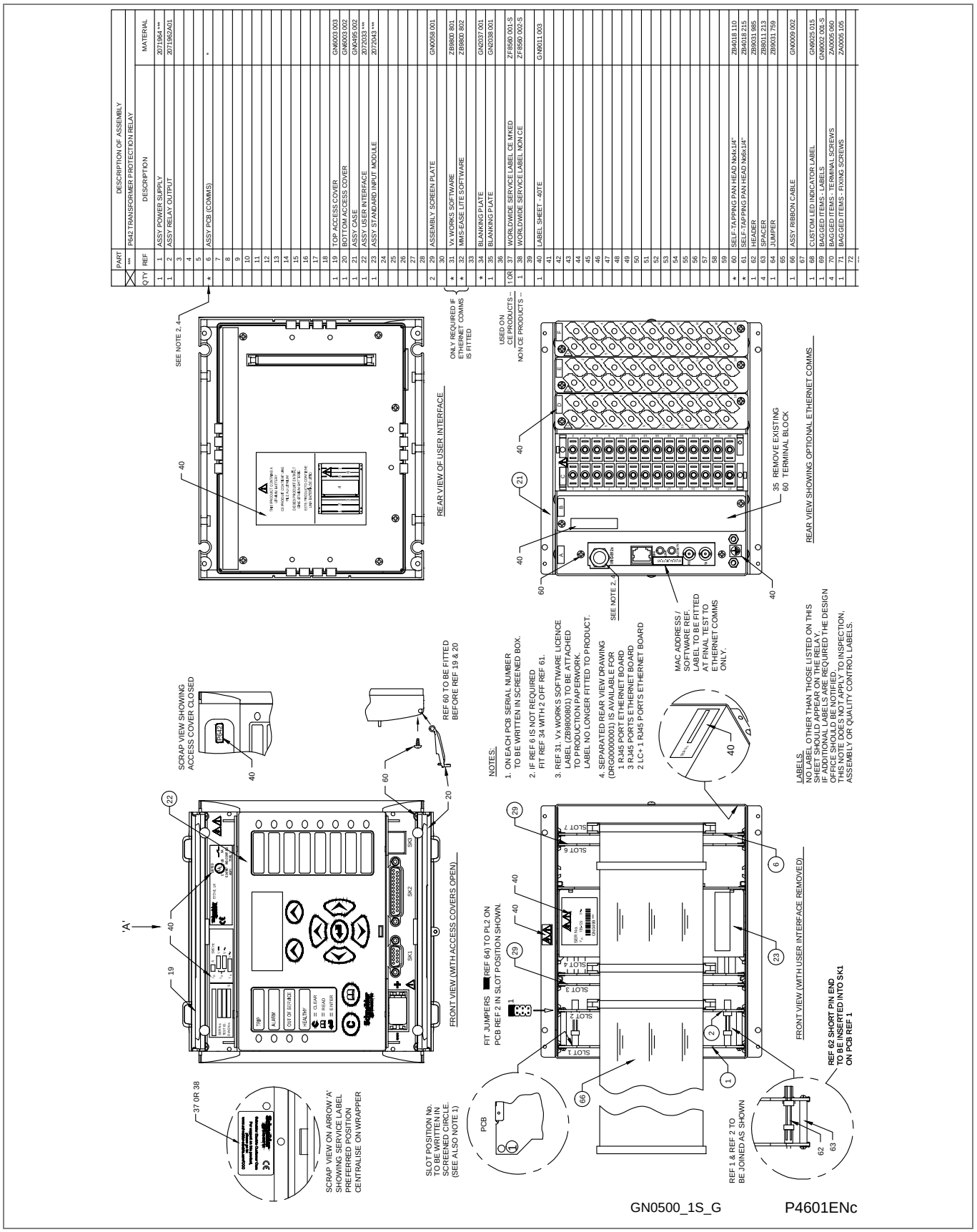


Figure 44 - P642 assembly relay (60TE)

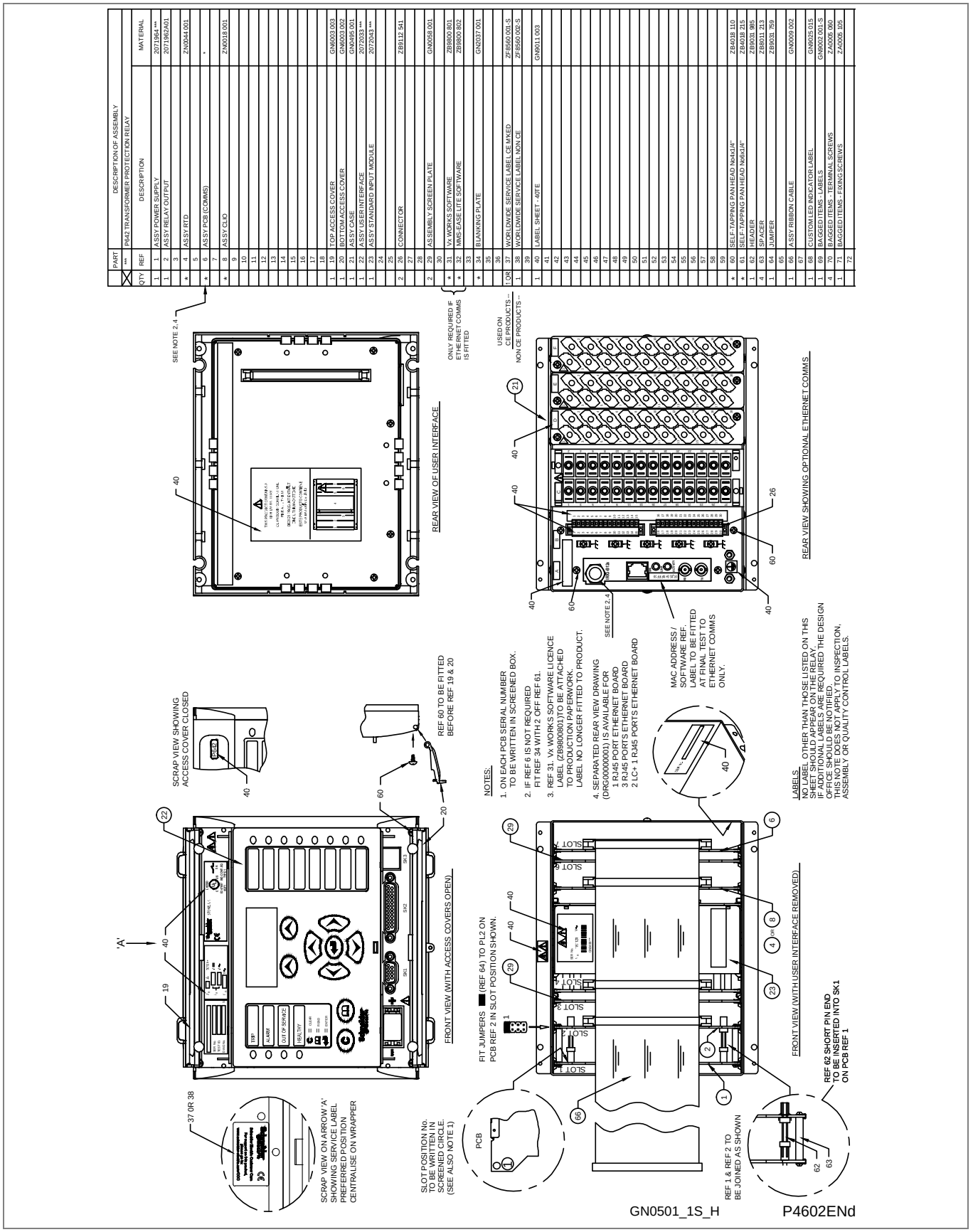


Figure 45 - P642 assembly relay (40TE)

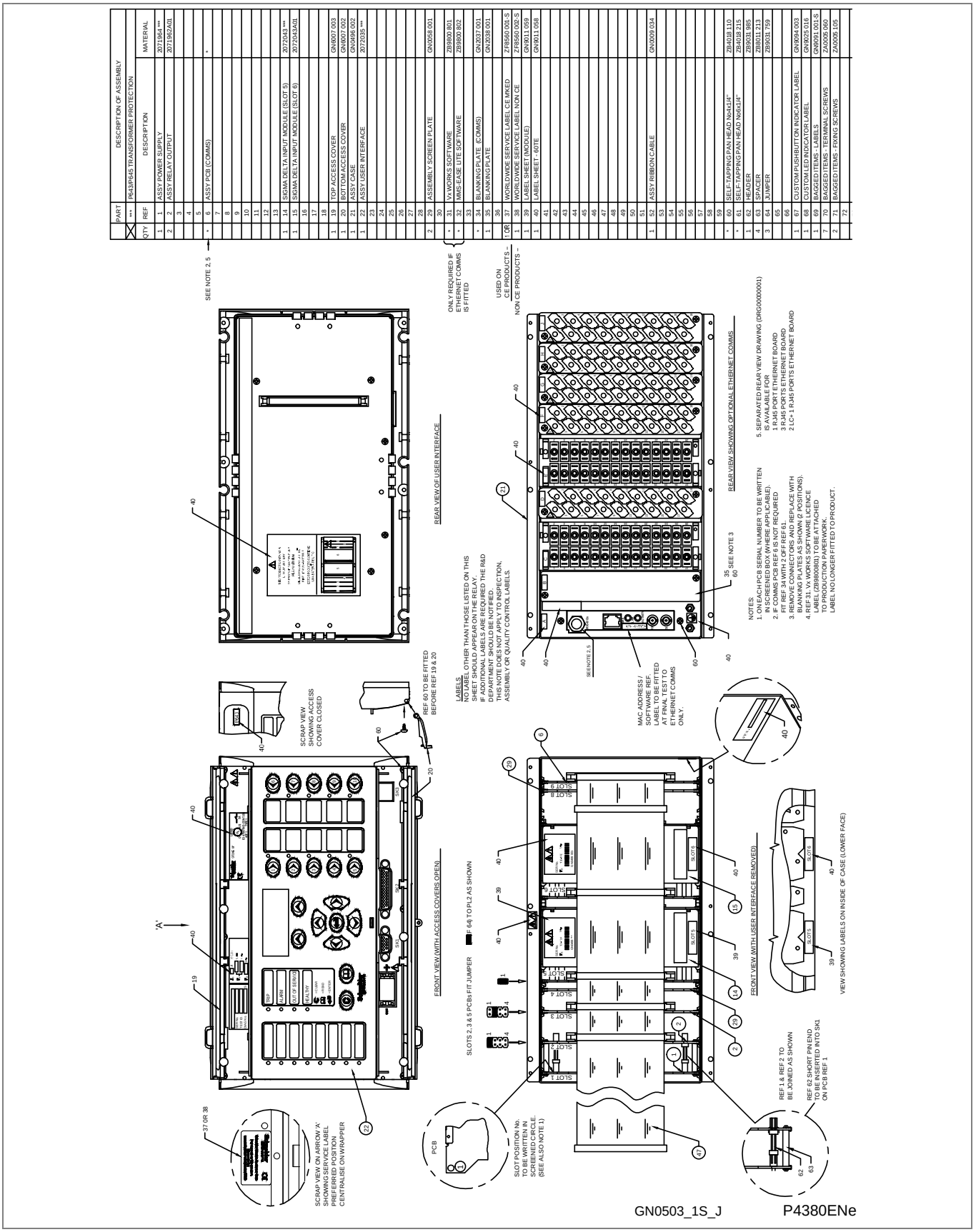
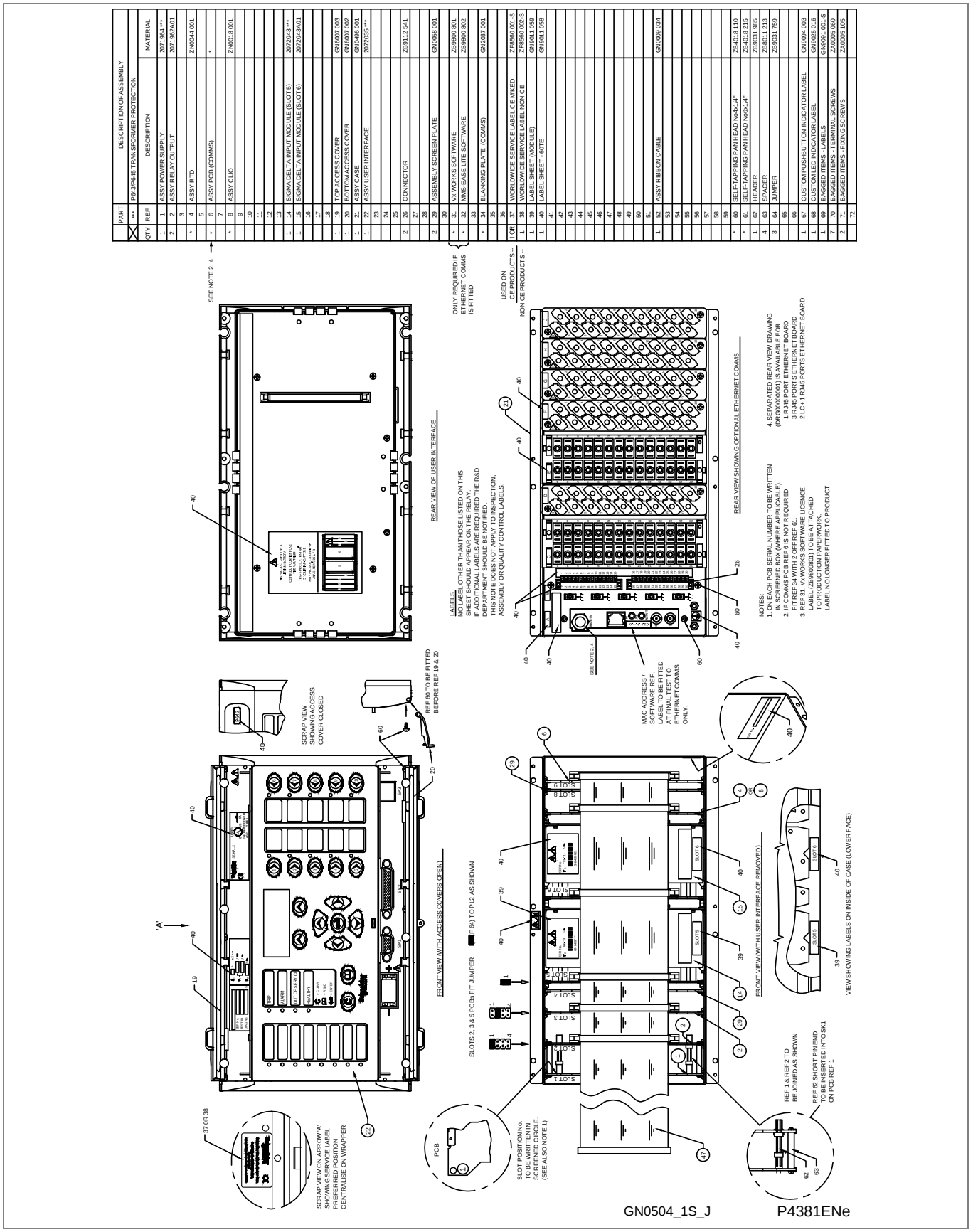


Figure 46 - P643/P645 assembly relay (60TE)



PART		DESCRIPTION OF ASSEMBLY	
	***	P643/P645 TRANSFORMER PROTECTION	
QTY	REF	DESCRIPTION	MATERIAL
1	1	ASSY POWER SUPPLY	2071964 ***
2	2	ASSY RELAY OUTPUT	2071962A01
*	3	ASSY RTD	ZN0044 001
	5		
*	6	ASSY PCB (COMMS)	*
	7		
*	8	ASSY CLIO	ZN0018 001
	9		
	10		
	11		
	12		
	13		
1	14	SIGMA DELTA INPUT MODULE (SLOT 5)	2072043 ***
1	15	SIGMA DELTA INPUT MODULE (SLOT 6)	2072043A01
	16		
	17		
	18		
1	19	TOP ACCESS COVER	GN0007 003
1	20	BOTTOM ACCESS COVER	GN0007 002
1	21	ASSY CASE	GN0486 001
1	22	ASSY USER INTERFACE	2072035 ***
	23		
	24		
	25		
2	26	CONNECTOR	ZB9112 541
	27		
	28		
2	29	ASSEMBLY SCREEN PLATE	GN0058 001
	30		
*	31	Vx WORKS SOFTWARE	ZB9800 801
*	32	MMS-EASE LITE SOFTWARE	ZB9800 802
	33		
*	34	BLANKING PLATE (COMMS)	GN2037 001
	35		
	36		
1 OR	37	WORLDWIDE SERVICE LABEL CE MARKED	ZF9560 001-S
1	38	WORLDWIDE SERVICE LABEL NON CE	ZF9560 006-S
1	39	LABEL SHEET (MODULES)	GN7011 059
1	40	LABEL SHEET - 60TE	GN7011 058
	41		
	42		
	43		
	44		
	45		
	46		
	47		
	48		
	49		
	50		
1	51		
1	52	ASSY RIBBON CABLE	GN0009 034
	53		
	54		
	55		
	56		
	57		
	58		
	59		
*	60	SELF-TAPPING PAN HEAD No4x14"	ZB4018 110
*	61	SELF-TAPPING PAN HEAD No6x14"	ZB4018 215
1	62	HEADER	ZB9031 985
4	63	SPACER	ZB8011 213
3	64	JUMPER	ZB9031 759
	65		
	66		
1	67	CUSTOM PUSHBUTTON INDICATOR LABEL	GN9094 003
1	68	CUSTOM LED INDICATOR LABEL	GN9025 016
1	69	BAGGED ITEMS - LABELS	GN8091 001-S
7	70	BAGGED ITEMS - TERMINAL SCREWS	ZA0005 060
2	71	BAGGED ITEMS - FIXING SCREWS	ZA0005 105
	72		

Figure 47 - P643/P645 assembly relay (60TE)

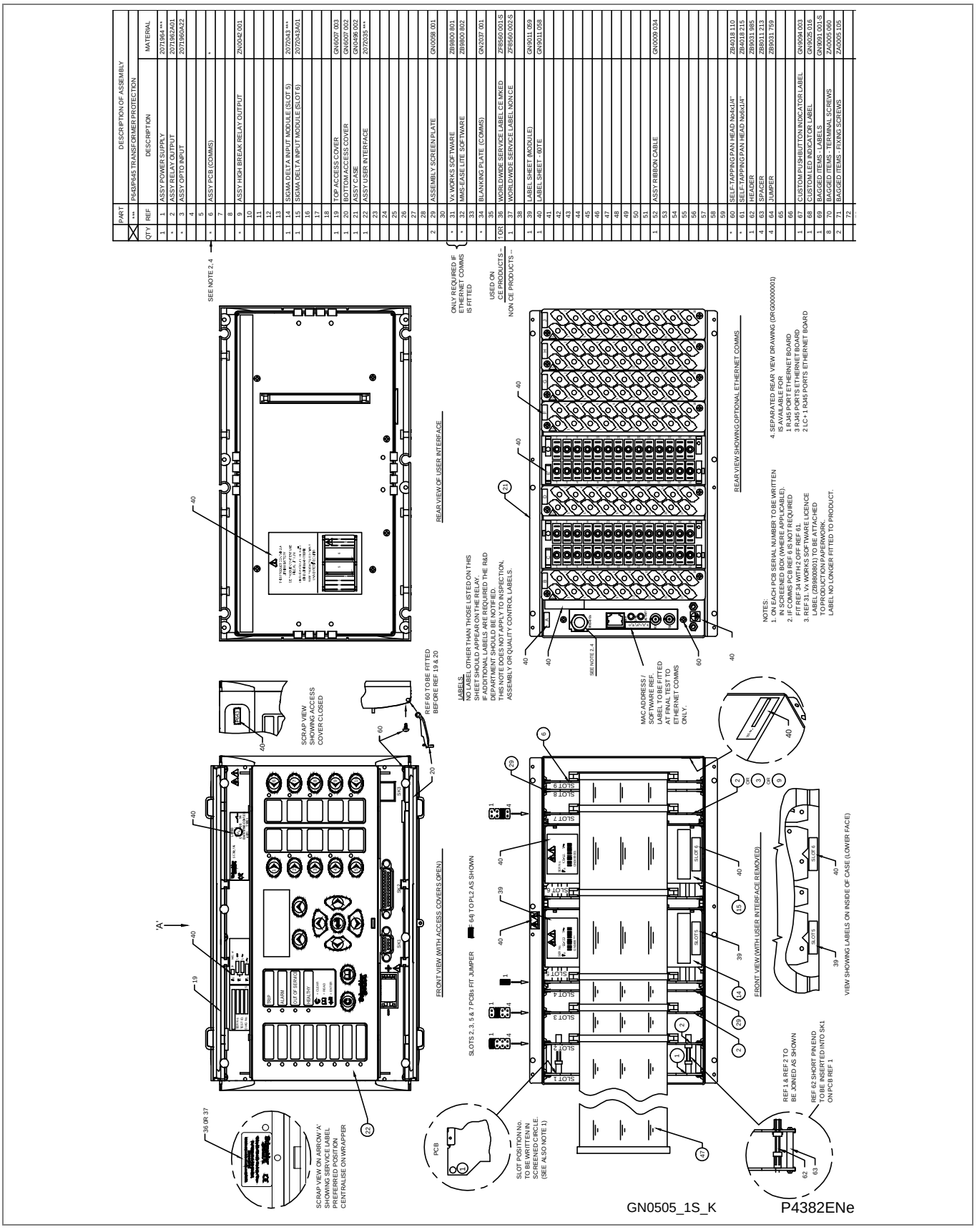


Figure 48 - P643/P645 assembly relay (60TE)

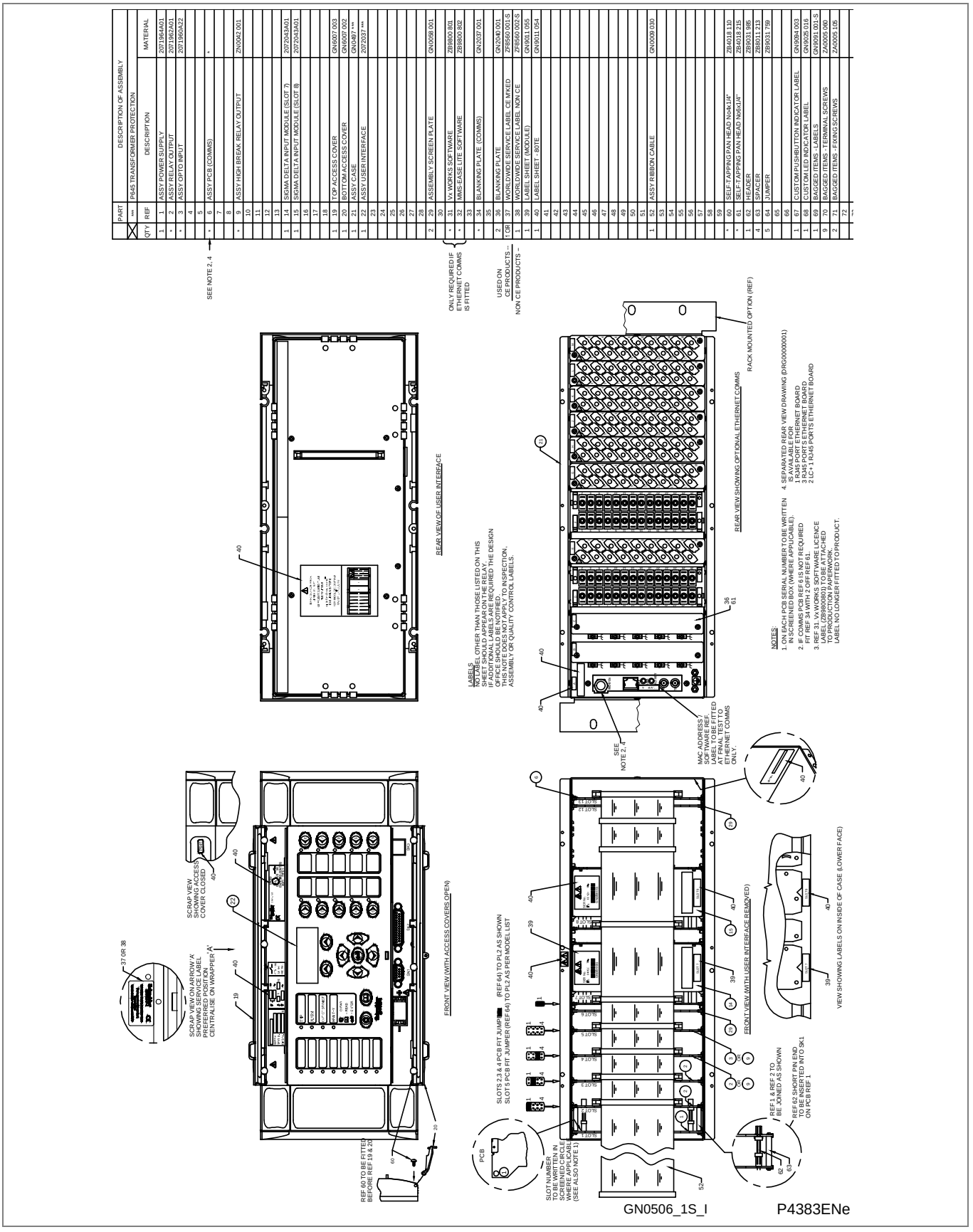


Figure 49 - P645 assembly relay (80TE)

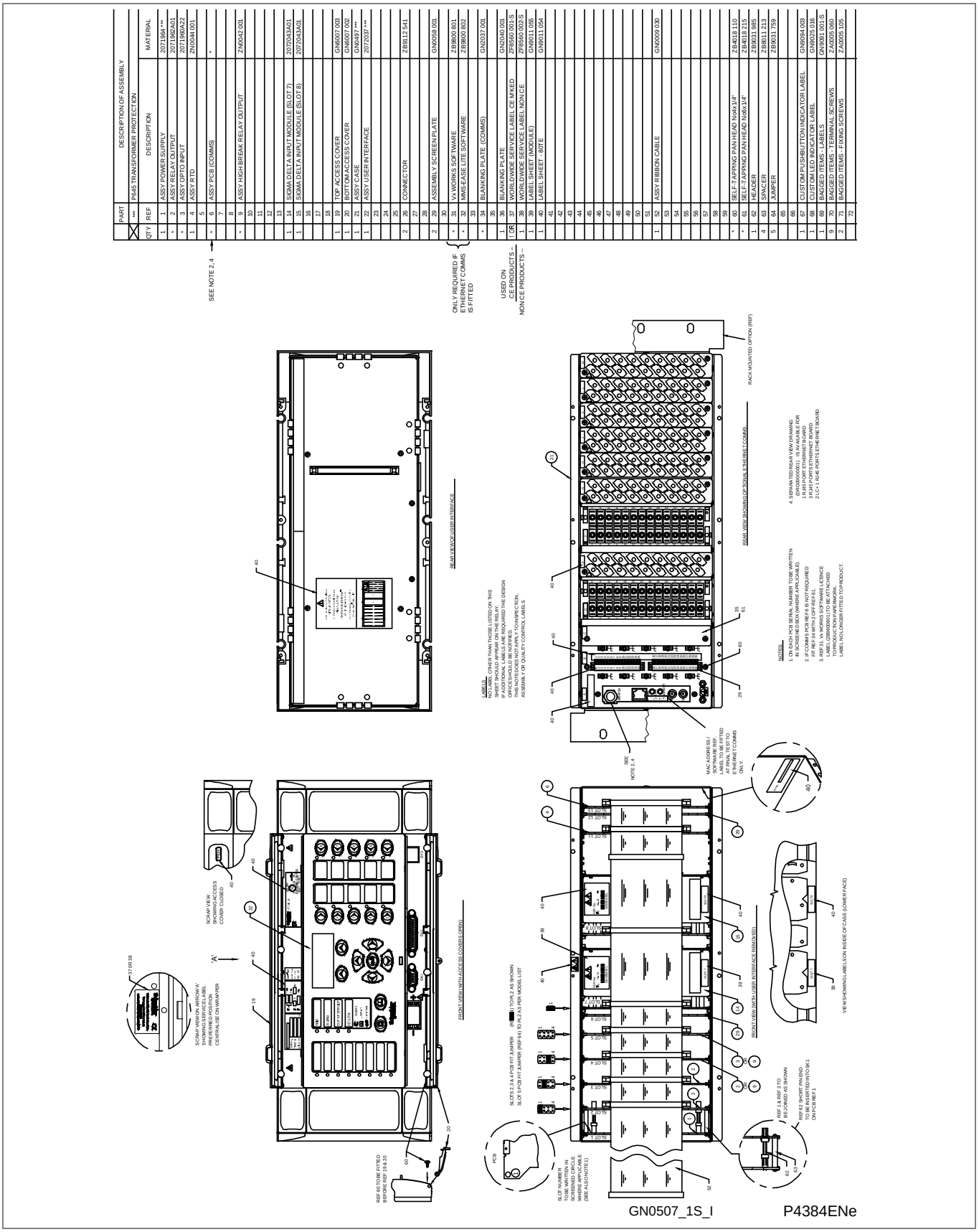


Figure 50 - P645 assembly relay (80TE)

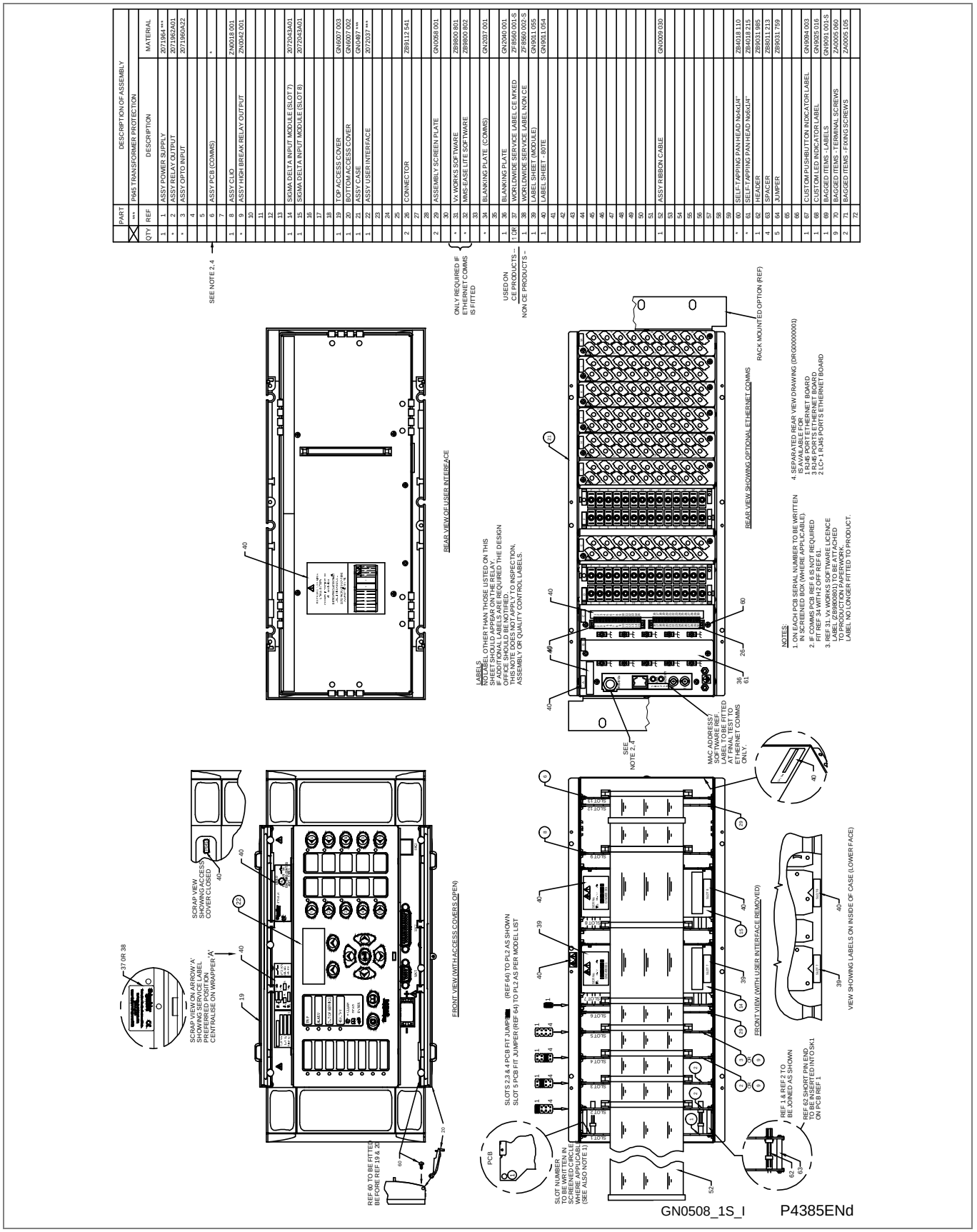


Figure 51 - P645 assemby relay (80TE)

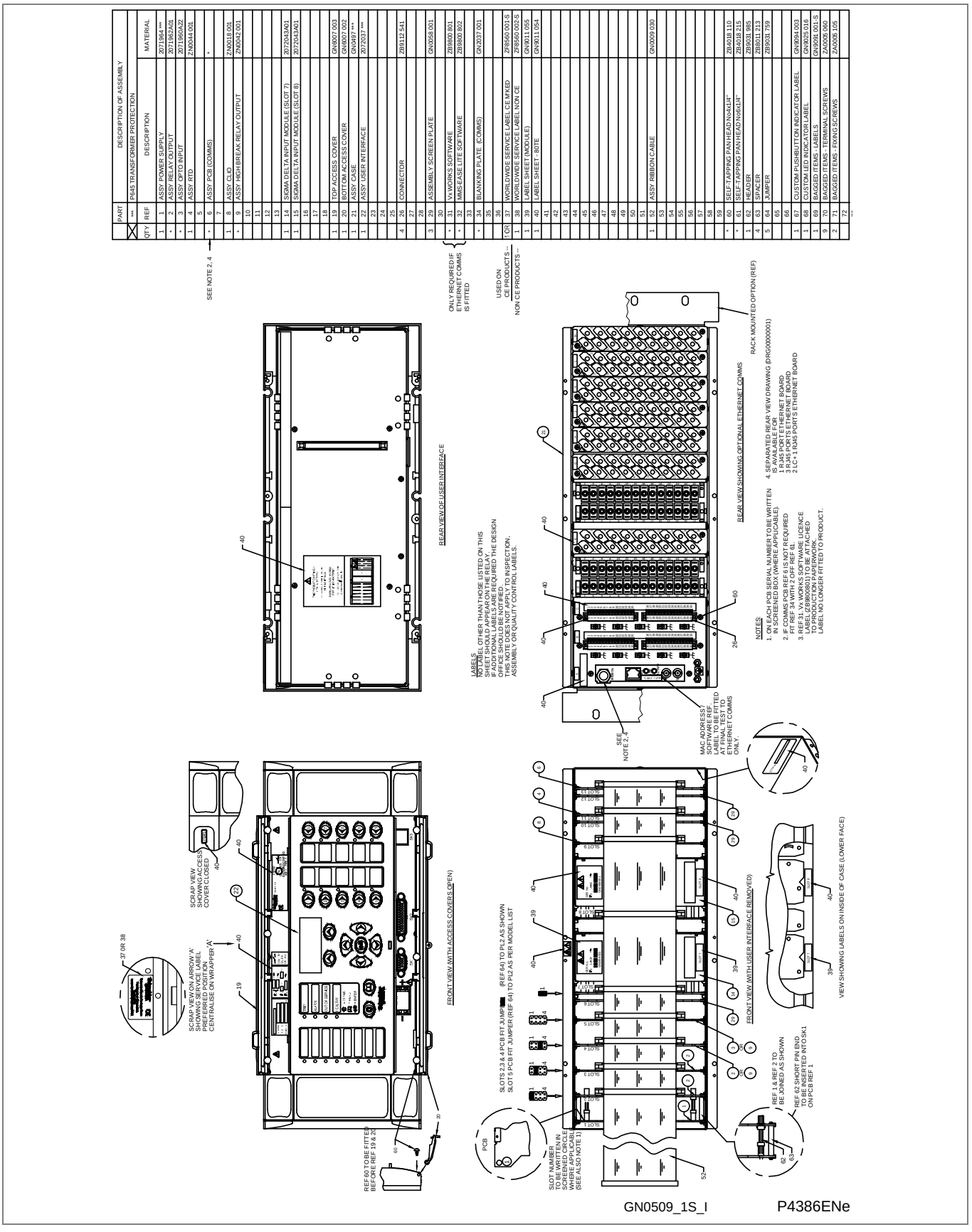


Figure 52 - P645 assembly relay (80TE)

CYBER SECURITY

CHAPTER 18

Date (month/year):	02/2018			
Products covered by this chapter:	This chapter covers the specific versions of the MiCOM products listed below. This includes ***only*** the following combinations of Software Version and Hardware Suffix.			
Hardware Suffix:	P445 P44y (P443/P446)	L M	P54x (P543/P544/P545/P546) P841A (one circuit breaker) P841B (two circuit breakers)	M M M
Software Version:	P445 P44y (P443/P446)	J8 H8	P54x (P543/P544/P545/P546) P841A (one circuit breaker) P841B (two circuit breakers)	H8 G8 H8
Connection Diagrams:	P14x (P141, P142, P143 & P145): 10P141xx (xx = 01 to 02) 10P142xx (xx = 01 to 05) 10P143xx (xx = 01 to 11) 10P145xx (xx = 01 to 11) P445: 10P445xx (xx = 01 to 04) P44x (P442 & P444): 10P44201 (SH 1 & 2) 10P44202 (SH 1) 10P44203 (SH 1 & 2) 10P44401 (SH 1) 10P44402 (SH 1) 10P44403 (SH 1 & 2) 10P44404 (SH 1) 10P44405 (SH 1) 10P44407 (SH 1 & 2) P44y (P443 & P446): 10P44303 (SH 01 and 03) 10P44304 (SH 01 and 03) 10P44305 (SH 01 and 03) 10P44306 (SH 01 and 03) 10P44600 10P44601 (SH 1 to 2) 10P44602 (SH 1 to 2) 10P44603 (SH 1 to 2)		P54x (P543, P544, P545 & P546): 10P54302 (SH 1 to 2) 10P54303 (SH 1 to 2) 10P54400 10P54404 (SH 1 to 2) 10P54405 (SH 1 to 2) 10P54502 (SH 1 to 2) 10P54503 (SH 1 to 2) 10P54600 10P54604 (SH 1 to 2) 10P54605 (SH 1 to 2) 10P54606 (SH 1 to 2) P64x (P642, P643 & P645): 10P642xx (xx = 01 to 10) 10P643xx (xx = 01 to 06) 10P645xx (xx = 01 to 09) P746: 10P746xx (xx = 00 to 21) P841: 10P84100 10P84101 (SH 1 to 2) 10P84102 (SH 1 to 2) 10P84103 (SH 1 to 2) 10P84104 (SH 1 to 2) 10P84105 (SH 1 to 2) P849: 10P849xx (xx = 01 to 06)	
	Note *This chapter covers the combinations of Products, Software Versions and Hardware Suffixes identified here. If you are using earlier software or hardware, please refer to the Schneider Electric Customer Care Centre (www.schneider-electric.com/ccc) for details of which version of this chapter to refer to.*			

CONTENTS

Page (CS) 18-

TABLES

FIGURES

1 OVERVIEW

1.1 Definition

Cyber security is a domain that addresses attacks on or by computer systems and through computer networks that can result in accidental or intentional disruptions. Cyber security addresses not only deliberate attacks, such as from disgruntled employees, industrial espionage, and terrorists, but also inadvertent compromises of the information infrastructure due to user errors, equipment failures, and natural disasters.

1.2 Introduction to Cyber Security

The objective of cyber security is to provide increased levels of protection for information and physical assets from theft, corruption, misuse, or accidents while maintaining access for their intended users.

To achieve this objective the owner of the grid must take into account Cyber Security at every level of his organization by the management of an ongoing process that encompasses procedures, policies, technical (software, and hardware asset) and regulatory constraints.

The following diagram outlines some of the associated topics.

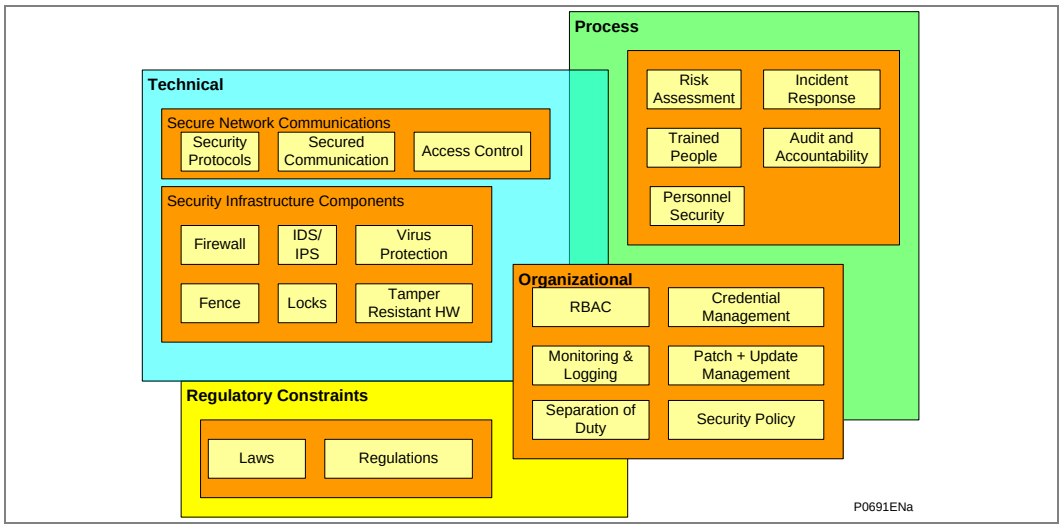


Figure 1 - Associated topics

The asset owner needs to run a continuous improvement process as outlined here:

Figure 2 - Continuous improvement process

No single solution can provide adequate protection against all cyber attacks on the control network. Schneider Electric recommends employing a “defense in depth” approach using multiple security techniques to help mitigate risk.
A secured system is to offer:

- Detective controls: Monitor and record specific types of events: Security logs, Intrusion, detection systems, Video Surveillance etc.
- Preventive controls: Help blocking or controlling specific event : Antivirus, White listing, Firewall etc.
- Recovery controls: Help achieve Business continuity and Disaster recovery planning objectives in case of an incident: Backup and Restore solution.

As protective relay vendor, Schneider Electric helps the grid owner to achieve by providing technical features inside the IED, described in the next chapters.

Important	**This product contains a cyber-security function, which manages the encryption of the data exchanged through some of the communication channels. The aim is to protect the data (configuration and process data) from any corruption, malice, attack. Subsequently, this product might be subject to control from customs authorities. It might be necessary to request special authorization from these customs authorities before any export/import operation. For any technical question relating to the characteristics of this encryption please contact your Customer Care Centre - www.schneider-electric.com/ccc.**

1.3 Roles, Rights and relationship between IEC62351 and MiCOM Px4x

1.3.1 Role Based Access Control (RBAC)

The Role Based Access Control (RBAC) is a method to restrict resource access to authorized users. RBAC is an alternative to traditional Mandatory Access Control (MAC) and Discretionary Access Control (DAC).

A key feature of RBAC model is that all access is through roles. A role is essentially a collection of permissions, and all users receive permissions only through the roles to which they are assigned, or through roles they inherit through the role hierarchy.

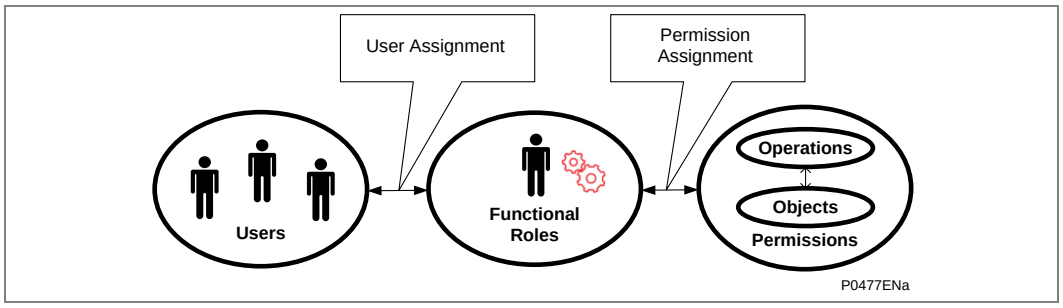


Figure 3 - RBAC Role structure

Roles are created for various job activities. The ***Permissions***, to perform certain operations, are assigned to specific roles. ***Users*** are assigned particular roles, and through those role assignments acquire the computer permissions to perform particular computer-system functions. Since ***users*** are not assigned permissions directly, but only acquire them through their role (or roles), management of individual user rights becomes a matter of simply assigning appropriate roles to the user's account; this simplifies common operations, such as adding a user, or changing user's account.

RBAC defines four different concepts:

RBAC Standard Definition	Description
Object	An ***object*** can represent information containers (e.g. files, directories in an operating system, tables and views in a database management system) or device resources, such as IEDs.
Subject	A ***subject*** is a user of the system. Note that a subject can be a person, or an automated agent / device.
Right	A ***right*** is the ability to access an object in order to perform certain operations (e.g. setting a data or reading a file)
Role	A ***role*** defines a certain authority level in the system. Rights are assigned to roles.

Table 1 – RBAC object, subject, rights and roles definitions

RBAC defines three primary rules:

RBAC Rule	Description
Role assignment	A subject can exercise a permission only if the subject has selected or been assigned a role.
Role authorization	A subject's active role must be authorized for the subject. With rule 1 above, this rule ensures that users can take on only roles for which they are authorized.
Permission authorization	A subject can exercise permission only if the permission is authorized for the subject's active role. With rules 1 and 2, this rule ensures that users can exercise only permissions for which they are authorized.

Table 2 – RBAC permission and authorization rules

1.3.2 User Roles

Different named roles are associated with different access rights. Roles and Rights are setup in a pre-defined arrangement, according to the IEC62351 standard, but customized to the MiCOM Px4x equipment.

When the user tries to access an IED, they need to login using their own username and their own password. The username/password combination is then checked against the records stored on the IED. If they are allowed to login, a message appears which shows them what Role they have been assigned to. It is the role that defines their access to the relevant parts of the system.

The default user roles for MiCOM Px4x are shown here:

Role	Description
VIEWER	Can View what objects are present within a Logical-Device by presenting the type ID of those objects.
OPERATOR	An Operator can view what objects and values are present within a Logical-Device by presenting the type ID of those objects as well as perform control actions.
ENGINEER	An Engineer can view what objects and values are present within a Logical-Device by presenting the type ID of those objects. Moreover, an engineer has full access to Datasets and Files and can configure the server locally or remotely.
SECADM	Security Administrator can change subject-to-role assignments (outside the device) and role-to-right assignment (inside the device) and security policy setting; change security setting such as certificates for subject authentication and access token verification.
SECAUD	Security Auditor can view audit logs

Table 3 – Default user roles summary for MiCOM Px4x

Each authorized user must be placed into at least ONE of these roles that most suits their job description. It is possible to assign a user into a different role; and/or to change the rights associated with a particular role. This means that the administrator can change the access rights for one role; and this will affect ALL the users who are assigned to that role.

It is possible for MiCOM Px4x to create the customized user roles.

1.3.3 Rights

In a similar way in which a set of pre-defined Roles have been created, a pre-defined set of Rights have been created.

These Rights give different permissions to look at what devices may be present, what those devices may contain, manage data within those devices (directly or by using files) and configure rights for other people.

A list of the pre-defined Rights for IEC 62351-8 is given here:

Right	Description
VIEW	Allows the subject/role to discover what objects are present within a Logical-Device by presenting the type ID of those objects. If this right is not granted to a subject/role, the Logical-Device for which the View right has not been granted shall not appear
READ	Allows the subject/role to obtain all or some of the values in addition to the type and ID of objects that are present within a Logical-Device;
DATASET	Allows the subject/role to have full management rights for both permanent and non-permanent Datasets;
REPORTING	Allows a subject/role to use buffered reporting as well as un-buffered reporting;
FILEREAD	Allows the subject/role to have read rights for file objects;
FILEWRITE	Allows the subject/role to have write rights for file objects. This right includes the FILEREAD right
CONTROL	Allows a subject to perform control operations;
CONFIG	Allows a subject to locally or remotely configure certain aspects of the server;
SETTINGGROUP	Allows a subject to remotely configure Settings Groups;
FILEMNGT	Allows the role to transfer files to the Logical-Device, as well as delete existing files on the Logical-Device;
SECURITY	Allows a subject/role to perform security functions at both a Server/Service Access Point and Logical-Device basis. To add Information about the concept of Rights.

Table 4 – Pre-defined rights for IEC 62351-8

The specific Rights for MiCOM Px4x are listed below. These are dependent on the IED data type. Please refer to each product MD file (Menu Database) for the IED data type.

Rights	Authorized Actions to IED	IED_DESC	IED_DATA	DISPLAY	IED_CONFIG	PROT_CONFIG	IEC_COMMAND	AUDIT	IED_FN_KEY	IED_CLEAR
Read Only (SAT default_access_right)	Read	x	x	x	x		x			
	Write	x								
IED Configuration (SAT configuration_right)	Read/write/upload/download				x					
HMI Display Settings (SAT display_action_right)	Read/write/select			x						
Protection Configuration (SAT protection_configuration_right)	Read/write					x				
IED Commands (SAT control_right)	Read/write/clear/reset/select						x			
Reading of Records & Events (SAT audit_read_right)	Read/select/upload							x		
Extraction of Records and Events (SAT audit_write_right)	Send/accept							x		
IED Function Key (SAT fn_key_access_right)	Write								x	
IED Records Clear (SAT clear_right)	Read/write/clear									x

Table 5 – Specific rights for MiCOM Px4x

1.3.4 Roles and their Access Rights

A complete list of the Roles and their access Rights is shown in this table:

Rights \ Roles		VIEWER	OPERATOR	ENGINEER	SECADM	SECAUD
Pre-defined Rights for IEC 62351	VIEW	X	X	X	X	X
	READ		X	X	X	X
	DATASET			X		
	REPORTING	X	X	X		X
	FILEREAD					X
	FILEWRITE			X	X	
	FILEMNGT			X	X	
	CONTROL		X		X	
	CONFIG			X	X	
	SETTINGGROUP				X	
	LOGS				X	X
	SECURITY				X	
Specific Rights for MiCOM Px4x	Read Only	X	X	X		X
	IED Configuration			X		
	HMI Display Settings		X	X		
	Protection Configuration			X		
	IED Commands		X	X		
	Reading of Records and Events	X	X	X		X
	Extraction of Records and Events		X	X		X
	IED Function Key		X	X		
	IED Clear			X		

Table 6 – Pre-defined roles (and rights) for IEC 62351-8 and MiCOM Px4x

Important	**The reason why these are described as Default, is that it is possible to change the definitions of Roles and Rights, using the full version of the SAT software. Depending on the work done by the system administrator, it is possible that your own situation may vary from these initial recommendations.**

1.4 Security Administration Tool (SAT) Software

Important	**This can only be used with Px4x relays with cyber security CSL1 features.**

Important	**For Dual Ethernet cards the SAT functionality is available from communication interface 1. The connection to the SAT would be available from interface 2 only when interface 1 is disconnected from the network.**

The Security Administration Tool (SAT) is the security configuration tool of MiCOM Px4x equipment. It allows the security administrator to define the security policy to the IEDs.

The Security Administrator manages RBAC and security policies data. Security Administrator defines needs to protect devices in accordance with user privileges. Thus, the system security can be configured easily and precisely.

The SAT is used by the Security Administrator to manage the system's security database and deploys security configurations to IED(s).

The SAT allows to Manage User Accounts, Roles, Permission, Elements to Secure (ETS) and Security Server parameters without connection with devices. Information is store on the MS SQL database. This is the Offline mode. SAT allows devices management connected on network. This is the online mode.

The Role Based Access Control (RBAC) is a method to restrict resource access to authorized users. Please refer to this documentation on section "*System RBAC Management*" for more details.

The following table contains the main user main functions of the SAT:

Category	User Function	Note
Offline General Administration	User Accounts Management	User Account Functions: * Creation * Edition * Suppress * Viewing * Sorting * Filtering
	Server Configuration	
	Users Accounts & Roles association Management	Associate a role to the user account
Offline Advanced Administration	Roles Management	Roles Functions: * Creation * Edition * Suppress * Viewing * Sorting
	Element To Secure (ETS) Management	Define ETS which are in fact the PACiS assets present in the project (C264, PACiS Gateway, ECOSUI, IED and SAM). Add, Suppress and Sort permissions associated with the ETS.
	Global Security Management	The Global Security allows scope(s) and associate or disassociate role(s) management for each user account. The security administrator manages the current scope by the Roles: * View Roles List, User Account List and associations User-Roles or Role-Users * Associate / dissociate role(s) for each User Account * Add / Suppress User account(s) for each Role
	Permission access	Define parameters: * Password validity * Inactivity period * Automatic logout period * Maximum attempts of login and lockout period
Communication	Refresh IED list	
	Display IED Logs	
	Display SAM Logs	
	Push RBAC and Security Policies	Send Security Configuration to all Devices integrating Security features.

Table 7 – Main SAT user functions

The details of how to use the SAT are provided in the SAT documentation:

SAT (Security Administration Tool) Documentation - User Guide

This is available from the Schneider Electric website: www.schneider-electric.com.

2 MICOM PX4X CYBER SECURITY IMPLEMENTATION

Schneider Electric MiCOM Px4x IEDs have always been and will continue to be equipped with state-of-the-art security measures. Due to the ever-evolving communication technology and new threats to security, this requirement is not static. Hardware and software security measures are continuously being developed and implemented to mitigate the associated threats and risks.

Considered some users may not want to use the cyber security, Schneider Electric offers MiCOM Px4x relays with CSL0 and CSL1 as below:

CSL0: Simple password management, No SAT required.

CSL1: Advanced cyber security, SAT required.

This depends on the model number, as CSL1 is depend on the Ethernet communication. Hence if the IED if supports only legacy protocol this will be CLS0 default as. The digit position number 9 (protocol options) in the Cortec / model number is used to distinguish it.

Protocol Option Number	Protocol options	Cyber Security options
1	K-Bus/Courier	CSL0
2	Modbus	CSL0
3	IEC 60870 -5 - 103	CSL0
4	DNP3.0	CSL0
6	IEC 61850 Edition 1 / 2 and Courier via rear K-Bus/RS485	CSL0
7	IEC 61850 Edition 1 / 2 and CS103 via rear port RS485	CSL0
B	IEC 61850 Edition 1 / 2 and DNP3oE and DNP Serial	CSL0
G	IEC 61850 Edition 1 / 2 and Courier via rear K-Bus/RS485	CSL1
H	IEC 61850 Edition 1 / 2 and CS103 via rear port RS485	CSL1
L	IEC 61850 Edition 1 / 2 and DNP3oE and DNP3 serial	CSL1

Table 8 – MiCOM Px4x protocol options for cyber security options

2.1 MiCOM Px4x with CSL1 - Advanced Cyber Security

For MiCOM Px4x IEDs which support CSL1, this means the IED supports advanced user account right management. Moreover, the IED supports security logs/events and secure administration capability.

If you want to use cyber security, you need to order the IED that supports CSL1. In this case, the Security Administration Tool (SAT) is required for RBAC configuration.

At the IED level, these cyber security features have been implemented:

- Passwords management (via the SAT)
- RBAC Management (via the SAT)
- User Locking
- Inactivity Timer
- RBAC recovery
- Port Disablement (via Easergy Studio or the front panel)
- Security Logs

2.1.1 Password Management (via the SAT)

For the IED if CSL1 supported, there are two types of password possible for the IED access: alphanumeric password or Arrow Key password.

The alphanumeric password is only settable via the SAT:

- Passwords may be any length between 1 and 32 characters long
- Passwords may contain any ASCII character in the range ASCII code 33 (21 Hex) to ASCII code 122 (7A Hex) inclusive
- Passwords may or may not be NERC/IEEE 1686 compliant
- The alphanumeric password will used for courier client access

For more details about NERC/IEEE 1686 password compliant, please check the standard.

The Arrow Key password is only settable via the SAT:

- The Arrow Key password is a combination of the four arrow keys on the front panel
- The Arrow Key password may be any length between 1 and 8 of arrow keys long
- The Arrow Key password can only used in the front panel
- The user also can disable the Arrow Key password by not setting it

Important	**If the Arrow Key password is not configured, the alphanumeric password will be used for the front panel access. In this case, alphanumeric passwords longer than 16 characters are not allowed.** **Easergy Studio and the front panel are not allowed to change the password.**

2.1.2 RBAC Management (via the SAT)

By default, the IED includes a factory RBAC which has three users, and for each user, the Rights depend on the user Role. Please refer to the *Roles and their Access Rights* section for more details.

Username	Role	Default password
SecurityAdmin	SECADM	AAAAAAAA
EngineerLevel	ENGINEER	AAAA
OperatorLevel	OPERATOR	AAAA

Table 9 – Factory RBAC

A Local Default Access function also available for the default RBAC, with the VIEWER role, which allows everyone login the IED in the front panel with VIEWER role. For more details about the Local Default Access function, please refer to the *Local Default Access* section.

For more information about how the SAT management the RBAC and cyber security policies, please see the *Security Administration Tool (SAT)* section.

2.1.3 User Locking

The user is locked out temporarily, after a defined number of failed password entry attempts.

Important	**If a user is locked out, the block is applied to that named user and to the all IED interfaces. The blocking of one user, does not apply blocks to others.** **If the user entry is blocked, recover the RBAC or push a new RBAC will not reset the blocked user entry, but IED reboot will reset the blocking time and attempts count, so the user entry will be unblocked.**

An invalid password entry will display a 'Login Failed PW Incorrect' message for 2s. It also reduces the Attempts Remaining Counter (Attempts Remain) by 1 and it remains at this level until the interface inactivity timer expires (CSL0 models) or until the Password Attempts Timer configured in SAT expires (CSL1 models) or another password entry is made. If Attempts Remain equals 1 then a '1 Attempt Left' warning will also be issued for 2s. When Attempts Remain equals 0 then a 'USER LOCKED OUT' warning is displayed for 2s and access for that user is blocked. If the Blocking Timer expires, or the correct password is entered before Attempts Remain reaches zero, then the Attempts Remain is reset to the Attempts Limit.

Once the user entry is blocked, the Blocking Timer is initiated. If the locked out user is selected whilst the Attempts Remain is zero a 'USER LOCKED OUT' error message is displayed.

2.1.4 Inactivity Timer

The MiCOM device runs an inactivity timer, which means that it records the last time an action was taken by a user who was logged in.

If the user does not perform an action within a pre-defined interval, the user will be logged off. This is to reduce the risk that a device can accidentally be left open to access by unauthorized people.

The inactivity timer is separate for each interface.

The inactivity timer is configurable by using the SAT.

Important	**In case of a connection through an Ethernet interface, the actual inactive time depends on the setting value of both "Minimum inactivity period" & "[0E A7] ETH Tunl Timeout", the smaller value of both timers will be applied.**

Refer to the Table 12 for more details about the settings.

2.1.5 RBAC Recovery

RBAC recovery is the means by which the device can be reset to the factory RBAC settings if required. To obtain the recovery password, the customer must go to www.schneider-electric.com/ccc to raise a recovery password request and supply the IED *Security Code*.

Caution	**The "recovery" password gives you access to the Factory RBAC Configuration. This action deletes all existing users (and their passwords), and restores to Factory RBAC Configuration. Recover the RBAC does not affect relay proper settings and does not provoke reboot of the relay - the protection functions of the relay are always maintained.**

2.1.5.1 Generate Security Code

The security code is a 16-character ASCII string. It is a read-only parameter. The IED generates its own random security code. This is when a new code is generated:

- On power up
- On expiry of validity timer (see below)
- When the recovery password is entered

As soon as the security code is ***first*** displayed on the LCD display, a validity timer is started. This validity timer is set to 120 hours and is not configurable. The validity timer is not reset if you request a subsequent code within the 120 hour period.

To prevent accidental reading of the IED security code the cell will initially display a warning message on the front panel of the IED:

```
PRESS ENTER TO
READ SEC. CODE
```

The security code will be displayed on confirmation, whereupon the validity timer will be started. Note that the security code can only be read from the front panel.

Important	**The recover password will be invalid once the new Security Code is generated, so please make sure the IED is always powered on before you get the reover password, and make sure you input the recover password within 120 hours.**

2.1.5.2 Entry of the Recovery Password

The "recovery" password is intended for recovery only. It is not a replacement password that can be used continually. It can only be used once – for password recovery.

Entry of the recovery password is done at the local front panel and it causes the IED to reset the RBAC back to default.

On this action, the following message is displayed on the front panel of the IED:

```
RBAC reset done
Press any key
```

2.1.6 Port Disabling (Equipment Hardening)

The availability of unused ports could provide a security risk. Hence, unused ports can be disabled (also known as equipment hardening) – either via the front panel or by Easergy Studio software. An Engineer role is needed to perform this action.

These physical ports and logical ports can be enabled/disabled:

Port types	Menu text	Col	Row	Default Setting	Available Value
Physical Ports	Front port	25	05	Enable	Enable/Disable
	Rear Port 1	25	06	Enable	Enable/Disable
	Rear Port 2	25	07	Enable	Enable/Disable
	Ethernet Port 1	25	08	Enable	Enable/Disable
	Ethernet Port 1/2	25	09	Enable	Enable/Disable
	Ethernet Port 2/3	25	0A	Enable	Enable/Disable
	Ethernet Port 3	25	0B	Enable	Enable/Disable
Logical Ports	Courier Tunnel	25	0C	Enable	Enable/Disable
	IEC61850	25	0D	Enable	Enable/Disable
	DNP3oE	25	0E	Enable	Enable/Disable

Table 10 - Port hardening settings

Note	*The port disabling setting cells are not provided in the settings file. In addition, it is not possible to disable simultaneously more than one physical port or Logical port.* *New redundant Ethernet boards have three physical ports but total two interfaces. The actual disabled physical port is depended on the redundant communication mode (PRP, HSR, RSTP or Dual IP). Refer to the Dual Redundant Ethernet Board (Upgrade) (DREB) chapter (Px4x/EN EB) for more details.*

When the Ethernet board related physical ports or logical ports are disabled or enabled, the Ethernet card will reboot. The status of the ports will be available after reboot of the Ethernet board.

For more details about how to disable/enable the unused ports, please see sections:

- How to Disable a Physical Port
- How to Disable a Logical Port

2.1.7 Security Logs

The Security Logs needs to store logs from each item of equipment. These logs are generated by the system, and cannot be edited by the user. A variety of different items are recorded, including: bad/faulty access attempts, login attempts, authentication errors, changes to roles, users and access control lists, network backup and configuration changes, communication failures and so on.

Security logs emissions depend on the security standards that are configurable by the SAT.

The security logs will push to a Syslog server if the Syslog server IP address and Syslog server IP port are configured and connected.

SAT also can be used to explore the security logs but Easergy studio is not supported.

The settings for the security log standards and Syslog server IP address and ports are listed in the *Configurable cyber security settings* table. For more detail about the security log configuration, please refer to the SAT documentation.

Note	*The Security logs time stamp may be time shifted by several milliseconds compared with local event log.* *The security logs will not be generated if the Ethernet card is starting up.* *If the Syslog server is unavailable, the new logs will be stored and overwriting the oldest logs.*

This table lists the security logs categories available for each standard.

Log ID	Additional field	Explanation	Level	Standards					
				BDEW	E3	NERC CIP	IEEE 1686	IEC 62351	CS Phase 1
CONNECTION_SUCCESS	The additional field will contain the issuer of the connection: LOCAL or NETWORK	Successful connection	INFO	x	x	x	x		x
CONNECTION_FAILURE		Failed connection (wrong credentials)	WARNING	x	x	x	x		x
CONNECTION_FAILURE_ AND_BLOCK		Failed connection (wrong credentials) triggering the blocking of the account on the IED	DANGER	x	x	x	x		x
CONNECTION_FAILURE_ ALREADY_BLOCKED		Failed connection because of a blocked userID on this IED	DANGER	x	x	x	x		x
DISCONNECTION		Disconnection triggered by the peer /user	INFO	x	x	x	x		x
DISCONNECTION_TIMEOUT		Disconnection triggered by a timeout	INFO	x	x	x	x		x
CONTROL_OPERATION	Type & Data associated to the control	Trace and control / override of real data from a peer	INFO				x		
CONFIGURATION_ DOWNLOAD	Version	Download of the configuration file from the device - Files include PSL, Courier setting, DNP setting, MCL/CID and user curves (crv)	INFO				x		
CONFIGURATION_UPLOAD	Version	Upload of a new configuration file into the device - Files include PSL, Courier setting, DNP setting, MCL and user curves (crv)	INFO				x		
RBAC_UPDATE	Version	Update of the RBAC cache in the IED	INFO				x		x
SEC_LOGS_RETRIEVAL	Version	Retrieval of the security logs of the IED	INFO				x		
TIME_CHANGE	New & Old time	Modification of the time of the IED	INFO				x		
REBOOT_ORDER	None	Reboot order sent to the IED / IED start up	DANGER				x		x
PORT_MANAGEMENT	Port, action (enable / disable)	Any comms port enabled / disabled	INFO						x
AUTHORIZATION_REQ	Action, object	Any authorization request sent to the CS brick	INFO			x		x	x

Table 11 – Security logs recorded

2.1.8 Common Cyber Security Settings

The System Administrator can customize the cyber security settings at the SAT. The following table shows the common cyber security settings. Parts of settings also are visible on the IED with specific Courier cells but not editable in IED or Easergy Studio. These are shown in the right-hand columns of this table:

Setting in SAT	Default Setting	Available Value	Menu in IED	Col	Row
Minimum inactivity period	15	1 to 99 Minutes	-	-	-
If the user does not perform any action within this interval, the user will be logged off.					
Allow user locking	Yes	Yes/No	-	-	-
Option allows user account locking					
Maximum login attempts	5	1 to 99	Attempts Limit	25	02
The maximum failed password entry attempts, the user will lock once the attempts reached.					
Password attempts timer	3	1 to 30 Minutes	Attempts timer	25	03
The time for reset the attempts count to 0. The user got to maximum login attempts.					
Automatic user account unlocking	Yes	Yes/No	-	-	-
Enable/disable the attempts times aromatic reset function.					
Locking period duration	240	1 to 86400 Seconds	Blocking timer	25	04
The Locking period duration (seconds)					
Password Complexity	None	None / IEEE1686/ NERC	-	-	-
Set the password compliant standard.					
Log and monitoring standard	BDEW	BDEW / E3 /NERC-CIP / IEE1686 / IEC62351/ CS_PH1	-	-	-
Setup security log emission standard					
Syslog server IP address	0.0.0.0		-	-	-
Syslog server IP address					
Syslog server IP port	601	1 to 65535	-	-	-
Syslog server IP port					

Table 12 – Configurable cyber security settings

These settings show some common information about cyber security, which are not configurable whether by SAT, or Easergy Studio or the front panel.

Menu in IED	Col	Row	Description
User Banner	25	01	Show user banner information: ACCESS ONLY FOR AUTHORITY USERS
Attempts remain	25	11	Show the remains attempt times for user login.
Blk time remain	25	12	Show the remains time for blocked user to unlock
User Name	25	21~2F	Configured user name (in SAT)
Security Code	25	FE	The security code used to recovery the password.
RBAC Password	25	FF	Enter 16 characters recover password to recovery password

Table 13 – Un-configurable cyber security settings

2.1.9 Local Default Access

Local Default Access function can be disabled/enabled in the SAT.
The intention for Local Default Access function is to allow the user easy to access the IED from the front panel and without any authorization required. This means if the Local Default Access function is enabled, everyone will be authorized to access the front panel with associated Rights.
By default, the Local Default Access has the VIEWER role, it is also possible to associate the other Roles to the Local Default Access, which is configurable in the SAT.
Local Default Access function is only available in the front panel.
The Local Default Access login/logout process is invisible for the user.

2.2 MiCOM Px4x with CSL0- Simple Password Management

For MiCOM Px4x IED with CSL0, as the Security Administration Tool (SAT) is not supported, all the cyber security features which need SAT support will not be available.

This section describes the different implementations by comparing with CLS1.

The cyber security features that are not mentioned in this section will default to be the same as CSL1.

2.2.1 Password Management

For MiCOM Px4x IED with CSL0, SAT is not supported for the configuration, so only the alphanumeric password can be used.

- The alphanumeric password is settable via Easergy Studio and the Front panel
- Passwords may be any length between 1 and 16 characters long
- Passwords may contain any ASCII character in the range ASCII code 33 (21 Hex) to ASCII code 122 (7A Hex) inclusive
- No password compliance is required
- The alphanumeric password will used for Courier access and the front panel access

Arrow key password is not available for IED with CLS0.

2.2.2 Fixed Factory RBAC

For MiCOM Px4x IED with CSL0, the user list and its role/right will be fixed as factory RBAC and not configurable. Refer to the *Factory RBAC* table for more details.

2.2.3 Security Logs Services

The security logs services are not available for MiCOM Px4x IED with CSL0.

2.2.4 Cyber Security Settings

For MiCOM Px4x IED with CSL0, all cyber security settings are fixed as default setting and un-configurable. Refer to the *Configurable cyber security settings* table for the default settings.

2.2.5 Disable/Blank Password

For MiCOM Px4x IED with CSL0, it is possible to remove the user password. In MiCOM S1 Studio, this is achieved by click the BOX “Disable the password”. In the IED, this is achieved by setting the password as blank.

Once the password is disabled/blank, the user can login to the IED directly and there is no need to enter the password.

3 HOW TO USE CYBER SECURITY FEATURES

These sections shows the most common tasks associated with Cyber Security features. For many of these tasks, the steps you take are the same as you have performed previously; with the main changes being in the steps you use to login and/or logout.

3.1 How to Login

3.1.1 Local Default Access

If the Local Default Access is enabled, the user may login to the front panel with associated roles.

See Table 14 for the applied cases.

3.1.2 Auto Login

Auto login means the user will login the IED automatically and no need to select the user name and enter the password. In this case, the user will be authorized with relevant rights. The auto login will be applied in these cases:

CS Version	Interface	RBAC/PW Cases	Login Process
CSL1	Front panel	Factory RBAC	Auto login with **EngineerLevel**
		Customized RBAC	Local Default Access Enabled: Login with **Local Default Access** Local Default Access Disabled: Login with **Prompt User List**
	Courier Interface	All cases	Login with **Prompt User List**
CSL0	Front panel	Factory RBAC	Auto login with **EngineerLevel**
		Password changed	**EngineerLevel** password is “AAAA” or is disabled/blank: Auto login with **EngineerLevel** **OperatorLevel** password is “AAAA” or is disabled/blank: Auto login with **OperatorLevel** **EngineerLevel** and **OperatorLevel** password changed: Auto login with **ViewerLevel Access**
	Courier Interface	Factory RBAC	Auto login with **EngineerLevel**
		Password changed	**EngineerLevel** password is “AAAA” or is disabled/blank: Auto login with **EngineerLevel** **OperatorLevel** password is “AAAA” or is disabled/blank: Auto login with **OperatorLevel** **EngineerLevel** and **OperatorLevel** password changed: Login with **Prompt User List**

Table 14 – Auto Login process

For more details about the Factory RBAC, please refer to Table 9.

3.1.3 Login with Prompt User List

This login process will happen if:

- The Auto login process is not applied.
- Or high authorization is required for the current operation.

In this case, the IED will prompt the user list, and the user needs to select proper user name and enter the password to login.

3.2 How to Logout

3.2.1 How to Logout at the IED

For security consideration, it would be better to “logout' the IED once the configuration done. You can do this by going up to the default display. When you are at the default display and you press the ‘Cancel’ button, you may be prompted to log out with the following display:

```
ENTER TO LOGOUT
CLEAR TO CANCEL
```

You will be asked this question if you are logged in.

If you confirm, the following message is displayed for 2 seconds:

```
LOGGED OUT
User Name
```

If you decide not to log out (i.e. you cancel), the following message is displayed for 2 seconds.

```
LOGOUT CANCELLED
User Name
```

Note	*The MiCOM IED runs a timer, which logs the user out after a period of inactivity. For more details, refer to the Inactivity Timer section.*

3.2.2 How to Logout at Easergy Studio

- Right-click on the device name and select Log Off.
- In the Log Off confirmation dialog click Yes.

3.3 How to Disable a Physical Port

Using Easergy Studio or the front panel it is possible to disable unused physical ports. This can not be done by the SAT. By default, an Engineer-role is needed to perform this action.

To prevent accidental disabling of a port, a warning message is displayed according to whichever port is required to be disabled. For example if rear port 1 is to be disabled, the following message appears:

```
REAR PORT 1 TO BE
DISABLED.CONFIRM
```

There are between two and four ports eligible for disablement:

- Front port
- Rear port 1
- Rear port 2 (available in the specific models)
- Ethernet port (available in the specific models)

Important	**It is not possible to disable a port from which the disabling port command originates.**

3.4 How to Disable a Logical Port

Using Easergy Studio or the front panel it is possible to disable unused logical ports. This can't be done by the SAT. An Engineer-role is needed to perform this action.

Caution **Disabling the Ethernet port will disable all Ethernet based communications.**

If it is not desirable to disable the Ethernet port, it is possible to disable selected protocols on the Ethernet card and leave others functioning.

These protocols can be disabled:

- IEC61850 (available in the specific models)
- Courier Tunnelling (available in the specific models)
- IEC61850 + DNPoE (available in the specific models)

3.5 How to Secure a Function Key (When Available)

In cyber security implementation, this function has been linked to the front panel authorization.

- When the function key pressed, if there is no user login in the front panel or the logged- in user is not authorized, a prompt message will be raised in the front panel to ask the user to login. Once the user is logged-in, they need to press the function key again to execute the command.
- If the user is already logged in and the authorization is OK, the command will be executed immediately.
- By default, the OPERATOR or ENGINEER Roles are able to operate the function keys.
- The function key will be executed immediately if the auto login process is applied and the user is authorized.
- If unauthorized users press the Function Key during the setting change, they need to commit the changes first then login with authorized user to operate the function key.

4 GLOSSARY FOR CYBER SECURITY

Term	Meaning
CIP Standards	Critical Infrastructure Protection standards. NERC CIP standards have been given the force of law by the Federal Energy Regulatory Commission (FERC)
DCS	Distributed Control System
HMI	Human Machine Interface
IED	Intelligent Electronic Device. It is a power industry term to describe microprocessor-based controllers of power system equipments (e.g. Circuit breaker, transformer, etc)
LOGS	All the operations related to the security (connection, configuration…) are automatically caught in events that are logged in order to provide a good visibility of the previous actions to the security administrators.
MIB	Management Information Base
NERC	North American Electric Reliability Corporation
RBAC	Role Based Access Control. Authentication and authorization mechanism based on roles granted to a user. Roles are made of rights, themselves being actions that can be applied on objects. Each user's action is authorized or not based on his roles
Roles	A role is a logical representation of a person activity. This activity authorizes or forbids operations within the tool suite thanks to permissions that are associated to the role. A role needs to be attached to a user account to have a real purpose.
SAM	Security Administration Module. Device in charge of security management on an IP-over-Ethernet network.
SAT	Security Administration Tool TSF based application used to define and create security configuration
Secured IED	Devices embedding security mechanisms defined in the security architecture document
Security Administrator	A user of the system granted to manage its security
TAT	Transfer Administration Tool
Unsecured IED	Relay/IEDs with no security mechanisms.

Table 15 – Glossary for cyber security

DUAL REDUNDANT ETHERNET BOARD (DREB)

CHAPTER 19

Date (month/year):	07/2018			
Products covered by this chapter:	This chapter covers the specific versions of the MiCOM products listed below. This includes ***only*** the following combinations of Software Version and Hardware Suffix.			
Hardware Suffix:	P141/P142/P143 P145 P445 P44x (P442/P444) P44y (P443/P446)	L M L M M	P54x (P543/P544/P545/P546) P642 P643/P645 P746 P841A (one circuit breaker) P841B (two circuit breakers)	M L M M M M
Software Version:	P14x (P141/P142/P143/P145) P445 P44x (P442/P444) P44y (P443/P446)	B4 J9 E3 H9	P54x (P543/P544/P545/P546) P64x (P642/P643/P645) P746 P841A P841B	H9 B4 B5/C5 G9 H9
Connection Diagrams:	P14x (P141, P142, P143 & P145): 10P141xx (xx = 01 to 02) 10P142xx (xx = 01 to 05) 10P143xx (xx = 01 to 11) 10P145xx (xx = 01 to 11) P44x (P442 & P444): 10P44201 (SH 1 & 2) 10P44202 (SH 1) 10P44203 (SH 1 & 2) 10P44401 (SH 1) 10P44402 (SH 1) 10P44403 (SH 1 & 2) 10P44404 (SH 1) 10P44405 (SH 1) 10P44407 (SH 1 & 2) P44y (P443 & P446): 10P44303 (SH 01 and 03) 10P44304 (SH 01 and 03) 10P44305 (SH 01 and 03) 10P44306 (SH 01 and 03) 10P44600 10P44601 (SH 1 to 2) 10P44602 (SH 1 to 2) 10P44603 (SH 1 to 2) P445: 10P445xx (xx = 01 to 04)		P54x (P543, P544, P545 & P546): 10P54302 (SH 1 to 2) 10P54303 (SH 1 to 2) 10P54400 10P54404 (SH 1 to 2) 10P54405 (SH 1 to 2) 10P54502 (SH 1 to 2) 10P54503 (SH 1 to 2) 10P54600 10P54604 (SH 1 to 2) 10P54605 (SH 1 to 2) 10P54606 (SH 1 to 2) P547: 10P54702xx (xx = 01 to 02) 10P54703xx (xx = 01 to 02) 10P54704xx (xx = 01 to 02) 10P54705xx (xx = 01 to 02) P64x (P642, P643 & P645): 10P642xx (xx = 01 to 10) 10P643xx (xx = 01 to 06) 10P645xx (xx = 01 to 09) P746: 10P746xx (xx = 00 to 21) P841: 10P84100 10P84101 (SH 1 to 2) 10P84102 (SH 1 to 2) 10P84103 (SH 1 to 2) 10P84104 (SH 1 to 2) 10P84105 (SH 1 to 2)	

CONTENTS

Page (EB) 19-

FIGURES

Page (EB) 19-

TABLES

1 INTRODUCTION

The redundant Ethernet board assures redundancy at IED level. It is fitted into the following MiCOM IEDs from Schneider Electric.

- P14x = P141, P142, P143, P145
- P24x = P241, P242, P243
- P34x = P341, P342, P343, P344, P345
- P44x = P442, P444
- P44y = P443, P446
- P445
- P54x = P543, P544, P545, P546
- P547
- P64x = P642, P643, P645
- P74x = P741, P743, P746
- P841
- P849

1.1 Standard Safety Statements

For safety information please see the Safety Information chapter of the relevant Px4x Technical Manual.

2 HARDWARE DESCRIPTION

IEC 61850 works over Ethernet. Three boards are available:

- 1RJ45 Port Ethernet Board
- 3RJ45 Ports Redundant Ethernet Board
- 2LC+1RJ45 Ports Redundant Ethernet Board.

All are required for communications but 3RJ45 Ports and 2LC+1RJ45 Ports Redundant Ethernet Board allow an alternative path to be always available, providing bumpless redundancy.

Industrial network failure can be disastrous. Redundancy provides increased security and reliability, but also devices can be added to or removed from the network without network downtime.

The following list shows Schneider Electric's implementation of Ethernet redundancy, which has two variants with embedded IEC 61850 over Ethernet, plus PRP, HSR and RSTP redundancy protocols.

- Parallel Redundancy Protocol (PRP)/High-availability Seamless Redundancy (HSR)/Rapid Spanning Tree Protocol (RSTP) with 1310 nm multi mode 100BaseFx fiber optic Ethernet ports (LC connector) and modulated/un- modulated IRIG-B input. Part number 2072069A01.

Note	*The board offers compatibility with any PRP/HSR/RSTP device.*

- Parallel Redundancy Protocol (PRP)/High-availability Seamless Redundancy (HSR)/Rapid Spanning Tree Protocol (RSTP) with 100BaseTx Ethernet ports (RJ45) and modulated/un- modulated IRIG-B input. Part number 2072071A01.

Note	*The board offers compatibility with any PRP/HSR/RSTP device.*

The redundant Ethernet board is fitted into Slot A of the IED, which is the optional communications slot. Each Ethernet board has three MAC addresses for two groups, one group (PORT 1) including one host MAC address, the other group (PORT 2 & 3) used for redundant application, including one host MAC address and one redundant agency device MAC address. Two host MAC addresses of the IED are printed on the rear panel of the IED.

In additional above for HSR/PRP/RSTP redundant protocols, the redundant Ethernet board also can operate on Dual IP mode. In this case, each Ethernet board has two host MAC addresses.

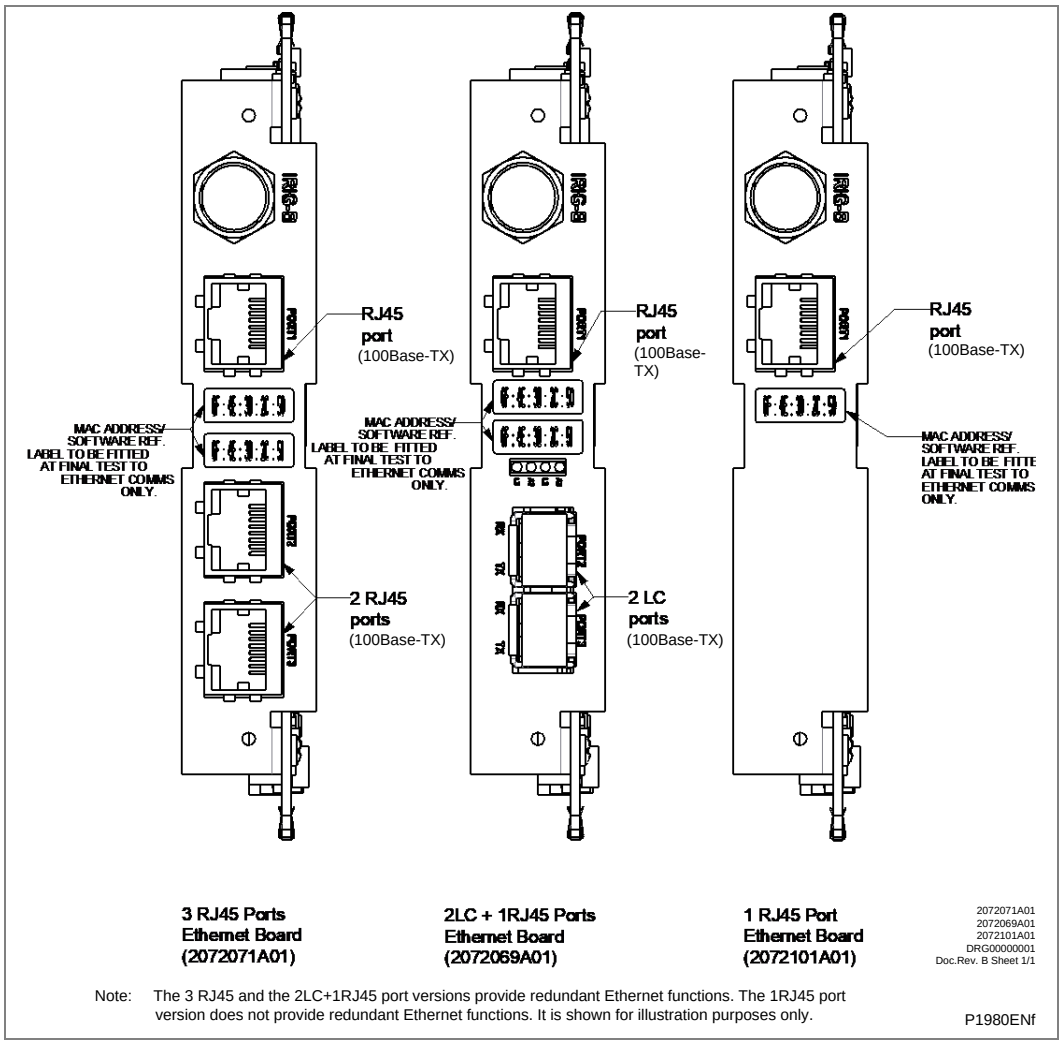


Figure 1 - Ethernet board connectors (3 RJ45 or 2 LC + RJ45 or 1 RJ45)

2.1 IRIG-B Connector

This is available as a modulated/un-modulated input.
See section 6.1.

2.2 LEDs

LED	Function	On	Off	Flashing
Green	Link	Link ok	Link broken	
Yellow	Activity			Traffic activity

Table 1 - LED functionality

2.3 Optical Fiber Connectors

Use 1310 nm multi mode 100BaseFx and LC connectors.
See Figure 1 and section 6.1.

Connector	PRP	HSR	RSTP
2	R_X	R_X	R_X
2	T_X	T_X	T_X
3	R_X	R_X	R_X
3	T_X	T_X	T_X

Table 2 - Optical fiber connector functionality

3 REDUNDANCY PROTOCOLS

There are two redundancy protocols available:

- PRP (Parallel Redundancy Protocol)
- HSR (High-availability Seamless Redundancy)
- RSTP (Rapid Spanning Tree Protocol)

3.1 Parallel Redundancy Protocol (PRP)

When the upper protocol layers send a data packet, the PRP interface creates a “twin packet” from this. The PRP interface then transmits redundant data packet of the twin pair to each participating LAN simultaneously. As they are transmitted via different LANs, the data packets may have different run times.
The receiving PRP interface forwards the first packet of a pair towards the upper protocol layers and discards the second packet. When viewed from the application, a PRP interface functions like a standard Ethernet interface.
The PRP interface or a Redundancy Box (RedBox) injects a Redundancy Control Trailer (RCT) into each packet. The RCT is a 48-bit identification field and is responsible for the identification of duplicates. This field contains, LAN identification (LAN A or B), information about the length of the payload, and a 16-bit sequence number. The PRP interface increments the sequence number for each packet sent. Using the unique attributes included in each packet, such as Physical MAC source address and sequence number, the receiving RedBox or Double Attached Node (DAN) interface identifies and discards duplicates.
Depending on the packet size, with PRP it attains a throughput of 93 to 99% of the available bandwidth.

3.1.1 PRP Network Structure

PRP uses two independent LANs. The topology of each of these LANs is arbitrary, and ring, star, bus and meshed topologies are possible.
The main advantage of PRP is loss-free data transmission with an active (transit) LAN. When the terminal device receives no packets from one of the LANs, the second (transit) LAN maintains the connection. As long as 1 (transit) LAN is available, repairs and maintenance on the other (transit) LAN have no impact on the data packet transmission.
The elementary devices of a PRP network are known as RedBox (Redundancy Box) and DANP (Double Attached Node implementing PRP).
Both devices have one connection each to the (transit) LANs.
The devices in the (transit) LAN are conventional switches that do not require any PRP support. The devices transmit PRP data packets transparently, without evaluating the RCT information.
Terminal devices that are connected directly to a device in the (transit) LAN are known as SAN (Single Attached Node). If there is an interruption, these terminal devices cannot be reached via the redundant line. To use the uninterruptible redundancy of the PRP network, you integrate your device into the PRP network via a RedBox.

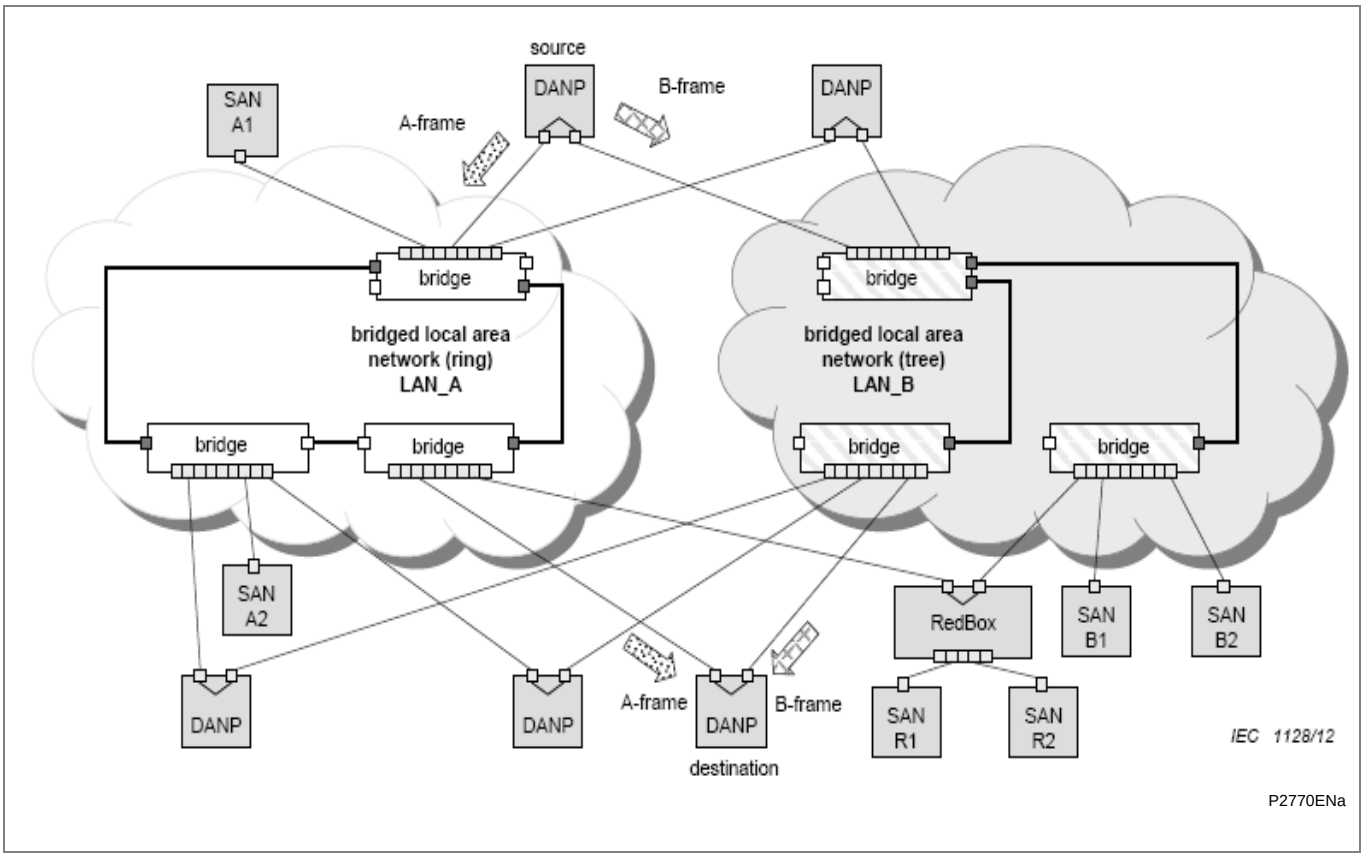


Figure 2 - PRP example of general redundant network

3.1.2 Example Configuration

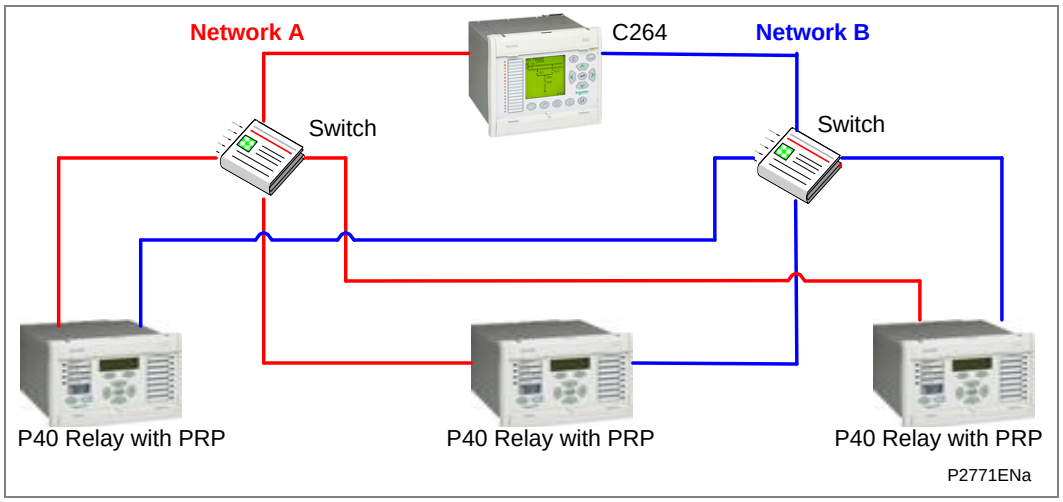


Figure 3 - PRP Relay Configuration

3.2 High-availability Seamless Redundancy (HSR)

High-availability Seamless Redundancy (HSR) can only be used in a ring topology, This section describes the application of the PRP principles (IEC 62439-3- Clause 4) to implement a High-availability Seamless Redundancy (HSR), retaining the PRP property of zero recovery time, applicable to rings. With respect to PRP, HSR allows you to greatly reduce the network infrastructure. With respect to rings based on IEEE 802.1D (RSTP), IEC 62439-2 (MRP), IEC 62439-6 (DRP) or IEC 62439-7 (RRP), the available network bandwidth for network traffic is somewhat reduced depending on the type of traffic. Nodes within the ring are restricted to be HSR-capable bridging nodes, thus avoiding the use of dedicated bridges. Singly Attached Nodes (SANs) such as laptops or printers cannot be attached directly to the ring, but need attachment through a RedBox (redundancy box).

3.2.1 HSR Network Structure

As in PRP, a node has two ports operated in parallel; it is a DANH (Doubly Attached Node with HSR protocol).
A simple HSR network consists of doubly-attached bridging nodes, each having two ring ports, interconnected by full-duplex links, as shown in these examples for a ring topology:

- Figure 4 (multicast)
- Figure 5 (unicast)

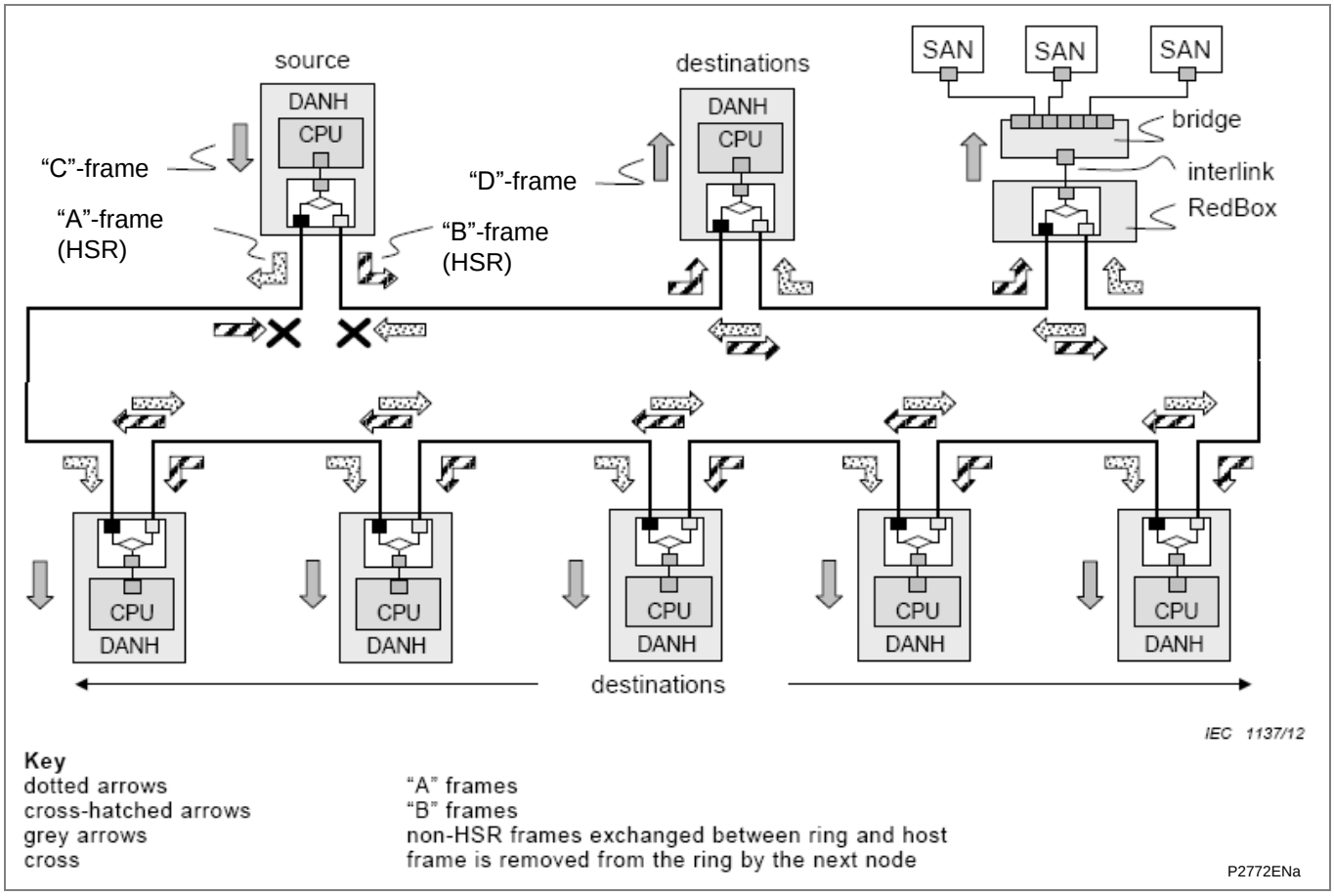


Figure 4 - HSR example of ring configuration for multicast traffic

A source DANH sends a frame passed from its upper layers ("C" frame), prefixes it by an HSR tag to identify frame duplicates and sends the frame over each port ("A"-frame and "B"-frame). A destination DANH receives, in the fault-free state, two identical frames from each port within a certain interval, removes the HSR tag of the first frame before passing it to its upper layers ("D"-frame) and discards any duplicate.

The nodes support the IEEE 802.1D bridge functionality and forward frames from one port to the other, except if they already sent the same frame in that same direction. In particular, the node will not forward a frame that it injected into the ring.

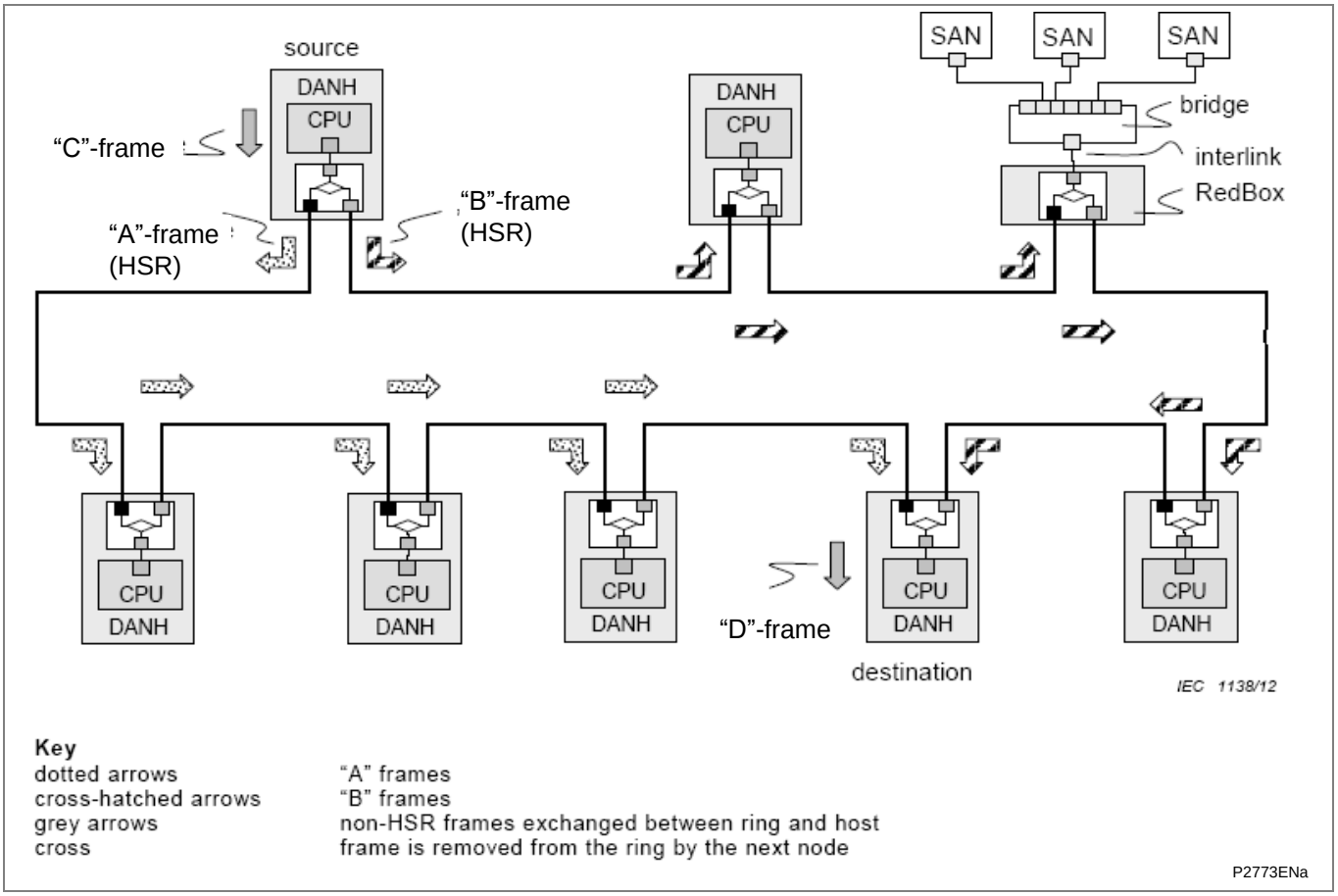


Figure 5 - HSR example of ring configuration for unicast traffic

A destination node of a unicast frame does not forward a frame for which it is the only destination, except for testing.

Frames circulating in the ring carry the HSR tag inserted by the source, which contains a sequence number. The doublet {source MAC address, sequence number} uniquely identifies copies of the same frame.

Singly Attached Nodes (SANs), for instance maintenance laptops or printers cannot be inserted directly into the ring since they have only one port and cannot interpret the HSR tag in the frames. SANs communicate with ring devices through a RedBox (redundancy box) that acts as a proxy for the SANs attached to it, as shown in the diagram.

Connecting non-HSR nodes to ring ports, breaking the ring, is allowed to enable configuration. Non-HSR traffic within the closed ring is supported in an optional mode.

3.2.2 Example Configuration

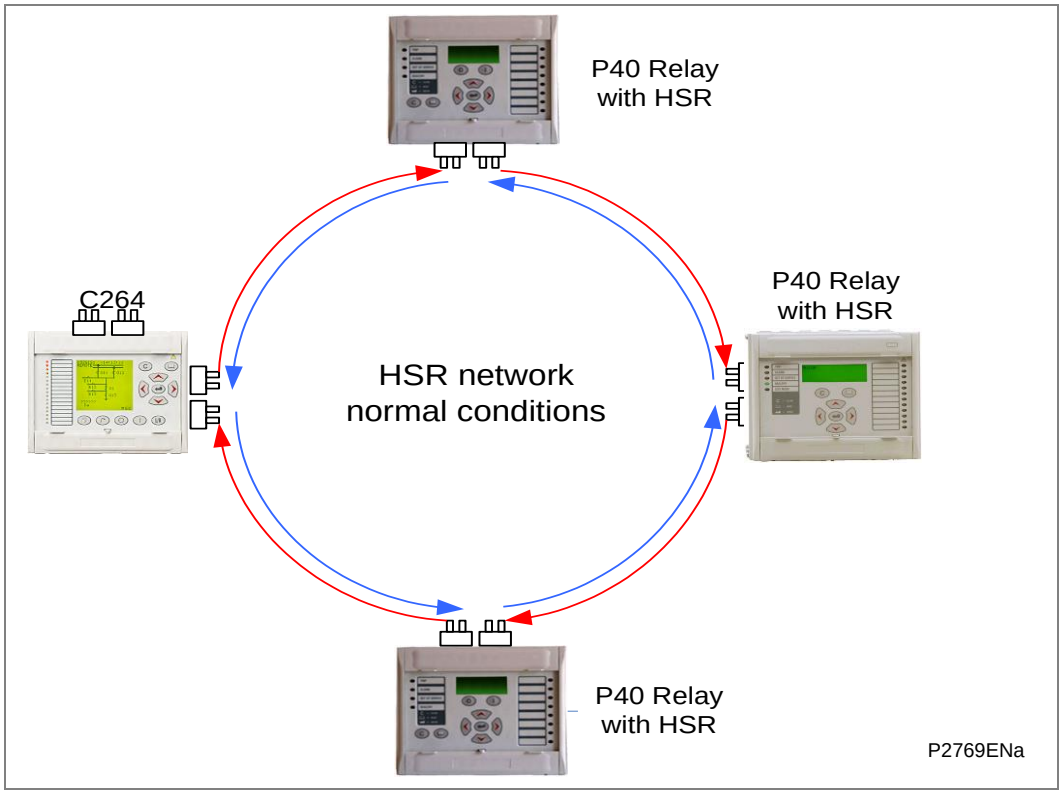


Figure 6 - HSR Relay Configuration

3.3 Rapid Spanning Tree Protocol (RSTP)

3.3.1 RSTP Network Structure

RSTP is a standard used to quickly reconnect a network fault by finding an alternative path, allowing loop-free network topology. Although RSTP can recover network faults quickly, the fault recovery time depends on the number of devices and the topology. The recovery time also depends on the time taken by the devices to determine the root bridge and compute the port roles (discarding, learning, forwarding). The devices do this by exchanging Bridge Protocol Data Units (BPDUs) containing information about bridge IDs and root path costs.

See the IEEE 802.1D 2004 standard for further information.

3.3.2 Example Configuration

The Px4x redundant Ethernet board uses the RSTP protocol (802.1w), so a Px4x can attach onto a network as shown in Figure 7:

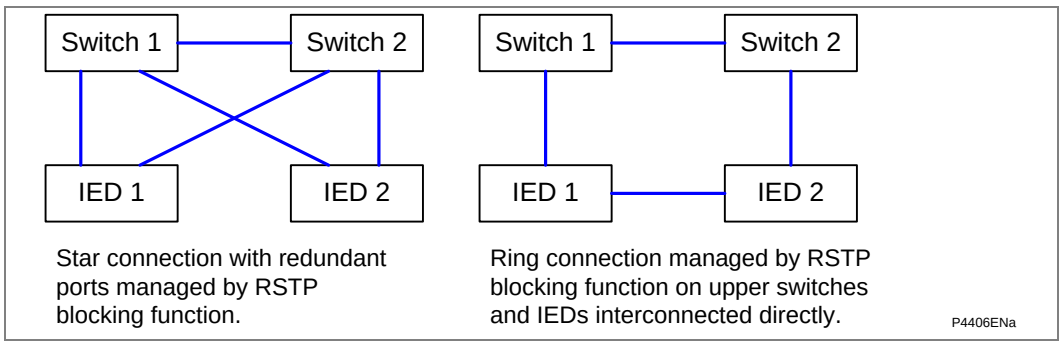


Figure 7 - Px4x attached to a redundant Ethernet star or ring circuit

The RSTP solution is based on open standards. It is therefore compatible with other manufacturers' IEDs that use the RSTP protocol. The RSTP recovery time is typically 300ms but it increases with network size.

3.4 Generic Functions for all Redundant Ethernet Boards

The following apply to the redundant Ethernet protocols (PRP, HSR and RSTP).

3.4.1 Priority Tagging

802.1p priority is enabled on all ports.

3.4.2 Simple Network Time Protocol (SNTP)

Simple Network Time Protocol (SNTP) is supported by both the IED and the redundant Ethernet switch. SNTP is used to synchronize the clocks of computer systems over packet-switched, variable-latency data networks. A jitter buffer is used to reduce the effects of variable latency introduced by queuing in packet switched networks, ensuring a continuous data stream over the network.

The IED receives the synchronization from the SNTP server. This is done using the IP address of the SNTP server entered into the IED from the IED Configurator software.

3.4.3 Dual Ethernet Communication (Dual IPs)

3.4.3.1 Dual IP Introduction

Dual IP means the IED provides two independent IEC 61850 interfaces, and both these interfaces support MMS and GOOSE message.

The IED which supports Dual IP can provide the customer with more flexible network connections: two fully segregated Station BUS networks, or one Station Bus and one Process Bus (for GOOSE message transmission).

Dual IP is not mutually exclusive with PRP/HSR/RSTP - Dual IP is automatically supported even if the IED is operate under HSR/PRP/RSTP mode.

3.4.3.2 Dual IP in MiCOM

Dual IP is only supported for devices with the new Ethernet board assembly. This is shown by the model number, where the 7th digit is either hardware option Q or R. These boards have three Ethernet ports, as shown in Figure 1.

A setting is provided in the HMI to switch the operation mode between PRP / HSR / RSTP / Dual IP.

Operation mode	Port 1	Port 2	Port3
PRP	Interface 1	Interface 2 (PRP)	Interface 2 (PRP)
HSR	Interface 1	Interface 2 (HSR)	Interface 2 (HSR)
RSTP	Interface 1	Interface 2 (RSTP)	Interface 2 (RSTP)
Dual IP	* Interface 1 on Port 1 or Port 2		Interface 2

** Note* *In Dual IP mode, interface 1 can be available on port 1 or port 2. If both of port 1 and port 2 are connected, only port 1 will work.*

Table 3 - Ethernet ports operation mode

For each interface, the fully IEC 61850 functions (GOOSE and MMS services) are supported independently.

For outgoing GOOSE messages, you need to configure whether a message is to be transmitted across one or both Ethernet connections. You also need to configure the destination parameters such as multicast MAC address, AppID, VLAN, etc.

Two communication parameters also need to be configured for each interface (IP address, MAC address, subnet mask). For the CID which is exported from SCD file, the second interface communication parameters are not configured. This needs to be done by manually editing in the IED configurator (this being invisible by the SCD file). This process needs to be completed before the exported CID file is downloaded to the IED. (this being invisible by the SCD file).

3.4.3.3 Typical User Cases

Below for Interface 1 and Interface 2, from a functional point of view it is same. The customer has flexibility to define the functionality according their requirements.

- Both for Station Bus to have duplicated network for DCS.
- One for Station Bus and one for process bus (Goose message)

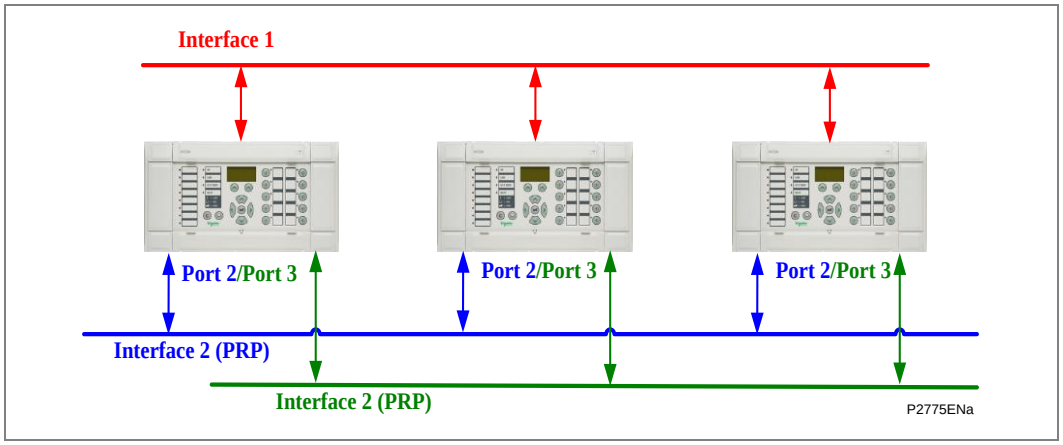


Figure 8 - PRP + Dual IP (Ethernet Mode PRP)

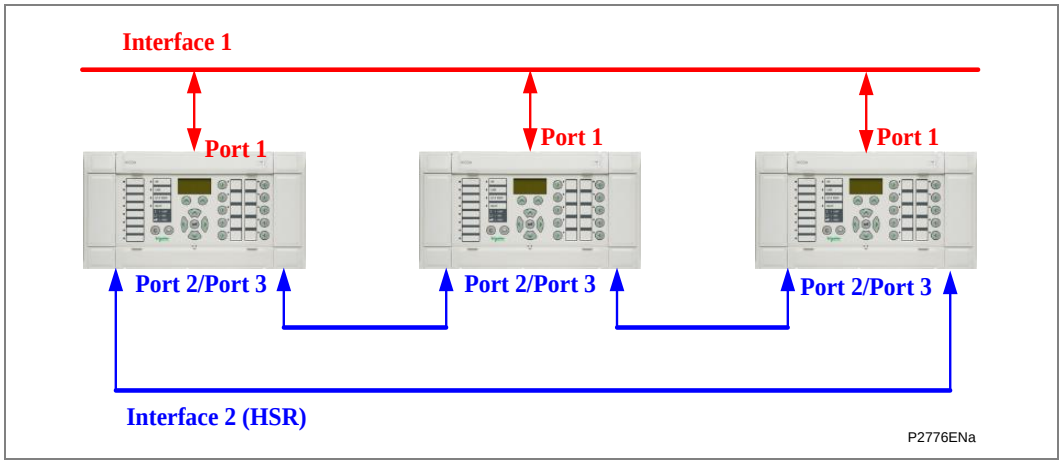


Figure 9 - HSR + Dual IP (Ethernet Mode HSR)

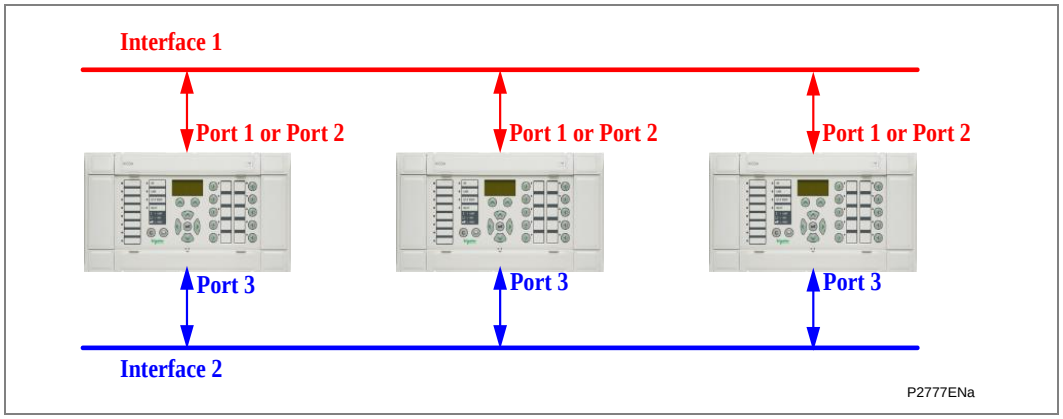


Figure 10 - Dual IP (Ethernet Mode Dual IP)

3.4.4 Precision Time Protocol (PTP)

Precision Time Protocol (PTP) provides higher time accuracy (500us) than IRIG-B.

PTP communication uses the IEEE 802.3 protocol.

3.4.4.1 Introduction to the IEEE1588 Standard

A protocol is provided in this standard that enables precise synchronization of clocks in measurement and control systems implemented with technologies such as network communication, local computing, and distributed objects. The protocol is applicable to systems communicating via packet networks. Heterogeneous systems are enabled that include clocks of various inherent precision, resolution, and stability to synchronize. System-wide synchronization accuracy and precision in the sub-microsecond range are supported with minimal network and local clock computing resources. Simple systems are installed and operated without requiring the management attention of users because the default behaviour of the protocol allows for it.

3.4.4.2 PTP Implementation

PTP implementation is compliant with IEC61850-9-3.

PTP communication is supported in all Ethernet interfaces (redundant ports or single port) with all communication protocols (PRP/HSR/RSTP).

A Slave only Ordinary Clock (OC) is supported by the single port of the Ethernet boards. A Transparent Clock (TC) is supported on the HSR ring.

Peer-to-Peer mode and Best Master Clock algorithm (BMCA) are supported.

The priority of time synchronization is PTP then, if not provided IRIG-B then, if not provided SNTP.

PTP is only supported by the model number, where the 7th digit is Q, R or S.

3.4.4.3 PTP Settings

PTP Settings	Value	Description
DATE AND TIME		
1588 Sync	0: Disabled 1: Interface1 Enabled 2: Interface2 Enabled 3: Interface1&2 Enabled	For Q or R board, the setting value can be 0,1,2,3. For S board, the setting value can be 0, 1. If the setting value is 0, PTP communication is disabled.
1588 DomainNum	[0, 255]	Define the permitted domainNumber of master clock. If the domainNumber in received PTP message header is different from the configuration parameter, the message will be rejected.
1588 PdelInterv	[0, 5]	Define the PDelay interval (2^0~2^5) sent by IED.

PTP is linked with Interface 2 configuration. If there is no IP configured for Interface 2, PTP on interface 2 will not work.

3.4.4.4 IEC61850-9-3 PICS

PICS proforma reference	Capability	Base	Support
CLOCK_TYPE_OC	clock is OC according to this base	m	True
CLOCK_TYPE_TC	clock is TC according to this base	m	True
CLOCK_TYPE_BC	clock is BC according to this base	m	False
NR_PORTS	number of clock ports (total)	m	2

PICS proforma reference	Capability	Base	Support
PORTS_STEP	1: all ports support 1- step on egress 2: all ports support 2- step on egress 3: all ports support both 1 - step and 2.	m	{1 or 2} For PRP/HSR/RSTP mode: Port1 support 2 step on egress. Port2&3 support 1 step on egress For Dual IP mode: Port1&2 support 2 step on egress Port3 support 1 step on egress
SLAVE_ONLY	all ports of the clock are slave - only	m	True
TIME_TRACEABLE	connectable to a time reference outside of PTP (e.g. GPS)	m	
FREQ_TRACEABLE	connectable to a frequency reference outside of PTP (e.g. GPS)	m	
DAC	doubly attached OC	o	True (in HSR, PRP or RSTP mode)
PORTS_PAIRED	paired clock ports for redundancy (e.g. {3-4})	o	{0,1} 0=A, 1=B
REDBOX_DATC	Redbox as TC	o	
REDBOX_SLTC	Redbox as Stateless TC	o	
REDBOX_TWBC	Redbox as three- way BC	o	
REDBOX_DABC	Redbox as DAC BC	o	
MIB_SNMP	supports MIB of IEC 2439-3 :2015, Annex E	m	False
MIB_61850	supports IEC 6 1859- 90- 4 Clock Objects	m	False
MIB_OTHER	clock supports fixed values or a mechanism defined by the manufacturer (If True, this list is appended to this PICS)	m	True Some management requests for time synchronization information are supported in PTP protocol. The following lists the supported datasets. CURRENT_DATA_SET - stepsRemoved - offsetFromMaster - meanPathDelay PORT_DATA_SET - portIdentity - portState - logMinDelayReqInterval - peerMeanPathDelay - logAnnounceInterval - announceReceiptTimeout - logSyncInterval - delayMechanism - logMinPdelayReqInterval - versionNumber

4 CONFIGURATION

The new redundant Ethernet board supports three communication operation modes. These can be achieved by change the setting in HMI. It is not necessary to flash the firmware.

Also for the two interfaces, the communication parameters need to be configured. These include the IP address, MAC address, and subnet mask, etc.

For redundant protocols, the communication parameters for redundant agency device also need to be configured.

4.1 Configuring Ethernet Communication Mode

Menu Text	Cell Add.	Default Setting	Available Setting
ETH COMM Mode	0016	Dual IP	Dual IP, PRP, HSR or RSTP
Sets the redundancy protocol. This setting can only be changed via the UI. The setting is linked with Interface2. If there is no IP configured for Interface 2, the setting is not configurable. By default, this setting is configurable thanks to the default IP.			

Table 4 - Ethernet communication mode setting

4.2 Configuring the IED Communication Parameters

The communication parameter for each interface is configured using the IED Configurator software in MiCOM S1 Studio. **Customers can configure these parameters according to their needs, but the IP address for these two interfaces should not be in the same subnet.**

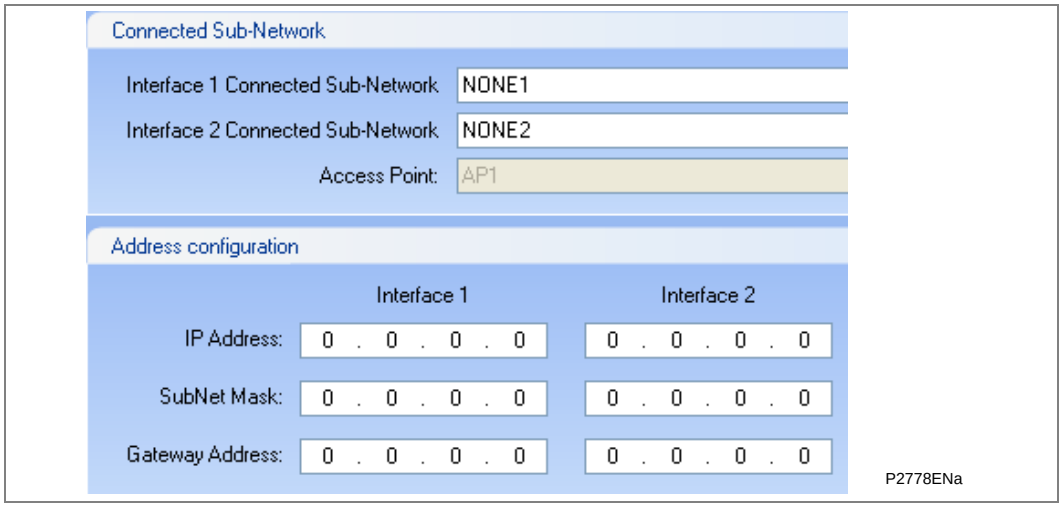


Figure 11 - Communication Parameters for two Interfaces

To use the device configuration with Courier Tunneling, for each interface, a default IP address has been applied. The default IP address for the first three bytes is fixed for each interface as below:

Interface	First three Bytes for IP address
Interface 1	169.254.0.xxx
Interface 2	169.254.1.yyy

Note *xxx = Mod (the last byte MAC1 address, 128) + 1*
yyy = Mod (the last byte MAC2 address, 128) + 1

Table 5 - First three bytes for default IP address

The default IP address can be found in the ***IED CONFIGURATOR*** column. Also, you can also calculate it according the MAC address label which is mounted on the rear panel of the Ethernet card.

4.3 Configuring GOOSE Publish Parameters

For outgoing GOOSE messages, you need to configure whether a message is to be transmitted over one or both Ethernet connections. You also need to configure the destination parameters including multicast MAC address, AppID, VLAN, etc.

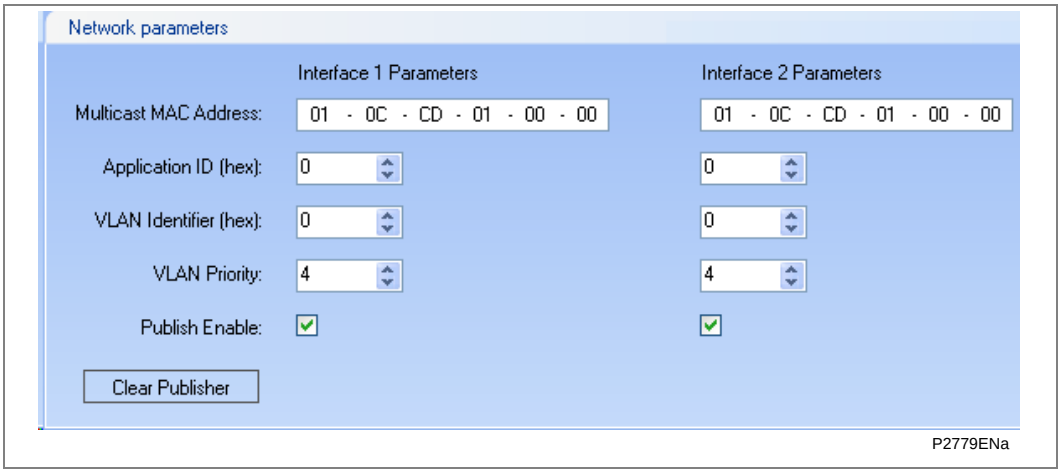


Figure 12 - Goose Publish Parameters for two Interfaces

5 COMMISSIONING

5.1 PRP Star Connection

The following diagram shows the Px4x IEDs with the PRP variant of Redundant Ethernet boards connected in a STAR topology. The STAR topology can have one or more high-end PRP-enabled Ethernet switches to interface with another network. The Ethernet switch is an HSR-enabled switch with a higher number of ports, which should be configured as the root bridge.

The number of IEDs that can be connected in the STAR can be up to 128.

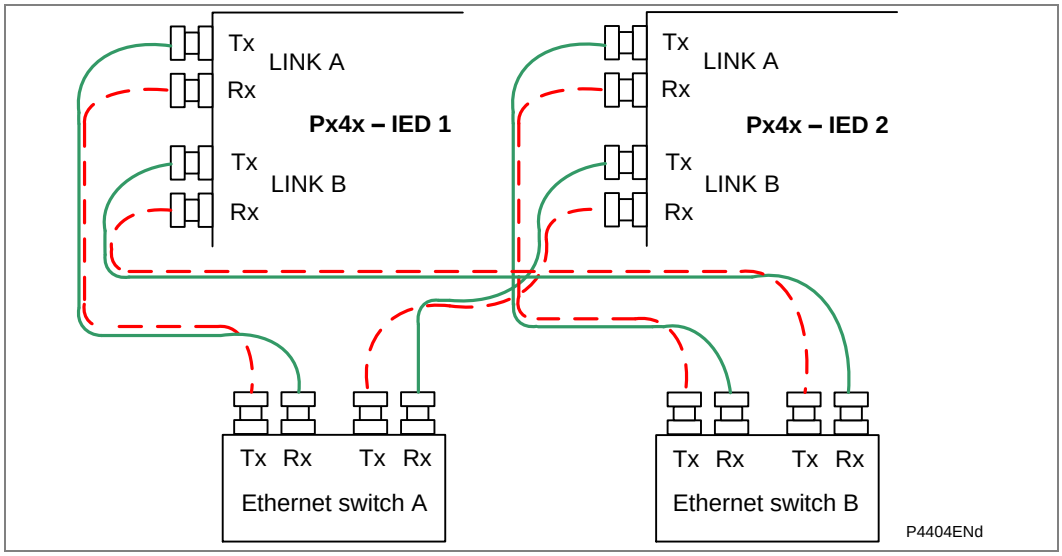


Figure 13 - PRP star connection

5.2 HSR Ring Connection

The following diagram shows the Px4x IEDs (Px4x - IED 1 to IED N) with the HSR variant of redundant Ethernet boards connected in a ring topology. The ring topology can have one or more high-end HSR-enabled Ethernet switches to interface with another network or a control center. The Ethernet switch is an HSR enabled switch with a higher number of ports.

The Ethernet switch, which is connected to the controlling PC, should be configured as the root bridge.

The number of IEDs that can be connected in the ring can be up to 128.

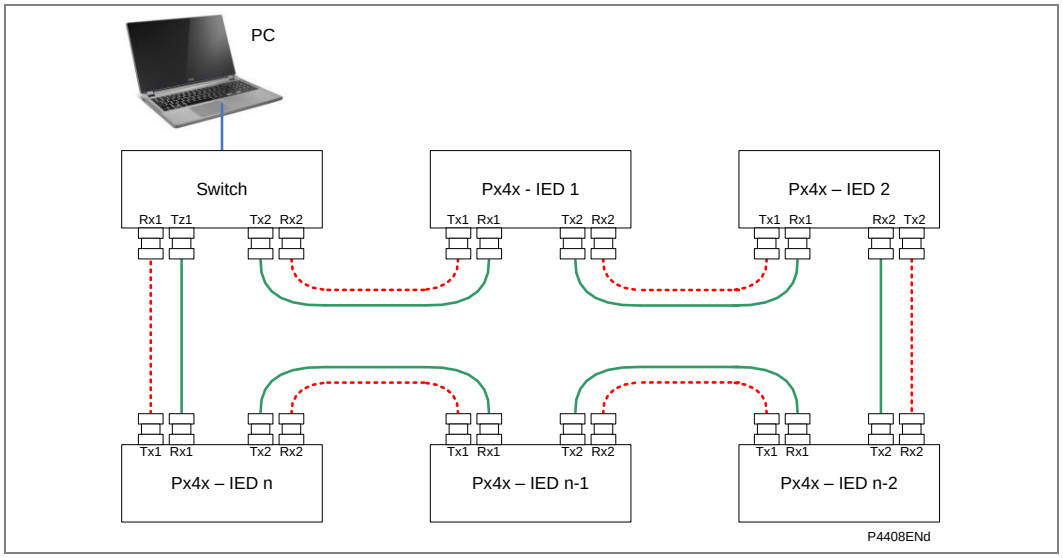


Figure 14 - HSR ring topology

The number of IEDs that can be connected in the ring can be up to 128.

5.3 RSTP Ring Connection

Figure 15 shows the Px4x IEDs (Px4x – IED 1 to IED N) with the RSTP variant of redundant Ethernet boards connected in a ring topology. The ring topology can have one or more high-end RSTP-enabled Ethernet switches to interface with another network or control center.

The Ethernet switch is an RSTP enabled switch with a higher number of ports.

The Ethernet switch, which is connected to the controlling PC, should be configured as the root bridge. The bridge priority of the Ethernet switch should be configured to the minimum value in the network shown in Figure 15.

The maximum number of IEDs that can be connected in the ring network depends on the Max Age parameter configured in the root bridge, see Figure 17.

The Max Age parameter can be varied from 6 to 40 seconds.

If Max Age = 6 seconds, the maximum number of IEDs in the ring is 6 - 1 = 5.

If Max Age = 40 seconds, the maximum number of IEDs in the ring is 40 - 1 = 39.

Therefore, the number of IEDs that can be connected in the ring can vary from 5 to 39.

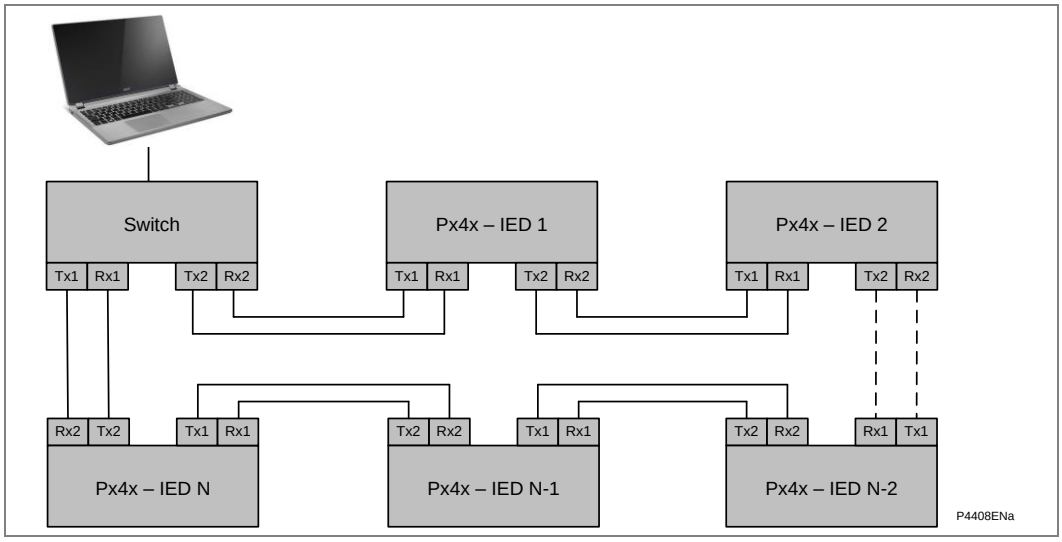


Figure 15 - Dual Ethernet ring topology

5.4 RSTP Star Connection

Figure 16 shows the Px4x IEDs (Px4x – IED 1 to IE D N) with the RSTP variant of redundant

Ethernet boards connected in a star topology. The star topology can have one or more high-end RSTP-enabled Ethernet switches to interface with other networks, control centers, or Px4x IEDs. The Ethernet switch is an RSTP enabled switch with a greater number of ports.

The Ethernet switch, which is connected to the controlling PC, should be configured as the root bridge. The bridge priority of the Ethernet switch should be configured to the minimum value in the network shown in Figure 3.

The Px4x IEDs are placed at two hop distance from the root bridge, therefore the Max Age meter has no impact on star topology.

The maximum number of IEDs that can be connected in the star network depends on the number of ports available in the Ethernet switch, provided that the hop count from the root bridge is less than the Max Age parameter.

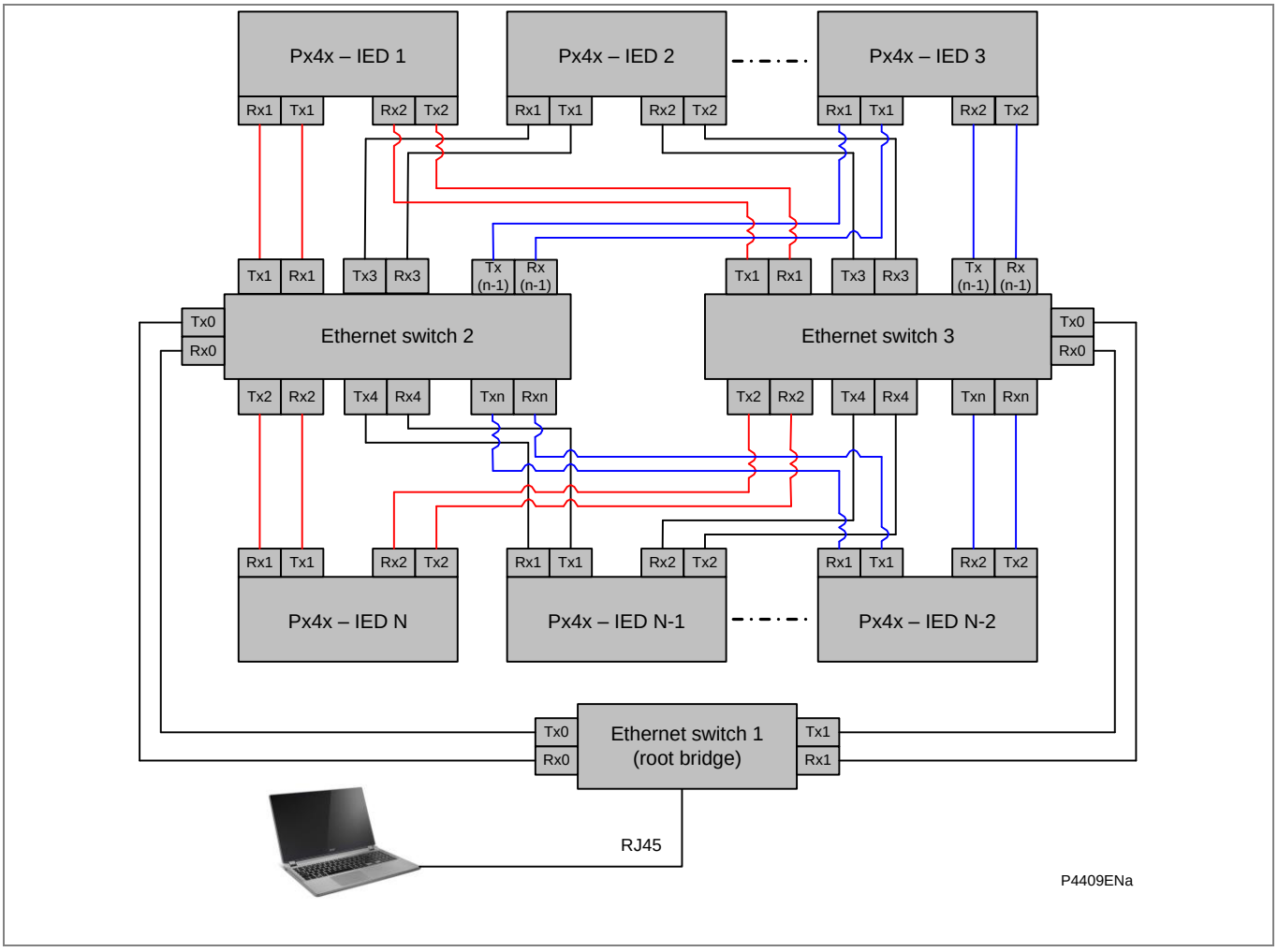


Figure 16 - Dual Ethernet star topology

5.5 Large RSTP Networks combining Star and Ring

Figure 17 shows a star of four rings. Each ring is connected to the root bridge. The root bridge is a high-end RSTP enabled bridge with the maximum number of ports as required.

The devices A1, A2…Anmax, B1, B2…Bnmax, C1, C2…Cnmax, D1, D2…Dnmax, represent the RSTP variant of redundant Ethernet boards.

The maximum number of boards that can be connected in single ring in an RSTP-enabled network depends on the Max Age parameter. The hop count from the root bridge cannot be greater than the Max Age parameter.

The maximum number of RSTP bridges in a ring is given by:

Nmax = (Max Age – 1)

Where:
Nmax = maximum number of devices in a ring
Max Age = Max Age value configured in the root bridge

Assuming the default value of Max Age as 20 seconds in the topology shown 0, the maximum number of devices that can be connected in ring A is 19.

If Max Age is configured as 40 seconds, the maximum number of IEDs that can be connected in the network is (40-1) = 39. According to the IEEE 802.1D 2004 standard, the maximum value for the Max Age parameter is limited to 40. To use the maximum number of IEDs in the ring, the following configuration should be used.

Max Age	40 seconds
Forward Delay	30 seconds
Hello Time	2 seconds
Bridge Priority	As required by the end user

The IEEE 802.1D 2004 standard defines the relation between Max Age and Forward Delay as:

2 * (Forward Delay – 1.0 seconds) >= Max Age

To have the maximum number of nodes in the RSTP network, the number of rings can be increased, depending on the number of ports available in the root bridge.

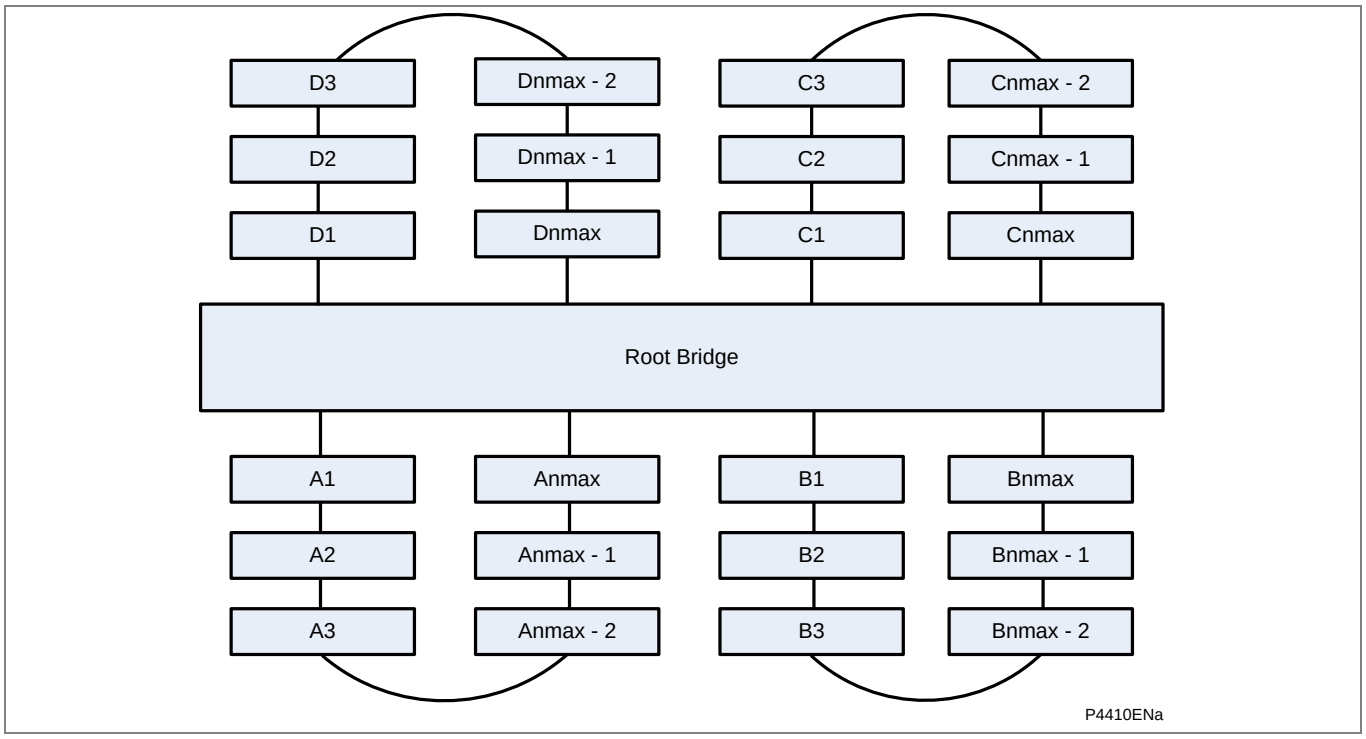


Figure 17 - Combined RSTP star and ring topology

6 TECHNICAL DATA

The technical data applies to a Redundant Ethernet board fitted into these products.

- P14x = P141, P142, P143, P145
- P24x = P241, P242, P243
- P34x = P341, P342, P343, P344, P345
- P44x = P442, P444
- P44y = P443, P446
- P445
- P54x = P543, P544, P545, P546
- P547
- P64x = P642, P643, P645
- P74x = P741, P743, P746
- P841
- P849

6.1 Board Hardware

6.1.1 100 Base TX Communications Interface (in accordance with IEEE802.3 and IEC 61850)

Cable type	Screened Twisted Pair (STP)
Connector type	RJ45
Maximum distance	100m
Full Duplex	100 Mbps

Table 6 - 100 Base TX interface

6.1.2 100 Base FX Communications Interface (in accordance with IEEE802.3 and IEC 61850)

Optical fiber cable	Multi-mode 50/125 µm or 62.5/125 µm
Center wavelength	1310 nm
Connector type	LC
Maximum distance	2 km
Full Duplex	100 Mbps

Table 7 - 100 Base FX interface

6.1.3 Transmitter Optical Characteristics

(TA = -40° C to 85° C)

Parameter	Sym	Min.	Typ.	Max.	Unit
Output Optical Power 62.5/125 µm, NA = 0.275 Fiber	PO	-20	-17.0	-14	dBm avg.
Output Optical Power 50/125 µm, NA = 0.20 Fiber	PO	-23.5	-20.0	-14	dBm avg.
Optical Extinction Ratio				10	dB
Output Optical Power at Logic “0” State	PO (“0”)			-45	dBm avg.

Table 8 - Tx optical characteristics

6.1.4 Receiver Optical Characteristics

(TA = -40° C to 85° C)

Parameter	Sym	Min.	Typ.	Max.	Unit
Input Optical Power	PIN	-31		-14	dBm avg.

Table 9 - Rx optical characteristics

6.1.5 IRIG-B and Real-Time Clock

6.1.5.1 Performance

Year 2000:	Compliant
Real time accuracy:	< ±2 seconds / day
External clock synchronization:	Conforms to IRIG standard 200-98, format B

6.1.5.2 Features

Real time 24 hour clock settable in hours, minutes and seconds
Calendar settable from January 1994 to December 2092
Clock and calendar maintained via battery after loss of auxiliary supply
Internal clock synchronization using IRIG-B Interface for IRIG-B signal is BNC

6.1.5.3 Self-adapted Rear IRIG-B interface (Modulated or Unmodulated)

BNC plug
Isolation to SELV level
50 ohm coaxial cable

6.2 Type Tests

6.2.1 Insulation

Per EN / IEC 60255-27:
Insulation resistance > 100 MΩ at 500 Vdc
(Using only electronic/brushless insulation tester).

6.2.2 Creepage Distances and Clearances

Per EN / IEC 60255-27:
Pollution degree 3, Overvoltage category III,

6.2.3 High Voltage (Dielectric) Withstand

(EIA RS-232 ports excepted and normally-open contacts of output relays excepted).

(i) As for EN / IEC 60255-27:

2 kV rms AC, 1 minute:
Between all independent circuits.
Between independent circuits and case earth (ground).
1 kV rms AC for 1 minute, across open watchdog contacts.
1 kV rms AC for 1 minute, across open contacts of changeover output relays.
1 kV rms AC for 1 minute for all D-type EIA(RS)-232 or EIA(RS)-485 ports between the communications port terminals and protective (earth) conductor terminal.
1 kV rms AC for 1 minute between RJ45 ports and the case earth (ground).

(ii) As for ANSI/IEEE C37.90:

1.5 kV rms AC for 1 minute, across open contacts of normally open output relays.
1 kV rms AC for 1 minute, across open watchdog contacts.
1 kV rms AC for 1 minute, across open contacts of changeover output relays.

6.2.4 Impulse Voltage Withstand Test

As for EN / IEC 60255-27:

(i) Front time: 1.2 µs, Time to half-value: 50 µs,
Peak value: 5 kV, 0.5 J
Between all independent circuits.
Between independent circuits and case earth ground.

(ii) Front time: 1.2 µs, Time to half-value: 50 µs,
Peak value: 1.5kV, 0.5 J
Between RJ45 ports and the case earth (ground).
EIA(RS)-232 & EIA(RS)-485 ports and normally open contacts of output relays excepted.

6.3 ElectroMagnetic Compatibility (EMC)

6.3.1 1 MHz Burst High Frequency Disturbance Test

As for EN / IEC 60255-22-1, Class III,

Common-mode test voltage:	2.5 kV,
Differential test voltage:	1.0 kV,
Test duration:	2 s,
Source impedance:	200 Ω

(EIA(RS)-232 ports excepted).

6.3.2 100 kHz and 1MHz Damped Oscillatory Test

EN / IEC 61000-4-18:	Level 3
Common mode test voltage:	2.5 kV
Differential mode test voltage:	1 kV

6.3.3 Immunity to Electrostatic Discharge

As for EN / IEC 60255-22-2, EN / IEC 61000-4-2:
15kV discharge in air to user interface, display, communication ports and exposed metalwork.
6kV contact discharge to the screws on the front of the front communication ports.
8kV point contact discharge to any part of the front of the product.

6.3.4 Electrical Fast Transient or Burst Requirements

As for EN / IEC 60255-22-4, Class B:
±4.0 kV, 5kHz and 100kHz applied to all inputs / outputs excluding communication ports
±2.0 kV, 5kHz and 100kHz applied to all communication ports

As for EN / IEC 61000-4-4, severity level 4:
±2.0 kV, 5kHz and 100kHz applied to all inputs / outputs and communication ports excluding power supply and earth.
±4.0 kV, 5kHz and 100kHz applied to all power supply and earth port

Rise time of one pulse:	5 ns
Impulse duration (50% value):	50 ns
Burst duration:	15 ms or 0.75ms
Burst cycle:	300 ms
Source impedance:	50 Ω

6.3.5 Surge Withstand Capability

As for IEEE/ANSI C37.90.1:
4 kV fast transient and 2.5 kV oscillatory
applied directly across each output contact, optically isolated input, and power supply circuit.

6.3.6 Surge Immunity Test

As for EN / IEC 61000-4-5, EN / IEC 60255-26:
Time to half-value: 1.2 to 50 µs,
Amplitude: 4 kV between all groups and case earth (ground),
Amplitude: 2 kV between terminals of each group.
Amplitude: 1kV for LAN ports

6.3.7 Conducted/Radiated Immunity

For RTDs used for tripping applications the conducted and radiated immunity performance is guaranteed only when using totally shielded RTD cables (twisted leads).

6.3.8 Immunity to Radiated Electromagnetic Energy

Per EN / IEC 61000-4-3 and EN / IEC 60255-22-3, Class 3
Test field strength, frequency band 80 to 1000 MHz and
1.4 GHz to 2.7GHz: 10 V/m,
Test using AM: 1 kHz / 80%
Spot tests at: 80, 160, 450, 900, 1850, 2150 MHz
Per IEEE/ANSI C37.90.2:
80MHz to 1000MHz, zero and 100% square wave modulated.
Field strength of 35V/m.

6.3.9 Radiated Immunity from Digital Communications

As for EN / IEC61000-4-3, Level 4:
Test field strength, frequency band 800 to 960 MHz,
and 1.4 to 2.0 GHz: 30 V/m, Test using AM: 1 kHz/80%.

6.3.10 Radiated Immunity from Digital Radio Telephones

As for EN / IEC 61000-4-3: 10 V/m, 900 MHz and 1.89 GHz.

6.3.11 Immunity to Conducted Disturbances Induced by Radio Frequency Fields

As for EN / IEC 61000-4-6, Level 3, Disturbing test voltage: 10 V.

6.3.12 Power Frequency Magnetic Field Immunity

As for EN / IEC 61000-4-8, Level 5,
100 A/m applied continuously, 1000 A/m applied for 3 s.
As for EN / IEC 61000-4-9, Level 5,
1000 A/m applied in all planes.
As for EN / IEC 61000-4-10, Level 5,
100 A/m applied in all planes at 100 kHz and 1 MHz with a burst duration of 2 s.

6.3.13 Conducted Emissions

As for CISPR 22 Class A:
Power supply:
0.15 - 0.5 MHz, 79 dBµV (quasi peak) 66 dBµV (average)
0.5 - 30 MHz, 73 dBµV (quasi peak) 60 dBµV (average)
Permanently connected communications ports:
0.15 - 0.5MHz, 97dBµV (quasi peak) 84dBµV (average)
0.5 - 30MHz, 87dBµV (quasi peak) 74dBµV (average)

6.3.14 Radiated Emissions

As for CISPR 22 Class A:
30 to 230 MHz, 40 dBµV/m at 10m measurement distance
230 to 1 GHz, 47 dBµV/m at 10 m measurement distance.
1 – 3GHz, 76dBµV/m (peak), 56dBµV/m (average) at 3m measurement distance.
3 – 5GHz, 80dBµV/m (peak), 60dBµV/m (average) at 3m measurement distance.

6.4 Environmental Conditions

6.4.1 Ambient Temperature Range

Per EN 60068-2-1 & EN / IEC 60068-2-2
Operating temperature range: -25°C to +55°C (or -13°F to +131°F)
Storage and transit: -25°C to +70°C (or -13°F to +158°F)

6.4.2 Ambient Humidity Range

Per EN /IEC 60068-2-78:

56 days at 93% relative humidity and +40 °C

Per EN / IEC 60068-2-14

5 cycles, -25°C to +55 °C
1°C / min rate of change

Per EN / IEC 60068-2-30

Damp heat cyclic, six (12 + 12) hour cycles, +25 to +55°C

6.4.3 Corrosive Environments

Per EN / IEC 60068-2-60, Part 2, Test Ke, Method (class) 3
Industrial corrosive environment/poor environmental control, mixed gas flow test.
21 days at 75% relative humidity and +30°C
Exposure to elevated concentrations of H_2S, (100 ppb), NO_2, (200 ppb) & Cl_2 (20 ppb).
Per EN / IEC 60068-2-52 Salt mist (7 days)
Per EN / IEC 60068-2-43 for H_2S (21 days), 15 ppm
Per EN / IEC 60068-2-42 for SO_2 (21 days), 25 ppm

6.5 EU Directives

6.5.1 EMC Compliance

As for 2004/108/EC:

Compliance to the European Commission Directive on EMC is demonstrated using a Technical File. Product Specific Standards were used to establish conformity:
EN 60255-26

6.5.2 Product Safety

Per 2006/95/EC:

Compliance to the European Commission Low Voltage Directive (LVD) is demonstrated using a Technical File. A product-specific standard was used to establish conformity.

CE EN 60255-27

6.5.3 R&TTE Compliance

Radio and Telecommunications Terminal Equipment (R&TTE) directive 99/5/EC.

Compliance demonstrated by compliance to both the EMC directive and the Low voltage directive, down to zero volts.

Applicable to rear communications ports.
Compliance demonstrated by Notified Body certificates of compliance.

6.5.4 Other Approvals

For ATEX Potentially Explosive Atmospheres directive 94/9/EC compliance, consult Schneider Electric.
For other approvals such as UL / CUL / CSA, consult Schneider Electric.

6.6 Mechanical Robustness

6.6.1 Vibration Test

Per EN / IEC 60255-21-1	Response Class 2 Endurance Class 2

6.6.2 Shock and Bump

Per EN / IEC 60255-21-2	Shock response Class 2 Shock withstand Class 1 Bump Class 1

6.6.3 Seismic Test

Per EN / IEC 60255-21-3:	Class 2

7 CORTEC

This is a generic Cortec to cover all IEDs using the **Redundant Ethernet** boards.
It does not necessarily include all the possible options for all products in the MiCOM Px4x range. Likewise, it is possible that options shown in this list, may not be available for all products

Variants	Order Number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
MiCOM Protection		P														
Application/Platform:																
Feeder Management:			1	4	*											
Motor Protection:			2	4	*											
Generator Protection Relay:			3	4	*											
Distance Protection Relay:			4	4	*											
Current Differential:			5	4	*											
Transformer:			6	4	*											
Busbar:			7	4	*											
Breaker Fail:			8	4	*											
Vx Aux Rating:																
24 - 32 Vdc						9										
48 - 110 Vdc						2										
110 - 250 Vdc (100 - 240 Vac)						3										
In/Vn Rating (model dependent):																
Product Dependent							*									
Hardware Options (model dependent):																
Standard - no options								1								
IRIG-B only (modulated)								2								
Fibre optic converter only								3								
IRIG-B (modulated) & fibre optic converter								4								
Ethernet with 100Mits/s fibre-optic port								6								
Second Rear Comms Port (Courier EIA232/EIA485/k-bus)								7								
Second Rear Comms Port + IRIG-B (modulated) (Courier EIA232/EIA485/k-bus)								8								
InterMiCOM + Courier Rear Port								E								
InterMiCOM + Courier Rear Port + IRIG-B modulated								F								
Redundant Ethernet (100Mbit/s) PRP or HSR or RSTP and Dual IP, 2 LC ports + 1 RJ45 port + Modulated/Un-modulated IRIG-B + 1588								Q								
Redundant Ethernet (100Mbit/s) PRP or HSR or RSTP and Dual IP, 3 RJ45 ports + Modulated/Un-modulated IRIG-B + 1588								R								
Ethernet (100Mbit/s), 1 RJ45 port + Modulated/Un-modulated IRIG-B + 1588								S								
Product Specific Options (model dependent):																
Product Dependent									*							
Protocol Options:																
K-Bus/Courier										1						
Modbus										2						
IEC60870-5-103 (VDEW)										3						
DNP3.0										4						
IEC 61850 over Ethernet and Courier via rear K-Bus/RS485 OR IEC 61850 Edition 1 and Edition 2 and Courier via rear K-Bus/RS485										6						
IEC 61850 over ethernet with CS103 rear port RS485 protocol OR IEC 61850 Edition 1 and Edition 2 and CS103 via rear port RS485										7						
IEC 61850 Edition 1 / 2 and DNPoE and DNP3 Serial with simple password management - (CSL0)										B						
IEC 61850 Edition 1 / 2 and Courier via rear K-Bus/RS485 with advanced Cyber Security - CSL1 - Security Administration Tool (SAT) required										G						
IEC 61850 Edition 1 / 2 and CS103 via rear port RS485 with advanced Cyber Security - CSL1 - Security Administration Tool (SAT) required										H						
IEC 61850 Edition 1 / 2 and DNPoE and DNP3 Serial with advanced Cyber Security - CSL1 - Security Administration Tool (SAT) required										L						
Mounting Options:																

Flush Panel Mounting	M					
Rack Mounting (80TE only)	N					
Language Options:						
English, French, German, Spanish		0				
English, French, German, Russian		5				
Chinese, English or French via HMI, with English or French only via Communications port		C				
Software Version:						
			*	*		
Customisation:						
Default					8	
Customer Specific					9	
Design Suffix:						
Phase 3 CPU						L
Extended Phase 3 CPU						M

Notes:

PRP NOTES

CHAPTER 20

Date (month/year):	02/2018			
Products covered by this chapter:	This chapter covers the specific versions of the MiCOM products listed below. This includes ***only*** the following combinations of Software Version and Hardware Suffix.			
Hardware Suffix:	P445 P44y (P443/P446)	L M	P54x (P543/P544/P545/P546) P841A (one circuit breaker) P841B (two circuit breakers)	M M M
Software Version:	P445 P44y (P443/P446)	J4/B0/B1/E0/E1 H4	P54x (P543/P544/P545/P546) P841A P841B	H4 G4 H4
Connection Diagrams:	P14x (P141, P142, P143 & P145): 10P141xx (xx = 01 to 02) 10P142xx (xx = 01 to 05) 10P143xx (xx = 01 to 11) 10P145xx (xx = 01 to 11) P24x (P241, P242 & P243): 10P241xx (xx = 01 to 02) 10P242xx (xx = 01) 10P243xx (xx = 01) P34x (P342, P343, P344, P345 & P391): 10P342xx (xx = 01 to 17) 10P343xx (xx = 01 to 19) 10P344xx (xx = 01 to 12) 10P345xx (xx = 01 to 07) 10P391xx (xx = 01 to 02) P445: 10P445xx (xx = 01 to 04) P44x(P442 & P444): 10P44201 (SH 1 & 2) 10P44202 (SH 1) 10P44203 (SH 1 & 2) 10P44401 (SH 1) 10P44402 (SH 1) 10P44403 (SH 1 & 2) 10P44404 (SH 1) 10P44405 (SH 1) 10P44407 (SH 1 & 2) P44y (P443 & P446): 10P44303 (SH 01 and 03) 10P44304 (SH 01 and 03) 10P44305 (SH 01 and 03) 10P44306 (SH 01 and 03) 10P44600 10P44601 (SH 1 to 2) 10P44602 (SH 1 to 2) 10P44603 (SH 1 to 2)		P54x (P543, P544, P545 & P546): 10P54302 (SH 1 to 2) 10P54303 (SH 1 to 2) 10P54400 10P54404 (SH 1 to 2) 10P54405 (SH 1 to 2) 10P54502 (SH 1 to 2) 10P54503 (SH 1 to 2) 10P54600 10P54604 (SH 1 to 2) 10P54605 (SH 1 to 2) 10P54606 (SH 1 to 2) P547: 10P54702xx (xx = 01 to 02) 10P54703xx (xx = 01 to 02) 10P54704xx (xx = 01 to 02) 10P54705xx (xx = 01 to 02) P64x (P642, P643 & P645): 10P642xx (xx = 01 to 10) 10P643xx (xx = 01 to 06) 10P645xx (xx = 01 to 09) P74x (P741, P742 & P743): 10P740xx (xx = 01 to 07) P746: 10P746xx (xx = 00 to 21) P841: 10P84100 10P84101 (SH 1 to 2) 10P84102 (SH 1 to 2) 10P84103 (SH 1 to 2) 10P84104 (SH 1 to 2) 10P84105 (SH 1 to 2) P849: 10P849xx (xx = 01 to 06)	

CONTENTS

TABLES

FIGURES

Notes:

1 PARALLEL REDUNDANCY PROTOCOL (PRP) NOTES

1.1 Introduction to PRP

This section gives an introduction to the Parallel Redundancy Protocol (PRP); and how it is implemented on MiCOM-based products manufactured by Schneider Electric.

1.2 Protocols

Industrial real-time Ethernets typically need much better levels of availability and uninterrupted operation than normal office-type Ethernet solutions. For power networks, even a short loss of connectivity may result in a significant loss of functionality or impaired safety. To recover from a network failure, various redundancy schemes have been considered, including: Rapid Spanning Tree Protocol (**RSTP**), Media Redundancy Protocol (**MRP**) and Parallel Redundancy Protocol (**PRP**). The key properties of these are as follows:

RSTP this uses mesh-based topologies or ring topology and computes a tree, based on path costs and priorities. In case of network failure, a typical reset time for RSTP-based system is normally a few seconds.

MRP This uses ring-based topologies. In case of network failure, the network is broken into two separate lines, which are reconnected by de-blocking the previously blocked part. The guaranteed reset time for MRP protocol-based systems is typically around 100ms.

PRP this does not change the active topology as it uses two independent networks. Each message is replicated and sent over both networks. The first network node to receive it acts on it, with all later copies of the message being discarded. Importantly, these details are controlled by the low-level PRP layer of the network architecture, with the two networks being hidden from the higher level layers. Consequently, PRP-based networks are continuously available.

Power networks need to be able to respond to problems very quickly (typically in less than 10ms), and PRP is an available protocol which is robust enough to achieve this. The PRP protocol used in the MiCOM relay/IEDs is defined in the IEC62439-3 (2012) standard and is configured using the existing redundant Ethernet card(s).

1.3 PRP Summary (IEC 62439-3 Clause 4)

A summary of the main PRP features is given below:

- Ethernet redundancy method independent of any Ethernet protocol or topology (tree, ring or mesh)
- Seamless switchover and recovery in case of failure, which supports real-time communication
- Supervises redundancy continuously for better management of network devices
- Suitable for hot swap - 24 hour/365 day operation in substations
- Allows the mixing of devices with single and double network attached nodes on the same Local Area Network (LAN)
- Allows laptops and workstations to be connected to the network with standard Ethernet adapters (on double or single attached nodes)
- Particularly suited for substation automation, high-speed drives and transportation

1.4 Example of a PRP Network

Essentially a PRP network is a pair of similar Local Area Networks (LANs) which can be any topology (tree, ring or mesh). An example of a PRP network is shown in Figure 1:

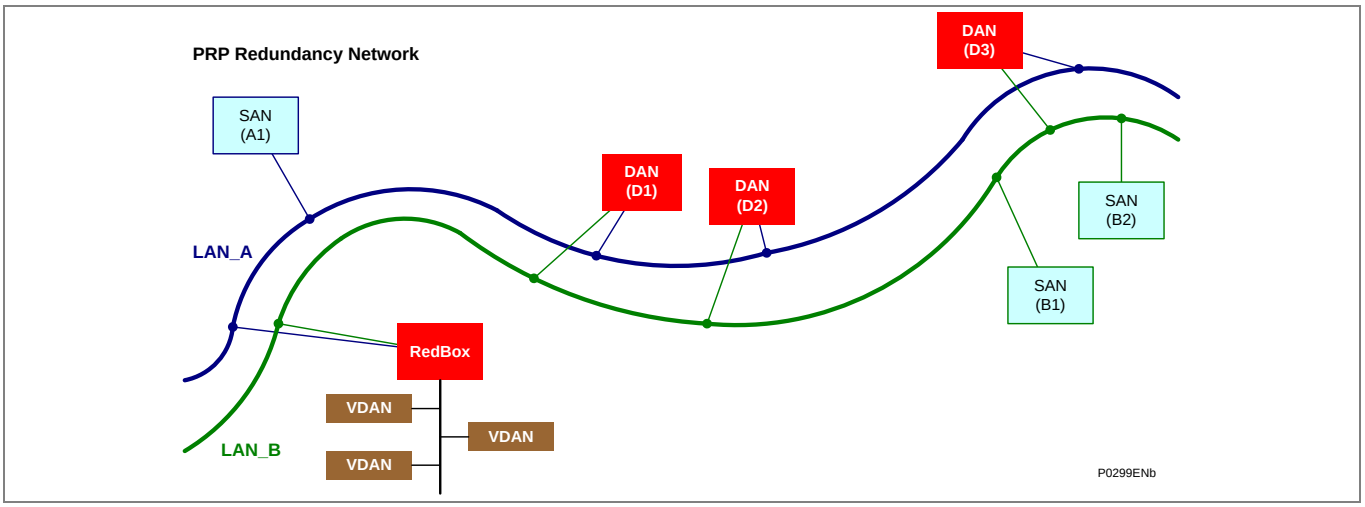


Figure 1 - PRP Redundancy Network

Figure 1 shows two similar Local Area Networks (LANs) which have various Nodes in common. The key features of these networks include:

- With the exception of a RedBox (see below), no direct cable connections can be made between the two LANs.
- Each of these LANs can have one or more Single Attached Nodes (SANs). These are normally non-critical devices that are attached only to a single network. SANs can talk to one another, but only if they are on the same LAN.
- Matched pairs of devices which are critical to the operation of the overall scheme are connected one to each network as Doubly Attached Nodes (DANs).
- To be sure that network messages (also known as frames) are transferred correctly to each DAN, each DAN must have the same Media Access Control (MAC) code and Internet Protocol (IP) address. This will also mean that TCP/IP traffic will automatically communicate with both of the paired devices, so it will be unaware of any two-layer redundancy or frame duplication issues.
- A Redundancy Box (RedBox) is used when a single interface node has to be connected to both networks. The RedBox can talk to all other nodes. So far as other nodes are concerned, the RedBox behaves like a DAN, so a SAN that is connected through a RedBox is also called a Virtual Doubly Attached Node (VDAN). The RedBox must have its own unique IP address.
- Transmission delays can be different between related Nodes of the two LANs.
- Each LAN (i.e. LAN_A and LAN_B) must be powered from a different power source and must be failure independent.

The two LANs can differ in terms of performance and topology. The redundant Ethernet interface can be made using an optical fiber connection with an LC or ST connector type or with RJ45 copper connector type. There is no need for an optical interface away from the relay.

1.5 PRP Network Structure

PRP uses two independent LANs. The topology of each of these LANs is arbitrary, and ring, star, bus and meshed topologies are possible.
The main advantage of PRP is loss-free data transmission with an active (transit) LAN. When the terminal device receives no packets from one of the LANs, the second (transit) LAN maintains the connection. As long as 1 (transit) LAN is available, repairs and maintenance on the other (transit) LAN have no impact on the data packet transmission.
The elementary devices of a PRP network are known as RedBox (Redundancy Box) and DANP (Double Attached Node implementing PRP).
Both devices have one connection each to the (transit) LANs.

The devices in the (transit) LAN are conventional switches that do not require any PRP support. The devices transmit PRP data packets transparently, without evaluating the RCT information.
Terminal devices that are connected directly to a device in the (transit) LAN are known as SAN (Single Attached Node). If there is an interruption, these terminal devices cannot be reached via the redundant line. To use the uninterruptible redundancy of the PRP network, you integrate your device into the PRP network via a RedBox.

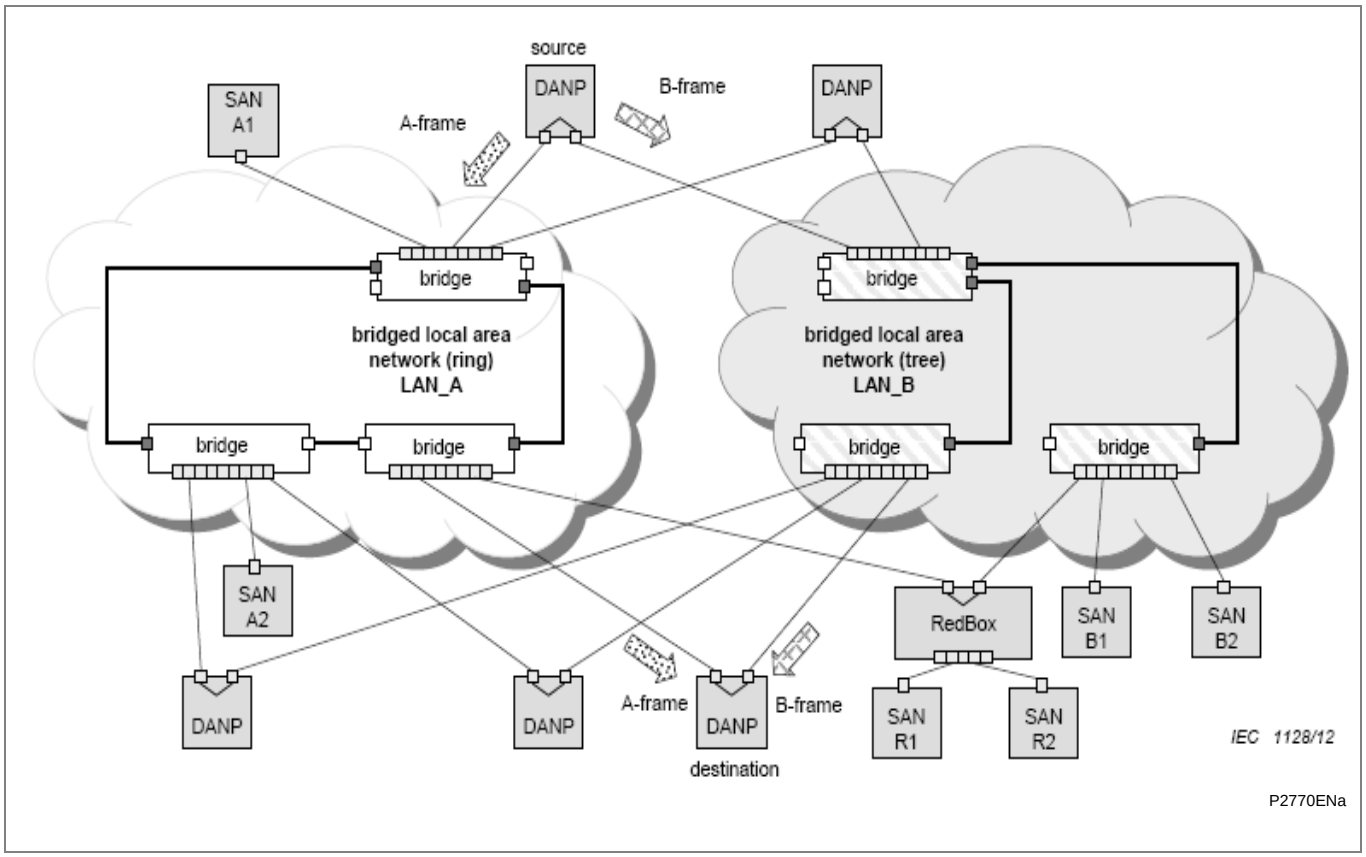


Figure 2 - PRP example of general redundant network

1.6 Structure of a DAN

A MiCOM P40 relay working in PRP Mode works as a DAN within the overall network topology. Each DAN has two ports that operate in parallel. They are attached to the upper layers of the communications stack through the Link Redundancy Entity (LRE) as in Figure 3:

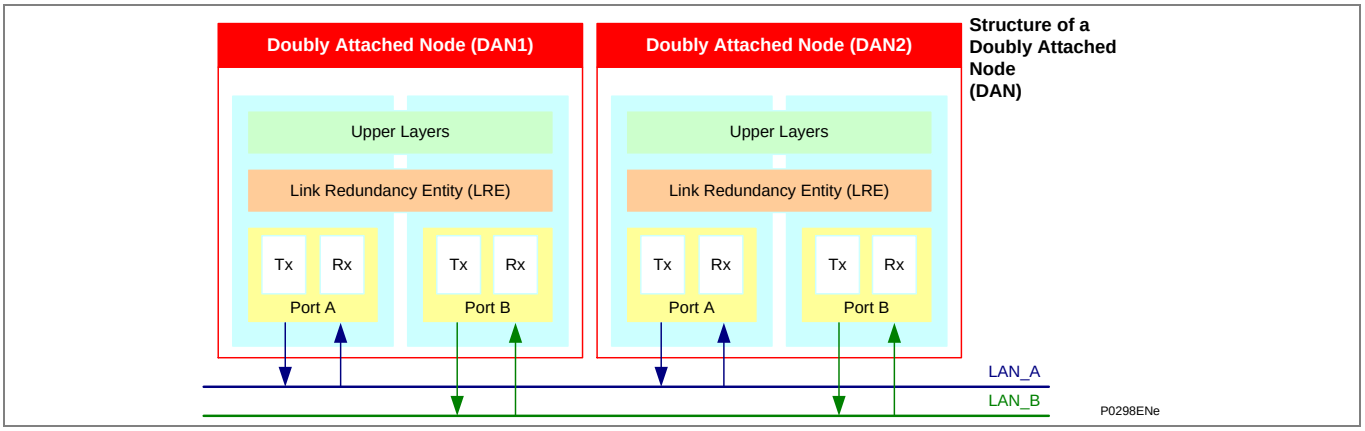


Figure 3 - Communication between two DANs (in PRP)

The LRE has two main tasks:

- handling message frames and
- management of redundancy

When an upper layer sends a frame to the LRE, the LRE replicates the frame and sends it through both its ports at nearly the same time. The two frames move through the two LANs with slightly different delays, ideally arriving at the destination node within a small time window.

When receiving frames, the LRE forwards the first frame it received to its upper layers and then discards the duplicate.

As both DAN nodes have the same MAC and IP addresses, this makes redundancy transparent to the upper layers. This allows the Address Resolution Protocol (ARP) to work in the same way as with a SAN. Accordingly, to the upper layers of a DAN, the LRE layer shows the same interface as the network adapter of a non-redundant adapter.

To manage redundancy, the LRE:

- Adds a 32-bit Redundancy Check Tag (RCT) to each frame it sends and
- Removes the RCT from each frame it receives

1.7 Communication between SANs and DANs

A SAN can be connected to any LAN and can communicate with any other SAN on the same LAN or any DAN. However, a SAN which connected to one LAN can not communicate directly to a SAN which is connected to the other LAN.

A DAN is connected to both LANs and can communicate with any RedBox or any other DANs or any SANs on either network. For communication purposes, a DAN “views” a SAN connected through a RedBox as a VDAN.

When a SAN generates a basic frame, it sends the frame only onto the LAN to which it is connected.

Originating at the SAN, a typical frame contains these parameters:

- dest_addr Destination Address
- src_addr Source Address
- type Type
- data
- fcs Frame Check Sequence (i.e. extra checksum characters added to allow error detection and correction)

The frame from the SAN is then received by the DAN; which sends the frame to its upper layers, which act accordingly.

When a DAN generates a frame, it needs to send the frame onto both of the LANs to which it is connected. When it does this, it extends the frame by adding the 48-bit Redundancy Control Trailer (RCT) into the frame.

The RCT consists of these parameters:

- 16-bit Sequence Number
- 4-bit LAN identifier, 1010 (0xA) for LAN_A and 1011 (0xB) for LAN_B
- 12-bit frame size
- PRP suffix

Note	*The Sequence number is a measure of the number of messages which have been sent since the last system reset. Each time the link layer sends a frame to a particular destination the sender increases the sequence number corresponding to that destination and sends the (nearly) identical frames over both LANs.*

Accordingly, originating at the DAN, a typical frame then contains these parameters:

- dest_addr Destination Address
- src_addr Source Address
- type Type
- lsdu Link Service Data Unit
- Padding if needed
- RCT data:
  - 16-bit sequence number:
    4-bit LAN identifier
    12-bit frame size
  - 16-bit PRP suffix (0X88 0XFB)
- fcs Frame Check Sequence

LSDU	*The Link Service Data Unit (LSDU) data allows PRP frames to be distinguished from none-PRP frames.*
Padding	*After the LSDU data, there may be some data padding. This is added to frames which would otherwise be too short for conventional network traffic (minimum frame size is 64 octets).*

Size	*The frame size will vary depending on the contents of the frame and how it has been tagged by the various SANs and DANs. In VLANs, frame tags may be added or removed during transit through a switch. To make the length field independent of tagging, only the LSDU and the RCT are considered in the size.*

Figure 4 shows the frame types with different types of data.

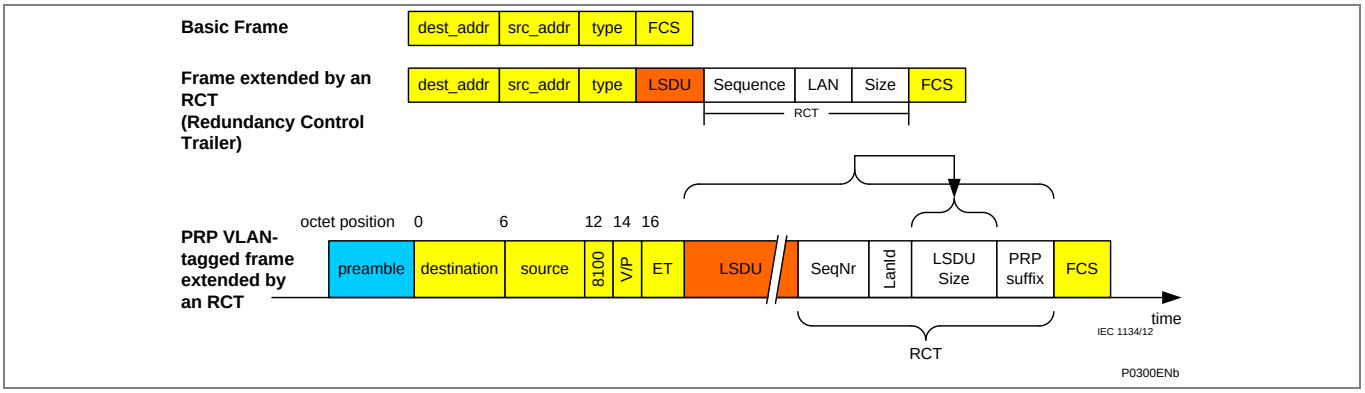


Figure 4 - Frames (basic, extended by an RCT and a VLAN tagged frame extended by RCT)

The key points about these differing frame structures is that:

- SANs do not implement any redundancy features, so they generate basic frames which SANs and DANs can understand.
- SANs can still understand the frames that come from DANs, as SANs ignore the RCT components in frames which come from DANs (a SAN cannot distinguish the RCT from the IEEE802.3 padding)
- If a DAN receives a frame which does not include the RCT component, it sends a single copy of the frame to its upper layers.
- If a DAN receives a frame which does include the RCT component, it does not send a duplicate copy of the frame to its upper layers.
- If a DANP cannot identify that the remote Node is a DAN, it inserts no RCT.

When using a Single Attached Nodes connected to the IED, a redbox is suggested to handle the case when the TPDU size for the client has been set above than 1024.

1.8 PRP Technical Data

- One VLAN tag supported.
- 128 publishers supported per receiver.
- Up to 100Mbit/s full duplex Ethernet.
- Dynamic frame memory allocation (page manager).
- Configurable duplicate detection.
- Wishbone interface for configuration and status registers.
- CPU port interface - Ethernet or Wishbone.
- Support for link-local protocols - CPU may send to specific ports only - CPU knows receive port.
- Configurable frame memory and queue length.
- Duplicate detection with configurable size and aging time.
- MAC address filtering (8 filter masks for interlink, 6 for CPU).
- Support for interfaces with or without Ethernet preamble.

Maximum Transmission Unit

According to the IEC 8802-3, the MTU (Ethernet maximum packet size) is:

- 1518 bytes without VLAN and without PRP
- 1522 bytes with VLAN and without PRP
- 1524 bytes without VLAN and with PRP
- 1528 bytes with VLAN and with PRP

Note: Check that the LAN switches setting for the MTU is at least 1528 bytes

2 PRP AND MICOM FUNCTIONS

2.1 MiCOM Products and PRP

The PRP functions being introduced as part of the overall MiCOM product range provide additional functionality, which is backwards compatible with existing Schneider Electric MiCOM equipment. This means that existing MiCOM relays/IEDS can be used on networks which use PRP functions, with no changes being made to those relays/IEDs.

The new MiCOM products that use the PRP, will interrogate other equipment to determine the equipment model number, and then use the model number to decide (at runtime), whether that particular item of equipment can support PRP or not.

MiCOM models which include the following Ethernet board assembly provide the possibility of PRP function support. This is denoted by Digit 7 where the Hardware option is N, P, Q or R, as shown in Table 1:

Hardware Option	Type	Model No format
"N" at Digit No 7	2 ST ports redundant Ethernet board (Modulated IRIG-B)	**Px4xxxNx6Mxxx8K**
"P" at Digit No 7	2 ST ports redundant Ethernet board (Un-modulated IRIG-B)	**Px4xxxPx6Mxxx8K**
"Q" at Digit No 7	2 LC + 1 RJ45 ports redundant Ethernet board (Modulated/ Un-modulated IRIG-B)	**Px4xxxQx6Mxxx8M**
"R" at Digit No 7	3 RJ45 ports redundant Ethernet board (Modulated/ Un-modulated IRIG-B)	**Px4xxxRx6Mxxx8M**

Table 1 - MiCOM model numbers for PRP options

The MiCOM relay/IED firmware has been modified to allow the PRP options to be accepted for the power-up tests in addition to the implementation of the supervision frame transmission.

2.2 Easergy Studio Software and the PRP Function

The addition of this function has no impact of the Easergy Studio support files so there is no need to upgrade any Easergy Studio software.

2.3 MiCOM Relay Configuration and the PRP Function

There is no need to change the configuration of any relay (as relays which include support for this function will be able to recognize other devices which support it).

2.4 Hardware Changes for PRP Protocol

This protocol is implemented using the existing redundant Ethernet and dual redundant Ethernet card as a starting point. The Frame management is achieved by re-programming the Field-Programmable Gate Array (FPGA).

The low-level management of the redundant frames is performed within the FPGA; this being defined as the Link Redundancy Entity (LRE). This will involve the addition of the Redundancy Check Tag (RCT) to a frame to be transmitted; this identifies the LAN and the sequence number of the message over the two networks. The FPGA is also responsible for the stripping of the RCT from received frames and discarding the duplicated messages such that only a single application frame is received by the Ethernet processor.

The LRE functionality of the supervision frame transmission is performed by the Ethernet processor card.

2.5 PRP Parameters

The Redundant Ethernet standard (IEC 62439-3:2012) defines several parameters for the PRP protocol; these being fixed at a default value within this release. The following values are set:

Parameter	Value	Description
Supervision Frame Multicast Address	01-15-4E-00-01-00	Target MAC Address for multicast supervision frame
Life Check Interval	2 seconds	Period between transmission of supervision frames
PRP Mode	Duplicate Discard	This is normal PRP mode, Duplicate address will not be supported.
Node Forget Time	60 s	This is the time after which a node entry is cleared.
Entry Forget Time	400 ms	Duration that the received message Sequence number will be held to discard a duplicate message.
Node Reboot Interval	500ms	Duration following reboot for which no PRP frames should be transmitted.

Table 2 - PRP parameter values (for PRP Protocol Version 1)

2.6 Product Implementation Features

Here is a list of the main Product Requirements for MiCOM products which support PRP:

- The MiCOM relay/IED provides two redundant Ethernet ports using PRP.
- The MiCOM relay/IED must be connected to the redundant Ethernet network as a Double Attached Node (DAN) using PRP (DAN using PRP is known as DANP)
- The redundant Ethernet interface can be made using an RJ45 or an optical fibre connection with an LC or ST connector type (Ethernet card dependent).
- The management of the PRP redundancy is transparent to the application data provided via the Ethernet interface.
- The PRP option is available with any of the existing protocol options via the Ethernet Interface (IEC61850 and/or DNPoE)
- Loss of one of the LAN connections to the device does not cause any loss or degradation to the Application data over the Ethernet interface.
- The MiCOM relay/IED supports the transmission of the PRP Supervision frame at a fixed time period (LifeCheckInterval) of 2s (+/- 100ms)
- Each supervision frame includes a sequence number as defined in the IEC 62439-3:2012 specification. This is incremented for each supervision message and the value starts from zero following a system restart.
- The MiCOM relay/IED does not process received supervision frames to provide supervision of the redundant network.
- The MiCOM relay/IED does not provide for the PRP management to be configured (via either the MiCOM relay/IED HMI or the Ethernet interface). Accordingly, the default values (as defined within this document) are used for all PRP parameters.
- The performance of the Ethernet Interface is not degraded by using the PRP interface.

2.6.1 Abbreviations and Acronyms

Abbreviations / Acronyms	Meaning
CRC	Cyclic Redundancy Check
DAN	Doubly Attached Nodes
DANP	Doubly Attached Node implementing PRP
FPGA	Field-Programmable Gate Array
HMI	Human Machine Interface
IED	Intelligent Electronic Devices
IP	Internet Protocol
LAN	Local Area Network
LRE	Link Redundancy Entity
MAC	Media Access Control
MRP	Media Redundancy Protocol
PRP	Parallel Redundancy Protocol
RCT	Redundancy Check Tag
RedBox	Redundancy Box
RSTP	Rapid Spanning Tree Protocol
SAN	Singly Attached Node
TCP	Transmission Control Protocol
VDAN	Virtual Doubly Attached Node

Notes:

HSR NOTES

CHAPTER 21

Date (month/year):	02/2018	
Products covered by this chapter:	This chapter covers the specific versions of the MiCOM products listed below. This includes ***only*** the following combinations of Software Version and Hardware Suffix.	
Hardware Suffix:	P445 L P44y (P443/P446) M	P54x (P543/P544/P545/P546) M P841A (one circuit breaker) M P841B (two circuit breakers) M
Software Version:	P445 J4/B0/B1/E0/E1 P44y (P443/P446) H4	P54x (P543/P544/P545/P546) H4 P841A G4 P841B H4
Connection Diagrams:	P14x (P141, P142, P143 & P145): 10P141xx (xx = 01 to 02) 10P142xx (xx = 01 to 05) 10P143xx (xx = 01 to 11) 10P145xx (xx = 01 to 11) P24x (P241, P242 & P243): 10P241xx (xx = 01 to 02) 10P242xx (xx = 01) 10P243xx (xx = 01) P34x (P342, P343, P344, P345 & P391): 10P342xx (xx = 01 to 17) 10P343xx (xx = 01 to 19) 10P344xx (xx = 01 to 12) 10P345xx (xx = 01 to 07) 10P391xx (xx = 01 to 02) P445: 10P445xx (xx = 01 to 04) P44x(P442 & P444): 10P44201 (SH 1 & 2) 10P44202 (SH 1) 10P44203 (SH 1 & 2) 10P44401 (SH 1) 10P44402 (SH 1) 10P44403 (SH 1 & 2) 10P44404 (SH 1) 10P44405 (SH 1) 10P44407 (SH 1 & 2) P44y (P443 & P446): 10P44303 (SH 01 and 03) 10P44304 (SH 01 and 03) 10P44305 (SH 01 and 03) 10P44306 (SH 01 and 03) 10P44600 10P44601 (SH 1 to 2) 10P44602 (SH 1 to 2) 10P44603 (SH 1 to 2)	P54x (P543, P544, P545 & P546): 10P54302 (SH 1 to 2) 10P54303 (SH 1 to 2) 10P54400 10P54404 (SH 1 to 2) 10P54405 (SH 1 to 2) 10P54502 (SH 1 to 2) 10P54503 (SH 1 to 2) 10P54600 10P54604 (SH 1 to 2) 10P54605 (SH 1 to 2) 10P54606 (SH 1 to 2) P547: 10P54702xx (xx = 01 to 02) 10P54703xx (xx = 01 to 02) 10P54704xx (xx = 01 to 02) 10P54705xx (xx = 01 to 02) P64x (P642, P643 & P645): 10P642xx (xx = 01 to 10) 10P643xx (xx = 01 to 06) 10P645xx (xx = 01 to 09) P74x (P741, P742 & P743): 10P740xx (xx = 01 to 07) P746: 10P746xx (xx = 00 to 21) P841: 10P84100 10P84101 (SH 1 to 2) 10P84102 (SH 1 to 2) 10P84103 (SH 1 to 2) 10P84104 (SH 1 to 2) 10P84105 (SH 1 to 2) P849: 10P849xx (xx = 01 to 06)

CONTENTS

TABLES

FIGURES

Notes:

1 INTRODUCTION TO HSR

1.1 Introduction to High-availability Seamless Redundancy (HSR)

This section gives an introduction to the High-availability Seamless Redundancy (HSR); and how it is implemented on MiCOM-based products manufactured by Schneider Electric.

1.2 Protocols

Industrial real-time Ethernets typically need much better levels of availability and uninterrupted operation than normal office-type Ethernet solutions. For power networks, even a short loss of connectivity may result in a significant loss of functionality or impaired safety. To recover from a network failure, various redundancy schemes have been considered, including: Rapid Spanning Tree Protocol (**RSTP**), Media Redundancy Protocol (**MRP**), High-availability Seamless Redundancy (**HSR**). The key properties of these are as follows:

RSTP This uses mesh-based topologies or ring topology and computes a tree, based on path costs and priorities. In case of network failure, a typical reset time for RSTP-based system is normally a few seconds.

MRP This uses ring-based topologies. In case of network failure, the network is broken into two separate lines, which are reconnected by de-blocking the previously blocked part. The guaranteed reset time for MRP protocol-based systems is typically around 100ms.

HSR HSR basically uses ring topology, This Clause describes the application of the HSR principles (Clause 5) to implement a High-availability Seamless Redundancy (HSR), retaining the PRP property of zero recovery time, applicable to any topology, in particular rings and rings of rings. With respect to PRP, HSR allows to roughly halve the network infrastructure. With respect to rings based on IEEE 802.1D (RSTP), IEC 62439-2 (MRP), IEC 62439-6 (DRP) or IEC 62439-7 (RRP), the available network bandwidth for network traffic is somewhat reduced depending on the type of traffic. Nodes within the ring are restricted to be HSR-capable bridging nodes, thus avoiding the use of dedicated bridges. Singly Attached Nodes (SANs) such as laptops or printers cannot be attached directly to the ring, but need attachment through a RedBox (redundancy box).

Power networks need to be able to respond to problems very quickly (typically in less than 10ms), and HSR is an available protocol which is robust enough to achieve this. The HSR protocol used in the MiCOM relay/IED is defined in the IEC62439-3 (2012) standard and is configured using the existing redundant Ethernet card(s).

1.3 HSR Summary (IEC 62439-3 Clause 5)

A summary of the main HSR features is given below:

- HSR Ethernet redundancy method independent of any industrial Ethernet protocol and typically used in a ring topology
- Seamless switchover and recovery in case of failure, which supports real-time communication
- Supervises redundancy continuously for better management of network devices
- Suitable for hot swap, 24 hour/365 day operation in substations
- Allows laptops and workstations to be connected to the network with HSR Redbox
- Particularly suited for substation automation, high-speed drives and transportation

1.4 Example of an HSR Network

Essentially a HSR network is a ring topology. An example of a HSR network is shown in Figure 1:

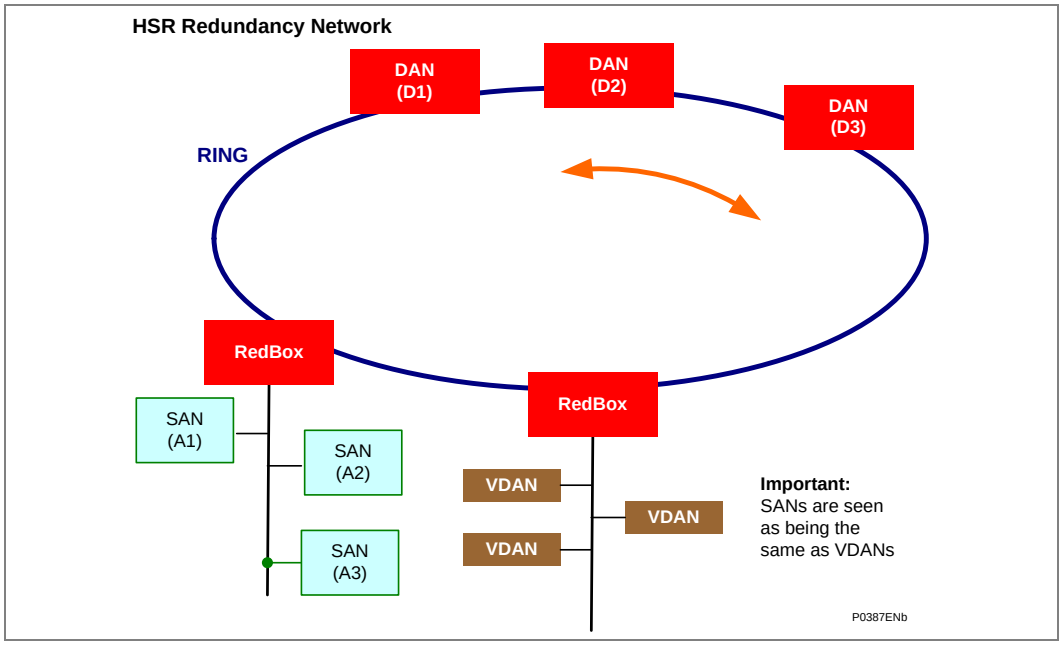


Figure 1 - HSR Redundancy Network

Figure 1 shows typical ring networks that have various Nodes in common.

The key features of the network include:

- Nodes within the ring are restricted to be HSR-capable bridging nodes, thus avoiding the use of dedicated bridges
- Singly Attached Nodes (SANs) such as laptops or printers cannot be attached directly to the ring, but need attachment through a RedBox (redundancy box)
- A simple HSR network consists of doubly attached bridging nodes, each having two ports, interconnected by full-duplex link
- A source DANH sends a frame passed from its upper layers, prefixes it by an HSR tag to identify frame duplicates and sends the frame over each port
- A destination DANH receives, in the fault-free state, two identical frames from each port within a certain interval, if it is a multicast frame, it instantaneously forwards it on the ring*, removes the HSR tag of the first frame before passing it to its upper layers and discards any duplicate.
- *:In particular, the node will not forward a frame that it injected into the ring.
- *:A destination node of a unicast frame does not forward a frame for which it is the only destination, except for testing.

1.5 Structure of a DAN

A MiCOM P40 relay working in HSR Mode works as a DAN within the overall network topology. Each DAN has two ports that operate in parallel. As in Figure 2, The two HSR ports A and B and the device port C are connected by the LRE, which includes a switching matrix allowing to forward frames from one port to the other. The switching matrix allows cut-through bridging. The Link Redundancy Entity (LRE) presents to the higher layers the same interface as a standard Ethernet transceiver would do.

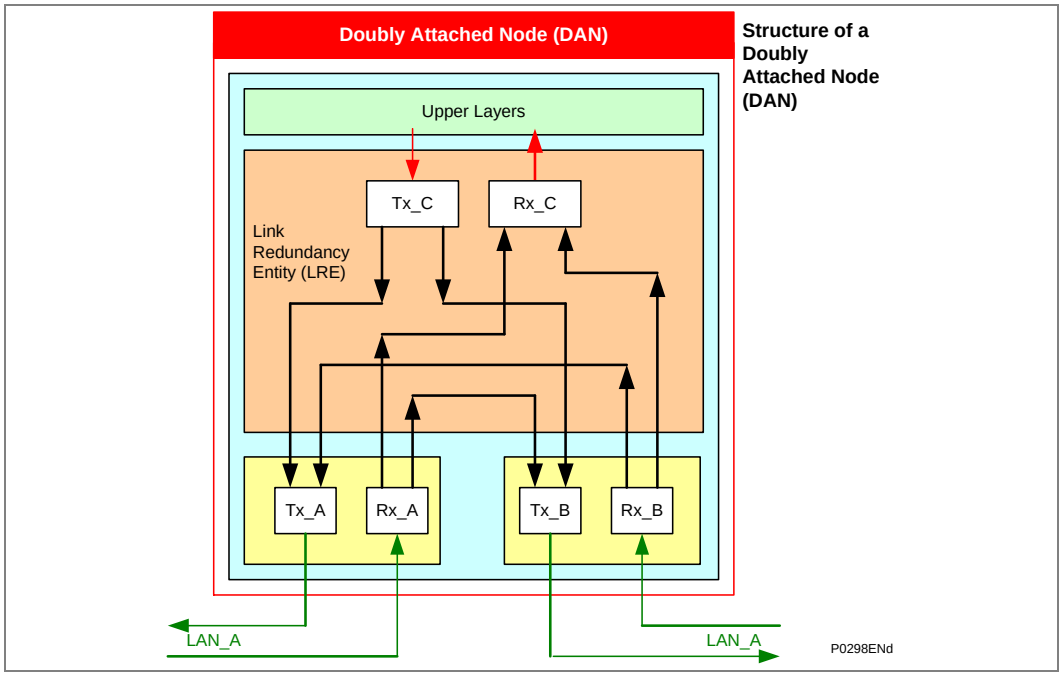


Figure 2 - DAN communication between two paths (in HSR)

DAN node is operable in HSR-tagged forwarding mode, the DAN inserts the HSR tag on behalf of its host and forwards the ring traffic, except for frames sent by the node itself. Duplicate frames and frames where the node is the unicast destination is not forwarded.

1.6 Structure of a RedBox

The RedBox has a LRE that performs the duties of the HSR protocol, in particular:

- forwards the frames received from one HSR port to the other HSR port, unless the frame receives frames addressed to its own upper protocols
- prefixes the frames sent by its own upper layers with the corresponding HSR tag before sending two copies over its HSR ports

The switching logic is incorporated into the RedBox, so interlink becomes an internal connection.

A simple RedBox is present in every node, since the LRE makes a transition to a single non-HSR host. In addition, it is usual to have more than one host in a node, since a port for maintenance often exists.

A node does not send over a port a frame that is a duplicate of a frame previously sent over that port in that same direction.

For the purpose of Duplicate Discard, a frame is identified by:

- its source MAC address;
- its sequence number.

The Duplicate Discard method forgets an entry identified by <Source MAC Address><Sequence number> after a time EntryForgetTime.

1.7 Communication between SANs, DANs and RedBoxs

Singly Attached Nodes (SANs), for instance maintenance laptops or printers cannot be inserted directly into the ring since they have only one port and cannot interpret the HSR tag in the frames. SANs communicate with ring devices through a RedBox (Redundancy Box) that acts as a proxy for the SANs attached to it.

A source DANH sends a frame passed from its upper layers, and prefixes it by an HSR tag to identify frame duplicates and sends the frame over both ports.

A destination DANH receives, in the fault-free state, two identical frames from each port within a certain interval, if it is a multicast frame, it instantaneously forwards it on the ring*,, removes the HSR tag of the first frame before passing it to its upper layers (“D”-frame) and discards any duplicate.

A typical frame contains these parameters:

- dest_addr Destination Address
- src_addr Source Address
- type Type
- data
- fcs Frame Check Sequence (i.e. extra checksum characters added to allow error detection and correction)

HSR frames are identified uniquely by their HSR tag.

The HSR tag consists of these parameters:

- 16-bit Ethertype (HSR_EtherType = 0x892F)
- 4-bit path identifier (PathId), 0000 for both HSR nodes A and B, and 0010-1111 for one of 7 PRP networks (A/B).
- 12-bit frame size (LSDUsize)
- 16-bit Sequence Number (SeqNr)

Note	*The 4-bit PathId field prevents reinjection of frames coming from one PRP network to another PRP network.*

Accordingly, a typical HSR frame then contains these parameters:

- dest_addr Destination Address
- src_addr Source Address
- HSR tag data:
  - 16-bit Ethertype (HSR_EtherType = 0x892F)
  - 4-bit path identifier
  - 12-bit frame size
  - 16-bit sequence number:
- type Type
- payload Payload
- Padding if needed
- fcs Frame Check Sequence

Padding	*After the payload data, there may be some data padding. This is added to frames which would otherwise be too short for conventional network traffic (minimum frame size is 70 octets).*
Size	*The frame size will vary depending on the contents of the frame and how it has been tagged by the various SANs and DANs. In VLANs, frame tags may be added or removed during transit through a switch. To make the length field independent of tagging, only the original LPDU and the HSR tag are considered in the size.*

Figure 3 and Figure 4 shows the frame types with different types of data.

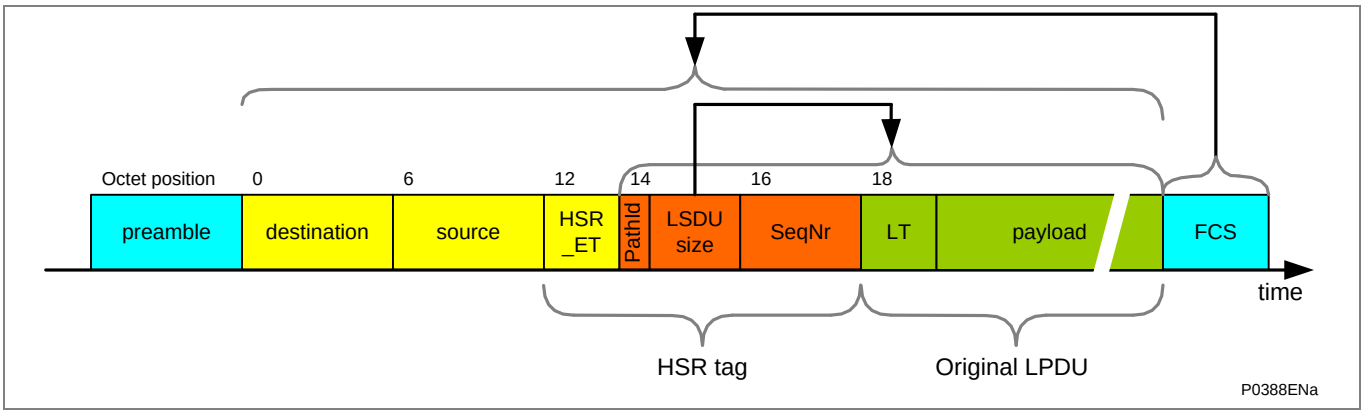


Figure 3 - HSR frame without a VLAN tag

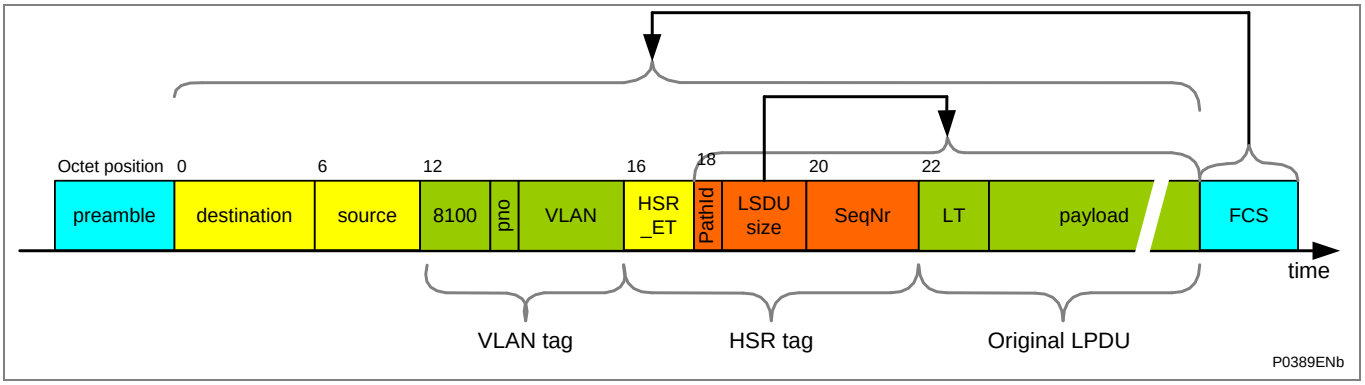


Figure 4 - HSR frame with VLAN tag

The key points about these differing frame structures are that:

- Unlike PRP, SANs cannot be attached directly to such a duplicated network unless they are able to interpret the HSR tag.
- In particular, the node will not forward a frame that it injected into the ring.
- A destination node of a unicast frame does not forward a frame for which it is the only destination, except for testing.
- DANH receiving from an HSR port, if this frame is not HSR-tagged and is a link local traffic, consume the frame and do not forward it.
- DANH receiving from an HSR port, if this frame is HSR-tagged and this node is not a destination, do not pass the frame to the link layer interface.
- A node accepts an HSR tagged frame also if the LanId does not correspond to the PortId and if the LSDUsize does not match the frame size.

1.8 HSR Technical Data

- One VLAN tag supported
- Up to 128 devices supported
- Up to 100Mbit/s full duplex Ethernet
- Dynamic frame memory allocation (page manager)
- Configurable duplicate detection
- Wishbone interface for configuration and status registers
- CPU port interface - Wishbone
- Support for link-local protocols - CPU may send to specific ports only - CPU knows receive port
- Configurable frame memory and queue length
- Duplicate detection with configurable size and aging time
- MAC address filtering (8 filter masks for interlink port, 6 for CPU port)
- Support for interfaces with or without Ethernet preamble

Limitations:

Number of IEDs on a same ring at 100Mbit/s:

Each hop (IED or RedBox) not only carries its own messages but also all the other IED messages thus the bandwidth used is proportional to the number of IEDs.

The maximum number of hops is around 20 when the GOOSE messages are highly used or 40 if the number and importance of GOOSE messages is not high.

When Precision Time Protocol («IEEE1588/IEC 61588») is used:

As the GPS receiver inaccuracy is 200ns and as each hop (IED or RedBox) can add a 50ns inaccuracy, the maximum number of hops is 16 if 1µs accuracy is required (PMU application or Process Bus)

2 HSR AND MICOM FUNCTIONS

2.1 MiCOM Products and HSR

The HSR functions being introduced as part of the overall MiCOM product range provide additional functionality, which is backwards compatible with existing Schneider Electric MiCOM equipment. This means that existing MiCOM relays/IEDS can be used on networks, which use HSR functions, with no changes being made to those relays/IEDs.

The new MiCOM products that use the HSR, will interrogate other equipment to determine the equipment model number, and then use the model number to decide (at runtime), whether that particular item of equipment can support HSR or not.

MiCOM models which include the following Ethernet board assembly provide the possibility of HSR function support. This is denoted by Digit 7 where the Hardware option is Q or R, as shown below:

Hardware Option	Type	Model No format
"Q" at Digit No 7	2 LC + 1 RJ45 ports redundant Ethernet board (Modulated/ Un-modulated IRIG-B)	**Px4xxxQx6Mxxx8M**
"R" at Digit No 7	3 RJ45 ports redundant Ethernet board (Modulated/ Un-modulated IRIG-B)	**Px4xxxRx6Mxxx8M**

Table 1 – Hardware option numbers with HSR functions

The MiCOM relay/IED firmware has been modified to allow the HSR options to be accepted for the power-up tests in addition to the implementation of the supervision frame transmission.

2.2 Easergy Studio Software and the HSR Function

The addition of this function has no impact of the Easergy Studio support files so there is no need to upgrade any Easergy Studio software.

2.3 MiCOM Relay Configuration and the HSR Function

There is no need to change the configuration of any relay (as relays which include support for this function will be able to recognize other devices which support it).

2.4 Hardware Changes for HSR Protocol

This protocol is implemented using the redundant Ethernet card as a starting point. The Frame management is achieved by programming the Field-Programmable Gate Array (FPGA).

The low-level management of the redundant frames is performed within the FPGA; this being defined as the Link Redundancy Entity (LRE). This will add the HSR tag to a frame to be transmitted. The FPGA is also responsible for the stripping of the HSR tag from received frames and discarding the duplicated messages so that only a single application frame is received by the Ethernet processor.

The LRE functionality of the supervision frame transmission is performed by the NIOS II.

The new version of the redundant Ethernet card is based on the 2072069A01 and 2072071A01 (both have modulated and un-modulated IRIG-B).

2.5 HSR Parameters

The Redundant Ethernet standard (IEC 62439-3:2012/FDIS) defines several parameters for the HSR protocol; these being fixed at a default value within this release. The following values are set:

Parameter	Value	Description
Supervision Frame Multicast Address	01-15-4E-00-01-00	Target MAC Address for multicast supervision frame
Life Check Interval	2 seconds	Period between transmission of supervision frames
HSR Mode	Duplicate Discard	This is normal HSR mode, Duplicate address will not be supported.
Node Forget Time	60 s	This is the time after which a node entry is cleared.
Entry Forget Time	400 ms	Duration that the received message Sequence number will be held to discard a duplicate message.
Node Reboot Interval	500ms	Duration following reboot for which no HSR frames should be transmitted.
MulticastFilterSize	16	Number of multicast addresses to be filtered

Table 2 - HSR parameter values

2.6 Product Implementation Features

Here is a list of the main Product Requirements for MiCOM products that support HSR:

- The MiCOM relay/IED provides two redundant Ethernet ports using HSR.
- The MiCOM relay/IED must be connected to the redundant Ethernet network as a Double Attached Node (DAN) using HSR (DAN using HSR is known as DANH)
- The redundant Ethernet interface can be made using an RJ45 or an optical fibre connection with an LC connector type.
- The management of the HSR redundancy is transparent to the application data provided via the Ethernet interface.
- The HSR option is available with any of the existing protocol options via the Ethernet Interface (IEC61850)
- Loss of one of the Node connections to the device does not cause any loss or degradation to the Application data over the Ethernet interface.
- The MiCOM relay/IED supports the transmission of the HSR Supervision frame at a fixed time period (LifeCheckInterval) of 2s (+/- 100ms)
- Each supervision frame includes a sequence number as defined in the IEC 62439-3:2012/FDIS specification. This will be incremented for each supervision message and the value will start from zero following a system restart.
- The MiCOM relay/IED does not provide for the HSR management to be configured (via either the MiCOM relay/IED HMI or the Ethernet interface). Accordingly, the default values (as defined within this document) are used for all HSR parameters.
- The performance of the Ethernet Interface is not degraded by using the HSR interface.

2.6.1 Abbreviations and Acronyms

Abbreviations / Acronyms	Meaning
CRC	Cyclic Redundancy Check
DAN	Doubly Attached Nodes
DANH	Doubly Attached Node implementing HSR
FPGA	Field-Programmable Gate Array
HMI	Human Machine Interface
HSR	High-availability Seamless Redundancy
IED	Intelligent Electronic Devices
IP	Internet Protocol
LAN	Local Area Network
LRE	Link Redundancy Entity
MAC	Media Access Control
MRP	Media Redundancy Protocol
PRP	Parallel Redundancy Protocol
HSR	High-availability Seamless Redundancy
RedBox	Redundancy Box
RSTP	Rapid Spanning Tree Protocol
SAN	Singly Attached Node
TCP	Transmission Control Protocol
VDAN	Virtual Doubly Attached Node

RSTP NOTES

CHAPTER 22

Date (month/year):	02/2018			
Products covered by this chapter:	This chapter covers the specific versions of the MiCOM products listed below. This includes ***only*** the following combinations of Software Version and Hardware Suffix.			
Hardware Suffix:	P141/P142/P143 P145 P445 P44x (P442/P444) P44y (P443/P446)	L M L M M	P54x (P543/P544/P545/P546) P642 P643/P645 P746 P841A (one circuit breaker) P841B (two circuit breakers)	M L M M M M
Software Version:	P14x (P141/P142/P143/P145) P445 P44x (P442/P444) P44y (P443/P446)	B4 J4/B0/B1/E0/E1 E3 H4	P54x (P543/P544/P545/P546) P64x (P642/P643/P645) P746 P841A P841B	H4 B4 B5/C5 G4 H4
Connection Diagrams:	P14x (P141, P142, P143 & P145): 10P141xx (xx = 01 to 02) 10P142xx (xx = 01 to 05) 10P143xx (xx = 01 to 11) 10P145xx (xx = 01 to 11) P445: 10P445xx (xx = 01 to 04) P44x(P442 & P444): 10P44201 (SH 1 & 2) 10P44202 (SH 1) 10P44203 (SH 1 & 2) 10P44401 (SH 1) 10P44402 (SH 1) 10P44403 (SH 1 & 2) 10P44404 (SH 1) 10P44405 (SH 1) 10P44407 (SH 1 & 2) P44y (P443 & P446): 10P44303 (SH 01 and 03) 10P44304 (SH 01 and 03) 10P44305 (SH 01 and 03) 10P44306 (SH 01 and 03) 10P44600 10P44601 (SH 1 to 2) 10P44602 (SH 1 to 2) 10P44603 (SH 1 to 2)		P54x (P543, P544, P545 & P546): 10P54302 (SH 1 to 2) 10P54303 (SH 1 to 2) 10P54400 10P54404 (SH 1 to 2) 10P54405 (SH 1 to 2) 10P54502 (SH 1 to 2) 10P54503 (SH 1 to 2) 10P54600 10P54604 (SH 1 to 2) 10P54605 (SH 1 to 2) 10P54606 (SH 1 to 2) P547: 10P54702xx (xx = 01 to 02) 10P54703xx (xx = 01 to 02) 10P54704xx (xx = 01 to 02) 10P54705xx (xx = 01 to 02) P64x (P642, P643 & P645): 10P642xx (xx = 01 to 10) 10P643xx (xx = 01 to 06) 10P645xx (xx = 01 to 09) P746: 10P746xx (xx = 00 to 21) P841: 10P84100 10P84101 (SH 1 to 2) 10P84102 (SH 1 to 2) 10P84103 (SH 1 to 2) 10P84104 (SH 1 to 2) 10P84105 (SH 1 to 2)	

CONTENTS

TABLES

FIGURES

Notes:

1 RAPID SPANNING TREE PROTOCOL (RSTP) NOTES

1.1 Introduction to RSTP

This section gives an introduction to the Rapid Spanning Tree Protocol (RSTP); and how it is implemented on MiCOM-based products manufactured by Schneider Electric.

1.2 Protocols

Industrial real-time Ethernets typically need much better levels of availability and uninterrupted operation than normal office-type Ethernet solutions. For power networks, even a short loss of connectivity may result in a significant loss of functionality or impaired safety. To recover from a network failure, various redundancy schemes have been considered, including: Rapid Spanning Tree Protocol (**RSTP**), Media Redundancy Protocol (**MRP**), High-availability Seamless Redundancy (**HSR**). The key properties of these are as follows:

RSTP This uses mesh-based topologies or ring topology and computes a tree, based on path costs and priorities. In case of network failure, a typical reset time for RSTP-based system is normally a few seconds.

MRP This uses ring-based topologies. In case of network failure, the network is broken into two separate lines, which are reconnected by de-blocking the previously blocked part. The guaranteed reset time for MRP protocol-based systems is typically around 100ms.

HSR HSR basically uses ring topology, This Clause describes the application of the HSR principles (Clause 5) to implement a High-availability Seamless Redundancy (HSR), retaining the PRP property of zero recovery time, applicable to any topology, in particular rings and rings of rings. With respect to PRP, HSR allows to roughly halve the network infrastructure. With respect to rings based on IEEE 802.1D (RSTP), IEC 62439-2 (MRP), IEC 62439-6 (DRP) or IEC 62439-7 (RRP), the available network bandwidth for network traffic is somewhat reduced depending on the type of traffic. Nodes within the ring are restricted to be HSR-capable bridging nodes, thus avoiding the use of dedicated bridges. Singly Attached Nodes (SANs) such as laptops or printers cannot be attached directly to the ring, but need attachment through a RedBox (redundancy box).

Power networks need to be able to respond to problems very quickly (typically in less than 10ms), and HSR is an available protocol which is robust enough to achieve this. The HSR protocol used in the MiCOM relay/IED is defined in the IEC62439-3 (2012) standard and is configured using the existing redundant Ethernet card(s).

1.3 Example of an RSTP Network

The Px4x Redundant Ethernet board uses the RSTP protocol (802.1w), so a Px4x can attach onto a network as shown in Figure 1:

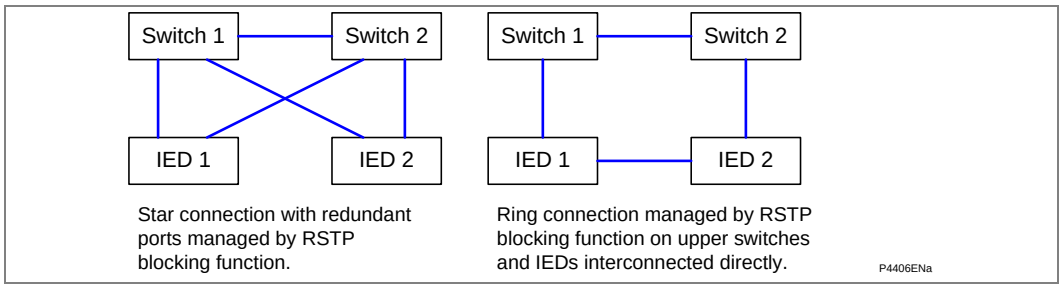


Figure 1 - Px4x attached to a redundant Ethernet star or ring circuit

The RSTP solution is based on open standards. It is therefore compatible with other manufacturers' IEDs that use the RSTP protocol. The RSTP recovery time is typically 300ms but it increases with network size.

2 RSTP AND MICOM FUNCTIONS

2.1 MiCOM Products and RSTP

The RSTP functions being introduced as part of the overall MiCOM product range provide additional functionality, which is backwards compatible with existing Schneider Electric MiCOM equipment. This means that existing MiCOM relays/IEDS can be used on networks, which use RSTP functions, with no changes being made to those relays/IEDs.

The new MiCOM products that use the RSTP, will interrogate other equipment to determine the equipment model number, and then use the model number to decide (at runtime), whether that particular item of equipment can support RSTP or not.

MiCOM models which include the following Ethernet board assembly provide the possibility of HSR function support. This is denoted by Digit 7 where the Hardware option is Q or R, as shown below:

Hardware Option	Type	Model No format
"Q" at Digit No 7	2 LC + 1 RJ45 ports redundant Ethernet board (Modulated/ Un-modulated IRIG-B)	**Px4xxxQx6Mxxx8M**
"R" at Digit No 7	3 RJ45 ports redundant Ethernet board (Modulated/ Un-modulated IRIG-B)	**Px4xxxRx6Mxxx8M**

Table 1 – Hardware option numbers with RSTP functions

The MiCOM relay/IED firmware has been modified to allow the RSTP options to be accepted for the power-up tests in addition to the implementation of the supervision frame transmission.

2.2 Easergy Studio Software and the RSTP Function

The addition of this function has no impact of the Easergy Studio support files so there is no need to upgrade any Easergy Studio software.

2.3 MiCOM Relay Configuration and the RSTP Function

There is no need to change the configuration of any relay (as relays which include support for this function will be able to recognize other devices which support it).

2.4 Hardware Changes for RSTP Protocol

This protocol is implemented using the redundant Ethernet card as a starting point. The Frame management is achieved by programming the Field-Programmable Gate Array (FPGA).

The low-level management of the redundant frames is performed within the FPGA; this being defined as the Link Redundancy Entity (LRE). This will add the RSTP tag to a frame to be transmitted. The FPGA is also responsible for the stripping of the RSTP tag from received frames and discarding the duplicated messages so that only a single application frame is received by the Ethernet processor.

The LRE functionality of the supervision frame transmission is performed by the NIOS II.

The new version of the redundant Ethernet card is based on the 2072069A01 and 2072071A01 (both have modulated and un-modulated IRIG-B).

2.5 RSTP Parameters

You can use the following settings to configure the RSTP function. The IEEE 802.1D 2004 standard defines the relation between Max Age and Forward Delay as:

2 * (Forward Delay – 1.0 seconds) >= Max Age

RSTP Settings

RSTP Settings	Value	Description
COMMUNICATIONS		

RSTP Settings	Value	Description
RSTPPriority	0 to 61440 with step 4096	Bridge Priority
RSTPMaxAge	6.0 to 40.0 with step 0.1	The max age time of RSTP
RSTPForwardDelay	4.0 to 30.0 with step 0.1	The timer of the RSTP forward delay
RSTPHelloTime	1.0 to 2.0 with step 0.1	The RSTP hello time settings

RSTP Status

RSTP Status	Value	Description
COMMUNICATIONS		
RSTPPortAStatus	FORWARDING, DISCARDING, DISABLED	The status RSTP Port A
RSTPPortBStatus	FORWARDING, DISCARDING, DISABLED	The status RSTP Port B

Notes *These two parameters are only visible on front panel (HMI).*
The following relays do not use any independent RSTP Configuration tool:
P14x (Software Version B4 and later)
P44x (Software Version E3 and later)
P445 (Software Version J9 and later)
P44y (Software Version H9 and later)
P54x (Software Version H9 and later)
P841 (Software Version G9 (P841A) & H9 (P841B) and later)
P64x (Software Version B4 and later)
P746 (Software Version B5/C5 and later)
All the RSTP parameters are configured via HMI and Easergy S1 Studio.

2.6 Product Implementation Features

Here is a list of the main Product Requirements for MiCOM products that support RSTP:

- The MiCOM relay/IED provides two redundant Ethernet ports using RSTP.
- The redundant Ethernet interface can be made using an RJ 45 or an optical fibre connection with an LC connector type.
- The management of the RSTP is transparent to the application data provided via the Ethernet interface.
- The RSTP option is available with any of the existing protocol options via the Ethernet Interface (IEC61850 and/or DNPoE)
- Loss of one of the Node connections to the device does not cause any loss or degradation to the Application data over the Ethernet interface.
- The MiCOM relay/IED supports the transmission of the RSTP RST BPDU at a fixed time interval.
- The MiCOM relay/IED provide for the RSTP management to be configured and RSTP status to be monitored via either the MiCOM relay or IED HMI.
- The performance of the Ethernet Interface is not degraded by using the RSTP interface.

2.7 Abbreviations and Acronyms

Abbreviations / Acronyms	Meaning
CRC	Cyclic Redundancy Check
DAN	Doubly Attached Nodes
DANP	Doubly Attached Node implementing PRP
FPGA	Field-Programmable Gate Array
HMI	Human Machine Interface
IED	Intelligent Electronic Devices
IP	Internet Protocol
LAN	Local Area Network
LRE	Link Redundancy Entity
MAC	Media Access Control
MRP	Media Redundancy Protocol
PRP	Parallel Redundancy Protocol
RCT	Redundancy Check Tag
RedBox	Redundancy Box
RSTP	Rapid Spanning Tree Protocol
SAN	Singly Attached Node
TCP	Transmission Control Protocol
VDAN	Virtual Doubly Attached Node

PROCESS BUS NOTES

CHAPTER 23

Date (month/year):	09/2018			
Products covered by this chapter:	This chapter covers the specific versions of the MiCOM products listed below. This includes ***only*** the following combinations of Software Version and Hardware Suffix.			
Hardware Suffix:	P141/P142/P143 P145 P445 P44x (P442 only for PB) P44y (P443/P446)	L M L M M	P54x (P543/P546 only for PB) P642 P643/P645 P746 P841A (one circuit breaker) P841B (two circuit breakers)	M L M M M M
Software Version:	P14x (P141/P142/P143/P145) P445 P44x (P442 only for PB) P44y (P443/P446)	B4 J9 E3 H9	P54x (P543/P546 only for PB) P64x (P642/P643/P645) P746 P841A (one circuit breaker) P841B (two circuit breakers)	H9 B4 B5/C5 H9 H9
Connection diagrams:	This includes a list of the Connection Diagrams for the Products covered by this document. All Models 10PX002 10PX003			

CONTENTS

TABLES

Page (PB) 23-

FIGURES

Page (PB) 23-

1 INTRODUCTION

The Process Bus board interfaces to IEC 61850-9-2LE and IEC61869-9 compliant Merging Units (MU). The Process Bus board replaces the conventional analogue inputs (analogue module) and is available in these Easergy protection relays:

- P141, P142, P143, P145 (feeder protection)
- P442, P443, P445 and P446 (distance protection)
- P543, P546 (line differential protection)
- P642, P643 and P645 (transformer protection)
- P746 (busbar protection)
- P841(multifunction line terminal IED)

Process bus is mainly used to communicate the primary values of current and voltage to a protection relay via an Ethernet network. Merging Units form the data acquisition layer in the network. They connect to the primary sensor, determining the instantaneous primary measurements and publishing them on the process bus.

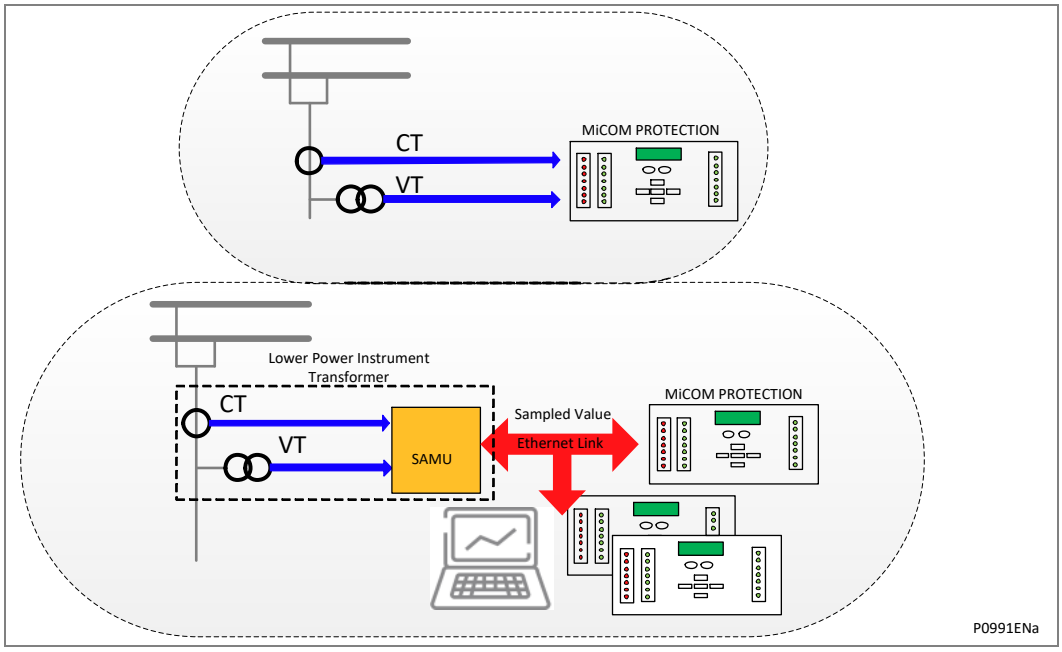


Figure 1 - Process Bus principle

The Process Bus philosophy is to be able to isolate from the secondary system such as protection or control IEDs the primary interfaces such as the breakers, isolators by interposing Breaker IED or Switch IED and/or CTs or VTs by interposing new primary equipment called LPIT (Low Power Instrument Transformers), previously known as NCIT (Non-Conventional Instrument Transformers) or Stand Alone Merging Units (SAMU). The Stand Alone Merging Unit (SAMU) converts 1/5A and 100/110V signals to process bus measurements (called Sampled Values). One feature that is mandatory for the Merging Unit is a very accurate clock source. Time is unique and common in the "analogue world" but is not in the digital world. Sampled values must be synchronized via IEC61850-9-3 (refer to IEC 61588/IEEE1588 Precision Time Protocol) or 1 Pulse Per Second (PPS) signal. The measurement values provided must be suitable for the protection application. This performance is ensured by the selection of primary sensors meeting the CT requirements of the protection application. These requirements must now be met by both the primary CT and the Merging Unit.

An IMU can embed other digital functionality, sending information such as position of breaker and isolators and receiving digital information such as close, open, trip or reclose commands over the process bus.

The process bus links allow multiple measurement streams as well as the digital information to be sent over common ethernet link which saves on the installation of secondary wiring. Also, the same stream can be utilized by multiple relays reducing the number of primary sensors required. This does, however, expose the system to a greater outage due to a link or switch failure. In most cases, redundancy such as IEC62439 PRP will be required to ensure system availability.

2 HARDWARE DESCRIPTION

2.1 Relay Rear Panel

2.1.1 Relay with Process Bus

The Process Bus board provides a IEC61850-9-2LE (80 samples/cycle) or IEC61869 (F4800S2IiUu where i+u<24) Ethernet link and IEC61850-8-1 (GOOSE).

The board fits into a dedicated slot of the Easergy P40 protection. The board can be connected to the network using:

- For the 3 RJ45 connectors board, either the top or both the bottom RJ45 connectors or
- For the 1 RJ45 connector and two optical fibre connectors board, either the top RJ45 connector or both the bottom LC connectors

Optical fiber connectors

- 1300nm multimode 100BaseFx LC® connectors

RJ45 connection

- 100BaseTx RJ45 connector

Case size

- The case size of all Easergy MiCOM P40 Process Bus relays is fixed at 60TE

Board Location

- The Process Bus board is fitted in slot C

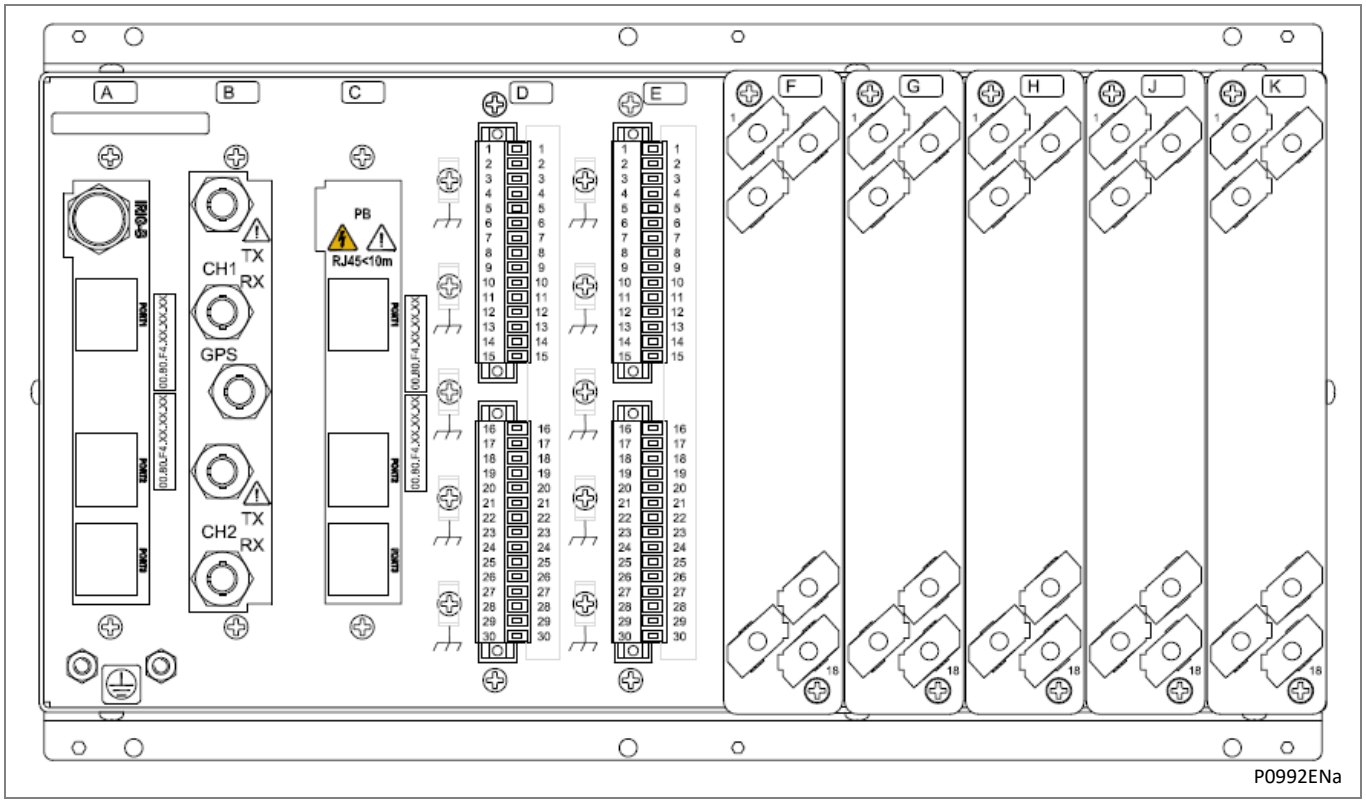


Figure 2 - Rear view of the process bus relay

3 OPERATION

When fitted, the Process Bus board replaces the analogue module board(s) with conventional CTs and VTs. In this case, the Process Bus board resamples the IEC 61850-9-2LE or IEC 61869 samples received from the process bus network and transforms them to the same format sent by the analogue module.

According to the application, Merging Units (MUs) are:

- MUs included in LPITs
- SAMUs, connected to Conventional CTs and/or VTs

Depending on the products, up to 6 or 7 MUs can be simultaneously subscribed by one Easergy P40 protection relay (for P746, the maximum number is 7, for other P40 relays, the maximum number is 6).

The protection algorithms are unchanged, they are the same for the Process Bus board and the analogue module(s).

The number of MUs varies depending upon the product, the SV configuration is flexible to support different kinds of products and application.

Note the derived quality bit introduced in IEC61850-9-2LE (no longer used in IEC61869) is ignored by the relay.

3.1 Single Merging Unit (MU) Configuration

A single MU can be directly connected to the process bus card on a dedicated Ethernet link allowing process bus to be used without any additional network components.

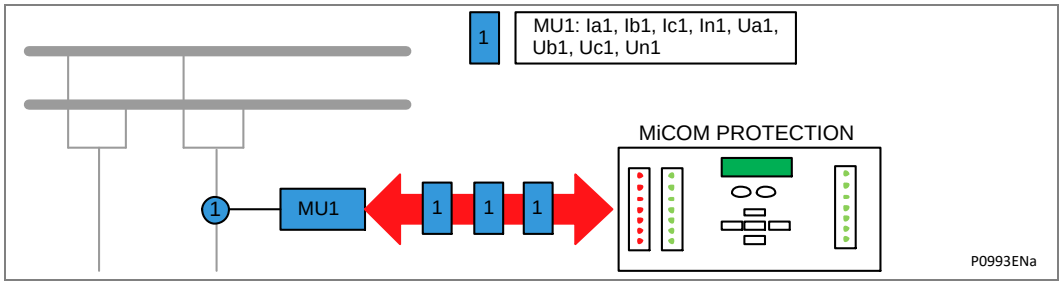


Figure 3 – Single Merging Unit (MU) configuration

3.1.1 SV Configuration Example

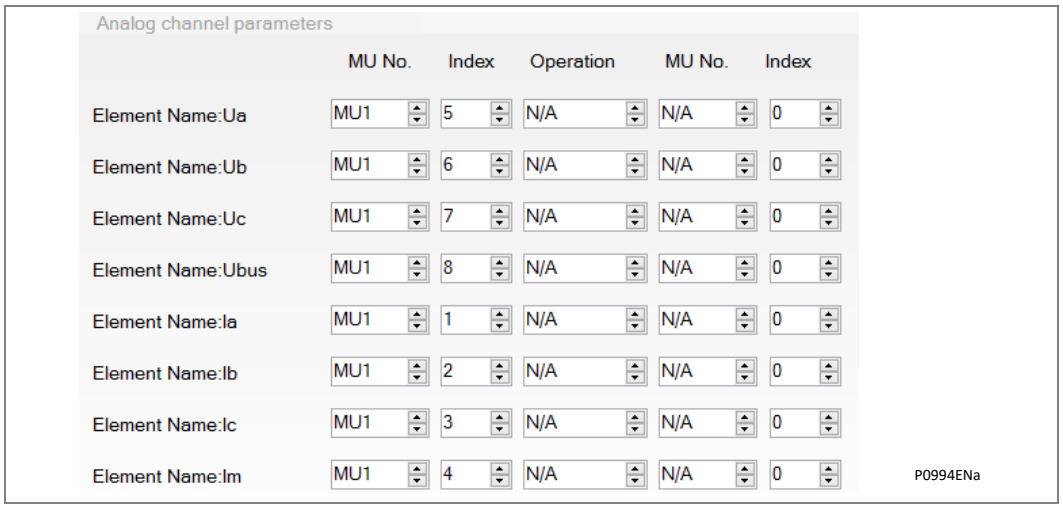


Figure 4 – CID configuration for one Merging Unit (MU)

In the above example the wiring normally brought to the relay has been connected to the merging unit. The check synch voltage input and mutual current input would normally require access to additional streams, however, in this case they have been wired to the neutral inputs of the MU. Since the relay inputs are configured by index it is then possible to allocate these channels to the appropriate analogue input.

3.2 Multiple Merging Unit (MU) Configuration

When the relay requires SV streams from multiple MUs an Ethernet network is required to provide the required streams to the relay. An example of a double bus application is shown below. In this case local synchronization is required for the check synch and mutual coupling functions.

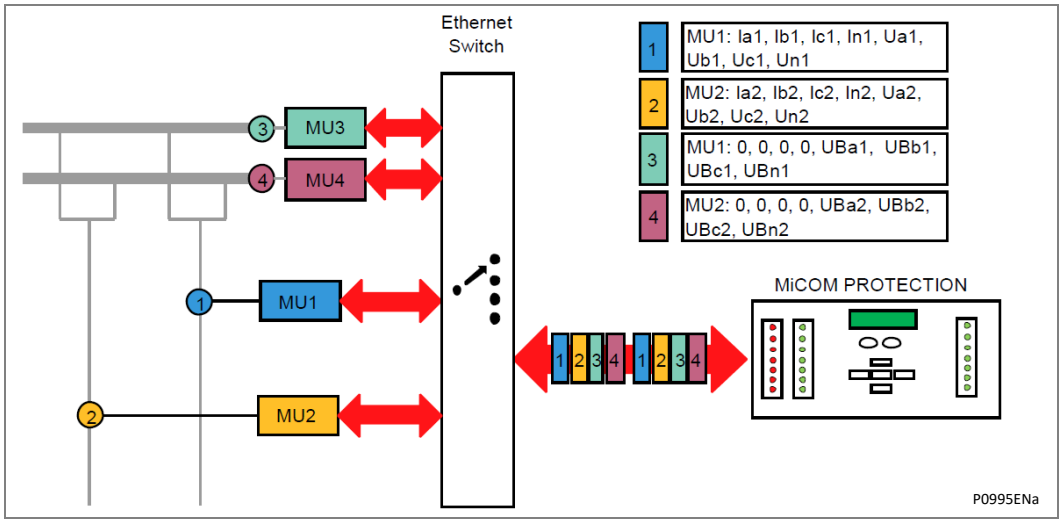


Figure 5 – Multiple Merging Unit (MU) configuration

The analogue channels are:

- MU1 = “Ia1, Ib1, Ic1, In1, Ua1, Ub1, Uc1, Un1”
- MU2 = “Ia2, Ib2, Ic2, In2, Ua2, Ub2, Uc2, Un2”
- MU3 = “0, 0, 0, 0, UBa1, UBb1, UBc1, UBn1”
- MU4 = “0, 0, 0, 0, UBa2, UBb2, UBc2, UBn2”

3.2.1 SV Configuration

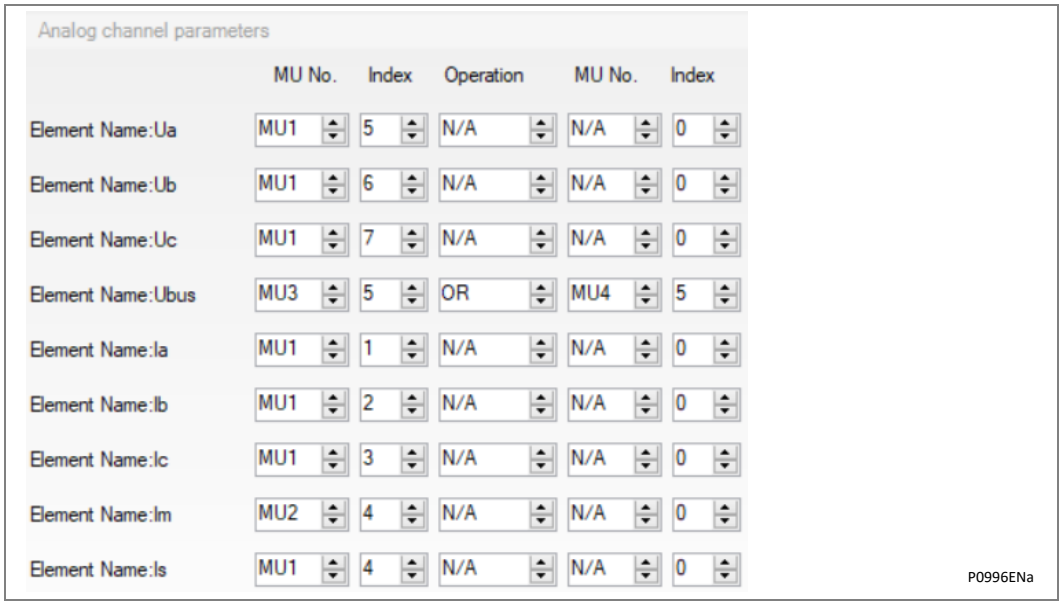


Figure 6 – CID configuration for four Merging Units (MUs)

In this example the main currents and voltages are provided by MU1. MU2 provides its neutral current to the mutual coupling input. The A phase voltage is used from MU3 or MU4 for the check synch input. The correct stream to use will depend upon which primary isolators are closed. The second bus isolator status is connected to the "Check Synch Alt1" DDB in the relay PSL to select MU4 for check synch when feeder is connected to the second bus. If this signal is low then the Check Synch input will come from MU3.

3.3 Multiple Relays

Since the SV streams are Ethernet signals they can be simultaneously used by multiple relays. In the example above, the feeder currents could also be used by a busbar protection and the busbar voltages would likely be used by other feeder protections. Care must be taken with sharing to avoid overloading the process bus network. VLANs are normally used to control the traffic to ensure that each IED only receives the SVs it uses ensuring no link is overloaded.

3.4 Data Resampling

The Process Bus relay receives 80 Sampled Values per cycle (4000 Sampled Values per second at 50Hz) or 4800 Sampled Values per second from the Merging Unit depending upon whether IEC61850-9-2LE or IEC61869 mode is used. The Process Bus board then resamples these Sampled Values and divides the values received by the input CT/VT ratio to make the data appear the same to the IED as analogue signals would do on its normal inputs from CTs and VTs. When a SAMU is used the ratios should match the primary CT/VT values. If a LPIT is used then the nominal switchgear ratings would normally be used to set the CT/VT ratios.

Caution	***The CT and VT ratios must be set to suitable values to ensure the relay has correct measuring and setting ranges***

The resampling frequency depends on the IED:

- P543, P546, P443, P445, P446, P841 - 48 samples/cycle
- P141, P142, P143, P145, P442, P642, P643, P645, P746 - 24 samples/cycle

Note	*The relay uses frequency tracking to follow the supply frequency, changing the number of samples per second when the frequency changes, where the process bus samples are fixed at 4000 samples/sec (50Hz) or 4800 samples/sec per different standard edition.*

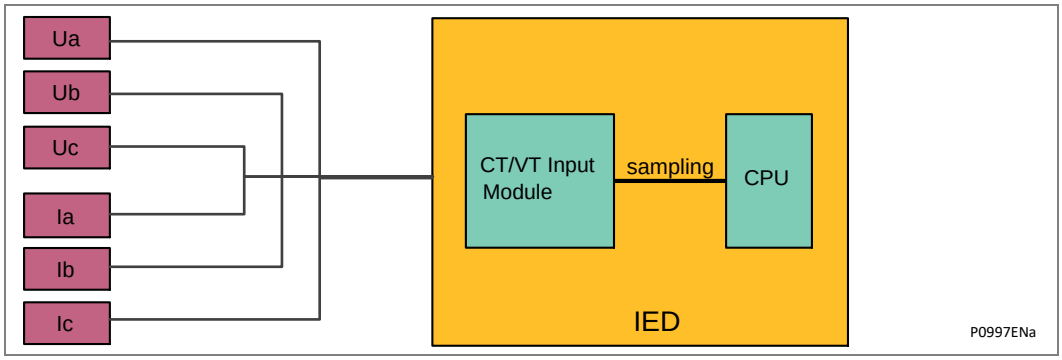


Figure 7 – Data sampling using CTs/VTs and an input board

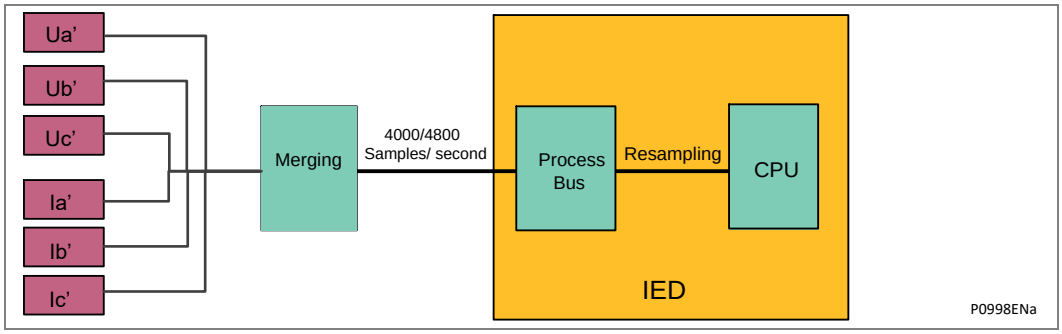


Figure 8 – Data sampling using Process Bus interface

4 CONFIGURATION

4.1 Settings

The Process Bus board must be configured to the system and application by means of appropriate settings. The sequence in which the settings are listed and described in this section will be the ***PB CONFIG*** submenu in the IED submenu.

Col	Row	Menu Text	Default Setting	Available Setting
00	13	Software Ref. 3	<Software Ref. 3>	Not settable
Relay Process Bus card software reference. Visible when Process Bus card fitted.				
00	15	IEC61850 Edition	Ed2	Not settable
This cell displays the supported IEC61850 Edition, only Ed2 is supported in Process Bus relays.				
00	17	PB COMM Mode	Dual IP	Dual IP, PRP
Sets the redundancy protocol of Process Bus board. This setting can only be changed via the UI and will cause the Process Bus board to reboot.				

Table 1 – Column 00 Settings for Process Bus Devices

Col	Row	Menu Text	Default Setting	Available Setting
18	00	PB CONFIG	Column Heading	
This column contains settings and status parameters relative to process bus				
18	01	MU OOS Config	00000000(bin)	
Used to set one or more Merging Units to be run in Out of Service mode.				
18	02	AntiAlias Filter	Disabled	0 = Disabled, 1 = Enabled
This cell activates or deactivates the anti-aliasing filter, which conditions the Sampled Values from the Process Bus network.				
18	03	SMV Version	IEC61850-9-2LE	0=IEC61850-9-2LE, 1 = IEC61869
This cell selects which version of sampled values are used, if it is set to IEC61850-9-2LE, the relay will subscribe the sampled value compliant with IEC61850-9-2LE, otherwise, device will subscribe the sampled value compliant with IEC61869.				
18	04	MUs Delay Offset	0s	From 0s to 3ms step 250us
This cell adjusts the maximum time-delay offset starting at the reception of the Ethernet message from the “first” Merging Unit (MU) to the reception of the Ethernet message from the “last” Merging Unit (MU). This time-delay should be adjusted to ensure all MU samples for the same time instant are received before sending to the relay processor.				
18	05	Mon Delay Offset	No	0 = No, 1 = Yes
When sampled values are received at the IED from different Merging Units, they do not arrive simultaneously due to differences in Merging Unit performance or different network path delays. After this setting is set to Yes, a command to monitor the maximum time-delay will be sent to Process Bus board. After Process Bus board has calculated a delay, it will send the delay time to main board for users to set a proper MUs Delay Offset.				
18	06	Max Delay Offset		Not Settable
This setting specifies the maximum time-delay supervised, supervision starting at the reception of the sampled value frame from the "first" Merging Unit to the reception of the sampled value frame from the last Merging Unit for each sample count. If >3ms, a -1 will be displayed.				
18	30	Synchro Mode	No SYNC CLK	0 = No SYNC CLK, 1 = Local Clock, 2 = Global Clock
This setting specifies the type of Sampled Value synchronization expected by the IED, depending on the application. Global Clock: The Sampled Values are synchronized with a global area clock (GPS like clock). Local Clock: The Sampled Values are synchronized with a local area clock signal at the substation. Sampled Value frames received with Global or Local synchronization are acceptable with this setting. No SYNC CLK: The Sampled Values do not need to be synchronized. With this setting the IED ignores the synchronization flag in the Sampled Value frames.				
18	31	SV Absence Alm		Not Settable

Col	Row	Menu Text	Default Setting	Available Setting
This is a data cell with 8 binary flags. It indicates the presence or absence of Sampled Values from each of the Merging Units the IED is communicating with. The cell data for each Merging Unit is continuously refreshed. Unused MUs will indicate a 0. 0: Sampled Values being received from the Merging Unit. 1: No Sampled Values being received from the Merging Unit.				
18	32	SV SmpSynch Alm		Not Settable
This is a data cell with 8 binary flags. It indicates the healthiness of the Sampled Values being received from each of the Merging Units configured. 0: Sampled Values received are synchronized. 1: Sampled Values received are not synchronized.				
18	33	SV Test Alm		Not Settable
This is a data cell with a binary flag for each of the analogue groups within the relay. It indicates the status of the IEC 61850 Quality attribute 'Test' in the Sampled Value frame used for that channel. If a channel is marked Test then functions associated with that channel are blocked unless the relay is in 'Test Mode'				
18	34	SV Invalid Alm		Not Settable
This is a data cell with a binary flag for each of the analogue groups within the relay. It indicates the status of the IEC 61850 Quality attribute 'Invalid' in the Sampled Value frame used for that channel. If a channel is marked Invalid then functions associated with that channel are blocked.				
18	35	SV Quest Alm		Not Settable
This is a data cell with a binary flag for each of the analogue groups within the relay. It indicates the status of the IEC 61850 Quality attribute 'Questionable' in the Sampled Value frame used for that channel. If a channel is marked Questionable then functions associated with that channel are blocked.				

Table 2 – Column 18 Settings for Process Bus Devices

4.2 DDB Signals for Process Bus Relays

The meaning of the DDB signals for Process Bus Relays. The relevant DDB signals are shown in these sections:

- DDB Signals for Process Bus for P14x (P141, P142, P143 & P145)
- DDB Signals for Process Bus for P445 and P44y (P443 & P446)
- DDB Signals for Process Bus for P54x (P543 & P546 for PB)
- DDB Signals for Process Bus for P64x (P642, P643 & P645)
- DDB Signals for Process Bus for P841 (P841A & P841B)

4.2.1 DDB Signals for Process Bus for P14x (P141, P142, P143 & P145)

DDB No.	Source	Description	English Text	P141	P142	P143	P145
314	SW	IEC 61850 accept simulated GOOSE and SV alarm	Sim.Signal Alm	*	*	*	*
778	SW	MU OOS Alarm	MU OOS Alarm	*	*	*	*
792	SW	Invalid IEC 61850 Configuration Alarm for PB	Invalid SV conf.	*	*	*	*
793	SW	SV Absence Alm	SV Absence Alm	*	*	*	*
794	SW	SV SmpSynch alarm	SV SmpSynch Alm	*	*	*	*
795	SW	SV Test alarm	SV Test Alm	*	*	*	*
796	SW	SV Invalid alarm	SV Invalid Alm	*	*	*	*
797	SW	SV Questionable alarm	SV Quest Alm	*	*	*	*
1216	SW	Process Bus Network Interface link 1 fail indication	PB Link 1 Fail	*	*	*	*
1217	SW	Process Bus Network Interface link 2 fail indication	PB Link 2 Fail	*	*	*	*
1218	SW	Process Bus Network Interface link 3 fail indication	PB Link 3 Fail	*	*	*	*
1219	SW	DDB_MU1_ABSENCE	MU1 Absence	*	*	*	*
1220	SW	DDB_MU2_ABSENCE	MU2 Absence	*	*	*	*
1221	SW	DDB_MU3_ABSENCE	MU3 Absence	*	*	*	*
1222	SW	DDB_MU4_ABSENCE	MU4 Absence	*	*	*	*
1223	SW	DDB_MU5_ABSENCE	MU5 Absence	*	*	*	*
1224	SW	DDB_MU6_ABSENCE	MU6 Absence	*	*	*	*
1225	SW	DDB_MU7_ABSENCE	MU7 Absence	*	*	*	*
1226	SW	DDB_MU8_ABSENCE	MU8 Absence	*	*	*	*
1227	SW	Main VT Inhibit	Main VT Inhibit	*	*	*	*
1228	SW	CS VT Inhibit	CS VT Inhibit			*	*
1229	SW	Phs CT Inhibit	Phs CT Inhibit	*	*	*	*
1230	SW	In CT Inhibit	In CT Inhibit	*	*	*	*
1231	SW	SEF CT Inhibit	SEF CT Inhibit	*	*	*	*
1232	SW	Main VT Synch alarm	Main VT Synch alarm	*	*	*	*
1233	SW	CS VT Synch alarm	CS VT Synch alarm			*	*
1234	SW	Phs CT Synch alarm	Phs CT Synch alarm	*	*	*	*
1235	SW	In CT Synch alarm	In CT Synch alarm	*	*	*	*
1236	SW	SEF CT Synch alarm	SEF CT Synch alarm	*	*	*	*
1914	PSL	Alternate other analogue channels	Channel Alt	*	*	*	*
1915	PSL	Signal used to alternate VCS 1	Check Sync Alt1	*	*	*	*

Table 3 – DDB Signals for Process Bus for P14x (P141, P142, P143 & P145)

4.2.2 DDB Signals for Process Bus for P445 and P44y (P443 & P446)

DDB No.	Source	Description	English Text	P443	P445	P446
360	SW	MU OOS alarm	MU OOS Alarm	*	*	*
361	SW	Invalid IEC 61850 Configuration alarm for PB	Invalid SV conf.	*	*	*
362	SW	SV Absence alarm	SV Absence Alm	*	*	*
379	SW	Accept simulated GOOSE and SV alarm	Sim.Signal Alm	*	*	*
380	SW	SV Synchronization alarm	SV SmpSynch Alm	*	*	*
381	SW	SV Test alarm	SV Test Alm	*	*	*
382	SW	SV Invalid alarm	SV Invalid Alm	*	*	*
383	SW	SV Questionable alarm	SV Quest Alm	*	*	*
1914	PSL	Signal used to alternate analogue channels except check synchronization voltages	Channel Alt	*	*	*
1915	PSL	Signal used to alternate VCS 1	Check Sync Alt1	*	*	*
1916	PSL	Signal used to alternate VCS 2	Check Sync Alt2			*
1917	SW	Process Bus Ethernet port 1 link fail indication	PB Link 1 Fail	*	*	*
1918	SW	Process Bus Ethernet port 2 link fail indication	PB Link 2 Fail	*	*	*
1919	SW	Process Bus Ethernet port 3 link fail indication	PB Link 3 Fail	*	*	*
1920	SW	MU1 Absence indication	MU1 Absence	*	*	*
1921	SW	MU2 Absence indication	MU2 Absence	*	*	*
1922	SW	MU3 Absence indication	MU3 Absence	*	*	*
1923	SW	MU4 Absence indication	MU4 Absence	*	*	*
1924	SW	MU5 Absence indication	MU5 Absence	*	*	*
1925	SW	MU6 Absence indication	MU6 Absence	*	*	*
1926	SW	MU7 Absence indication	MU7 Absence	*	*	*
1927	SW	MU8 Absence indication	MU8 Absence	*	*	*
1928	SW	Main VT inhibit indication	Main VT Inhibit	*	*	*
1929	SW	CS VT1 inhibit indication	CS VT1 Inhibit	*	*	*
1930	SW	Phs CT1 inhibit indication	Phs CT1 Inhibit	*	*	*
1931	SW	Mcomp CT inhibit indication	Mcomp CT Inhibit	*		*
1932	SW	SEF CT inhibit indication	SEF CT Inhibit	*	*	*
1933	SW	Phs CT2 inhibit indication	Phs CT2 Inhibit			*
1934	SW	CS VT2 inhibit indication	CS VT2 Inhibit			*
1935	SW	Main VT synchronization alarm	Main VT Sync Alm	*	*	*
1936	SW	CS VT1 synchronization alarm	CS VT1 Sync Alm	*	*	*
1937	SW	Phs CT1 synchronization alarm	Phs CT1 Sync Alm	*	*	*
1938	SW	Mcomp CT synchronization alarm	McompCT Sync Alm	*		*
1939	SW	SEF CT synchronization alarm	SEF CT Sync Alm	*	*	*
1940	SW	Phs CT2 synchronization alarm	Phs CT2 Sync Alm			*
1941	SW	CS VT2 synchronization alarm	CS VT2 Sync Alm			*

Table 4 – DDB Signals for Process Bus for P445 and P44y (P443 & P446)

4.2.3 DDB Signals for Process Bus for P54x (P543 & P546 for PB)

DDB No.	Source	Description	English Text	P543	P546
360	SW	MU OOS alarm	MU OOS Alarm	*	*
361	SW	Invalid IEC 61850 Configuration alarm for PB	Invalid SV conf.	*	*
362	SW	SV Absence alarm	SV Absence Alm	*	*
379	SW	Accept simulated GOOSE and SV alarm	Sim.Signal Alm	*	*
380	SW	SV Synchronization alarm	SV SmpSynch Alm	*	*
381	SW	SV Test alarm	SV Test Alm	*	*
382	SW	SV Invalid alarm	SV Invalid Alm	*	*
383	SW	SV Questionable alarm	SV Quest Alm	*	*
1914	PSL	Signal used to alternate analogue channels except check synchronization voltages	Channel Alt	*	*
1915	PSL	Signal used to alternate VCS 1	Check Sync Alt1	*	*
1916	PSL	Signal used to alternate VCS 2	Check Sync Alt2		*
1917	SW	Process Bus Ethernet port 1 link fail indication	PB Link 1 Fail	*	*
1918	SW	Process Bus Ethernet port 2 link fail indication	PB Link 2 Fail	*	*
1919	SW	Process Bus Ethernet port 3 link fail indication	PB Link 3 Fail	*	*
1920	SW	MU1 Absence indication	MU1 Absence	*	*
1921	SW	MU2 Absence indication	MU2 Absence	*	*
1922	SW	MU3 Absence indication	MU3 Absence	*	*
1923	SW	MU4 Absence indication	MU4 Absence	*	*
1924	SW	MU5 Absence indication	MU5 Absence	*	*
1925	SW	MU6 Absence indication	MU6 Absence	*	*
1926	SW	MU7 Absence indication	MU7 Absence	*	*
1927	SW	MU8 Absence indication	MU8 Absence	*	*
1928	SW	Main VT inhibit indication	Main VT Inhibit	*	*
1929	SW	CS VT1 inhibit indication	CS VT1 Inhibit	*	*
1930	SW	Phs CT1 inhibit indication	Phs CT1 Inhibit	*	*
1931	SW	Mcomp CT inhibit indication	Mcomp CT Inhibit	*	*
1932	SW	SEF CT inhibit indication	SEF CT Inhibit	*	*
1933	SW	Phs CT2 inhibit indication	Phs CT2 Inhibit		*
1934	SW	CS VT2 inhibit indication	CS VT2 Inhibit		*
1935	SW	Main VT synchronization alarm	Main VT Sync Alm	*	*
1936	SW	CS VT1 synchronization alarm	CS VT1 Sync Alm	*	*
1937	SW	Phs CT1 synchronization alarm	Phs CT1 Sync Alm	*	*
1938	SW	Mcomp CT synchronization alarm	McompCT Sync Alm	*	*
1939	SW	SEF CT synchronization alarm	SEF CT Sync Alm	*	*
1940	SW	Phs CT2 synchronization alarm	Phs CT2 Sync Alm		*
1941	SW	CS VT2 synchronization alarm	CS VT2 Sync Alm		*

Table 5 – DDB Signals for Process Bus for P54x (P543 & P546 for PB)

4.2.4 DDB Signals for Process Bus for P64x (P642, P643 & P645)

DDB No.	Source	Description	English Text	P642	P643	P645
520	SW	MU OOS alarm	MU OOS Alarm	*	*	*
521	SW	Invalid IEC 61850 Configuration alarm for PB	Invalid SV conf.	*	*	*
522	SW	SV Absence alarm	SV Absence Alm	*	*	*
539	SW	Accept simulated GOOSE and SV alarm	Sim.Signal Alm	*	*	*
540	SW	SV Synchronization alarm	SV SmpSynch Alm	*	*	*
541	SW	SV Test alarm	SV Test Alm	*	*	*
542	SW	SV Invalid alarm	SV Invalid Alm	*	*	*
543	SW	SV Questionable alarm	SV Quest Alm	*	*	*
1267	PSL	Signal used to alternate analogue channels except check synchronization voltages	Channel Alt	*	*	*
1268	SW	Process Bus Ethernet port 1 link fail indication	PB Link 1 Fail	*	*	*
1269	SW	Process Bus Ethernet port 2 link fail indication	PB Link 2 Fail	*	*	*
1270	SW	Process Bus Ethernet port 3 link fail indication	PB Link 3 Fail	*	*	*
1271	SW	MU1 Absence indication	MU1 Absence	*	*	*
1272	SW	MU2 Absence indication	MU2 Absence	*	*	*
1273	SW	MU3 Absence indication	MU3 Absence	*	*	*
1274	SW	MU4 Absence indication	MU4 Absence	*	*	*
1275	SW	MU5 Absence indication	MU5 Absence	*	*	*
1276	SW	MU6 Absence indication	MU6 Absence	*	*	*
1277	SW	MU7 Absence indication	MU7 Absence	*	*	*
1278	SW	MU8 Absence indication	MU8 Absence	*	*	*
1279	SW	Main VT inhibit indication	Main VT Inhibit		*	*
1280	SW	AUX VT Inhibit indication	Aux VT Inhibit	*	*	*
1281	SW	CT1 Inhibit indication	Phs CT1 Inhibit	*	*	*
1282	SW	CT2 Inhibit indication	Phs CT2 Inhibit	*	*	*
1283	SW	CT3 Inhibit indication	Phs CT3 Inhibit		*	*
1284	SW	CT4 Inhibit indication	Phs CT4 Inhibit			*
1285	SW	CT5 Inhibit indication	Phs CT5 Inhibit			*
1286	SW	TN1 Inhibit indication	IN T1 Inhibit	*	*	*
1287	SW	TN2 Inhibit indication	IN T2 Inhibit	*	*	*
1288	SW	TN3 Inhibit indication	IN T3 Inhibit		*	*
1289	SW	Main VT synchronization alarm	Main VT Sync Alm		*	*
1290	SW	AUX VT synchronization alarm	Aux VT Sync Alm	*	*	*
1291	SW	CT1 synchronization alarm	Phs CT1 Sync Alm	*	*	*
1292	SW	CT2 synchronization alarm	Phs CT2 Sync Alm	*	*	*
1293	SW	CT3 synchronization alarm	Phs CT3 Sync Alm		*	*
1294	SW	CT4 synchronization alarm	Phs CT4 Sync Alm			*
1295	SW	CT5 synchronization alarm	Phs CT5 Sync Alm			*
1296	SW	TN1 synchronization alarm	IN T1 Sync Alm	*	*	*

DDB No.	Source	Description	English Text	P642	P643	P645
1297	SW	TN2 synchronization alarm	IN T2 Sync Alm	*	*	*
1298	SW	TN3 synchronization alarm	IN T3 Sync Alm		*	*

Table 6 – DDB Signals for Process Bus for P64x (P642, P643 & P645)

4.2.5 DDB Signals for Process Bus for P841 (P841A & P841B)

DDB No.	Source	Description	English Text	P841A	P841B
360	SW	MU OOS alarm	MU OOS Alarm	*	*
361	SW	Invalid IEC 61850 Configuration alarm for PB	Invalid SV conf.	*	*
362	SW	SV Absence alarm	SV Absence Alm	*	*
379	SW	Accept simulated GOOSE and SV alarm	Sim.Signal Alm	*	*
380	SW	SV Synchronization alarm	SV SmpSynch Alm	*	*
381	SW	SV Test alarm	SV Test Alm	*	*
382	SW	SV Invalid alarm	SV Invalid Alm	*	*
383	SW	SV Questionable alarm	SV Quest Alm	*	*
1914	PSL	Signal used to alternate analogue channels except check synchronization voltages	Channel Alt	*	*
1915	PSL	Signal used to alternate VCS 1	Check Sync Alt1	*	*
1916	PSL	Signal used to alternate VCS 2	Check Sync Alt2		*
1917	SW	Process Bus Ethernet port 1 link fail indication	PB Link 1 Fail	*	*
1918	SW	Process Bus Ethernet port 2 link fail indication	PB Link 2 Fail	*	*
1919	SW	Process Bus Ethernet port 3 link fail indication	PB Link 3 Fail	*	*
1920	SW	MU1 Absence indication	MU1 Absence	*	*
1921	SW	MU2 Absence indication	MU2 Absence	*	*
1922	SW	MU3 Absence indication	MU3 Absence	*	*
1923	SW	MU4 Absence indication	MU4 Absence	*	*
1924	SW	MU5 Absence indication	MU5 Absence	*	*
1925	SW	MU6 Absence indication	MU6 Absence	*	*
1926	SW	MU7 Absence indication	MU7 Absence	*	*
1927	SW	MU8 Absence indication	MU8 Absence	*	*
1928	SW	Main VT inhibit indication	Main VT Inhibit	*	*
1929	SW	CS VT1 inhibit indication	CS VT1 Inhibit	*	*
1930	SW	Phs CT1 inhibit indication	Phs CT1 Inhibit	*	*
1931	SW	Mcomp CT inhibit indication	Mcomp CT Inhibit	*	*
1932	SW	SEF CT inhibit indication	SEF CT Inhibit	*	*
1933	SW	Phs CT2 inhibit indication	Phs CT2 Inhibit		*
1934	SW	CS VT2 inhibit indication	CS VT2 Inhibit		*
1935	SW	Main VT synchronization alarm	Main VT Sync Alm	*	*
1936	SW	CS VT1 synchronization alarm	CS VT1 Sync Alm	*	*
1937	SW	Phs CT1 synchronization alarm	Phs CT1 Sync Alm	*	*
1938	SW	Mcomp CT synchronization alarm	McompCT Sync Alm	*	*
1939	SW	SEF CT synchronization alarm	SEF CT Sync Alm	*	*
1940	SW	Phs CT2 synchronization alarm	Phs CT2 Sync Alm		*
1941	SW	CS VT2 synchronization alarm	CS VT2 Sync Alm		*

Table 7 – DDB Signals for Process Bus for P841

4.3 Setting Guide

This section details non-protection functions in addition to where and how they may be applied. It provides some worked examples on how the settings are applied to the relay.

4.3.1 Anti-Alias Filter

The Anti-Aliasing filter prevents high frequency noise from being sampled by the process bus board. Except for some special applications, where very high-speed processing is required, always enable this setting. For these special applications, the frequency response of the Merging Unit needs to checked to ensure aliasing does not occur at the relays internal sampling rate.

4.3.2 MUs Delay Offset

When Sampled Value frames come from different Merging Units (MUs) on the Process Bus network, they do not arrive at the same time at the IED. The transmission delay depends on the background Ethernet traffic and how many switches are used in the Process Bus network.

Transmission delays do not usually matter for functions such as three-phase overcurrent protection where current signals are all received in a single frame. However, a function such as distance protection uses voltage and current signals which may be from different MUs with different transmission delays. The Process Bus board synchronizes the voltage and current samples that are sent to the IEDs distance protection function. The IED then uses the **MUs Delay Offset** setting, which is set to the maximum expected delay between the first and last Sampled Value of the same count.

The following examples show how you would need to set the delay.

- If the IED subscribes to SV from one MU only, no delay is needed so it operates correctly with a **MUs Delay Offset** setting of '0ms'.
- If the IED subscribes to SVs from several MUs which arrive within the period of two consecutive SV frames, no delay is needed so it operates correctly with a **Merging Unit Delay** setting of '0ms'.
- If the IED subscribes to SVs from several MUs but the streams do not arrive within the period of two consecutive SV frames, set the **MUs Delay Offset** to an appropriate value for the IED to operate correctly.

To set the MU delay during commissioning, set **Mon Delay Offset** to **Yes**. The IED then monitors the Sampled Value frames received for the next one second and displays the maximum delay between identical time tagged samples (SmpCnt).

The setting will directly impact protection performance, as shown in this diagram:

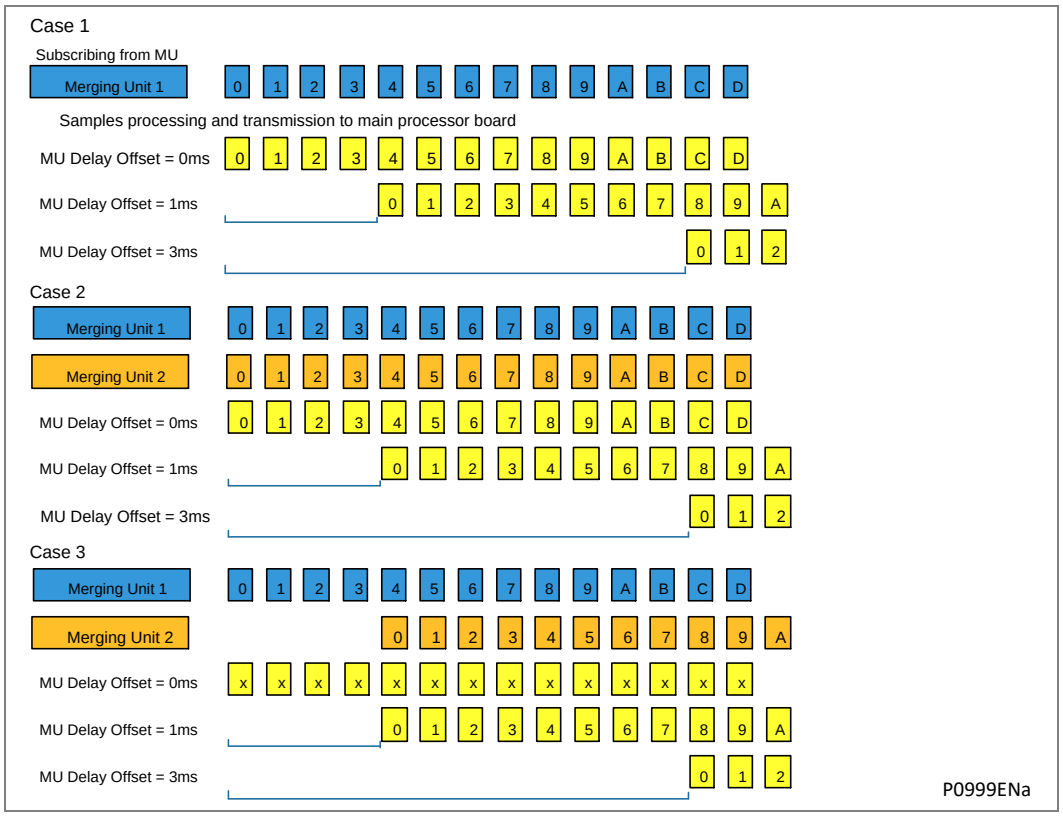


Figure 9 – Different MU Delay Offset for 400Hz Sample Rate

4.3.3 Synchro Mode

To process algorithms that need synchronized samples (for example distance with multiple MUs) coming from several Merging Units, we need to differentiate if the Sample Values (SV) are:

- not synchronized (one Merging Unit),
- synchronized with a local area clock (substation),
- synchronized with a global area clock (GPS…)

Three values are available:

- Global Clock — The relay will generate an alarm if MU synchronization is not “global area synchronization”
- Local Clock — The relay will generate an alarm if the MU synchronization is not global or local synchronization
- No SYNC CLK — The relay will not generate a synchronization alarm

With the exception of current differential, the loss of synchronization does not automatically block functions using these inputs. Whether a function needs to be blocked will depend on whether it uses signals from separate MUs. This will vary by application and affected functions should be blocked by linking the Synch Alarm to the affected function block input in the PSL.

4.3.4 Data Quality

Any degradation in the measurement or transmission of Sampled Values means that the protection function of the IED may not operate correctly. Therefore, to be able to detect invalid or questionable data, the IEC 61850 protocol assigns quality flags to each channel in the Sampled Value frame.

Data frames from a typical MU with, for example, four voltages and four currents [VA, VB, VC, VN, IA, IB, IC, IN] have quality flags for each of the channels. The IED adapts the behaviour of protection functions according to the quality flags. See the examples in the *Analogue Channel Groups* section.

The front panel of the IED shows the quality flags for each of the analogue channel groups configured. The number of analogue channel groups depends on the IED type.

To make protection functions work correctly, the Sampled Values arriving at the IED should have Good quality, as defined by the IEC 61850 or IEC61869 standards. Samples that have an Invalid or Questionable quality could result in unacceptable performance from the protection functions.

A protection function operates normally when all the necessary Sampled Value inputs are available and have a Good quality flag. When the flag for one or more of the Sampled Value inputs changes to Invalid or Questionable, the protection function is temporarily inhibited. The protection function returns to normal state when the quality flags for all the necessary Sampled Value inputs are Good. The quality flags can change with each sample, therefore there is a one-cycle transition delay between the Normal and Inhibit states for each protection function.

4.3.5 Analogue Channel Groups

The following tables shows how Sampled Value errors affect protection functions in the IED in different products.

Note	*The quality for analogue groups is commoned. For example, if one CT channel has poor quality, all channels in the CT group are given poor quality. When the P746 is used in 3 box mode the same quality is given to each group of 3 current channels.*

For example, overcurrent protection can be configured as directional, in which case the voltage inputs have an impact on the function. In another case, the quality of the voltage input is not important if the overcurrent is nondirectional. The meanings as shown here:

- ● = the SMV quality affects inhibit states of the protection function.
- ❍ = the protection function is affected where configured to work with this input.
- ■ = the protection operates if any input has good quality.
- □ = the protection operates if configured to work with this input and it has good quality.

The possible options are in these sections:

- Products with one set of CT, P141, P142
- Products with one set of CT, P143, P145
- Products with one set of CT, P443, P445, P543, P841A
- Products with two sets of CT, P446, P546, P841B
- Products with two sets of CT, P642
- Products with three sets of CT, P643
- Products with five sets of CT, P645

4.3.5.1 Products with one set of CT, P141, P142

Protection for Products with one set of CT, P141, P142	Groups				Comments
	CT	VT	IN CT	SEN CT	
Overcurrent Protection	●	❍			
Negative Sequence	●	❍			
Broken Conductor	●				
Earth Fault 1 Protection		❍	●		
Earth Fault 2 Protection	●	❍			
REF Protection	❍		❍	❍	
SEF Protection		❍		●	
Residual Overvoltage		●			
Voltage Protection		●			
System check		●			
Thermal Overload	●				
Admit Protection		●	❍	❍	
Sensitive Power Protection		●		●	
Power Protection	●	●			
VTS	●	●			
CTS	●	●			
CB Fail	■		■	■	
Frequency Protection	■	■			

Table 8 – How sample quality impacts protection (products with one set of CT, P141, P142)

4.3.5.2 Products with one set of CT, P143, P145

Protection for Products with one set of CT, P143, P145	Groups					Comments
	CT	VT	CS VT	IN CT	SEN CT	
Overcurrent Protection	●	❍				
Negative Sequence	●	❍				
Broken Conductor	●					
Earth Fault 1 Protection		❍		●		
Earth Fault 2 Protection	●	❍				
REF Protection	❍			❍	❍	
SEF Protection		❍			●	
Residual Overvoltage		●				
Voltage Protection		●				
System check		●	❍			
Thermal Overload	●					
Admit Protection		●		❍	❍	
Power Protection	●	●				
Sensitive Power Protection		●			●	
VTS	●	●				
CTS	●	●				
CB Fail	■			■	■	
Frequency Protection	■	■				

Table 9 – How sample quality impacts protection (products with one set of CT, P143, P145)

4.3.5.3 Products with one set of CT, P443, P445, P543, P841A

Protection for Products with one set of CT, P443, P445, P543, P841A	Group					
	CT1	Mutual CT	VT	CS VT1	Sen CT	Comments
Differential Protection	●		❍			
Distance Protection	●	❍	●			
Directional Earth Fault	●		●			
Overcurrent Protection	●		❍			
Negative Sequence	●		❍			
Broken Conductor	●					
Earth Fault Protection	●		❍			
REF Protection					●	
SEF Protection			❍		●	
Residual Overvoltage			●			
Voltage Protection			●			
Check Sync			●	●		
Loss of Load	●					
Thermal Overload	●					
VTS	●				●	
CTS	●				❍	
CB Fail	■				■	
Frequency Protection	■		■			

Table 10 – How sample quality impacts protection (products with one set of CT, P443, P445, P543, P841A)

4.3.5.4 Products with two sets of CT, P446, P546, P841B

Protection for Products with two sets of CT, P446, P546, P841B	Group							
	CT1	CT2	Mutual CT	VT	CS VT1	CS VT2	Sen CT	Comments
Differential Protection	●	●		❍				
Distance Protection	●	●	❍	●				
Directional Earth Fault	●	●		●				
Overcurrent Protection	❍	❍		❍				
Negative Sequence	●	●		❍				
Broken Conductor	●	●						
Earth Fault Protection	●	●		❍				
REF Protection							●	
SEF Protection				❍			●	
Residual Overvoltage				●				
Voltage Protection				●				
Check Sync				●	❍	❍		
Loss of Load	●	●						
Thermal Overload	●	●						
VTS	●	●		❍				
CTS	●	●		❍				
CB1 Fail	■						■	
CB2 Fail		■					■	
Frequency Protection	■	■		■				

Table 11 – How sample quality impacts protection (products with two sets of CT, P446, P546, P841B)

If only one CT is configured the first table would apply to whichever CT is configured.
When both CTs are configured within IED configurator the second table would apply.

4.3.5.5 Products with two sets of CT, P642

Protection for Products with two sets of CT, P642	Groups					Comments
	CT1	CT2	TN1	TN2	Aux VT	
Overcurrent protection	❍	❍			❍	
Negative phase sequence overcurrent	❍	❍			❍	
Earth Fault protection (Derived)	❍	❍				
Earth Fault protection (Measured)			❍	❍		
REF protection (REF HV)	❍		●			
REF protection (REF LV)		❍		●		
Thermal overload (HV)	●					
Thermal overload (LV)		●				
Thermal overload (Bias)	●	●				
Overvoltage protection					●	
Undervoltage protection					●	
Negative sequence overvoltage					●	
Differential protection	●	●				
Overfluxing protection					●	
Through fault (HV)	●					
Through fault (LV)		●				
CTS	●	●				
T1 CB Fail	■		□	□		
T2 CB Fail		■	□	□		
Frequency protection	■	■			■	

Table 12 – How sample quality impacts protection (products with two sets of CT, P642)

4.3.5.6 Products with three sets of CT, P643

Protection for Products with three sets of CT, P643	Groups								Comments
	CT1	CT2	CT3	TN1	TN2	TN3	Main VT	Aux VT	
Overcurrent protection	❍	❍	❍				❍		
Negative phase sequence overcurrent	❍	❍	❍				❍		
Earth Fault protection (Derived)	❍	❍	❍				❍		
Earth Fault protection (Measured)				❍	❍	❍	❍		
REF protection (REF HV)	❍	❍		●					
REF protection (REF LV)		❍	❍		●				
REF protection (REF TV)		❍				●			
Residual overvoltage							●		
Thermal overload (HV)	●	❍							
Thermal overload (LV)		❍	●						
Thermal overload (TV)		●							
Thermal overload (Bias)	●	❍	●						
Overvoltage protection							●		
Undervoltage protection							●		
Negative sequence overvoltage							●		
Differential protection	●	❍	●						
Overfluxing protection		❍					❍	❍	
Through fault (HV)	●	❍							
Through fault (LV)		❍	●						
Through fault (TV)		●							
VTS	❍	❍	❍				●		
CTS	●	❍	●						
T1 CB Fail	■			□	□	□			
T2 CB Fail		■		□	□	□			
T3 CB Fail			■	□	□	□			
Frequency protection	■	■	■				■	■	

Table 13 – How sample quality impacts protection (products with three sets of CT, P643)

4.3.5.7 Products with five sets of CT, P645

Protection for Products with five sets of CT, P645	Groups										Comments
	CT1	CT2	CT3	CT4	CT5	TN1	TN2	TN3	Main VT	Aux VT	
Overcurrent protection	❍	❍	❍	❍	❍				❍		
Negative phase sequence overcurrent	❍	❍	❍	❍	❍				❍		
Earth Fault protection (Derived)	❍	❍	❍	❍	❍				❍		
Earth Fault protection (Measured)						❍	❍	❍	❍		
REF protection (REF HV)	❍	❍	❍	❍		●					
REF protection (REF LV)		❍	❍	❍	❍		●				
REF protection (REF TV)		❍	❍	❍				●			
Residual overvoltage									●		
Thermal overload (HV)	●	❍	❍	❍							
Thermal overload (LV)		❍	❍	❍	●						
Thermal overload (TV)		❍	●	❍							
Thermal overload (Bias)	●	❍	❍	❍	●						
Overvoltage protection									●		
Undervoltage protection									●		
Negative sequence overvoltage									●		
Differential protection	●	❍	❍	❍	●						
Overfluxing protection									❍	❍	
Through fault (HV)	●	❍	❍	❍							
Through fault (LV)		❍	❍	❍	●						
Through fault (TV)		❍	●	❍							
VTS	❍	❍	❍	❍					●		
CTS	●	❍	❍	❍	●						
T1 CB Fail	■					□	□	□			
T2 CB Fail		■				□	□	□			
T3 CB Fail			■			□	□	□			
T4 CB Fail				■		□	□	□			
T5 CB Fail					■	□	□	□			
Frequency protection	■	■	■	■	■				■	■	

Table 14 – How sample quality impacts protection (products with five sets of CT, P645)

4.4 Simulation SV

Process Bus relays can be configured to subscribe to normal or simulation SVs. This is achieved by modifying the setting cell ***Sub.Sim.Signal*** in ***IED Configurator*** menu. The setting can be set to Yes or No.

In the data package of the SV frame, one bit is used to indicate the SV is 'Simulated' SV or normal SV. When ***Sub.Sim.Signal*** is set to No, only normal SV will be subscribed. When ***Sub.Sim.Signal*** is set to Yes, an alarm "Sim.Signal Alm" will be raised, the behaviour of the relay is the same as handling simulation GOOSE. The relay will subscribe normal SV until it finds a corresponding simulation SV. It will then subscribe to the simulation SV.

Warning **The *Sub.Sim. Signal* must be disabled after testing.**

4.5 Merging Unit (MU) Out-Of-Service (OOS) Configuration

Primary plant and its associated Merging Unit (MU) may be placed out of service but require the protection to remain in service. For example, a tie breaker on a breaker-and-a-half scheme may be taken Out Of Service (OOS) for maintenance. During this time the feeder is still in service being fed from the other breaker, therefore the protection needs to be active. If the MU stream is missing, has bad quality or is in test mode the protection would normally be disabled. To enable the relay to operate under these conditions a setting ***MU OOS Config*** is implemented to set one or more MUs to be run in OOS mode. When a MU is set to OOS, no matter what the actual Sampled Value is, the process bus board will set the analogue value and the quality of the MU to 0 with good synchronization. When one or more MU are set to OOS mode, an alarm "MU OOS Alarm" will be raised.

4.6 Analogue Channel Switching

The analogue channels may need to be switched from one CT/VT to another CT/VT during operation. The analogue channels switching function is setup in the CID configuration. The PSL is then used to energize one or more dedicated DDB signals to switch the streams.

The relay allows the user to switch all main CT and VT analogue channels input between two independent Sampled Value frames while the IED is in service. This may correspond to two separate CT or VT in the primary system. The single-phase check synchronizing voltages is also allowed to be selected from two independent Sampled Value frames.

Every check synchronizing voltage channel is controlled by a DDB, but different products may have different number of check synchronizing voltage channels. For example, P543 only has one such channel (Vcs1), while P546 has two channels (Vcs1 and Vcs2). Vcs1 switching is always controlled by DDB_VCS1_ALT, Vcs2 switching is always controlled by DDB_VCS2_ALT. All other analogue channels are controlled by another DDB, which is DDB_CHAN_ALT. If a product does not have check synchronizing, it will only have one dedicated DDB to be used to control channel switching.

It can take up to 100ms for the relay to switch channels. This is normally performed when the affected function is off-line (e.g. check synch input is not switched at the same time as synch check is being performed). A switching transient may be produced, particularly if there is a phase difference between the signals. This transient could appear as a frequency change or current/voltage delta. If on line switching is to be used this may require elements to be blocked to ensure the transients do not affect connected functions.

4.6.1 Switch Check Synchronizing Voltage Channel

Assume we are using a P543 relay which only has Vline and Vcs1 which are compared for the check synch function. If the line is connected to B-I the relay needs to compare Vline vs VT B-I but if the line is connected to B-II the relay needs to compare VLine vs VT B-II. In process bus application VT B-I and VT B-II can be provided by 1 or 2 different Merging Units. The measured value of VT B-I and VT B-II will be published and the relay needs to be able to subscribe the appropriate stream based on the position of busbar isolators.

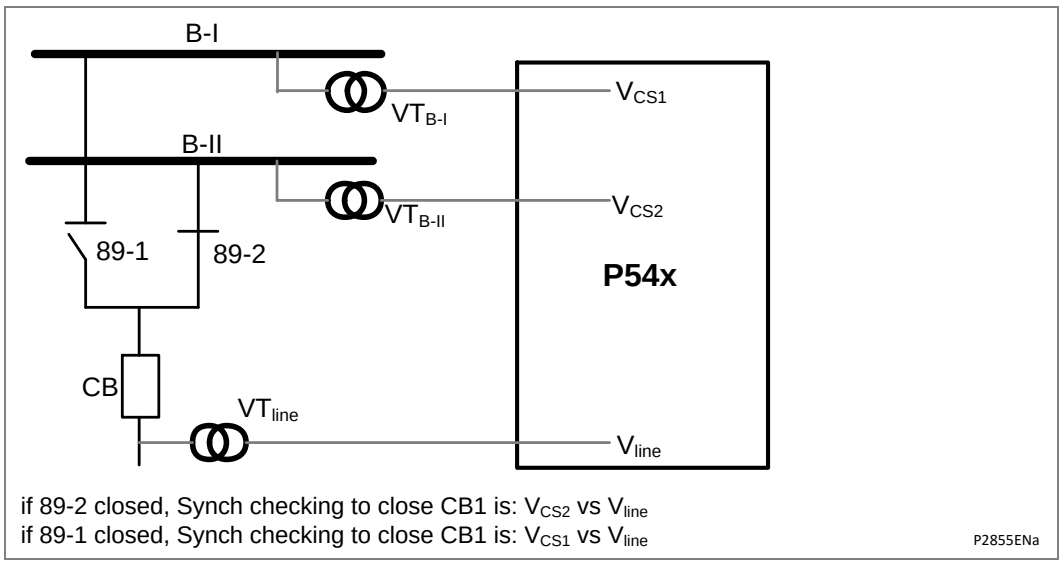


Figure 10 – A typical P543 application

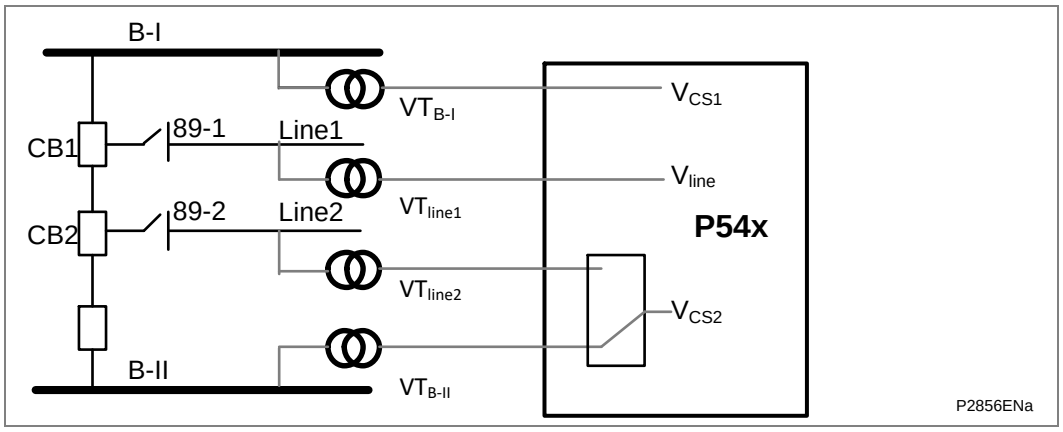


Figure 11 – One CB and a half application

As it can be seen in one-and-a-half breaker configuration, up to 4 VT measurements may be required. Therefore, the PB application requires access to the same measurements. In a traditional scheme the Vcs2 is fed from an external voltage selection scheme based on isolator positions. To replicate this functionality in PB we need to replace the voltage selection by stream switching based on the same logic used to operate the traditional voltage selection scheme.

To switch a check synchronizing channel, configure an OR operator using IED configurator as shown below:

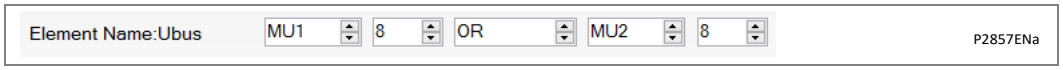


Figure 12 – IED configurator

The switching is controlled by the status of the DDB_VCS1_ALT. The PSL configuration and the logic is shown in the following table. When Opto Input 1 is energized, DDB_VCS_ALT becomes TRUE, and then Ubus is switched from the 8th channel of MU1 to the 8th channel of MU2.

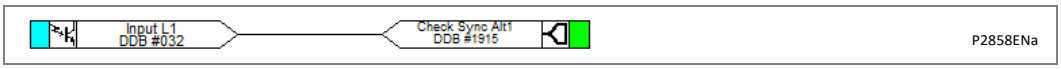


Figure 13 – PSL configuration and logic

DDB_VCS1_ALT Status	Check Sync Voltage Source
0	Check synchronizing voltage frames of MU1
1	Check synchronizing voltage frames of MU2

Table 15 - PSL configuration and logic

4.6.2 Switch Other Analogue Channels

To switch the three-phase voltage configure the CID as shown below:

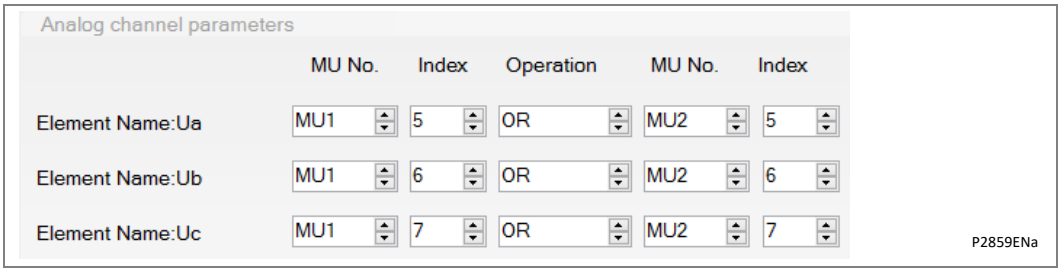


Figure 14 - OR operation

The switching is controlled by the status of the DDB_CHAN_ALT. The logic is shown in the following table.

DDB_CHAN_ALT Status	Three Phase-Voltage Source
0	Voltage frames of MU1
1	Voltage frames of MU2

Table 16 – Switching logic

4.7 Measurement Operation

Besides analogue channel switching, the relay also provides two Sampled Value operations for all channels, the two operations are plus and minus.

4.7.1 Measurement Addition Operation

An analogue channel can be configured to give the Sampled Value addition from two separate SVs.

Figure 15 – Configure analogue channel for addition

If Sampled Value addition operation is configured for Im, the actual value of of Im will be the Sampled Value summation of the 4th data channel of MU1 and the 4th data channel of MU2.

4.7.2 Measurement Subtraction Operation

An analogue channel can be configured to give the Sampled Value difference result from two separate SVs.

Figure 16 – Configure analogue channel for subtraction

If Sampled Value plus operation is configured for Ia, the actual value of Ia will be the Sampled Value difference of the 1st data channel of MU1 and the 1st data channel of MU2.

4.8 IEC61850 Enhanced Features

4.8.1 Two Dedicated GOOSE Control Blocks

In addition to the existing 16 GOOSE control blocks, the Process Bus relays provide two dedicated GOOSE Control Blocks, GCB17 and GCB18. Only these two GCBs can be published via the Process Bus board. The existing 16 GCBs can only be published via the Station Bus board.

Note that only digital information can be published via Process Bus GOOSE control blocks.

4.8.2 GOOSE VIP

All GOOSE VIP signals will be detected by both Station Bus and Process Bus boards, which means different VIP signals should be used in different networks, Station Bus network or Process Bus network.

If a GOOSE is published to both Station Bus network and Process Bus network, both Station Bus board and Process Bus board will subscribe to the GOOSE.

Caution	***The Station Bus and Process Bus boards should not be connected to the same network to avoid bandwidth and quality of service issues.***

4.9 Current Differential Function

The feeder differential function uses a P543 or P546 at each end of the protected circuit which can be a two ended or three-ended scheme depending on the application. The IEDs send local current information to the remote ends. The decisions whether to trip are made locally after calculating the bias and differential currents based on the received currents.

For the current differential function to work correctly, Sampled Values from each end of the feeder must be synchronized to correspond to the same time instant. This also applies to any other quantities derived from samples such as Fourier values. This is essential to properly evaluate bias and differential currents and if not synchronized could result in false differential currents and unwanted operation of the differential scheme.

In a differential scheme with conventional P543 or P546 IEDs, either:

- time stamps plus current information is exchanged between the IEDs
- all the IEDs in the scheme are synchronized to 1 PPS GPS inputs.

When the IEDs in the scheme have a Process Bus interface, the synchronization must account for delays in receiving Sampled Values over the Process Bus network. This is not important for conventional IEDs where the primary CTs are directly wired to the IED's analogue inputs. The following diagram shows P546 IEDs at both line ends with Process Bus. The Merging Units and the Sampled Value distribution networks at End A and End B are independent of each other. Therefore, the Sampled Values may arrive at the P546 IEDs with different delays.

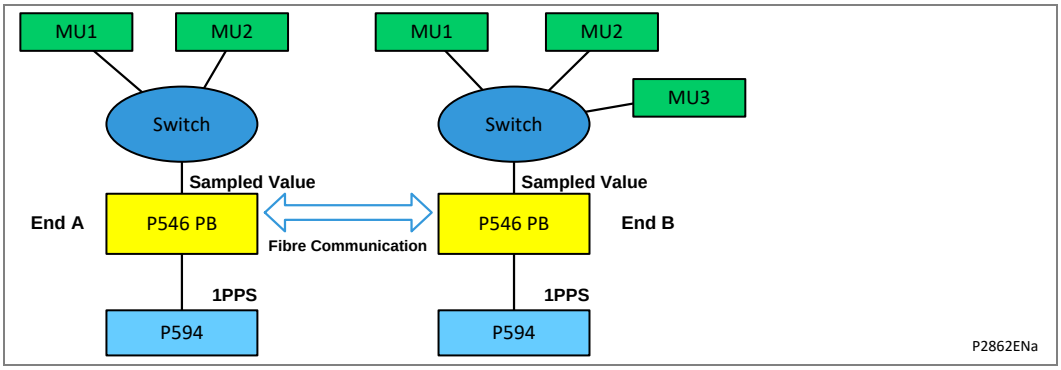


Figure 17 – Two-ended P54x scheme with Process Bus IEDs at both ends

To synchronize the Sampled Values across multiple P546 IEDs with Process Bus interfaces, all must be synchronized using a 1 PPS GPS signal from a P594. This applies for all IEDs in the scheme when one or more of the feeder ends uses Sampled Value inputs.

These conditions are also needed for the feeder differential function to work correctly:

- All P54x IEDs in the scheme must work in GPS Synchronized mode and must have 1PPS GPS inputs from the P594.
- At all line ends, the Merging Units in the feeder differential scheme must use a reference time clock for synchronization. For example, IEEE 1588 or GPS synchronized 1PPS.
- The GPS sources for the P54x IEDs and the Merging Units must be synchronized as they may not be common.
- The first Sampled Value frame from the Merging Units for each second has a sequence count of 0. This corresponds to a zero-time offset from the start of the second.

The P54x uses the sample count in the Sampled Value frames, plus its own 1PPS GPS synchronization input, to calculate delays between 1PPS trigger and the time when coprocessor board has detected the current sample is calculated based on the sample with SmpCnt 0. The P54x then phase shifts the current vectors to time-align them before performing bias and differential currents calculations. The delay is recalculated every second to adapt to any changes in the Process Bus, enhancing the security of the protection scheme.

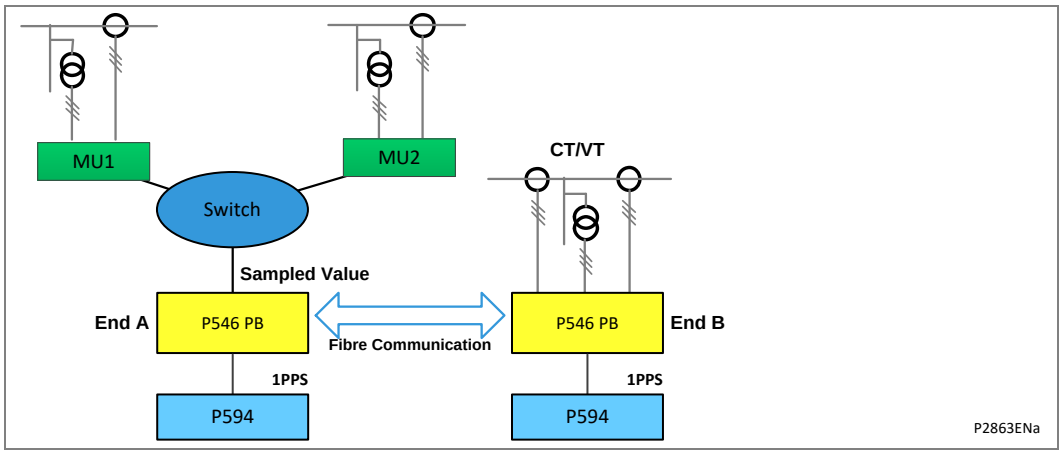


Figure 18 - P54x PB IED scheme and conventional P54x IED combined in a current differential scheme

The current differential scheme is inhibited at all feeder ends if any of the following conditions occur:

- The Sampled Value frames received at the P54x are not synchronized.
- The 1PPS input to the P54x is not GPS synchronized.
- The setting **PB CONFIG->Synchro Mode** is set to ***No_SYNC_CLK***.
- There is a delay of 10 ms or more between the receipt of a Sampled Value frame with SmpCnt 0, and the 1 PPS input pulse to the P54x indicating the start of the second.

When the GPS synchronization recovers in any of these cases, the current differential scheme inhibit is removed on the next occurrence of the ‘SmpCnt 0’ in the Sampled Value frames.

4.10 Configuration Examples

In this section, some configuration and connection examples will be displayed as references.

In the following diagrams, the Merging Units (MU) are illustrated as follows:

- The first line contains the measured currents and voltages
- The second line contains the Merging Unit reference
- The third line illustrates the dataset elements used by the Process Bus board

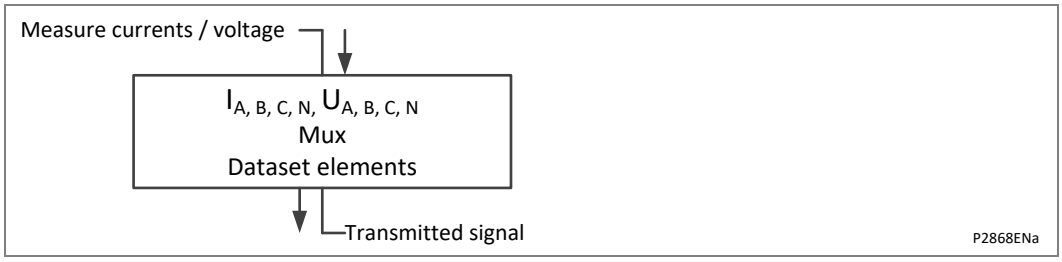


Figure 19 – Measured currents/voltages and transmitted signal

Note the standard inputs and outputs defined by PhsMeas1 have been used in these examples. In IEC61850-9LE this structure is fixed, however, the MU will send whatever signal is applied to the physical input on the corresponding channel. For example, a check synch voltage could be applied to the U_N input and the MU would send this value as U_N in the SV stream. Since the P40 relays allow flexible channel allocation the U_N element can be assigned to the check synch voltage input. This also applies to IEC61869, however, it also supports other PhsMeasx datasets allowing custom datasets to also be used. The flexible channel allocation can then be used to assign any relay input to the appropriate channel.

The examples given here include:

- Example 1 - Line Protection
- Example 2 - Line Protection with Mutual Coupling
- Example 3 - Line protection with Check Synch
- Example 4 - Double Bus Line Protection with Check Synch
- Example 5 - Breaker and a Half with Mutual Coupling and Check Synch

4.10.1 Example 1 - Line Protection

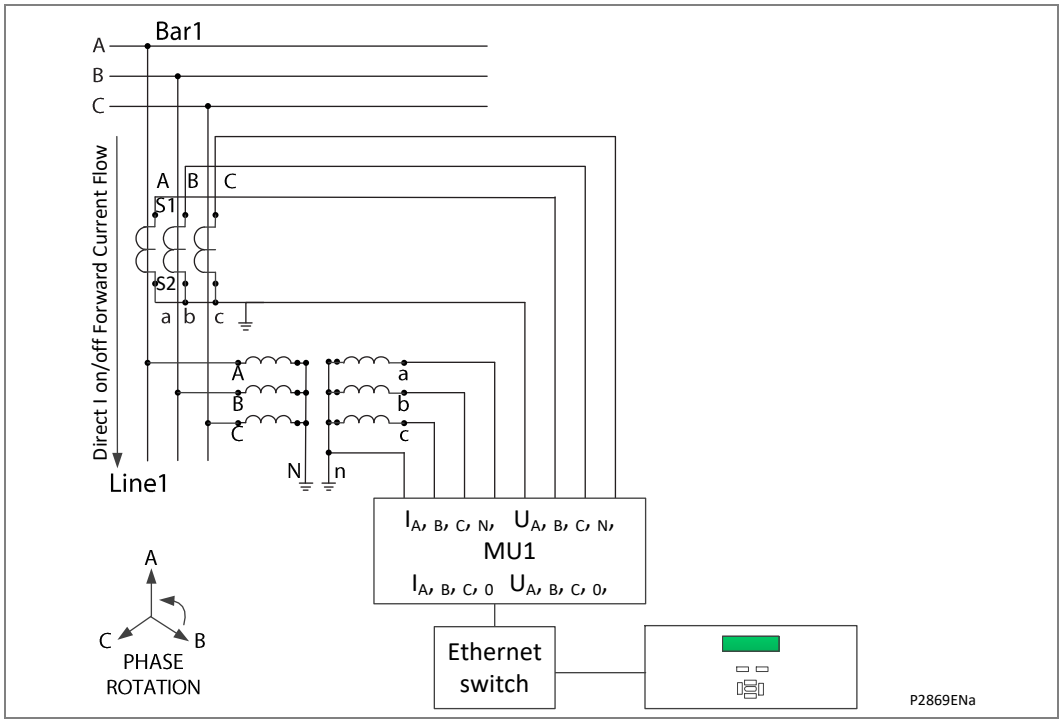


Figure 20 - Connection

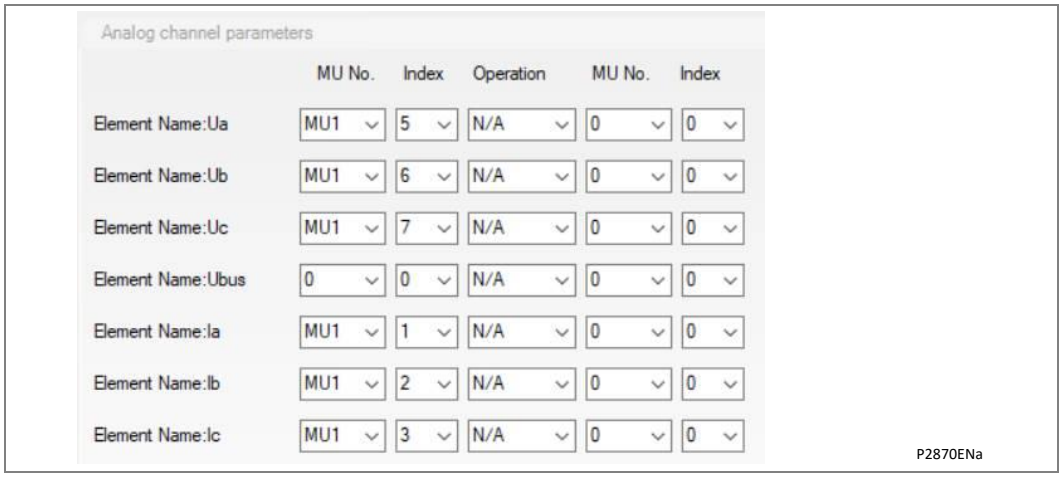


Figure 21 – CID configuration

4.10.2 Example 2 - Line Protection with Mutual Coupling

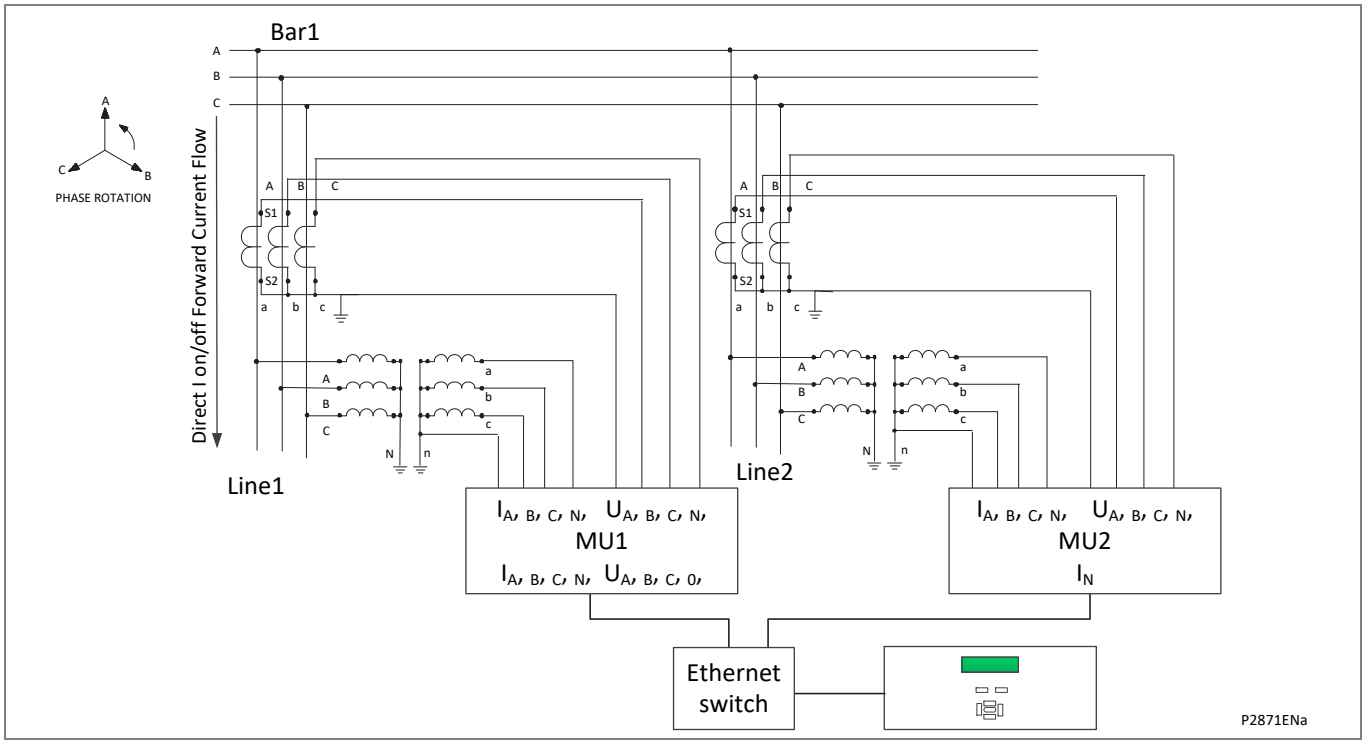


Figure 22 - Connection

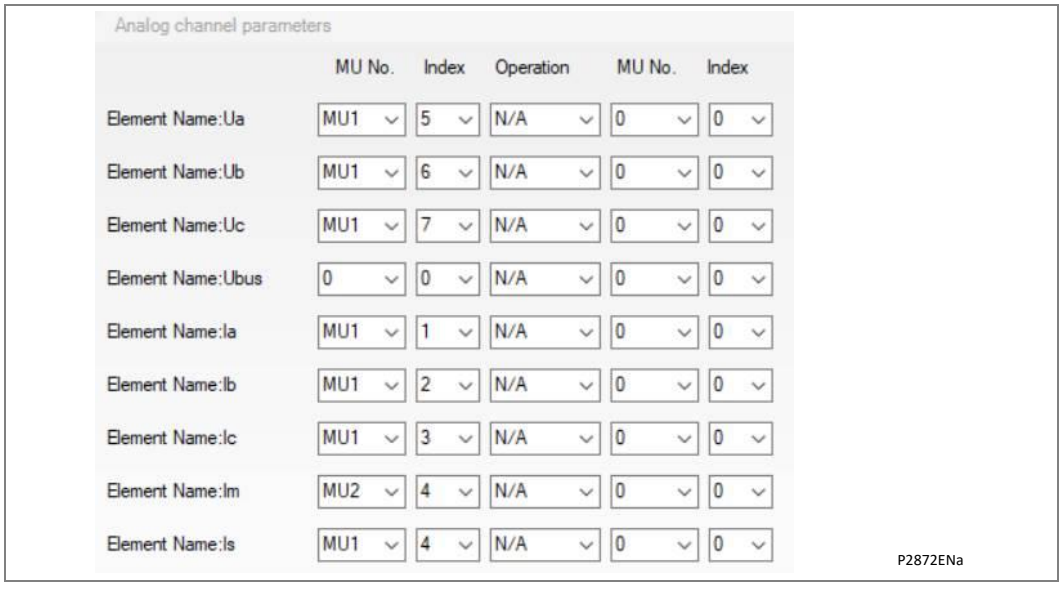


Figure 23 - CID configuration

4.10.3 Example 3 - Line protection with Check Synch

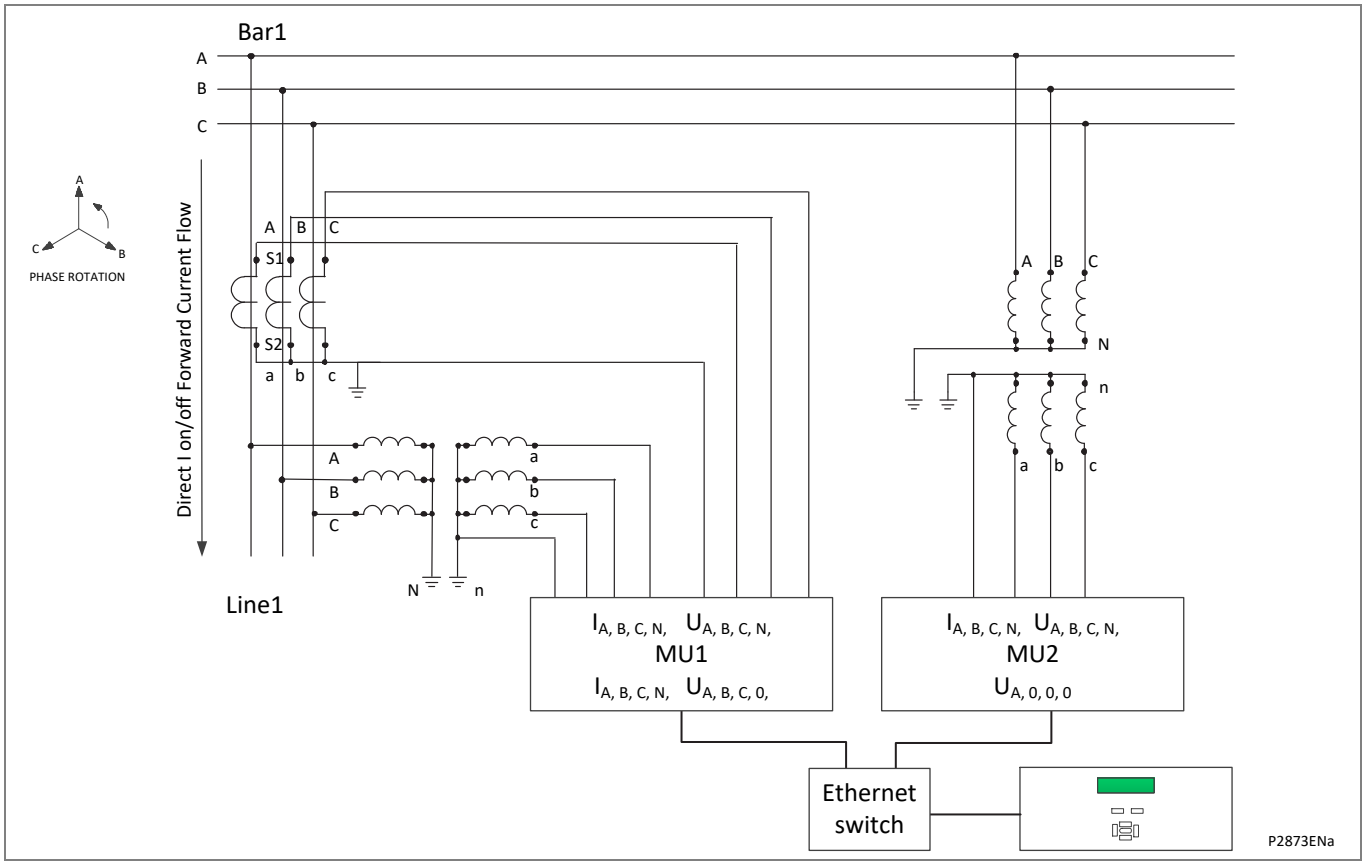


Figure 24 - Connection

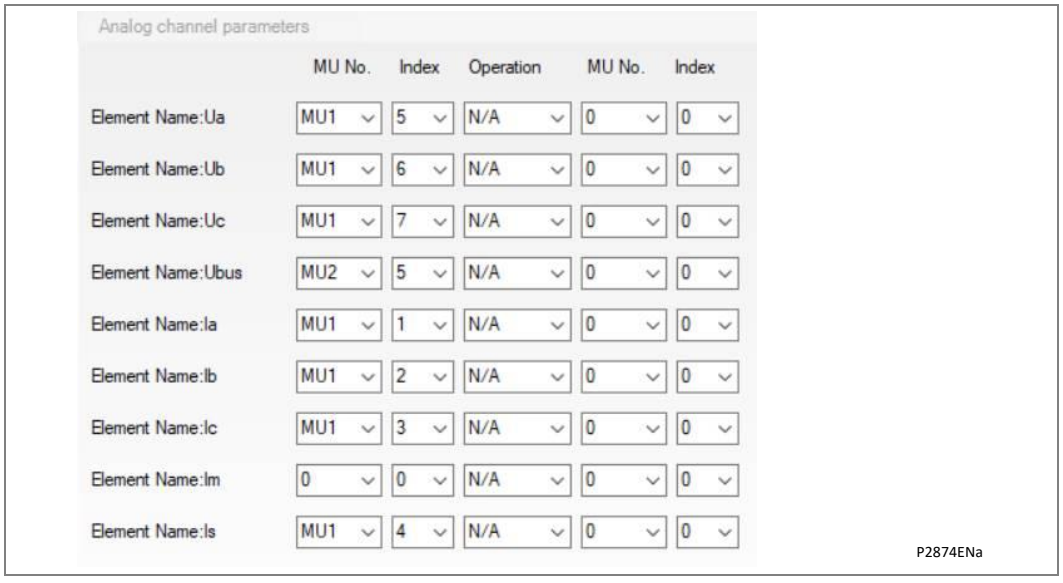


Figure 25 - CID configuration

4.10.4 Example 4 - Double Bus Line Protection with Check Synch

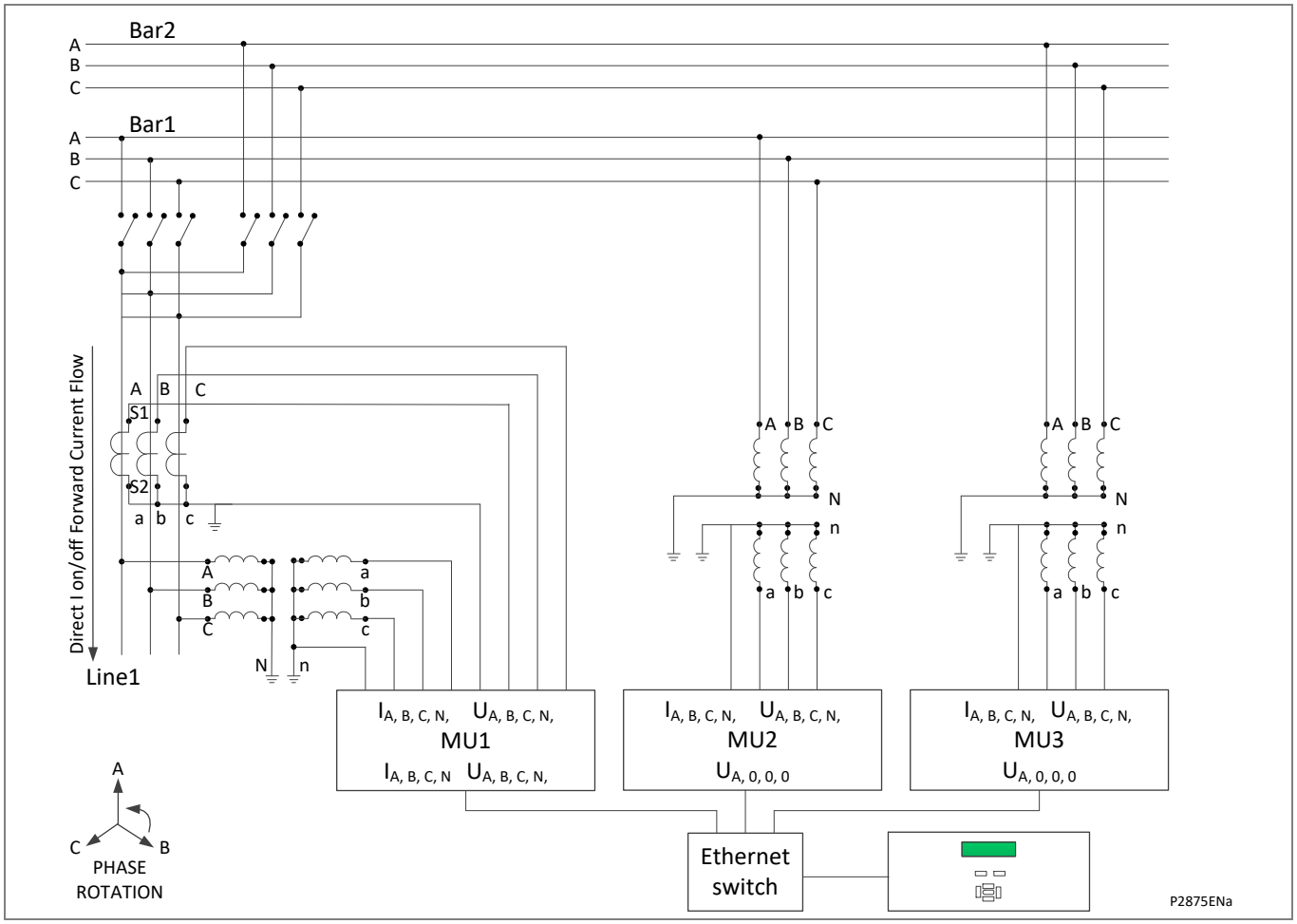


Figure 26 - Connection

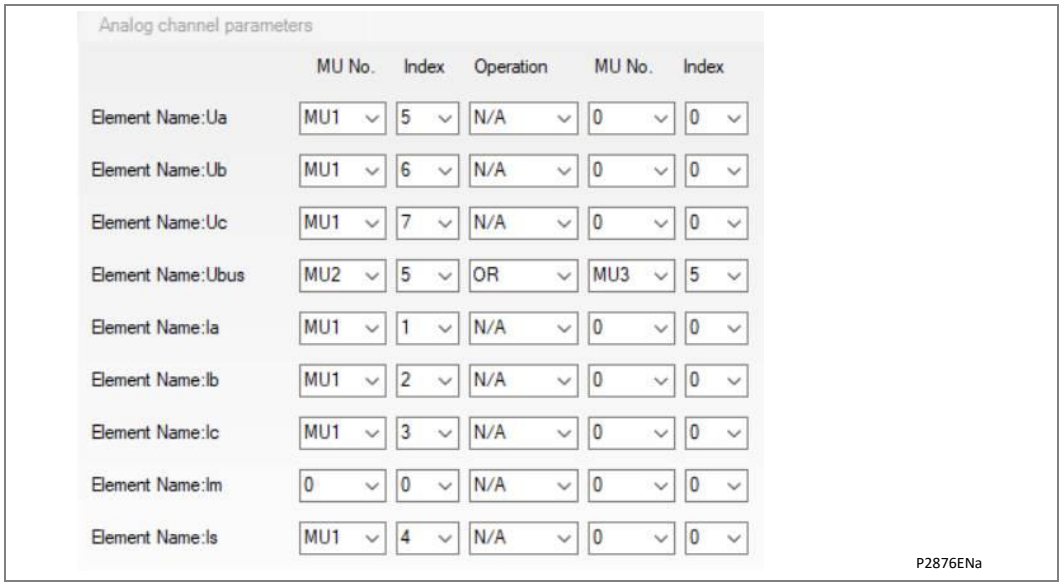


Figure 27 - CID configuration

4.10.5 Example 5 - Breaker and a Half with Mutual Coupling and Check Synch

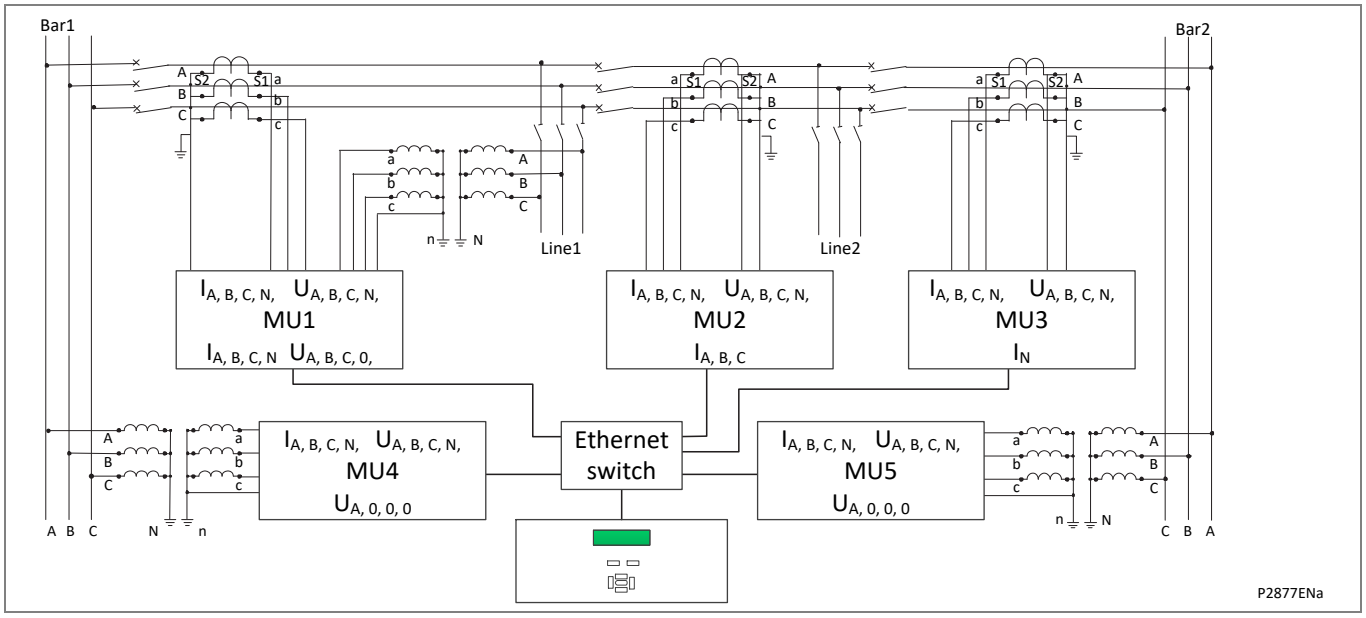


Figure 28 - Connection

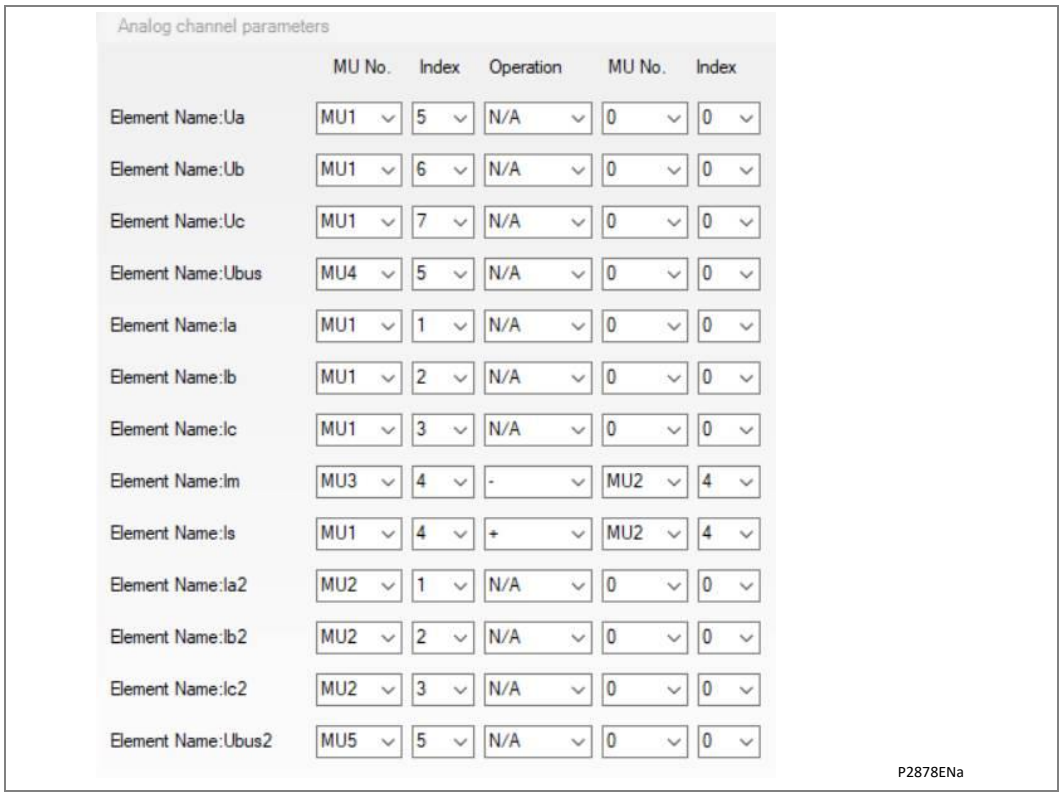


Figure 29 - CID configuration

5 COMMISSIONING

Commissioning methods differ slightly, depending on whether the relay uses the Process Bus Interface or not. The relevant details are shown in the ***Commissioning*** chapter, but are copied here for easy reference.

5.1 Product Checks for IEDs which use the Process Bus Interface

5.1.1 IED Configured with One Merging Unit (MU)

The settings for the Process Bus interface are in the IED menu ***IED Config***. See the Settings chapter.

1. If necessary, isolate or block any outgoing trips from the IED. If physical contacts from the IED are wired in the scheme, in ***COMMISSION TESTS*** menu, set ***Test Mode*** to *Contacts Blocked* if operation of the contacts is not desired. If GOOSE outputs are used, from the main IED menu COMMISIONING TEST column select ***Test Mode***.
2. Connect the IEDs Ethernet port on the Process Bus board to the Sampled Value source. If necessary this can be routed through an Ethernet switch.
3. Make a valid SV configuration (a CID file via **IED Configurator**) and download it to relay and activate the configuration bank.
4. Check that the MU configuration in the CID file matches the actual Sampled Value source (test kit or Merging Unit). Make any changes in the source Sampled Value configuration. This prevents mismatches in Sampled Value when the IED is put into service when testing existing schemes.
5. Set the IED ***Synchro Mode*** to *No SYNC CLK* so the IED accepts Sampled Value frames with or without synchronization.
6. Generate Sampled Value frames with the rated current and voltage as required in the IED's Sampled Value configuration.
7. In the ***MEASUREMENTS*** menu, check the magnitudes and phase angles are displayed correctly. The display may be in primary or secondary values. Also, the IED's CT ratio or VT ratio settings affect the display. A typical accuracy of 1% can be expected for magnitudes.
8. Change the SV configuration configured in the test kit or Merging Unit to mismatch the Sampled Value configuration of the relay. Check the data cell ***SV Absence Alm*** displays '*******1' (where * is a don't care state for this test, normally its value is 0) for the Merging Unit configured in the CID. Check that all ***MEASUREMENTS*** displays for voltage or current are zero.
9. Depending on the scheme, if Merging Unit is configured to publish SV in IEC61869 format, set ***SMV Version*** to *IEC61869*, if Merging Unit is configured to publish SV in IEC61850-9-2LE compatible format, set ***SMV Version*** to *IEC61850-9-2LE*.

5.1.2 IED Configured with Two or More Merging Units (MUs)

The settings for the IEC61850-9-2LE or IEC61869 interface are in the IED menu ***PB CONFIG***.

1. If necessary, isolate or block any outgoing trips from the IED. If physical contacts from the IED are wired in the scheme, in ***COMMISSION TESTS*** menu, set ***Test Mode*** to *Contacts Blocked* if operation of the contacts is not desired. If GOOSE outputs are used, from the main IED menu COMMISIONING TEST column select ***Test Mode***.
2. Connect the IEDs Ethernet port on Process Bus board to an Ethernet switch, which is connected to the Sampled Value sources. If necessary this can be routed through an Ethernet switch.
3. Make a valid SV configuration (a CID file via **IED Configurator**) and download it to relay and activate the configuration bank.
4. Check that the MU configuration in the CID file matches the actual Sampled Value source (test kit or Merging Unit). Make any changes in the source Sampled Value configuration. This prevents mismatches in Sampled Value when the IED is put into service when testing existing schemes.
5. Set the IED Synchro Alarm to 'Local Clock' so the IED accepts Sampled Value frames with local or global synchronization.
6. Check that the Sampled Value source (test kit or Merging Unit) is GPS synchronized.
7. Check the receipt of Sampled Value frames one by one for each Logical Node configured in the IED.

Repeat the following steps for each Merging Unit, configuring them one by one in the Sampled Value source(s).

1. Generate Sampled Value frames with the rated current and voltage as required in the IED's Logical Node configuration. You can check the receipt of Sampled Value frames for the configured Logical Node.
2. In the ***MEASUREMENTS*** menu, check the magnitudes and phase angles are displayed correctly. The display may be in primary or secondary values. Also, the IED's CT ratio or VT ratio settings affect the display. A typical accuracy of 1% can be expected for magnitudes.
3. Change the SV configuration configured in the test kit or Merging Unit to mismatch the Sampled Value configuration of the relay. Check the data cell ***SV Absence Alm*** displays '00000001' (where * is a don't care state for this test, normally its value is 0) for the first Merging Unit configured in the CID, or '******1*' (where * is a don't care state for this test, normally its value is 0) for the second Merging Unit configured in the CID. Check that all ***MEASUREMENTS*** displays for voltage or current are zero.

5.2 GPS Synchronization for IEDs which use the Process Bus Interface

The P54x has a feature whereby the timing information used to align the local and remote current vectors used in the phase differential algorithm can be very accurately synchronized via the Global Positioning Satellite (GPS) system. If specified, a P594 GPS synchronizing unit is employed to decipher GPS signals and provide the P54x relay with a suitable synchronizing signal.

If the P54x is using GPS synchronization to enhance the phase current differential protection, then the associated P594 unit will need to be commissioned in accordance with the relevant commissioning instructions. The P594 commissioning instructions can be found in the Commissioning chapter of the P594 Technical Manual.

If P594 synchronizing units are not employed, go to the *Setting Checks* section.

5.2.1 Commission the P594

The commissioning instructions and record sheets for the P594 GPS synchronization are available in the P594 Technical Manual. The P594 should be commissioned as per the instructions for a P594 being used to synchronize a P54x relay.

For more information refer to:

- 5.3 - Commissioning Mode for P54x Relay with Process Bus and then
- 5.4 - Commissioning Mode

5.3 Commissioning Mode for P54x Relay with Process Bus

The P54x needs a 1PPS GPS input to function correctly. See the IED manual for GPS synchronization tests. Use a P594 with version D firmware to comply with IEC 61850-9-2LE or IEC 61869 requirements for Local Clock and Global Clock.

5.3.1 Strength of P594 Optical Signal at IED for P54x Relay with Process Bus

1. Put the P594 in **Test Cycle Mode**. See the P594 manual.
2. Check the optical fibre cable to the P594 transmitter is connected correctly.
3. Disconnect the other end of the cable from the IED and measure the received signal strength.
4. Record the value. It should be -16.8 dBm to -25.4 dBm.
5. Reconnect the optical fibre to the IED.

5.3.2 Checking GPS Synchronization Signal at IED for P54x Relay with Process Bus

1. In the P594 menu, set Test Cycle Mode to 'Disable'.
2. Connect the transmit fibre from the P594 to the IED's GPS port.
3. At the IED, set ***PROT COMMS/IM64 > GPS Sync*** to *GPS Standard*. This enables GPS synchronization.
4. Select ***MEASUREMENTS 4 > Channel Status***. If the IED receives the GPS synchronization signal, the display reads **********11** (where * is a don't care state for this test). This means both the Local GPS and Remote GPS are received.
5. To check the GPS failure condition, disconnect the fibre from the P594 and check the display reverts to **********00**.
6. Reconnect the fibre and check the display reads **********11**.

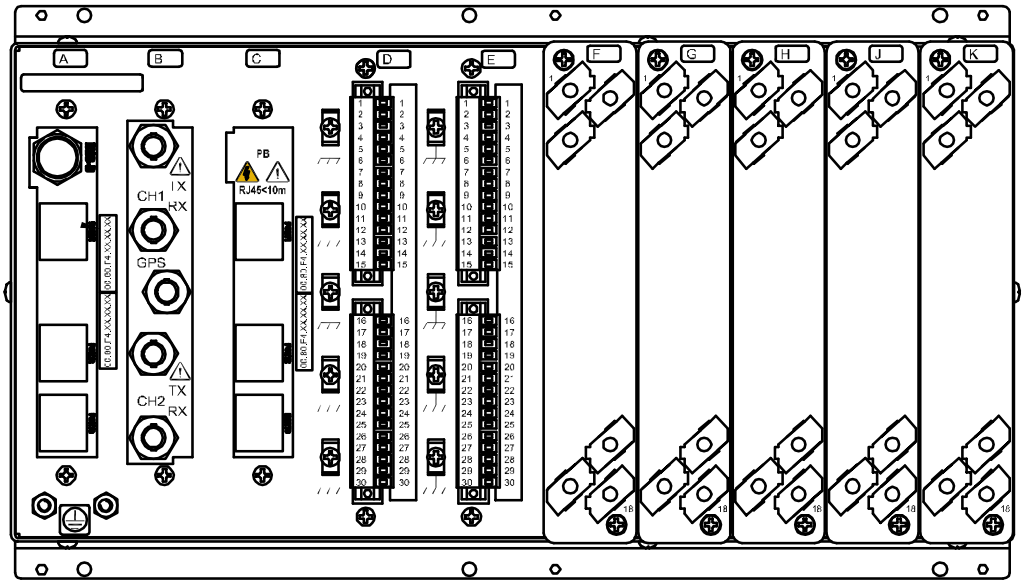
5.4 Commissioning Mode

Global synchronization is needed for a current differential scheme to function correctly. The protection function is inhibited if global synchronization is not present. As IED test kits may not be able to generate Sampled Value frames with global synchronization, the IED has a commissioning mode which allows the differential function to be tested with local synchronization alone.

1. In the ***PB CONFIG*** menu, set ***Synchro Mode*** to *Local Clock*. The current differential protection function then executed for Sampled Value frames received with either Local Clock or Global Clock synchronization. But if Merging Unit is not synchronized with global 1 PPS signal, the differential current will be compared to actual differential current, the value only can be used as a reference due to the phase rotation basis is not established.
2. Test the current differential protection function using a test kit synchronized to GPS, publishing Sampled Value frames with Local Clock synchronization.
3. When the commissioning tests are complete, set the ***Synchro Mode*** to *Global Clock* before the IED is returned to service. The current differential protection operates only with Global 1 PPS synchronization.
4. Check the Merging Unit's maximum delay and if necessary adjust the ***MUs Delay Offset*** setting. If the monitored maximum delay offset is -1, it means the time difference of different SV arrived at device is longer than 3ms, which cannot meet the protection running condition, the whole network needs to be reconfigured to find why there is such a huge transmission delay for some Merging Units.

6 CONNECTION DIAGRAMS

Some of the Connection Diagrams differ slightly, depending on whether the relay uses the Process Bus Interface or not. The relevant details are shown in the ***Connection Diagrams*** chapter, but are copied here for easy reference.



Code	Board		Code	Board
A	Ethernet Board		F	Opto input board *
B	Coprocessor board*		G	Opto input board
C	Process Bus Board		H	Output Relay Board *
D	RTD Board *		J	Output relay board
E	CILO Board*		K	Power Supply board
Where * means that this board is optional. Whether it is present or not depends on the model.				

Figure 30 – MiCOM Px40 process bus – rear view

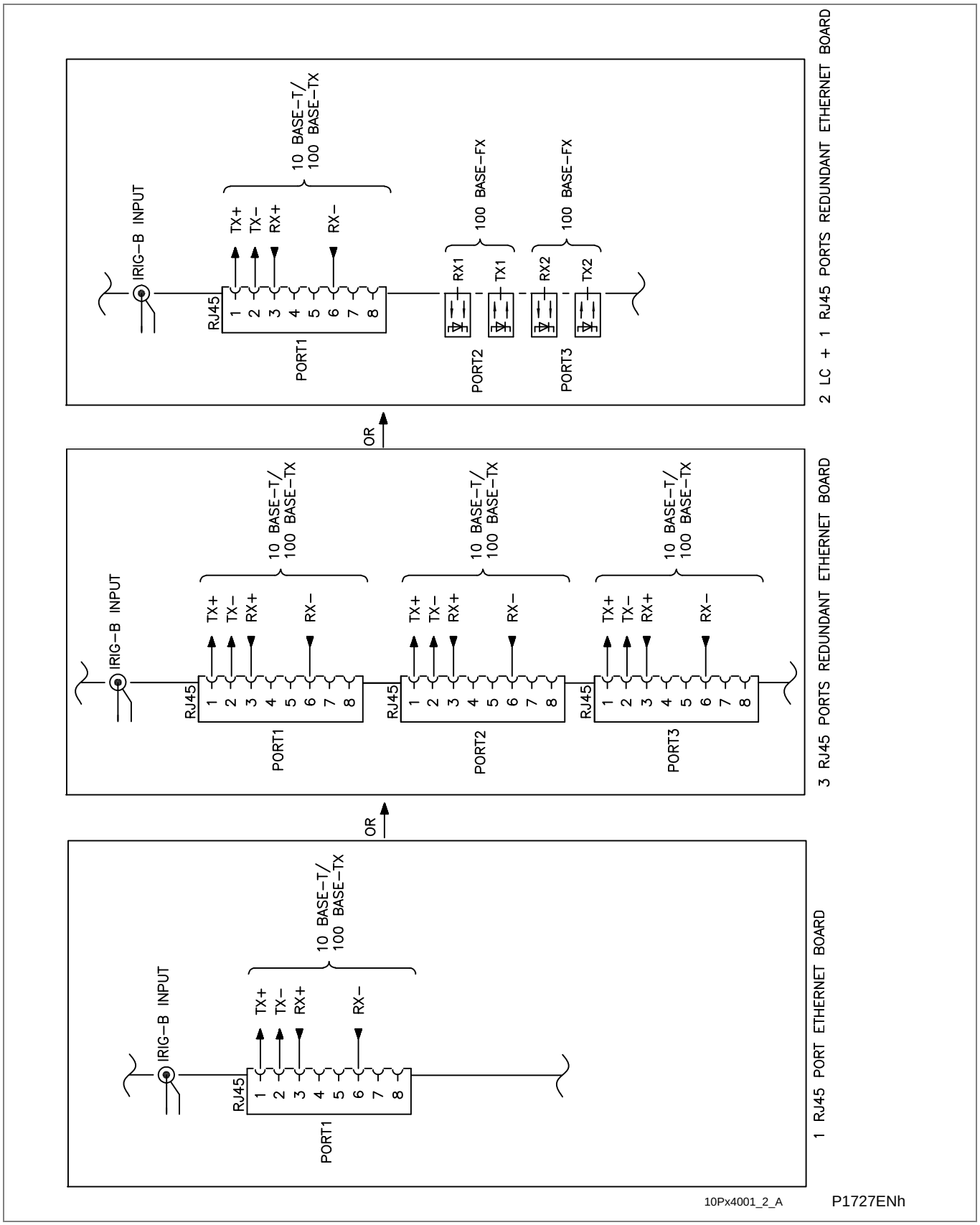


Figure 31 – Front Comm. and process bus comm. options MiCOM Px40 process bus platform

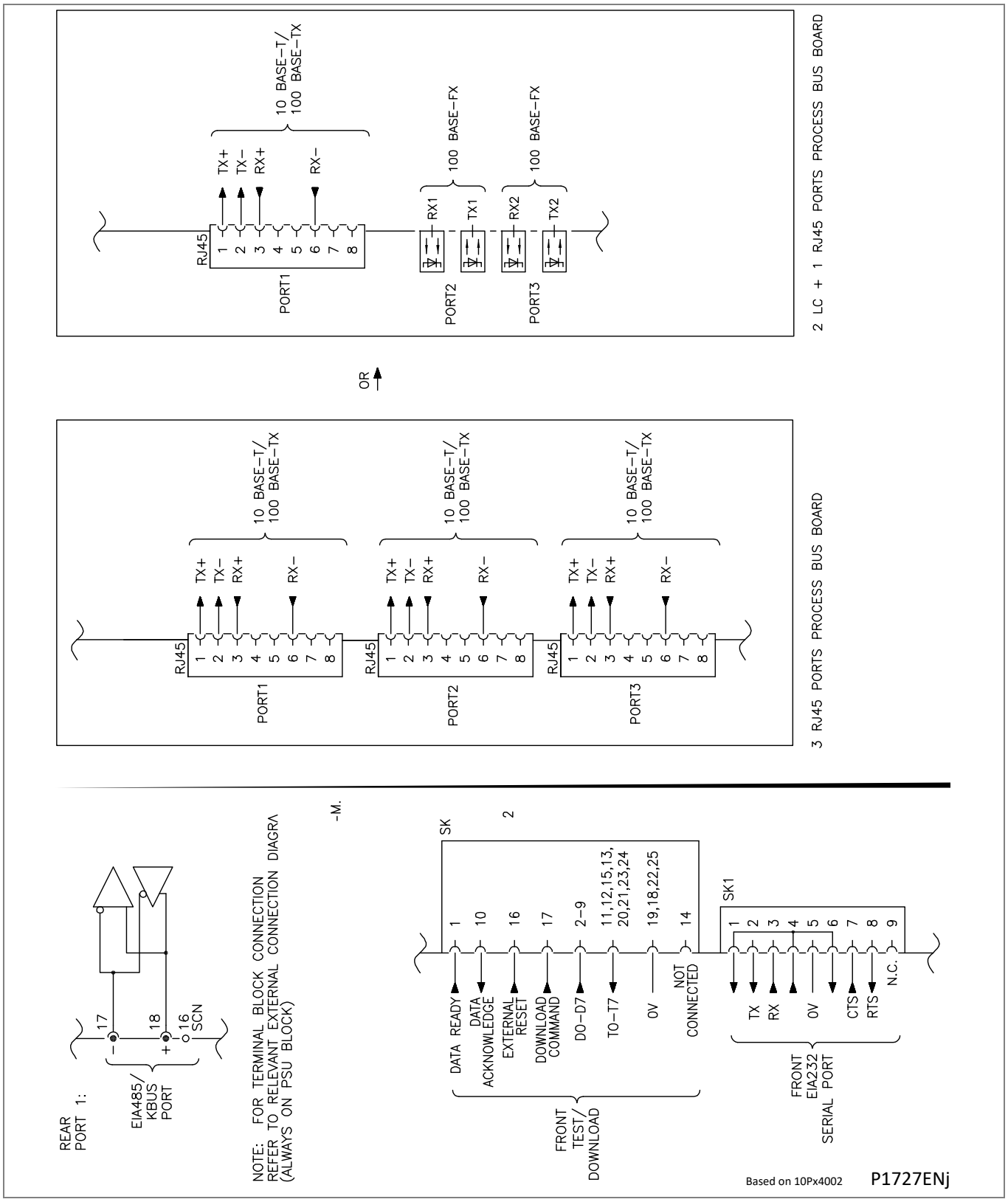


Figure 32 – Ethernet Communications option MiCOM Px40 process bus platform

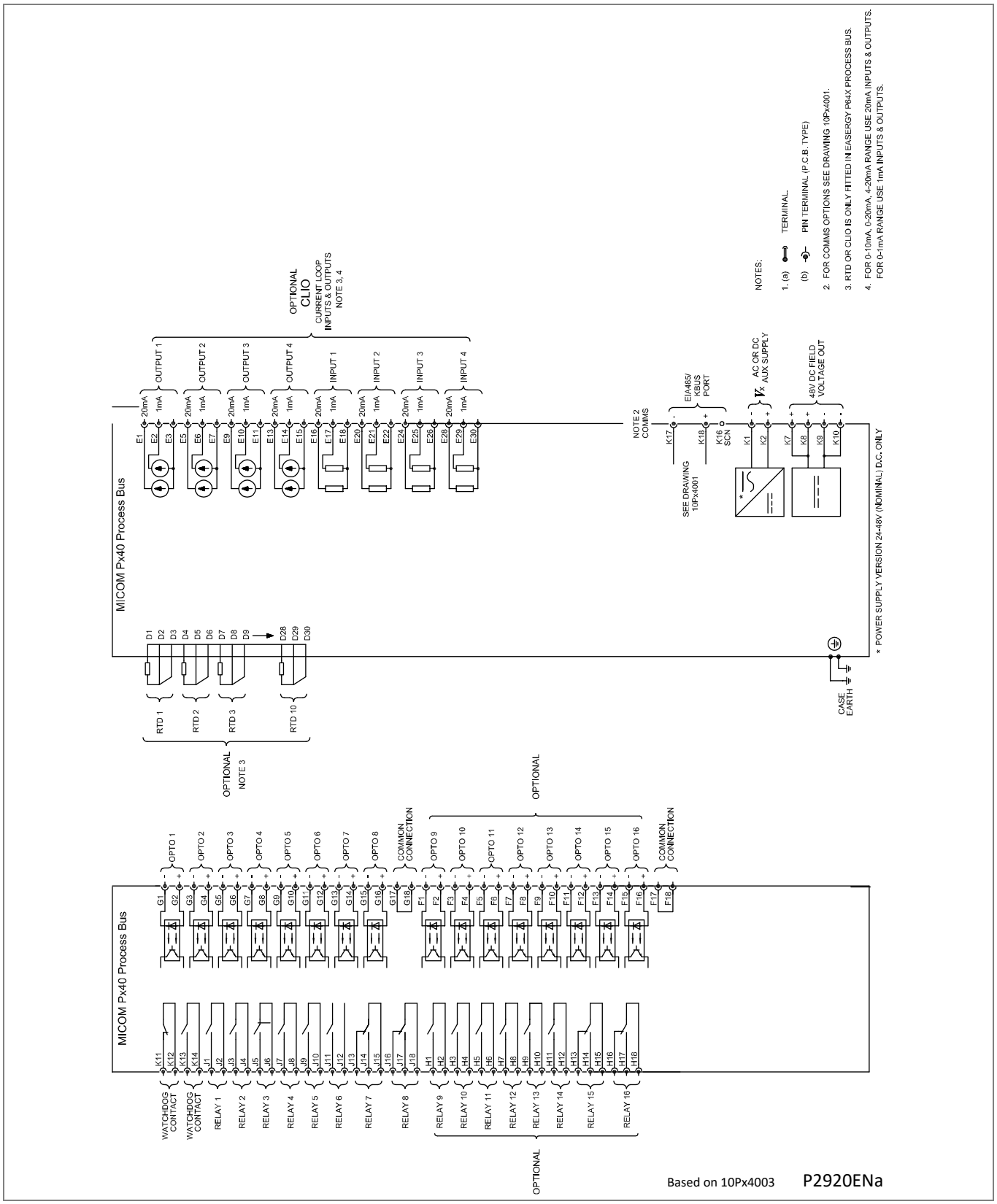


Figure 33 – MiCOM Px40 process bus 8 I/P 8 O/P or 16 O/P (+ CILO & RDT)

7 SAFETY INFORMATION

The Safety Information differs slightly, depending on whether the relay uses the Process Bus Interface or not. The relevant details are shown in the ***Safety Information*** chapter, but are copied here for easy reference.

7.1 Risk of Electric Shock using RJ45 cables

This diagram shows how a P40 IED could be connected to a Stand Alone Merging Unit (SAMU), using either an optical or an RJ45 cable. When connecting devices using RJ45 wired network cables, there is a potential risk of electrical shock.

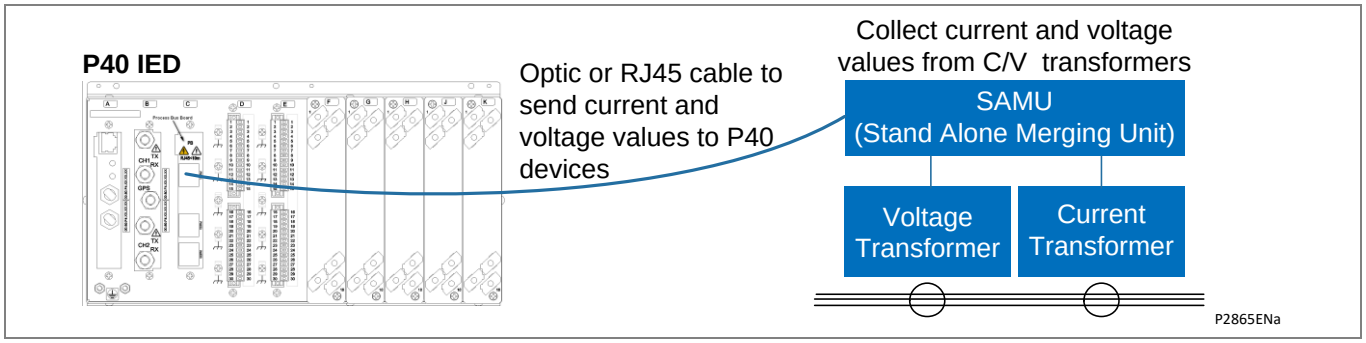


Figure 34 – Connecting a Px40 device to a SAMU

The risk arises due to the widely separated equipment having a different earth potential; and/or faults being propagated on the RJ45 cable. This diagram shows the possible risk:

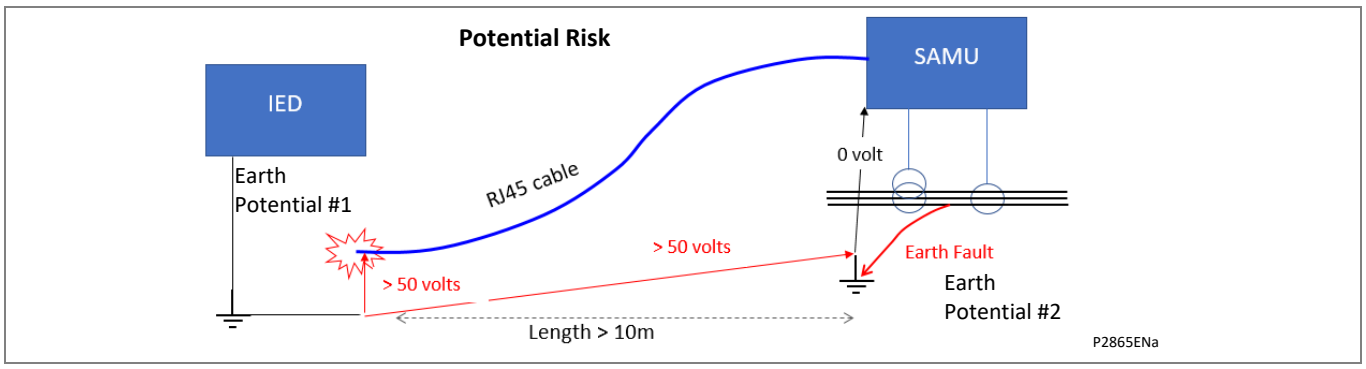


Figure 35 – RJ45 connection electric shock risk

Electric shock could occur if:

- An RJ45 cable is used instead of an optical cable
- The distance from the P40 IED (or a switch) to the SAMU is greater than 10m
- There is an earth potential difference between the two locations
- A fault occurs on SAMU/Voltage Transformer/Current Transformer side
- The earth potential difference and/or the fault is propagated along the RJ45 cable
- Someone comes into electrical contact with the other end of the RJ45 cable (when it is disconnected from P40 device) and they could receive an electric shock

The latest advice for connecting a Low Power Instrument Transformer (LPIT) or a Stand Alone Merging Unit (SAMU) to an IED/switch is, if the distance from the IED/switch is:

- greater than 10m: you must only use a fiber optic cable
- less than 10m: you can use fiber optic or RJ45 cable

When a connection to a LPIT or SAMU is made with the RJ45 cable, this RJ45 cable must not be longer than 10 meters.

The reason is that, during a ground fault, the ground potential of the LPIT or the SAMU rises and is transmitted by the RJ45 cable. If someone was touching the conductive sleeve at the other end of the cable, they could be electrocuted or seriously injured.

DANGER **If you connect items of equipment with different earth potentials with an RJ45 cable, there is a risk of electric shock, explosion or arc flash.**

DANGER **Do not use RJ45 cable longer than 10 meters. Failure to do this may result in death or serious injury.**

VERSION HISTORY

CHAPTER 24

Date:	09/2018
Products covered by this chapter:	This chapter covers the specific versions of the MiCOM products listed below. This includes ***only*** the following combinations of Software Version and Hardware Suffix.
Hardware Suffix:	L (P642) M (P643/P645)
Software Version:	B4 - P64x (P642, P643 & P645)
Connection Diagrams:	10P642xx (xx = 01 to 10) 10P643xx (xx = 01 to 06) 10P645xx (xx = 01 to 09)

CONTENTS

TABLES

Notes:

1 VERSION HISTORY

This table shows the Software Version together with the Hardware Suffix the particular software runs on. The changes introduced by each Software Version are shown with each change on one row.

The Easergy Studio software is updated periodically. These updates provide support for new features (such as allowing you to manage new MiCOM products, as well as using new software releases and hardware suffixes). The updates may also include fixes. **Accordingly, we strongly advise customers to use the latest Schneider Electric version of Easergy Studio.** This table shows the earliest version of the software which lets you use that feature. Unless otherwise stated in the Studio software, the latest version lets you to use all the features of previous versions.
If you need more information regarding bug fixes, please contact your **Schneider Electric** local support.

Software version		Hardware suffix	Original date of issue	Description of changes	Introduced in MiCOM S1 version	Technical document-ation
Major	**Minor**					
01	B	K	Oct. 2008	Original Issue for P643.	V2.14 V3.0	P64x/EN M/A11
01	D	J/K	Feb. 2009	Original Issue for P642/P645. The REF algorithm was enhanced, so that it can be applied in 1.5 breakers arrangements. The scaling factor used by the REF element is the right one. In the P643, the item “TV” is invisible from the options of the cell “Monit’d winding” when “Winding Config” is set to “HV+LV”. The REF fault record is independent from the Diff fault record. If the Diff is disabled, but the REF is enabled; the REF fault record is available. Is-CTS setting is invisible when CTS is disabled or in indication mode. The settings I>Inhibit and I2>Inhibit in the VTS function are in pu. PSL positional data extraction facility has been included.	V2.14 V3.0	P64x/EN AD/A21
02	B	J/K	April 2009	The differential and bias currents of the low impedance REF and differential functions are included in the disturbance recorder. The frequency measurement is included in the disturbance recorder. DNP3.0 over Ethernet. IEC-61850 Phases 2.0 and 2.1 are included. High-break contacts are included depending on the cortec option. An option to disable the VTS logic is included. Enhancement of the VTS logic.	V2.14 V3.0	P64x/EN M/A32

Software version		Hardware suffix	Original date of issue	Description of changes	Introduced in MiCOM S1 version	Technical document-ation
Major	**Minor**					
02	C	J/K	October 2009	Through fault monitoring function has been amended. The I2t calculation only starts when the current is above TF I> Trigger level and no differential element (87 or 64) has started. Date and time settings have been amended. The settings associated to UTC or SNTP have been included. In the default settings the circuitry fault alarm has been disabled since it is only intended for busbar protection. The cross blocking function has been enabled. A 100 ms dwell timer has been added to the fault record trigger input in the PSL to avoid triggering the trip led without generating a fault record when testing the relay. The dependency between the settings in simple and advanced mode has been improved. The relay recalls the settings (reactance, Is-HS1, Zero seq. Filt HV, Zero seq. Filt LV, Zero seq. Filt TV, HV Grounding, LV Grounding, and TV Grounding) when changing from simple to advanced mode and vice-versa. The setting cell 2nd harm blocked has been included. It can be set as either enabled or disabled. This is required in busbar applications where the second harmonic blocking is not needed. If the setting cell TOL status is disabled, Hot Spot T and Top Oil T measurements are not displayed. The setting cells Ambient T and Top Oil T can only be set to RTD or CLIO when the hardware is available. The thermal overload function has been improved. The DDB signal TFR De-energized and a corrected top oil time constant have been included. The CT para mismatch logic has been modified. If the amplitude matching factor of the TV winding is out of range and less than 0.05, the TV winding CT inputs are not considered in the differential calculation (under this condition the CT para mismatch alarm is not asserted and the differential is not automatically blocked).	V2.14 V3.1.1	P64x/EN M/A32
02	D	J/K	March 2010	It was reported that for P642 model, when 02C software with IEC61850 protocol was downloaded, an alarm was issued, indicating that NIC software miss-matched the main board software. This issue has been solved in 02D firmware. The latched states of relays or LEDs reflect the current properties of the individual relays and LEDs. The relays and LEDs are updated whenever their properties are changed, i.e. reset when their properties are not latch. IEC61850, the DDBs values that had not changed since startup are also reported. Integrity Period of X seconds results in Integrity reports being generated every X+1 seconds, hence an extra second is being added to the configured Integrity Period. IEC61850, the appropriate amendments were performed so that when the Integrity Period is set to “x” seconds the Integrity report is generated every “x” seconds and not “x+1” seconds. NIC no response alarm assertion has been amended. DNP3, the relay failure to respond to a class 1/2/3 poll following a confirmation to another relay has been corrected.	V2.14 V3.1.1	P64x/EN M/A32

Software version		Hardware suffix	Original date of issue	Description of changes	Introduced in MiCOM S1 version	Technical document-ation
Major	**Minor**					
02	E	J/K	October 2010	The appropriate amendments have been done to avoid displaying 1/25 of the injected power in 'MEASUREMENTS 2' column. DNP3.0 over Ethernet, appropriate amendments have been done so that when polling an offline analogue signal, the flag “Offline, Local forced” is displayed. Appropriate amendments have been done so that the menu text for setting "% Reactance” is displayed correctly in MiCOM Studio. The DNP3.0 over Ethernet application stack size has been enlarged to avoid asserting the error code 0X662005F8. IEC61850, the buffer has been enlarged to avoid loss of communication under heavy BRCB (buffer report circuit breaker). **Note** 02E firmware is only available for the P643.	V2.14 V3.1.1	P64x/EN M/A32
02	U	J/K	Feb 2011	Firmware rebranded from Areva to Schneider Electric.	V2.14 V3.1.1	P64x/EN M/A32
02	V	J/K		Support Dual Redundant Ethernet Board. Resolve the CT Ratio mismatch problem at LV and TV windings.	V2.14 V3.1.1	
02	W	J/K			V2.14 V3.1.1	
03	A	J/K	Not available (May 2011)	Cybersecurity Phase 1 has been included, for Software 03 only (i.e. not 01, 02 or 04). This is described only in the Cyber Security chapter. REB (Redundant Ethernet Board) has been included. **Note** Improvements in 02E for P643 were included in 03A for all P64x models.	V2.14 V3.1.1	P64x/EN M/A32
03	A	J/K	January 2011	Service Manual rebranded from Areva to Schneider Electric.	V2.14 V3.1.1	P64x/EN M/A42
03	U	J/K		Rebranded 03A		
03	V	J/K	May 2013	Parallel Redundancy Protocol (PRP) support: The IEC62439-3 (2012) PRP states “Each Double attached node implementing PRP (DANP) stall multicast a PRP_Supervision frame over both its ports”. Bug Fixes.	V2.14 V3.1.1	P64x/EN M/A62

Software version		Hardware suffix	Original date of issue	Description of changes	Introduced in MiCOM S1 version	Technical document-ation
Major	**Minor**					
04	U	J/K	May 2011	Software 04 does not include cyber security. CT saturation and no gap detection algorithms have been included algorithm to improve the differential element operating time. External fault detection algorithm has been included to prevent the CT saturation and no gap detection from blocking the 2nd harmonic element during external faults. CT input exclusion. If a CT input is excluded, then it is not considered by any of the current based functions. The CBF logic has been modified so that it resets in less than a cycle. Also the settings are per current transformer input. A setting for the neutral current has also been included. User alarms have been included and improved. 32 user alarms are available and they can be set in the setting files as self reset or latch. The label for each user alarm can be set in the setting file (no need to use the text editor). This label is also displayed in the PSL. Two voltage controlled overcurrent stages are available. All the current based functions are now settable; they are no longer fixed as HV, LV and TV. For example, there are three overcurrent elements (four stages each one). Any of the overcurrent elements can be set to protect a particular winding or a feeder. Assigned inputs extension, the selection of CT inputs for each winding has been increased. Now all the possible combinations are considered. For example, in a P645 four CT inputs can be assigned to the HV side and one to the LV side. High impedance REF has been included. Low impedance REF for autotransformer has been included.	V2.14 V3.1.1	P64x/EN M/A52
04	U	J/K	May 2011	Software 04 does not include cyber security. Negative sequence overvoltage has been implemented. The thermal overload function has been enhanced; four cooling modes have been included. The two first stages of the negative phase sequence overcurrent element can be set as IDMT. An additional VT input can be ordered in the P642. As a result voltage functions and directional functions are available to some extent. The first two stages of the negative phase sequence overcurrent element can be set as IDMT. REB (Redundant Ethernet Board) is available. An additional VT input can be ordered in the P642. As a result negative phase sequence overvoltage function and directional functions are available to some extent. **Note** Improvements in 02E for P643 were included in 04U for all P64x models.	V2.14 V3.1.1	P64x/EN M/A52
04	V	J/K	December 2011	Updated the Px4x software platform which has improved the GOOSE performance. Bug Fixes.	V2.14 V3.4.1	P64x/EN M/A52
04	W	J/K	June 2012	The GOOSE performance improvements that implemented in the old Platform will be modified to provide a better solution. The modification will be included in a new platform. Bug Fixes.	V2.14 V3.4.1	P64x/EN M/B52
04	X	J/K	May 2013	Parallel Redundancy Protocol (PRP) support: The IEC62439-3 (2012) PRP states “Each Double attached node implementing PRP (DANP) stall multicast a PRP_Supervision frame over both its ports”. Bug Fixes.	V2.14 V3.5.2	P64x/EN M/A62

Software version		Hardware suffix	Original date of issue	Description of changes	Introduced in MiCOM S1 version	Technical document-ation
Major	**Minor**					
A0	A	J/K	February 2014	Extend CT primary setting to be increased to 60kA. Added a new setting cell for this request to remove TV side from the differential protection calculation for P643/P645 only. Add MatchFac REF HV/LV/TV setting cell in the system config. Bug Fixes.	V2.14 V3.5.2	P64x/EN M/A62
A0	B	J/K	September 2015	Enhance the IEC61850 protocol and bug fixing.	V2.14 V3.5.2	P64x/EN M/B63
A1	A	L/M	September 2014	Add IEC61850 plus DNP3 serial protocol options Upgrade to CPU3/XCPU3 For LowZ RED, the reference CT changes from Neutral CT to Phase CT. The scope of REF Match Factor K is changed from 0.05<=K<=20 to 0.05<=K<=15.	V2.14 V3.5.2	P64x/EN M/A62
A1	B	L/M	February 2016	Special customized release, enhance the IEC61850 protocol and bug fixes.	V2.14 V3.5.2	P64x/EN M/B63
A2	A	L/M	August 2016	Add a new setting cell Transient Bias to make transient bias is settable, enhance the IEC61850 protocol and bug fixing.	V5.0.1	P64x/EN M/B63
B0	A	L/M	February 2014	Update design suffix to CPU3/XCPU3, Cyber Security Phase 1, IEC 61850 Ed.2, Goose performance and number improvement, HSR/PRP Redundancy, Dual communication with 2 IPs	V5.0.1	P64x/EN M/B63
B1	A	L/M	October 2014	**Hardware:** Update hardware design suffix to L/M. The 24-48 Vdc power supply range has been changed to cover 24-32 Vdc only. Three new Ethernet boards released. **Software:** IEC 61850 Ed.2 and Ed.1 by configuration. GOOSE number and GOOSE performance enhancement. Disturbance Record LN RDRE Enhancement. Time Synchronization via LTIM/LTMS. Monitor DDB for port physical link status. High-availability Seamless Redundancy (HSR). Dual Ethernet communications (Dual IP). Cyber Security. **Notes:** DNP Over Ethernet is not included in this release Bug Fixes.	V5.0.1	P64x/EN M/B63
B1	B	L/M	March 2015	Cyber Security Phase 1 (password based) without RBAC. Bug Fixes.	V5.0.1	P64x/EN M/B63
B2	A	L/M	September 2016	IEC61850 ed1/2 + DNP3.0 Over Ethernet, RBAC Cyber Security 3, Secured Communication (Replace RPC tunneling), Fault Record via DNP3.0 and IEC61850, Virtual I/O Naming, Two New DDB: Logic 0 and IRIG-B Valid. Bug Fixes.	V7.0.0 or later	P64x/EN M/C73

Software version		Hardware suffix	Original date of issue	Description of changes	Introduced in MiCOM S1 version	Technical document-ation
Major	**Minor**					
B3	A	L/M	October 2017	DNP3OE unsolicited messages feature. The setting value consistency (Primary /Secondary) in all ports can be configurable now. Additional setting cells included to allow the transient bias to be configured for differential and REF Low Z protection. Voltage Restrained Over Current Protection in addition to the existing Voltage Controlled Over Current. When CB FAIL IN<Input is set to derived, DDB_CTx_IN_UNDERCURRENT element works by IN derived. For internal fault, CB Fail is initiated by DDB_INT_CBF_INIT_Tx. Bug Fixes.	V8.0.0 or later	P64x/EN M/D83
B4	A	L/M	September 2018	PTP and RSTP has been added. SNMP has been removed. Pre-configured dataset High Performance GOOSE is removed.	V8.1.0 or later	P64x/EN M/E93
B4	B	L/M	November 2018	Process Bus is supported.	V8.1.0 or later	P64x/EN M/E93

This table shows the Software Version together with the Hardware Suffix the particular software runs on. The changes introduced by each Software Version are shown with each change on one row.

The Easergy Studio software is updated periodically. These updates provide support for new features (such as allowing you to manage new MiCOM products, as well as using new software releases and hardware suffixes). The updates may also include fixes. **Accordingly, we strongly advise customers to use the latest Schneider Electric version of Easergy Studio.** This table shows the earliest version of the software which lets you use that feature. Unless otherwise stated in the Studio software, the latest version lets you to use all the features of previous versions.
If you need more information regarding bug fixes, please contact your **Schneider Electric** local support.

Table 1 - Version history

2 SETTING FILE AND RELAY SOFTWARE

Setting File Software Version	Relay Software Version											
	01	02	03	04	A0	A1	A2	B0	B1	B2	B3	B4
01	✓	×	×	×	×	×	×	×	×	×	×	×
02	×	✓	×	×	×	×	×	×	×	×	×	×
03	×	×	✓	×	×		×	×	×	×	×	×
04	×	×	×	✓	×	×	×	×	×	×	×	×
A0	×	×	×	×	✓	×	×	×	×	×	×	×
A1	×	×	×	×	×	✓	×	×	×	×	×	×
A2	×	×	×	×	×	×	✓	×	×	×	×	×
B0	×	×	×	×	×	×	×	✓	×	×	×	×
B1	×	×	×	×	×	×	×	×	✓	×	×	×
B2	×	×	×	×	×	×	×	×	×	✓	×	×
B3	×	×	×	×	×	×	×	×	×	×	✓	×
B4	×	×	×	×	×	×	×	×	×	×	×	✓

Table 2 - Setting file and relay software

3 PSL FILE AND RELAY SOFTWARE

PSL File Software Version	Relay Software Version											
	01	02	03	04	A0	A1	A2	B0	B1	B2	B3	B4
01	✓	×	×	×	×	×	×	×	×	×	×	×
02	×	✓	×	×	×	×	×	×	×	×	×	×
03	×	×	✓	×	×		×	×	×	×	×	×
04	×	×	×	✓	×	×	×	×	×	×	×	×
A0	×	×	×	×	✓	×	×	×	×	×	×	×
A1	×	×	×	×	×	✓	×	×	×	×	×	×
A2	×	×	×	×	×	×	✓	×	×	×	×	×
B0	×	×	×	×	×	×	×	✓	×	×	×	×
B1	×	×	×	×	×	×	×	×	✓	×	×	×
B2	×	×	×	×	×	×	×	×	×	✓	×	×
B3	×	×	×	×	×	×	×	×	×	×	✓	×
B4	×	×	×	×	×	×	×	×	×	×	×	✓

Table 3 - PSL file and relay software

4 MENU TEXT FILE AND RELAY SOFTWARE

Menu Text File Software Version	Relay Software Version											
	01	02	03	04	A0	A1	A2	B0	B1	B2	B3	B4
01	✓	×	×	×	×	×	×	×	×	×	×	×
02	×	✓	×	×	×	×	×	×	×	×	×	×
03	×	×	✓	×	×		×	×	×	×	×	×
04	×	×	×	✓	×	×	×	×	×	×	×	×
A0	×	×	×	×	✓	×	×	×	×	×	×	×
A1	×	×	×	×	×	✓	×	×	×	×	×	×
A2	×	×	×	×	×	×	✓	×	×	×	×	×
B0	×	×	×	×	×	×	×	✓	×	×	×	×
B1	×	×	×	×	×	×	×	×	✓	×	×	×
B2	×	×	×	×	×	×	×	×	×	✓	×	×
B3	×	×	×	×	×	×	×	×	×	×	✓	×
B4	×	×	×	×	×	×	×	×	×	×	×	✓

Table 4 - Menu text file and relay software

Notes:

SYMBOLS AND GLOSSARY

CHAPTER SG

Date	02/2018	
Products covered by this chapter:	This chapter covers the specific versions of the MiCOM products listed below. This includes ***only*** the following combinations of Software Version and Hardware Suffix.	
Hardware Suffix	All MiCOM Px4x products	
Software Version	All MiCOM Px4x products	
Connection Diagrams:	P14x (P141, P142, P143 & P145): 10P141xx (xx = 01 to 02) 10P142xx (xx = 01 to 05) 10P143xx (xx = 01 to 11) 10P145xx (xx = 01 to 11) P24x (P241, P242 & P243): 10P241xx (xx = 01 to 02) 10P242xx (xx = 01) 10P243xx (xx = 01) P34x (P342, P343, P344, P345 & P391): 10P342xx (xx = 01 to 17) 10P343xx (xx = 01 to 19) 10P344xx (xx = 01 to 12) 10P345xx (xx = 01 to 07) 10P391xx (xx = 01 to 02) P445: 10P445xx (xx = 01 to 04) P44x (P442 & P444): 10P44201 (SH 1 & 2) 10P44202 (SH 1) 10P44203 (SH 1 & 2) 10P44401 (SH 1) 10P44402 (SH 1) 10P44403 (SH 1 & 2) 10P44404 (SH 1) 10P44405 (SH 1) 10P44407 (SH 1 & 2) P44y (P443 & P446): 10P44303 (SH 01 and 03) 10P44304 (SH 01 and 03) 10P44305 (SH 01 and 03) 10P44306 (SH 01 and 03) 10P44600 10P44601 (SH 1 to 2) 10P44602 (SH 1 to 2) 10P44603 (SH 1 to 2)	P54x (P543, P544, P545 & P546): 10P54302 (SH 1 to 2) 10P54303 (SH 1 to 2) 10P54400 10P54404 (SH 1 to 2) 10P54405 (SH 1 to 2) 10P54502 (SH 1 to 2) 10P54503 (SH 1 to 2) 10P54600 10P54604 (SH 1 to 2) 10P54605 (SH 1 to 2) 10P54606 (SH 1 to 2) P547: 10P54702xx (xx = 01 to 02) 10P54703xx (xx = 01 to 02) 10P54704xx (xx = 01 to 02) 10P54705xx (xx = 01 to 02) P64x (P642, P643 & P645): 10P642xx (xx = 01 to 10) 10P643xx (xx = 01 to 06) 10P645xx (xx = 01 to 09) P74x (P741, P742 & P743): 10P740xx (xx = 01 to 07) P746: 10P746xx (xx = 00 to 21) P841: 10P84100 10P84101 (SH 1 to 2) 10P84102 (SH 1 to 2) 10P84103 (SH 1 to 2) 10P84104 (SH 1 to 2) 10P84105 (SH 1 to 2) P849: 10P849xx (xx = 01 to 06)

CONTENTS

TABLES

FIGURES

Notes:

1 ACRONYMS AND ABBREVIATIONS

Term	Description
<	Less than: Used to indicate an “under” threshold, such as undercurrent (current dropout).
>	Greater than: Used to indicate an “over” threshold, such as overcurrent (current overload)
A	Ampere
AA	Application Association
AC / ac	Alternating Current
ACSI	Abstract Communication Service Interface
ACSR	Aluminum Conductor Steel Reinforced
ALF	Accuracy Limit Factor
AM	Amplitude Modulation
ANSI	American National Standards Institute
AR	Auto-Reclose
ARIP	Auto-Reclose In Progress
ASCII	American Standard Code for Information Interchange
ATEX	ATEX is the Potentially Explosive Atmospheres directive 94/9/EC
AUX / Aux	Auxiliary
AV	Anti virus
AWG	American Wire Gauge
BAR	Block Auto-Reclose signal
BCD	Binary Coded Decimal
BCR	Binary Counter Reading
BDEW	Bundesverband der Energie- und Wasserwirtschaft | Startseite (i.e. German Association of Energy and Water Industries)
BMP	BitMaP – a file format for a computer graphic
BN>	Neutral over susceptance in the context of the protection element: Reactive component of admittance calculation from neutral current and residual voltage.
BOP	Blocking Overreach Protection - a blocking aided-channel scheme.
BPDU	Bridge Protocol Data Unit
BRCB	Buffered Report Control Block
BRP	Beacon Redundancy Protocol
BU	Backup: Typically a back-up in the context of the protection element
Business Service Layer	This layer coordinates the application, processes commands, make logical decision and calculation according to the business rules
CA	Certification Authority
CAT	Computer Administration Tool , for replacing CMT
C/O	A ChangeOver contact having normally-closed and normally-open connections: Often called a “form C” contact.
CB	Circuit Breaker
CB Aux.	Circuit Breaker auxiliary contacts: Indication of the breaker open/closed status.
CBF	Circuit Breaker Failure in the context of protection element. Could be labelled 50BF in ANSI terminology.
CDC	Common Data Class
CET	Sepam Configuration tool
CF	Control Function
Ch	Channel: usually a communications or signaling channel
Check Synch	Check Synchronizing function

Term	Description
CID	Configured IED Description
CIFS	Common Internet File System. Microsoft protocol use to share resources on a network.
CIP	Critical Infrastructure Protection
CIP Standards	Critical Infrastructure Protection standards. NERC CIP standards have been given the force of law by the Federal Energy Regulatory Commission (FERC)
CLIO	Current Loop Input Output: 0-1 mA/0-10 mA/0-20 mA/4-20 mA transducer inputs and outputs CLI = current loop input - 0-1 mA/0-10 mA/0-20 mA/4-20 mA transducer input CLO = current loop output - 0-1 mA/0-10 mA/0-20 mA/4-20 mA transducer output
CLK / Clk	Clock
Cls	Close - generally used in the context of close functions in circuit breaker control.
CMC	Certificates Management over CMS. An IETF RFC for distribution and registration of public keys and certificates
CMP	Certificates Management Protocol. An IETF RFC for distribution and registration of public keys and certificates (RFC 4210)
CMV	Complex Measured Value
CNV	Current No Volts
COMFEDE	Common Format for Event Data Exchange
CPNI	Centre for the Protection of National Infrastructure
CRC	Cyclic Redundancy Check
CRL	Certificates Revocation List. A list of revoked certificates. Theoretically still valid, but forbidden by the Security Administrator or the Security Server
CRP	Cross-network Redundancy Protocol
CRV	Curve (file format for curve information)
CRx	Channel Receive: Typically used to indicate a teleprotection signal received.
Crypto Device	A small device embedding cryptographic capabilities and storage memory. It could be a smartcard, USB stick, serial dongle, etc.
CS	Cyber Security or Check Synchronism.
CSMS	Cyber Security Management System
CSV	Comma Separated Values (a file format for database information)
CT	Current Transformer
CTRL	Control - as used for the Control Inputs function
CTS	Current Transformer Supervision: To detect CT input failure.
CTx	Channel Transmit: Typically used to indicate a teleprotection signal send.
CUL	Canadian Underwriters Laboratory
CVT	Capacitor-coupled Voltage Transformer - equivalent to terminology CCVT.
CZ	Abbreviation of “Check Zone”: Zone taking into account only the feeders.
DA	Data Attribute
DAN	Double or Doubly Attached Node
DANH	Double or Doubly Attached Node with HSR protocol
DANP	Double or Doubly Attached Node implementing PRP
Data Layer	Consists of the domain-related objects and their relationships that are manipulated by the user during the interaction with the software
DAU	Data Acquisition Unit
DC	Data Concentrator
DC / dc	Direct Current

Term	Description
DCC	An Omicron compatible format
DCE	Data Communication Equipment
DCS	Distributed Control System
DDB	Digital Data Bus within the programmable scheme logic: A logic point that has a zero or 1 status. DDB signals are mapped in logic to customize the relay's operation.
DDR	Dynamic Disturbance Recorder
DEF	Directional Earth Fault (protection): A directionalized ground fault aided protection scheme. Could be labeled 67N in ANSI terminology.
df/dt	Rate of Change of Frequency (equivalent to ROCOF). Could be labeled 81R in ANSI terminology.
df/dt>1	First stage of df/dt in the context of protection element
DFT	Discrete Fourier Transform
DG	Distributed Generation
DHCP	Dynamic Host Configuration Protocol
DHM	Dual Homing Manager
DHP	Dual Homing Protocol
DHS	Dual Homing Star. Ethernet protocol allowing bumpless redundancy. Used with Redundant Ethernet board with dual homing protocol
Diff	Differential in the context of protection elements . Could be labeled 87 in ANSI terminology.
DIN	Deutsches Institut für Normung (German standards body)
Dist	Distance in the context of protection elements . Could be labeled 21 in ANSI terminology.
DITA	Darwinian Information Typing Architecture
DLDB	Dead-Line Dead-Bus: In system synchronism check, indication that both the line and bus are de-energized.
DLLB	Dead-Line Live-Bus: In system synchronism check, indication that the line is de-energised whilst the bus is energized.
DLR	Dynamic Line Rating
DLY / Dly	Time Delay
DMT	Definite Minimum Time
DNP	Distributed Network Protocol
DO	Data Object
DPWS	Device Profile for Web Services
DR	Disturbance Record
DREB	Dual Redundant Ethernet Board
DSP	Digital Signal Processor
DST	Daylight Saving Time
DT	Definite Time: in the context of protection elements: An element which always responds with the same constant time delay on operation. Or Abbreviation of "Dead Time" in the context of auto-reclose:
DTD	Document Type Definition
DTOC	Definite Time Overcurrent in the context of protection element
DTS	Date and Time Stamp
DVC	Direct Variable Cost
DZ	Dead Zone. Area between a CT and an open breaker or an open isolator.
EF or E/F	Earth Fault (directly equivalent to Ground Fault)
EIA	Electronic Industries Alliance
ELR	Environmental Lapse Rate

Term	Description
EMC	ElectroMagnetic Compatibility
ENA	Energy Networks Association
ER	Engineering Recommendation
ESD	ElectroStatic Discharge
ESP	Electronic Security Perimeter
ESS	Embedded Security Server
ETS	Element To Secure. An ETS is an entity that represents a tool, utility or application function block that can be protected within the tool suite. It gathers a list of corresponding permissions with their set of values. This list is pre-defined and cannot be edited by any business user. A same ETS can be associated to many roles with different set of authorizations.
FAA	Ageing Acceleration Factor: Used by Loss of Life (LOL) element
FCS	Frame Check Sequence
FFail	A field failure (loss of excitation) element: Could be labeled 40 in ANSI terminology.
FFT	Fast Fourier Transform
FIR	Finite Impulse Response
FLC	Full load current: The nominal rated current for the circuit.
FLT / Flt	Fault - typically used to indicate faulted phase selection.
Fn or FN	Function
FPGA	Field Programmable Gate Array
FPS	Frames Per Second
FTP	File Transfer Protocol or Foil Twisted Pair
FTPS	FTP over TLS protocol. The classic file transfer protocol (FTP) secured using TLS tunneling.
FWD, Fwd or Fwd.	Indicates an element responding to a flow in the “Forward” direction
Gen Diff	A generator differential element: Could be labeled 87G in ANSI terminology.
Gen-Xformer Diff	A generator-transformer differential element: Could be labeled 87GT in ANSI terminology.
GI	General Interrogation
GIF	Graphic Interchange Format – a file format for a computer graphic
GN>	Neutral over conductance in the context of protection element: Real component of admittance calculation from neutral current and residual voltage.
GND / Gnd	Ground: used in distance settings to identify settings that relate to ground (earth) faults.
GoCB	GOOSE Control Block
GOOSE	Generic Object Oriented Substation Event
GPS	Global Positioning System
GRP / Grp	Group. Typically an alternative setting group.
GSE	General Substation Event
GSSE	Generic Substation Status Event
GUESS	Generator Unintentional Energization at StandStill.
GUI	Graphical User Interface
HIPS	Host Intrusion Prevention System based on “white list” of accepted executables.
HMI	Human Machine Interface
HSR	High Availability Seamless Redundancy
HTML	Hypertext Markup Language
I	Current

Term	Description
I/O	Input/Output
I/P	Input
IANA	Internet Assigned Numbers Authority
ICAO	International Civil Aviation Organization
ICD	IED Capability Description
ID	Identifier or Identification. Often a label used to track a software version installed.
IDMT	Inverse Definite Minimum Time. A characteristic whose trip time depends on the measured input (e.g. current) according to an inverse-time curve.
IEC	International Electro-technical Commission
IED	Intelligent Electronic Device - a term used to describe microprocessor-based controllers of power system equipment. Common types of IEDs include protective relaying devices, load tap changer controllers, circuit breaker controllers, capacitor bank switches, recloser controllers, voltage regulators, etc.
IEEE	Institute of Electrical and Electronics Engineers
IET	IED Engineering ToolSuite. Similar to SET but dedicated to IED. Or IED Engineering Tool.
IETF	Internet Engineering Task Force
IID	Instantiated/Individual IED Description
IIR	Infinite Impulse Response
Inh	An Inhibit signal
Inst	An element with Instantaneous operation: i.e. having no deliberate time delay.
IP	Internet Protocol
IRIG	InterRange Instrumentation Group
ISA	International Standard Atmosphere or Instrumentation Systems and Automation Society
ISO	International Standards Organization
JPEG	Joint Photographic Experts Group – a file format for a computer graphic
L	Live
LAN	Local Area Network
LCB	Log Control Block
LCD	Liquid Crystal Display: The relay front-panel text display.
LD	Level Detector: An element responding to a current or voltage below its set threshold. Or Logical Device
LDAP	Lightweight Directory Access Protocol
LDOV	Level Detector for OverVoltage
LDUV	Level Detector for UnderVoltage
LED	Light Emitting Diode
LLDB	Live-Line Dead-Bus : In system synchronism check, indication that the line is energized whilst the bus is de-energized.
Ln	Natural logarithm
LN	Logical Node
LOGS	All the operations related to the security (connection, configuration…) are automatically caught in events that are logged in order to provide a good visibility of the previous actions to the security administrators.
LoL	A Loss of Load scheme, providing a fast distance trip without needing a signaling channel.
LPDU	Link Protocol Data Unit
LPHD	Logical Physical Device
LRE	Link Redundancy Entity

Term	Description
MAC	Media Access Control or Mandatory Access Control
MC	MultiCast
MCB	Miniature Circuit Breaker
MIB	Management Information Base
MICS	Model Implementation Conformance Statement
MMF	Magneto-Motive Force
MMS	Manufacturing Message Specification (IEC 61850)
MRP	Media Redundancy Protocol
MU	Merging Unit (function)
MV	Measured Value
N	Neutral
N/A	Not Applicable
N/C	A Normally Closed or “break” contact: Often called a “form B” contact.
N/O	A Normally Open or “make” contact: Often called a “form A” contact.
NERC	North American Reliability Corporation
NERO	NERC Electric Reliability Organization (ERO) certified by the Federal Energy Regulatory Commission to establish and enforce reliability standards for the bulk-power system.
NIC	Network Interface Card: i.e. the Ethernet card of the IED
NIST	National Institute of Standards and Technology
NPS	Negative Phase Sequence
NTP	The Network Time Protocol (NTP) is a protocol for synchronizing the clocks of computer systems.
NVD	Neutral Voltage Displacement: Equivalent to residual overvoltage protection.
NXT	Abbreviation of “Next”: In connection with hotkey menu navigation.
o	A small circle on the input or output of a logic gate: Indicates a NOT (invert) function.
OC	Ordinary clock: A clock that has a single Precision Time Protocol (PTP) port in a domain and maintains the timescale used in the domain. It may serve as a source of time, i.e., be a master clock, or may synchronize to another clock, i.e., be a slave clock.
O/C	Overcurrent
O/P	Output
OCB	Oil Circuit Breaker
OCSP	Online Certificate Status Protocol. An IETF RFC for online verification of certificates by servers (RFC 2560).
OID	Object IDentifier
OOS	Out-Of-Step
Opto	An Optically coupled logic input. Alternative terminology: binary input.
OSI	Open Systems Interconnection
PAP	Policy Administration Point. Software entity that manage the security Policy
PCB	Printed Circuit Board
PCT	Protective Conductor Terminal (Ground)
PDC	Phasor Data Concentrator
PDP	Policy Decision Point. Software entity that evaluates the applicable policy and takes an authorization decision
PEP	Policy Enforcement Point. Software entity that performs access control and enforces authorization decision.
Ph	Phase - used in distance settings to identify settings that relate to phase-phase faults.

Term	Description
PICS	Protocol Implementation Conformance Statement
PIP	Policy Information Point. Software entity acting as an information source for the PDP.
PKI	Public Key infrastructure
PMU	Phasor Measurement Unit
PNG	Portable Network Graphics – a file format for a computer graphic
Pol	Polarize - typically the polarizing voltage used in making directional decisions.
POR	A Permissive OverReaching transfer trip scheme (alternative terminology: POTT).
POTT	A Permissive Overreaching Transfer Trip scheme (alternative terminology: POR).
PRP	Parallel Redundancy Protocol
PSB	Power Swing Blocking, to detect power swing/out of step functions, could be labeled 78 in ANSI terminology.
PSL	Programmable Scheme Logic: The part of the relay's logic configuration that can be modified by the user, using the graphical editor within MiCOM S1 Studio software.
PSlip	A Pole slip (out-of-step - OOS) element: could be labeled 78 in ANSI terminology.
PSP	Physical Security Perimeter
PSTN	Public Switched Telephone Network (RTC in French)
PT	Power Transformer
PTP	Precision Time Protocol
PUR	A Permissive UnderReaching transfer trip scheme (alternative terminology: PUTT).
PURR	A Permissive Underreaching Transfer Trip scheme (alternative terminology: PUR).
Q	Quantity defined as per unit value
Qx	Isolator number x
R	Resistance
RA	Registration Authority
R&TTE	Radio and Telecommunications Terminal Equipment
RBAC	Role Based Access Control. Authentication and authorization mechanism based on roles granted to a user. Roles are made of rights, themselves being actions that can be applied on objects. Each user's action is authorized or not based on his roles
RBN	Lead burden for the neutral path.
RBPh	Lead burden for the phasepath.
RCA	Relay Characteristic Angle - The center of the directional characteristic.
RCB	Report Control Block
RCT	Redundancy Control Trailer or Redundancy Check Tag
REB	Redundant Ethernet Board
RedBox	Redundancy Box
REF	Restricted Earth Fault
Rev.	Indicates an element responding to a flow in the "reverse" direction
RMS / rms	Root mean square. The equivalent a.c. current: Taking into account the fundamental, plus the equivalent heating effect of any harmonics.
RoCoF	Rate of Change of Frequency
RP	Rear Port: The communication ports on the rear of the IED
RS232	A common serial communications standard defined by the EIA
RS485	A common serial communications standard defined by the EIA (multi-drop)
RST or Rst	Reset generally used in the context of reset functions in circuit breaker control.
RSTP	Rapid Spanning Tree Protocol.

Term	Description
RTCS	Real Time Certificate Status. Facility. An IETF draft for online certificates validation.
RTD	Resistance Temperature Device
RTU	Remote Terminal Unit
RX	Receive: Typically used to indicate a communication transmit line/pin.
SAM	Security Administration Module. Device in charge of security management on an IP-over-Ethernet network.
SAMU	Stand Alone Merging Unit (device)
SAN	Singly or Single Attached Node
SAS	Substation Automation Solutions / System
SAT	Security Administration Tool TSF based application used to define and create security configuration
SAU	Security Administration Utility
SBS	Straight Binary Second
SC	Synch-Check or system Synchronism Check.
SCADA	Supervisory Control and Data Acquisition
SCD	Substation Configuration Description
SCEP	Simple Certificate Enrollment Protocol. An IETF draft for distribution and registration of public keys and certificates
SCL	Substation Configuration Language. In IEC 61850, the definition of the configuration files.
SCSM	Specific Communication Service Mappings: In IEC 61850, the SCSMs define the actual information exchange mechanisms currently used (e.g. MMS).
SCU	Substation Control Unit
SCVP	Server-based Certificate Validation Protocol. An IETF RFC for online certificates validation.
SDEF	Sensitive Differential Earth Fault in the context of protection element. Could be labeled 87N in ANSI terminology.
SEF	Sensitive Earth Fault in the context of protection element
Sen	Sensitive
SET	System Engineering Tools. New Tools in place of SCE and SMT, to deal with complete life cycle for Systems (design, realization, testing, commissioning, maintenance).
SFTP	A Secured File Transfer Protocol based on SSH.
SGCB	Setting Group Control Block
SHM	Self-Healing Manager
SHP	Self Healing Protocol
SHR	Self Healing Ring: Ethernet protocol allowing bumpless redundancy. Used with Redundant Ethernet board with self-healing protocol.
SIR	Source Impedance Ratio
SLA	Service Level Agreement
SMB	Server Message Block. Microsoft protocol for network resources sharing. Called CIFS on NT
SMT	Substation Management Tool (previously used on PACIS project)
SMTP	Simple Mail Transfer Protocol (SMTP) is an Internet standard for electronic mail (e-mail) transmission across Internet Protocol (IP) networks.
SMV	Sampled Measured Values
SNMP	Simple Network Management Protocol (SNMP) is an "Internet-standard protocol for managing devices on IP networks
SNTP	Simple Network Time Protocol
SOA	Service Oriented Architecture
SOAP	Simple Object Access Protocol
SOC	Second of Century

Term	Description
SOTF	Switch on to Fault
SP	Single pole.
SPAR	Single pole auto-reclose.
SPC	Single Point Controllable
SPDT	Single Pole Dead Time. The dead time used in single pole auto-reclose cycles.
SPS	Single Point Status
SQRT	Square Root
SSD	Solid State Device
SSH	Secured Shell. A secured encrypted network protocol for remote administration of computers
SSL	Secured Socket Layer or Source Impedance Ratio or See TLS (TLS is based on SSLv3).
SSO	Single Sign On
STP	Shielded Twisted Pair or Spanning Tree Protocol
SUI	Substation User Interface
SV	Sampled Values
SVC	Static Var Compensator
SVM	Sampled Value Model
TAF	Turbine Abnormal Frequency
TAT	Transfer Administration Tool
TBD	To Be Defined
TC	Transparent Clock: A device that measures the time taken for a Precision Time Protocol (PTP) event message to transit the device and provides this information to clocks receiving this PTP event message. See also: end-to-end transparent clock; peer-to-peer transparent clock.
TCP	Transmission Control Protocol
TCS	Trip Circuit Supervision
TD	Time Dial. The time dial multiplier setting: Applied to inverse-time curves (ANSI/IEEE).
TE	Unit for case measurements: One inch = 5TE units
THD	Total Harmonic Distortion
TICS	Technical Issues Conformance Statement
TIFF	Tagged Image File Format – a file format for a computer graphic
TLS	Transport Layer Security network protocol successor to SSL. Or Transport Layer Security. Creates encrypted tunnel for TCP connections. Can guarantee authentication when used in a PKI.
TMS	Time Multiplier Setting: Applied to inverse-time curves (IEC)
TOC	Trip On Close (“line check”) (protection). Offers SOTF and TOR functionality.
TOR	Trip On Reclose (protection). Modified protection on autoreclosure of the circuit breaker.
TP	Two-Part
TSF	Tool Suite Foundation. Common framework for SET and IET. Mainly 3 parts Core, Workbench (for standardized HMI), Utilities (applicative components like trace viewer, installer)
TUC	Timed UnderCurrent
TVE	Total Vector Error
Tx	Transmit
UA	User Account. A user account is a logical representation of a person with some configurable parameters. It includes information about the user identity and gives him a login to be recognized within the tool suite. A user account is principally interesting when it is associated to some roles that will grant him authorizations.

Term	Description
UDP	User Datagram Protocol
UL	Underwriters Laboratory
UPCT	User Programmable Curve Tool
UTC	Universal Time Coordinated
V	Voltage
VA	Phase A voltage: Sometimes L1, or red phase
VB	Phase B voltage: Sometimes L2, or yellow phase
VC	Phase C voltage: Sometimes L3, or blue phase
VCO	Voltage Controlled Overcurrent element
VDAN	Virtual Double or Doubly Attached Node
VDEP OC>	A voltage dependent overcurrent element: could be a voltage controlled or voltage restrained overcurrent element and could be labeled 51V in ANSI terminology.
VDR	Voltage Dependent Resistor
VDS	Virtual Device Solution
V/Hz	An overfluxing element, flux is proportional to voltage/frequency: could be labeled 24 in ANSI terminology.
Vk	IEC knee point voltage of a current transformer.
VPN	Virtual Private Network (a secure private connection established on a public network or other unsecured environment).
VT	Voltage Transformer
VTS	Voltage Transformer Supervision: To detect VT failure.
WAN	Wide Area Network
XACML	eXtensible Access Control Markup Language. An OASIS standard defining an XML access control policy implementation.
Xformer	Transformer
XKMS	XML Keys Management Specifications. A 3C standard, XML based, for distribution and registration of public keys and certificates
XML	Extensible Markup Language
XSD	XML Schema Definition

Table 1 - Acronyms and abbreviations

2 COMPANY PROPRIETARY TERMS

Term	Description
Courier	Schneider Electric's proprietary SCADA communications protocol
Easergy	Schneider Electric's brand of protection relays and related software products
Metrosil	Brand of non-linear resistor produced by M&I Materials Ltd.
MiCOM	Schneider Electric's brand of protection relays

Table 2 - Company-proprietary terms

3 ANSI TERMS

ANSI no.	Description
3PAR	Three pole auto-reclose.
3PDT	Three pole dead time. The dead time used in three pole auto-reclose cycles.
52a	A circuit breaker closed auxiliary contact: The contact is in the same state as the breaker primary contacts
52b	A circuit breaker open auxiliary contact: The contact is in the opposite state to the breaker primary contacts
64R	Rotor earth fault protection
64S	100% stator earth (ground) fault protection using a low frequency injection method.
89a	An Isolator closed auxiliary contact: The contact is in the same state as the breaker primary contacts.
89b	An Isolator open auxiliary contact: The contact is in the opposite state to the breaker primary contacts.

Table 3 - ANSI abbreviations

ANSI no.	Function	Description
Current Protection Functions		
50/51	Phase overcurrent	Three-phase protection against overloads and phase-to-phase short-circuits.
50N/51N	Earth fault	Earth fault protection based on measured or calculated residual current values: • 50N/51N: residual current calculated or measured by 3 phase current sensors
50G/51G	Sensitive earth fault	Sensitive earth fault protection based on measured residual current values: • 50G/51G: residual current measured directly by a specific sensor such as a core balance CT
50BF	Breaker failure	If a breaker fails to be triggered by a tripping order, as detected by the non-extinction of the fault current, this backup protection sends a tripping order to the upstream or adjacent breakers.
46	Negative sequence / unbalance	Protection against phase unbalance, detected by the measurement of negative sequence current: • sensitive protection to detect 2-phase faults at the ends of long lines • protection of equipment against temperature build-up, caused by an unbalanced power supply, phase inversion or loss of phase, and against phase current unbalance
46BC	Broken conductor protection	Protection against phase imbalance, detected by measurement of I2/I1.
49RMS	Thermal overload	Protection against thermal damage caused by overloads on machines (transformers, motors or generators). The thermal capacity used is calculated according to a mathematical model which takes into account: • current RMS values • ambient temperature • negative sequence current, a cause of motor rotor temperature rise
Re-Closer		
79	Recloser	Automation device used to limit down time after tripping due to transient or semipermanent faults on overhead lines. The recloser orders automatic reclosing of the breaking device after the time delay required to restore the insulation has elapsed. Recloser operation is easy to adapt for different operating modes by parameter setting.
Directional Current Protection		
67N/67NC type 1 and 67	Directional phase overcurrent	Phase-to-phase short-circuit protection, with selective tripping according to fault current direction. It comprises a phase overcurrent function associated with direction detection, and picks up if the phase overcurrent function in the chosen direction (line or busbar) is activated for at least one of the three phases.

ANSI no.	Function	Description
67N/67NC	Directional earth fault	Earth fault protection, with selective tripping according to fault current direction. Three types of operation: • Type 1: the protection function uses the projection of the I0 vector • Type 2: the protection function uses the I0 vector magnitude with half-plane tripping zone • Type 3: the protection function uses the I0 vector magnitude with angular sector tripping zone
67N/67NC type 1	Directional current protection	Directional earth fault protection for impedant, isolated or compensated neutral systems, based on the projection of measured residual current.
67N/67NC type 2	Directional current protection	Directional overcurrent protection for impedance and solidly earthed systems, based on measured or calculated residual current. It comprises an earth fault function associated with direction detection, and picks up if the earth fault function in the chosen direction (line or busbar) is activated.
67N/67NC type 3	Directional current protection	Directional overcurrent protection for distribution networks in which the neutral earthing system varies according to the operating mode, based on measured residual current. It comprises an earth fault function associated with direction detection (angular sector tripping zone defined by 2 adjustable angles), and picks up if the earth fault function in the chosen direction (line or busbar) is activated.
Directional Power Protection Functions		

32P	Directional active overpower	Two-way protection based on calculated active power, for the following applications:
		• active overpower protection to detect overloads and allow load shedding
		• reverse active power protection:
		  • against generators running like motors when the generators consume active power
		  • against motors running like generators when the motors supply active power

32Q/40	Directional reactive overpower	Two-way protection based on calculated reactive power to detect field loss on synchronous machines: • reactive overpower protection for motors which consume more reactive power with field loss • reverse reactive overpower protection for generators which consume reactive power with field loss.
Machine Protection Functions		
37	Phase undercurrent	Protection of pumps against the consequences of a loss of priming by the detection of motor no-load operation. It is sensitive to a minimum of current in phase 1, remains stable during breaker tripping and may be inhibited by a logic input.

48/51LR/14	Locked rotor / excessive starting time	Protection of motors against overheating caused by:
		• excessive motor starting time due to overloads (e.g. conveyor) or insufficient supply voltage.
		The reacceleration of a motor that is not shut down, indicated by a logic input, may be considered as starting.
		• locked rotor due to motor load (e.g. crusher):
		  • in normal operation, after a normal start
		  • directly upon starting, before the detection of excessive starting time, with detection of locked rotor by a zero speed detector connected to a logic input, or by the underspeed function.

66	Starts per hour	Protection against motor overheating caused by:
		• too frequent starts: motor energizing is inhibited when the maximum allowable number of starts is reached, after counting of:
		  • starts per hour (or adjustable period)
		  • consecutive motor hot or cold starts (reacceleration of a motor that is not shut down, indicated by a logic input, may be counted as a start)
		• starts too close together in time: motor re-energizing after a shutdown is only allowed after an adjustable waiting time.

ANSI no.	Function	Description
50V/51V	Voltage-restrained overcurrent	Phase-to-phase short-circuit protection, for generators. The current tripping set point is voltage-adjusted in order to be sensitive to faults close to the generator which cause voltage drops and lowers the short-circuit current.
26/63	Thermostat/Buchholz	Protection of transformers against temperature rise and internal faults via logic inputs linked to devices integrated in the transformer.
38/49T	Temperature monitoring	Protection that detects abnormal temperature build-up by measuring the temperature inside equipment fitted with sensors: • transformer: protection of primary and secondary windings • motor and generator: protection of stator windings and bearings.
Voltage Protection Functions		
27D	Positive sequence undervoltage	Protection of motors against faulty operation due to insufficient or unbalanced network voltage, and detection of reverse rotation direction.
27R	Remanent undervoltage	Protection used to check that remanent voltage sustained by rotating machines has been cleared before allowing the busbar supplying the machines to be re-energized, to avoid electrical and mechanical transients.
27	Undervoltage	Protection of motors against voltage sags or detection of abnormally low network voltage to trigger automatic load shedding or source transfer. Works with phase-to-phase voltage.
59	Overvoltage	Detection of abnormally high network voltage or checking for sufficient voltage to enable source transfer. Works with phase-to-phase or phase-to-neutral voltage, each voltage being monitored separately.
59N	Neutral voltage displacement	Detection of insulation faults by measuring residual voltage in isolated neutral systems.
47	Negative sequence overvoltage	Protection against phase unbalance resulting from phase inversion, unbalanced supply or distant fault, detected by the measurement of negative sequence voltage.
Frequency Protection Functions		
81O	Overfrequency	Detection of abnormally high frequency compared to the rated frequency, to monitor power supply quality. Other organizations may use 81H instead of 81O.
81U	Underfrequency	Detection of abnormally low frequency compared to the rated frequency, to monitor power supply quality. The protection may be used for overall tripping or load shedding. Protection stability is ensured in the event of the loss of the main source and presence of remanent voltage by a restraint in the event of a continuous decrease of the frequency, which is activated by parameter setting. Other organizations may use 81L instead of 81U.
81R	Rate of change of frequency	Protection function used for fast disconnection of a generator or load shedding control. Based on the calculation of the frequency variation, it is insensitive to transient voltage disturbances and therefore more stable than a phase-shift protection function. **Disconnection** In installations with autonomous production means connected to a utility, the “rate of change of frequency” protection function is used to detect loss of the main system in view of opening the incoming circuit breaker to: • protect the generators from a reconnection without checking synchronization • avoid supplying loads outside the installation. **Load shedding** The “rate of change of frequency” protection function is used for load shedding in combination with the underfrequency protection to: • either accelerate shedding in the event of a large overload • or inhibit shedding following a sudden drop in frequency due to a problem that should not be solved by shedding.
Dynamic Line Rating (DLR) Protection Functions		

ANSI no.	Function	Description
49DLR	Dynamic line rating (DLR)	Protection of overhead lines based on calculation of rating or ampacity to dynamically take into account the effect of prevailing weather conditions as monitored by external sensors for: • Ambient Temperature • Wind Velocity • Wind Direction • Solar Radiation

Table 4 - ANSI descriptions

4 CONCATENATED TERMS

Term
Undercurrent
Overcurrent
Overfrequency
Underfrequency
Undervoltage
Overvoltage

Table 5 - Concatenated terms

5 UNITS FOR DIGITAL COMMUNICATIONS

Unit	Description
b	bit
B	Byte
kb	Kilobit(s)
kbps	Kilobits per second
kB	Kilobyte(s)
Mb	Megabit(s)
Mbps	Megabits per second
MB	Megabyte(s)
Gb	Gigabit(s)
Gbps	Gigabits per second
GB	Gigabyte(s)
Tb	Terabit(s)
Tbps	Terabits per second
TB	Terabyte(s)

Table 6 - Units for digital communications

6 AMERICAN VS BRITISH ENGLISH TERMINOLOGY

British English	American English
…ae…	…e…
…ence	…ense
…ise	…ize
…oe…	…e…
…ogue	…og
…our	…or
…ourite	…orite
…que	…ck
…re	…er
…yse	…yze
Aluminium	Aluminum
Centre	Center
Earth	Ground
Fibre	Fiber
Ground	Earth
Speciality	Specialty

Table 7 - American vs British English terminology

7 LOGIC SYMBOLS AND TERMS

Symbol	Description	Units
&	Logical “AND”: Used in logic diagrams to show an AND-gate function.	
Σ	“Sigma”: Used to indicate a summation, such as cumulative current interrupted.	
τ	“Tau”: Used to indicate a time constant, often associated with thermal characteristics.	
ω	System angular frequency	rad
<	Less than: Used to indicate an “under” threshold, such as undercurrent (current dropout).	
>	Greater than: Used to indicate an “over” threshold, such as overcurrent (current overload)	
o	A small circle on the input or output of a logic gate: Indicates a NOT (invert) function.	
1	Logical “OR”: Used in logic diagrams to show an OR-gate function.	
ABC	Clockwise phase rotation.	
ACB	Anti-Clockwise phase rotation.	
C	Capacitance	A
df/dt	Rate of Change of Frequency protection	Hz/s
df/dt>1	First stage of df/dt protection	Hz/s
F<	Underfrequency protection: Could be labeled 81-U in ANSI terminology.	Hz
F>	Overfrequency protection: Could be labeled 81-O in ANSI terminology.	Hz
F<1	First stage of under frequency protection: Could be labeled 81-U in ANSI terminology.	Hz
F>1	First stage of over frequency protection: Could be labeled 81-O in ANSI terminology.	Hz
f_{max}	Maximum required operating frequency	Hz
f_{min}	Minimum required operating frequency	Hz
f_n	Nominal operating frequency	Hz
I	Current	A
I^	Current raised to a power: Such as when breaker statistics monitor the square of ruptured current squared (^ power = 2).	An
I’f	Maximum internal secondary fault current (may also be expressed as a multiple of In)	A
I<	An undercurrent element: Responds to current dropout.	A
I>>	Current setting of short circuit element	In
I>	A phase overcurrent protection: Could be labeled 50/51 in ANSI terminology.	A
I>1	First stage of phase overcurrent protection: Could be labeled 51-1 in ANSI terminology.	A
I>2	Second stage of phase overcurrent protection: Could be labeled 51-2 in ANSI terminology.	A
I>3	Third stage of phase overcurrent protection: Could be labeled 51-3 in ANSI terminology.	A
I>4	Fourth stage of phase overcurrent protection: Could be labeled 51-4 in ANSI terminology.	A
I>BB	Minimum pick-up phase threshold for the local trip order confirmation.	A
I>DZ	Minimum pick-up phase threshold for the Dead Zone protection.	A
I_0	Earth fault current setting Zero sequence current: Equals one third of the measured neutral/residual current.	A
I_1	Positive sequence current.	A
I_2	Negative sequence current.	A
I2>	Negative sequence overcurrent protection (NPS element).	A
I2pol	Negative sequence polarizing current.	A
I2therm>	A negative sequence thermal element: Could be labeled 46T in ANSI terminology.	
IA	Phase A current: Might be phase L1, red phase.. or other, in customer terminology.	A
IB	Phase B current: Might be phase L2, yellow phase.. or other, in customer terminology.	A
IbiasPh> Cur.	SDEF blocking bias current threshold.	

Symbol	Description	Units
IC	Phase C current: Might be phase L3, blue phase.. or other, in customer terminology.	A
ID>1	Minimum pick-up phase circuitry fault threshold.	
ID>2	Minimum pick-up differential phase element for all the zones.	
IDCZ>2	Minimum pick-up differential phase element for the Check Zone.	
Idiff	Current setting of biased differential element	A
IDN>1	Minimum pick-up neutral circuitry fault threshold.	
IDN>2	Minimum pick-up differential neutral element for all the zones.	
IDNCZ>2	Minimum pick-up differential neutral element for the Check Zone.	
IDZ	Minimum pick-up differential neutral element for the Check Zone.	
If	Maximum secondary through-fault current	A
If max	Maximum secondary fault current (same for all feeders)	A
If max int	Maximum secondary contribution from a feeder to an internal fault	A
If Z1	Maximum secondary phase fault current at Zone 1 reach point	A
Ife	Maximum secondary through fault earth current	A
IfeZ1	Maximum secondary earth fault current at Zone 1 reach point	A
Ifn	Maximum prospective secondary earth fault current or 31 x I> setting (whichever is lowest)	A
Ifp	Maximum prospective secondary phase fault current or 31 x I> setting (whichever is lowest)	A
I_m	Mutual current	A
IM64	InterMiCOM64.	
IMx	InterMiCOM64 bit (x=1 to 16)	
I_n	Current transformer nominal secondary current. The rated nominal current of the relay: Software selectable as 1 amp or 5 amp to match the line CT input.	A
IN	Neutral current, or residual current: This results from an internal summation of the three measured phase currents.	A
IN>	A neutral (residual) overcurrent element: Detects earth/ground faults.	A
IN>1	First stage of ground overcurrent protection: Could be labeled 51N-1 in ANSI terminology.	A
IN>2	Second stage of ground overcurrent protection: Could be labeled 51N-2 in ANSI terminology.	A
IN>BB	Minimum pick-up neutral threshold for the local trip order confirmation.	
IN>DZ	Minimum pick-up neutral threshold for the Dead Zone protection.	
Inst	An element with “instantaneous” operation: i.e. having no deliberate time delay.	
I/O	Inputs and Outputs - used in connection with the number of optocoupled inputs and output contacts within the relay.	
I/P	Input	
Iref	Reference current of P63x calculated from the reference power and nominal voltage	A
IREF>	A Restricted Earth Fault overcurrent element: Detects earth (ground) faults. Could be labeled 64 in ANSI terminology.	A
IRm2	Second knee-point bias current threshold setting of P63x biased differential element	A
Is	Value of stabilizing current	A
IS1	Differential current pick-up setting of biased differential element	A
IS2	Bias current threshold setting of biased differential element	A
I_{SEF}>	Sensitive Earth Fault overcurrent element.	A
Isn	Rated secondary current (I secondary nominal)	A
Isp	Stage 2 and 3 setting	A
Ist	Motor start up current referred to CT secondary side	A
K	Dimensioning factor	

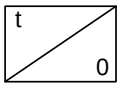
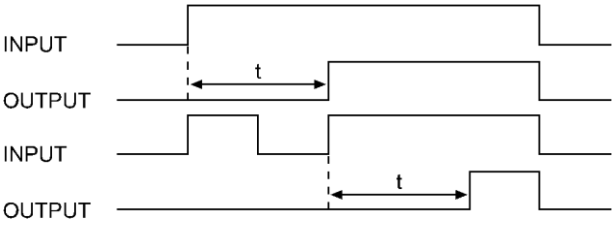
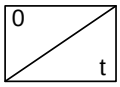
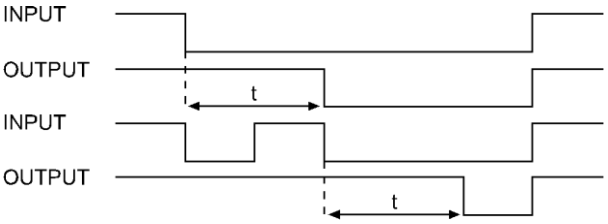
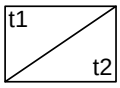
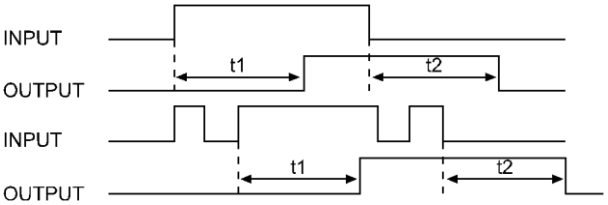
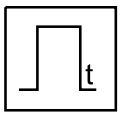
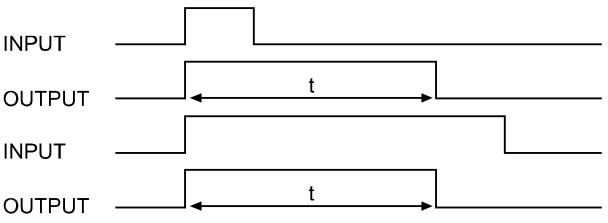
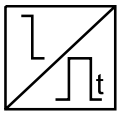
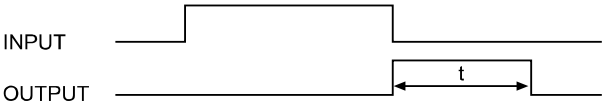
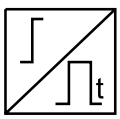
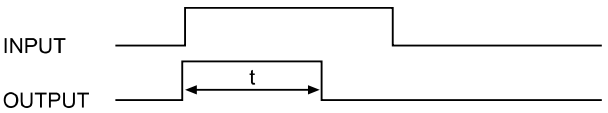
Symbol	Description	Units
K_1	Lower bias slope setting of biased differential element	%
K_2	Higher bias slope setting of biased differential element	%
KCZ	Slope of the differential phase element for the Check Zone.	
K_e	Dimensioning factor for earth fault	
km	Distance in kilometers	
K_{max}	Maximum dimensioning factor	
KNCZ	Slope of the differential neutral element for the Check Zone.	
K_{rpa}	Dimensioning factor for reach point accuracy	
K_s	Dimensioning factor dependent upon through fault current	
K_{ssc}	Short circuit current coefficient or ALF	
K_t	Dimensioning factor dependent upon operating time	
kZm	The mutual compensation factor (mutual compensation of distance elements and fault locator for parallel line coupling effects).	
kZN	The residual compensation factor: Ensuring correct reach for ground distance elements.	
L	Inductance	A
m1	Lower bias slope setting of P63x biased differential element	None
m2	Higher bias slope setting of P63x biased differential element	None
mi	Distance in miles.	
N	Indication of “Neutral” involvement in a fault: i.e. a ground (earth) fault.	
-P>	A reverse power (W) element: could be labeled 32R in ANSI terminology.	
P>	An overpower (W) element: could be labeled 32O in ANSI terminology.	
P<	A low forward power (W) element: could be labeled 32L in ANSI terminology.	
P1	Used in IEC terminology to identify the primary CT terminal polarity: Replace by a dot when using ANSI standards.	
P2	Used in IEC terminology to identify the primary CT terminal polarity: The non-dot terminal.	
P_n	Rotating plant rated single phase power	W
PN>	Wattmetric earth fault protection: Calculated using residual voltage and current quantities.	
Q<	A reactive under power (VAr) element	
R	Resistance (Ω)	Ω
R< or 64S R<	A 100% stator earth (ground) fault via low frequency injection under resistance element: could be labeled 64S in ANSI terminology.	
R Gnd.	A distance zone resistive reach setting: Used for ground (earth) faults.	
R Ph	A distance zone resistive reach setting used for Phase-Phase faults.	
Rct	Secondary winding resistance	Ω
RCT	Current transformer secondary resistance	Ω
Rl	Resistance of single lead from relay to current transformer	Ω
Rr	Resistance of any other protective relays sharing the current transformer	Ω
Rrn	Resistance of relay neutral current input	Ω
Rrp	Resistance of relay phase current input	Ω
Rs	Value of stabilizing resistor	Ω
Rx	Receive: typically used to indicate a communication receive line/pin.	
S<	An apparent under power (VA) element	
S1	Used in IEC terminology to identify the secondary CT terminal polarity: Replace by a dot when using ANSI standards.	

Symbol	Description	Units
S2	Used in IEC terminology to identify the secondary CT terminal polarity: The non-dot terminal. Also used to signify negative sequence apparent power, S2 = V2 x I2.	
S2>	A negative sequence apparent power element, S2 = V2 x I2.	
t	A time delay.	
t'	Duration of first current flow during auto-reclose cycle	s
T1	Primary system time constant	s
TF	Through Fault monitoring	
tfr	Auto-reclose dead time	s
Thermal I>	A stator thermal overload element: could be labeled 49 in ANSI terminology.	
Thru/TF	Through Fault monitoring	
tIdiff	Current differential operating time	s
Ts	Secondary system time constant	s
Tx	Transmit: typically used to indicate a communication transmit line/pin.	
V	Voltage.	V
V<	An undervoltage element: could be labeled 27 in ANSI terminology	V
V<1	First stage of undervoltage protection: Could be labeled 27-1 in ANSI terminology.	V
V<2	Second stage of undervoltage protection: Could be labeled 27-2 in ANSI terminology.	V
V>	An overvoltage element: could be labeled 59 in ANSI terminology	V
V>1	First stage of overvoltage protection: Could be labeled 59-1 in ANSI terminology.	V
V>2	Second stage of overvoltage protection: Could be labeled 59-2 in ANSI terminology.	V
V0	Zero sequence voltage: Equals one third of the measured neutral/residual voltage.	V
V1	Positive sequence voltage.	V
V2	Negative sequence voltage.	V
V2>	A Negative Phase Sequence (NPS) overvoltage element: could be labeled 47 in ANSI terminology.	
$V2_{pol}$	Negative sequence polarizing voltage.	V
V_A	Phase A voltage: Might be phase L1, red phase.. or other, in customer terminology.	V
V_B	Phase B voltage: Might be phase L2, yellow phase.. or other, in customer terminology.	V
V_C	Phase C voltage: Might be phase L3, blue phase.. or other, in customer terminology.	V
Vf	Theoretical maximum voltage produced if CT saturation did not occur	V
Vin	Input voltage e.g. to an opto-input	V
V_k	Required CT knee-point voltage. IEC knee point voltage of a current transformer.	V
VN	Neutral voltage displacement, or residual voltage.	V
VN>	A residual (neutral) overvoltage element: could be labeled 59N in ANSI terminology.	V
V_n	Nominal voltage	V
Vn	The rated nominal voltage of the relay: To match the line VT input.	V
VN>1	First stage of residual (neutral) overvoltage protection.	V
VN>2	Second stage of residual (neutral) overvoltage protection.	V
VN3H>	A 100% stator earth (ground) fault 3rd harmonic residual (neutral) overvoltage element: could be labeled 59TN in ANSI terminology.	
VN3H<	A 100% stator earth (ground) fault 3rd harmonic residual (neutral) undervoltage element: could be labeled 27TN in ANSI terminology.	
Vres.	Neutral voltage displacement, or residual voltage.	V
Vs	Value of stabilizing voltage	V
V_x	An auxiliary supply voltage: Typically the substation battery voltage used to power the relay.	V

Symbol	Description	Units
WI	Weak Infeed logic used in teleprotection schemes.	
X	Reactance	None
X/R	Primary system reactance/resistance ratio	None
Xe/Re	Primary system reactance/resistance ratio for earth loop	None
Xt	Transformer reactance (per unit)	p.u.
Y	Admittance	p.u.
YN>	Neutral overadmittance protection element: Non-directional neutral admittance protection calculated from neutral current and residual voltage.	
Z	Impedance	p.u.
Z<	An under impedance element: could be labeled 21 in ANSI terminology.	
Z0	Zero sequence impedance.	
Z1	Positive sequence impedance.	
Z1	Zone 1 distance protection.	
Z1X	Reach-stepped Zone 1X, for zone extension schemes used with auto-reclosure.	
Z2	Negative sequence impedance.	
Z2	Zone 2 distance protection.	
ZP	Programmable distance zone that can be set forward or reverse looking.	
Zs	Used to signify the source impedance behind the relay location.	
Φal	Accuracy limit flux	Wb
Ψr	Remanent flux	Wb
Ψs	Saturation flux	Wb

Table 8 - Logic Symbols and Terms

8 LOGIC TIMERS

Logic symbols	Explanation	Time chart
	Delay on pick-up timer, t	
	Delay on drop-off timer, t	
	Delay on pick-up/drop-off timer	
	Pulse timer	
	Pulse pick-up falling edge	
	Pulse pick-up raising edge	

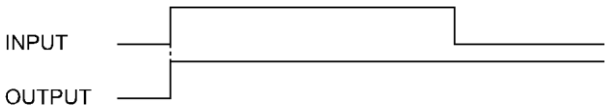
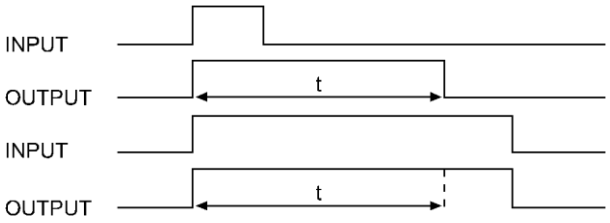
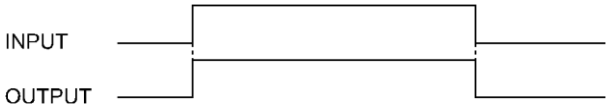
Logic symbols	Explanation	Time chart
Latching	Latch	
Dwell / Timer	Dwell timer	
Straight	Straight (non latching): Hold value until input reset signal	

Table 9 - Logic Timers

9 LOGIC GATES

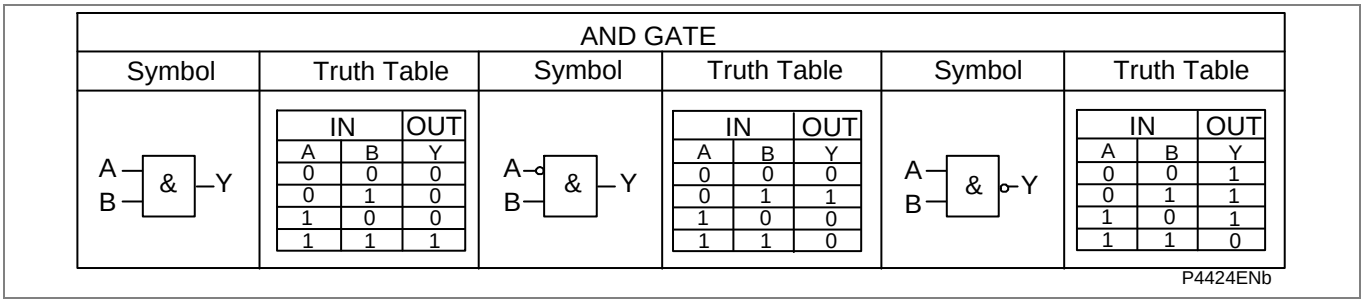


Figure 1 - Logic Gates - AND Gate

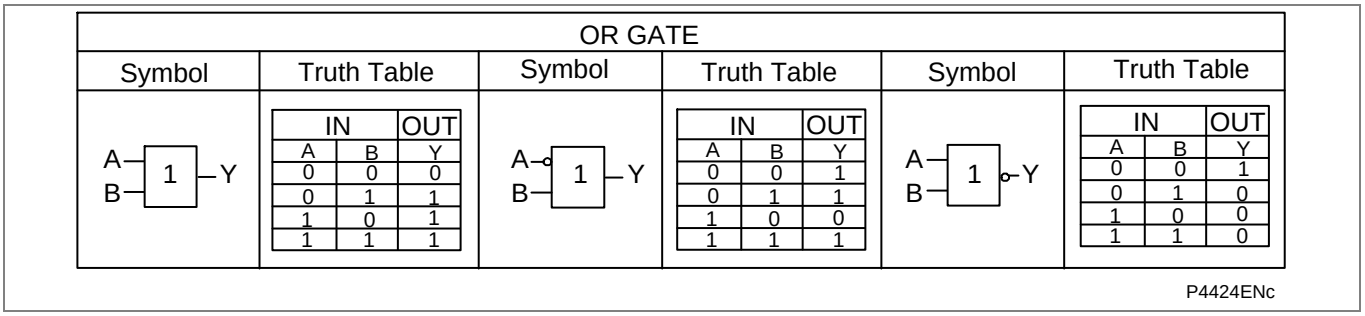


Figure 2 - Logic Gates - OR Gate

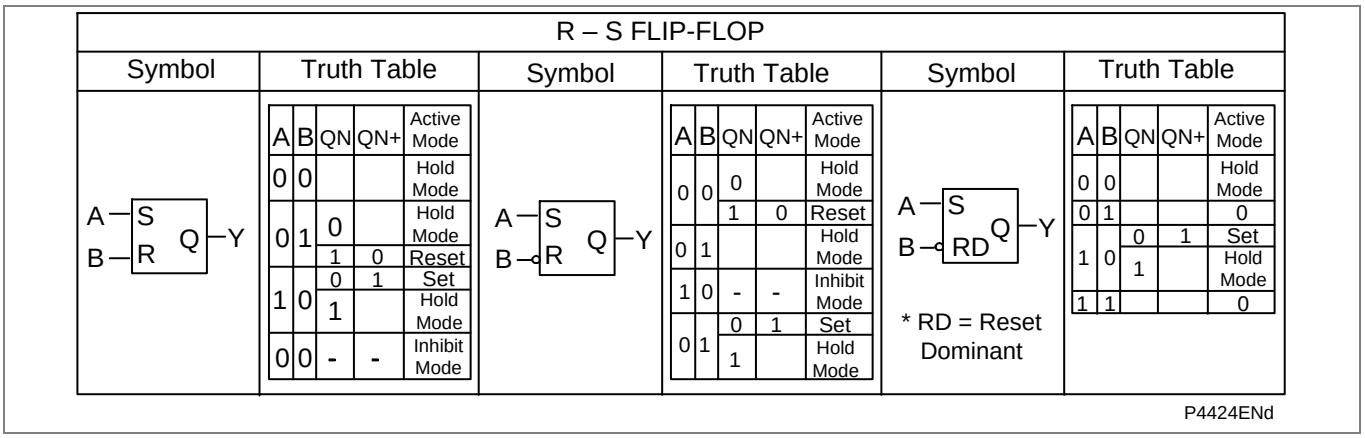


Figure 3 - Logic Gates - R-S Flip-Flop Gate

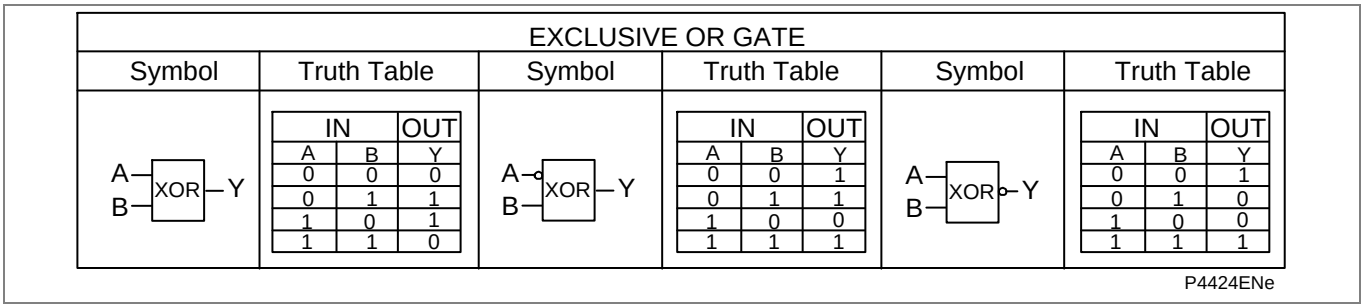


Figure 4 - Logic Gates - Exclusive OR Gate

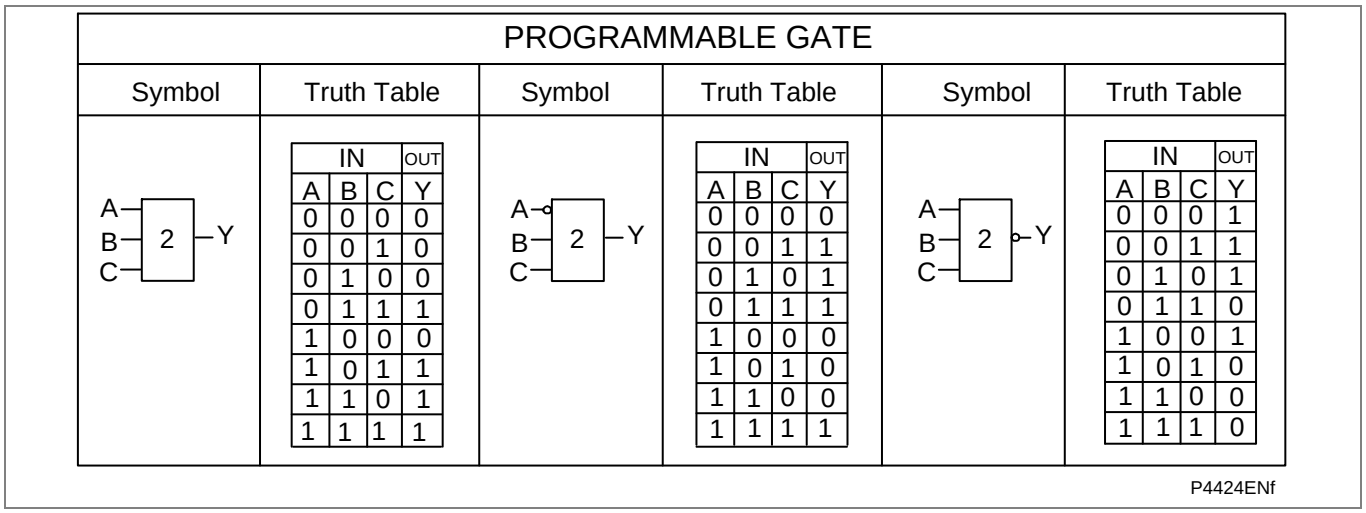


Figure 5 - Logic Gates - Programmable Gate

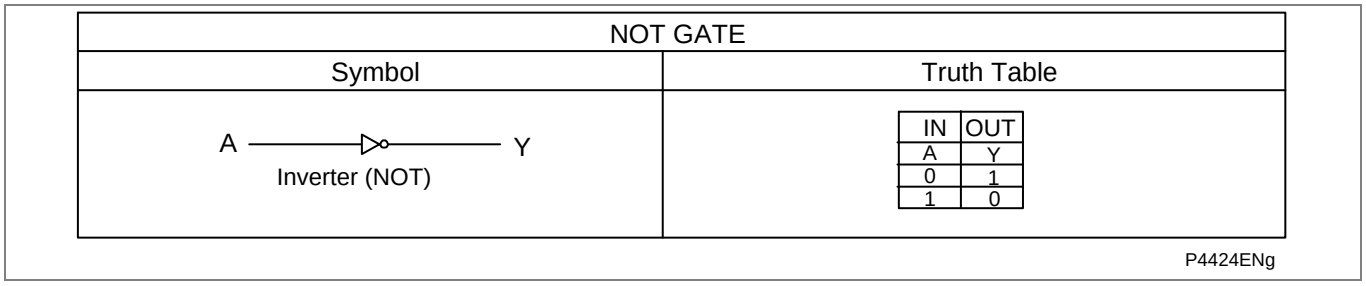


Figure 6 - Logic Gates - NOT Gate

Notes:

Customer Care Centre

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